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ADBS-A320

Optical Finger Navigation

Data Sheet

Description

The ADBS-A320 sensor is a small form factor (SFF) LED illuminated optical finger navigation system.

The ADBS-A320 is a low-power optical finger navigation sensor. It has a new, low-power architecture and automatic power management modes, making it ideal for battery- and power-sensitive applications such as mobile phones.

The ADBS-A320 is capable of high-speed motion detection – up to 15ips. In addition, it has an on-chip oscillator and integrated LED to minimize external components.

There are no moving parts which means high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly.

The sensor is programmed via registers through either a serial peripheral interface or a two wire interface port. It is packaged in a 28 I/O surface mountable package.

The ADBS-A320 is designed for use with ADBL-A321 lens. The ADBL-A321 lens is the optical component necessary for proper operation of the sensor.

Theory of Operation

The ADBS-A320 is based on Optical Finger Navigation (OFN) Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The ADBS-A320 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a communication system.

The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values.

The host reads the Δx and Δy information from the sensor serial port if a motion interrupt is published. The microcontroller then translates the data into cursor navigation, rocker switch, scrolling or other system dependent navigation data.

Features

- Low power architecture
- Surface mount technology (SMT) device
- Self-adjusting power-saving modes for longer battery life
- High speed motion detection up to 15ips
- Self-adjusting frame rate for optimum performance
- Motion detect pin output
- Finger detect pin output
- Internal oscillator – no clock input needed
- Selectable 250, 500, 750, 1000 and 1250 cpi resolution
- Dual 2.8V/1.8V or single 2.8V supply options
- Selectable Input/Output voltage at 2.8V or 1.8V nominal
- Serial peripheral interface (SPI) or Two wire interface (TWI)
- Integrated chip-on-board LED with wavelength of 870nm

Applications

- Finger input devices
- Mobile devices
- Integrated input devices
- Battery-powered input device

Avago customers purchasing the ADBS-A320 OFN product are eligible to receive a royalty free license to our US patents 6977645, 6621483, 6950094, 6172354 and 7289649, for use in their end products.

***CAUTION:** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

Pinout of ADBS-A320 Optical Sensor

Pin	Name	Description	Input/Output pin	Function
1	GND	Ground		
2	XY_LED	XY LED driver connection		Must connect to LED- (see schematics fig 7a,7b)
3	MOTION	Motion Detect (active low output)	O (CMOS output)	Open when not used Default active low signal, can be changed in Motion_Control register 0x1d
4	GPIO	General Purpose Input / Output for FPD function	O (CMOS output)	Pin indicate Finger Presence Detection, OFN engine 0x60 must be enabled (see application note OFN A320 firmware design guide). Open when not used
5	VDDIO	Voltage supply for I/O		Sets I/O voltage but not for nDREG_EN
6	IO_MOSI_A0	TWI address set or Master Out Slave In	I (Schmitt trigger input)	SPI : MOSI (Master Out Slave In) signal TWI : address select 0 Open when not used
7	IO_CLK	Serial clock input	I (Schmitt trigger input)	Serial clock signal
8	IO_MISO_SDA	TWI serial data or Master In Slave Out	In SPI – CMOS output. In TWI – open drain I/O	SPI : MISO (Master Input Slave Out) signal TWI : serial data signal
9	IO_NCS_A1	TWI address set or Chip Select	I (Schmitt trigger input)	SPI : NCS (chip select) signal TWI : address select 1 Open when not used Active low signal
10	NRST	Hardware Chip Reset	I (Schmitt trigger input)	Set to high when not used Active low signal
11	GND	Ground		
12	ORIENT	Sensor orientation input	I (Schmitt trigger input)	Set to high when not used
13	SHTDWN	Shutdown (active high input)	I (Schmitt trigger input)	Set to low when not used Active high signal
14	VDDIO	Voltage supply for I/O		Sets I/O voltage but not for nDREG_EN
15	IO_SELECT	SPI / TWI Select	I (Schmitt trigger input)	TWI : GND or SPI : High
16	DVDD	Digital Supply voltage or Regulator Output voltage		In regulator disabled, supply 1.8V. In regulator enabled, do not supply 1.8V.
17	nDREG_EN	Digital Regulator enable signal	I (Schmitt trigger input)	Tie to VDDA to disable internal regulator or GND to supply 1.8V to DVDD
18	NC	No Connect		No Connection
19	NC	No Connect		No Connection
20	VDDA	Analog Voltage input		
21	GND	Ground		
22	GND	Ground		
23	NC	No Connect		No connection
24	LED-	LED Cathode		Must connect to XY_LED
25	LED-	LED Cathode		Must connect to XY_LED
26	LED-	LED Cathode		Must connect to XY_LED
27	LED+	LED Anode		Provide 2.8V supply voltage
28	GND	Ground		

Note when A0, A1 is in NC, the sensor will drive the pin to 0 or low.

Overview of Optical Sensor Assembly

Avago Technologies provides an IGES file drawing describing the cover plate molding features.

The components interlock as they are mounted onto defined features on the cover plate.

The ADBS-A320 sensor is designed for surface mounting on a PCB, looking up. There is an aperture stop and features on the package that align to the lens.

The lens provides optics for the imaging of the surface as well as illumination of the surface at the optimum angle. Features on the lens align it to the sensor and cover plate. Contamination must be kept away from the lens. During assembly process, it is recommended to use a minimum of a 10K clean room environment or equivalent laminar flow workbench. See Application note OFN A320 Assembly Guide for more details on process flow.

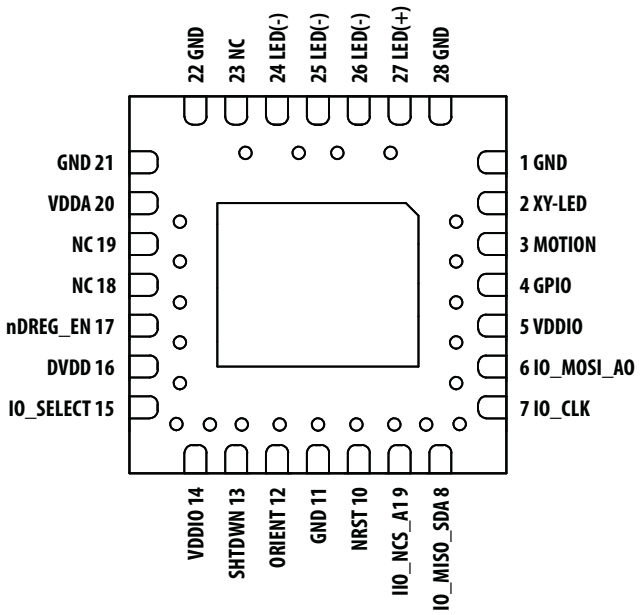


Figure 1a. Package outline drawing (bottom view)

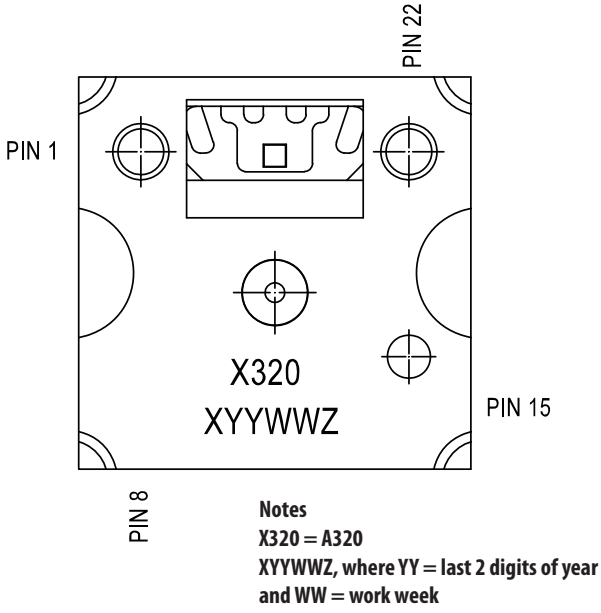
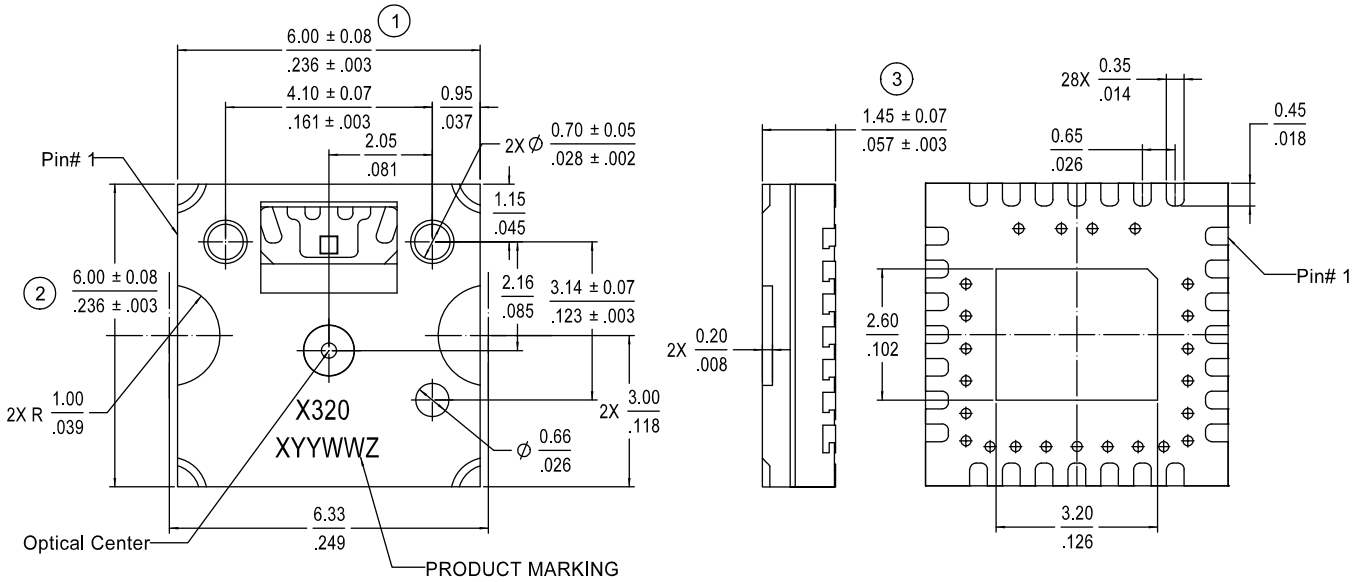


Figure 1b. Package outline drawing (top view)



Note:
1. Dimension in millimeters/inches
2. Coplanarity of pads : 0.08mm
3. Non Cumulative Pad pitch tolerance : ± 0.10mm
4. Maximum flash : ± 0.2mm
5. Dimensional tolerance (unless otherwise stated) : ± 0.10mm
6. All critical dimensions are indicated by number enclosed in a circle.

Figure 2. Package outline drawing

PCB Assembly Considerations

1. Surface mount the sensor and all other electrical components into PCB.
2. Reflow the entire assembly in a no-wash solder process.
3. Remove the protective kapton tape from optical aperture of the sensor and LED. Care must be taken to keep contaminants from entering the aperture. Recommend not to place the PCB facing up during the entire assembly process. Recommend to hold the PCB first vertically for the kapton removal process.
4. Press fit the lens onto the sensor until there is no gap between the lens and sensor, with force up to a maximum 2.2kgf. Care must be taken to avoid contaminating or staining the lens. The lens piece has alignment posts which will mate with the alignment holes on the sensor package.
5. Place and secure the optical navigation cover onto the lens to ensure the sensor and lens components are always interlocked to the correct vertical height. The cover design has a foolproof feature to avoid wrong orientation of the cover.
6. The optical position reference for the PCB is set by the navigation cover and lens.
7. Install device top casing. There MUST be a feature in either top casing or bottom casing to press onto the sensor to ensure the sensor and lens components are always interlocked to the correct vertical height.

Soldering Profile Information

Max rising slope	0.0°C/sec to 3°C/sec
Preheat time 150 – 200° C, ts	60 – 90 sec
Time above Reflow (T_L = 220° C)	50 – 100 sec
Peak Temperature	225 – 260° C

The recommended soldering profile is shown below.

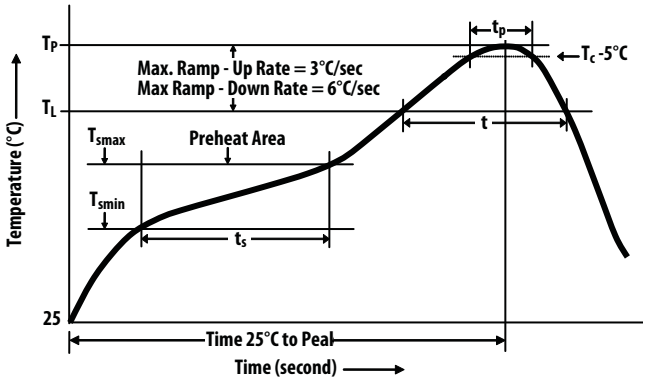
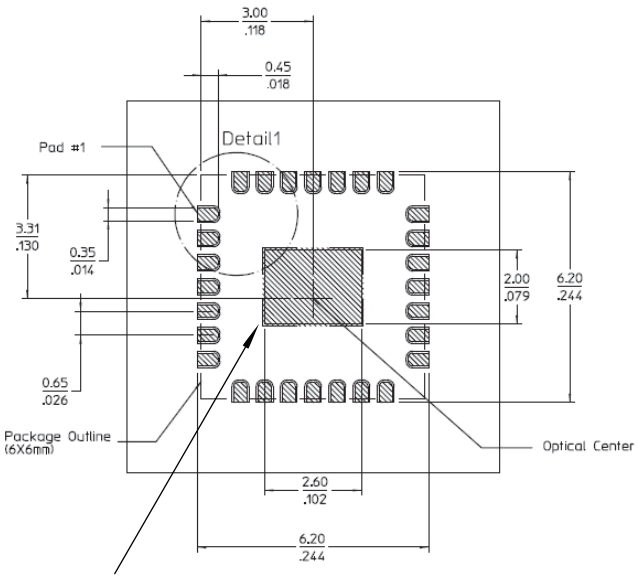


Figure 3a. Recommended reflow profile



Note: Rectangular shape pad on PCB or FPC should match in size (1:1) to sensor center GND pad

Figure 3b. Recommended Customer's PCB PADOUT and spacing

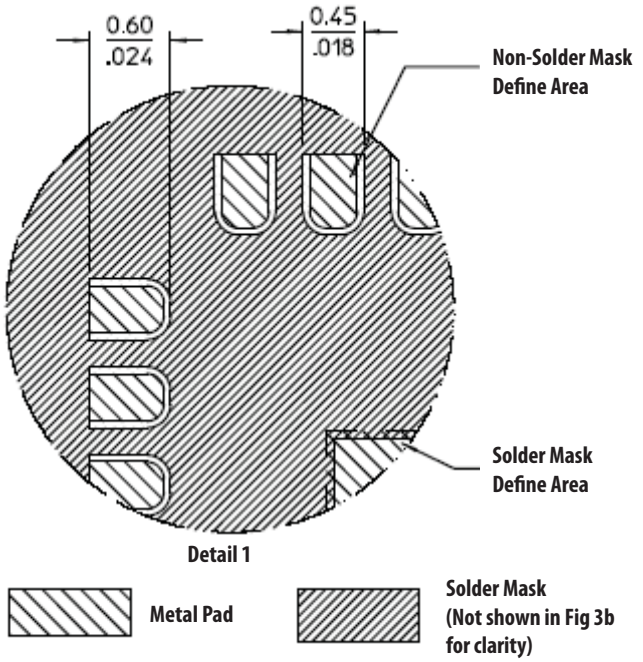


Figure 3c. Recommended Customer's PCB PADOUT and spacing

As ADBS-A320 is a QFN package, it is meant to be a contact-down package. The critical area for soldering ADBS-A320 is on the terminal undersides, while the terminal sides are deemed as non-critical area, and thus not intended to be wet-table. The non-wetting of the terminal sides is due to exposed copper on the package side (which is expected and accepted), occurred after the singulation step, which is a standard process in QFN assembly. This is in line with the Industry Standard (for more information, please refer to IPC-A-610D: Acceptability of Electronics Assemblies).

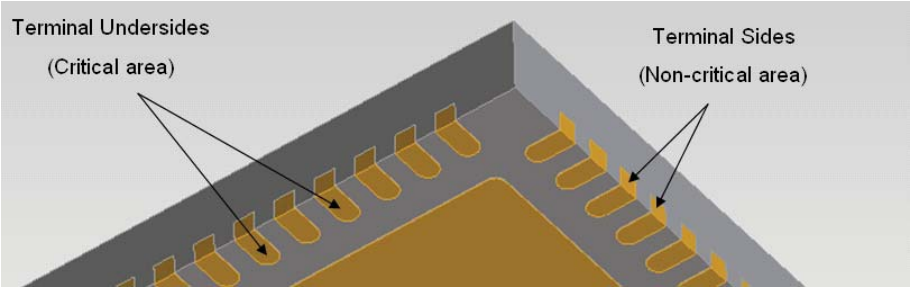


Figure 3d. Bottom view of A320 (QFN package)

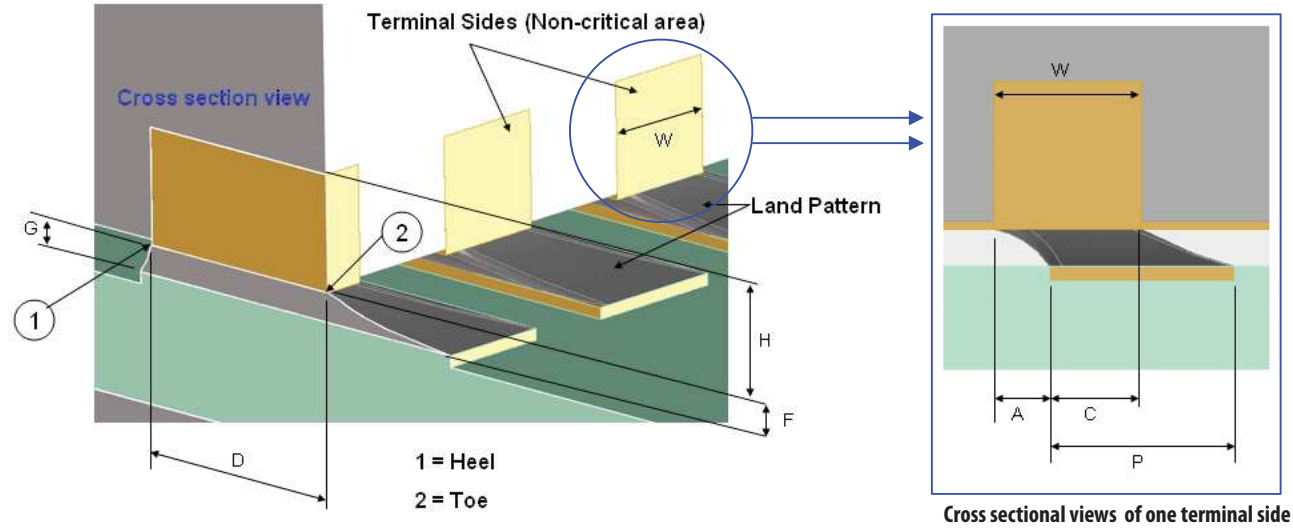


Figure 3e. Cross sectional views of A320

Critical and Non-critical areas of QFN soldering in Figure 3d and 3e

Feature	Dimension	Class 1	Class 2	Class 3
Maximum Side Overhang	A	50% W, Note 1	25% W, Note 1	25% W, Note 1
Minimum End Joint Width	C	50% W	75% W	75% W
Minimum Side Joint Length	D	Note 4	Note 4	Note 4
Minimum Fillet Height	F	Notes 2, 5	Notes 2, 5	Notes 2, 5
Solder Fillet Thickness	G	Note 3	Note 3	Note 3
Termination Height	H	Note 5	Note 5	Note 5
Land Width	P	Note 2	Note 2	Note 2
Termination Width	W	Note 2	Note 2	Note 2

Notes
1. Should not violate minimum electrical clearance.
2. Unspecified parameter. Variable in size as determined by design.
3. Good wetting is evident.
4. Is not a visual attribute for inspection.
5. Terminal sides are not required to be solderable. Toe fillets are not required.

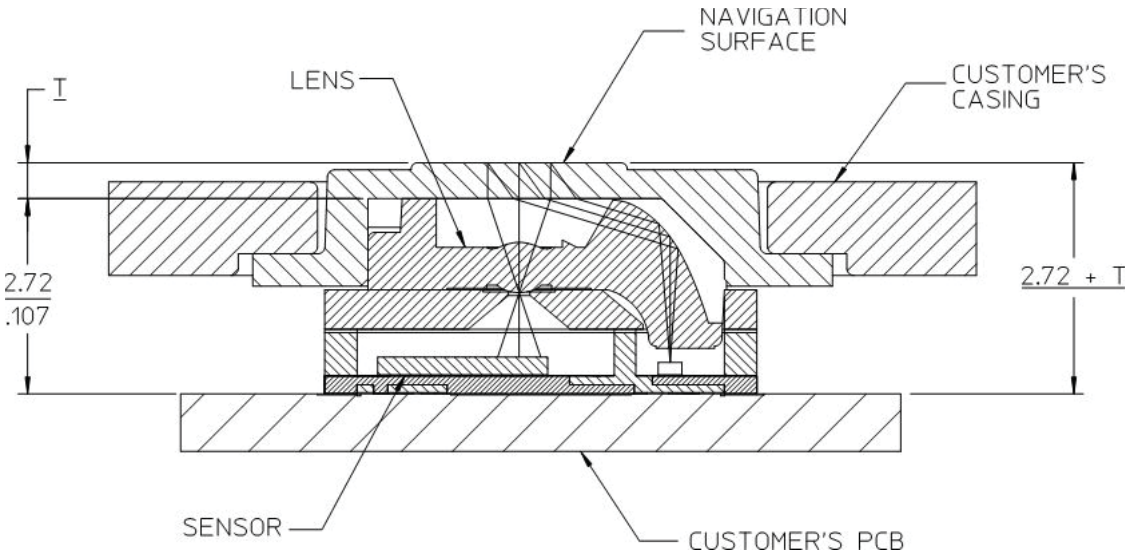


Figure 4. 2D Assembly drawing of ADBS-A320

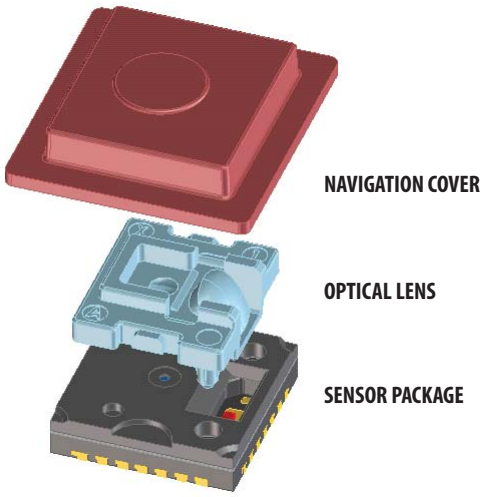


Figure 5a. Exploded Top view

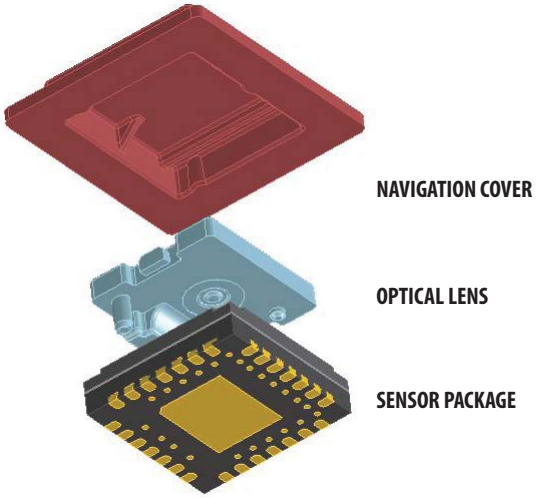
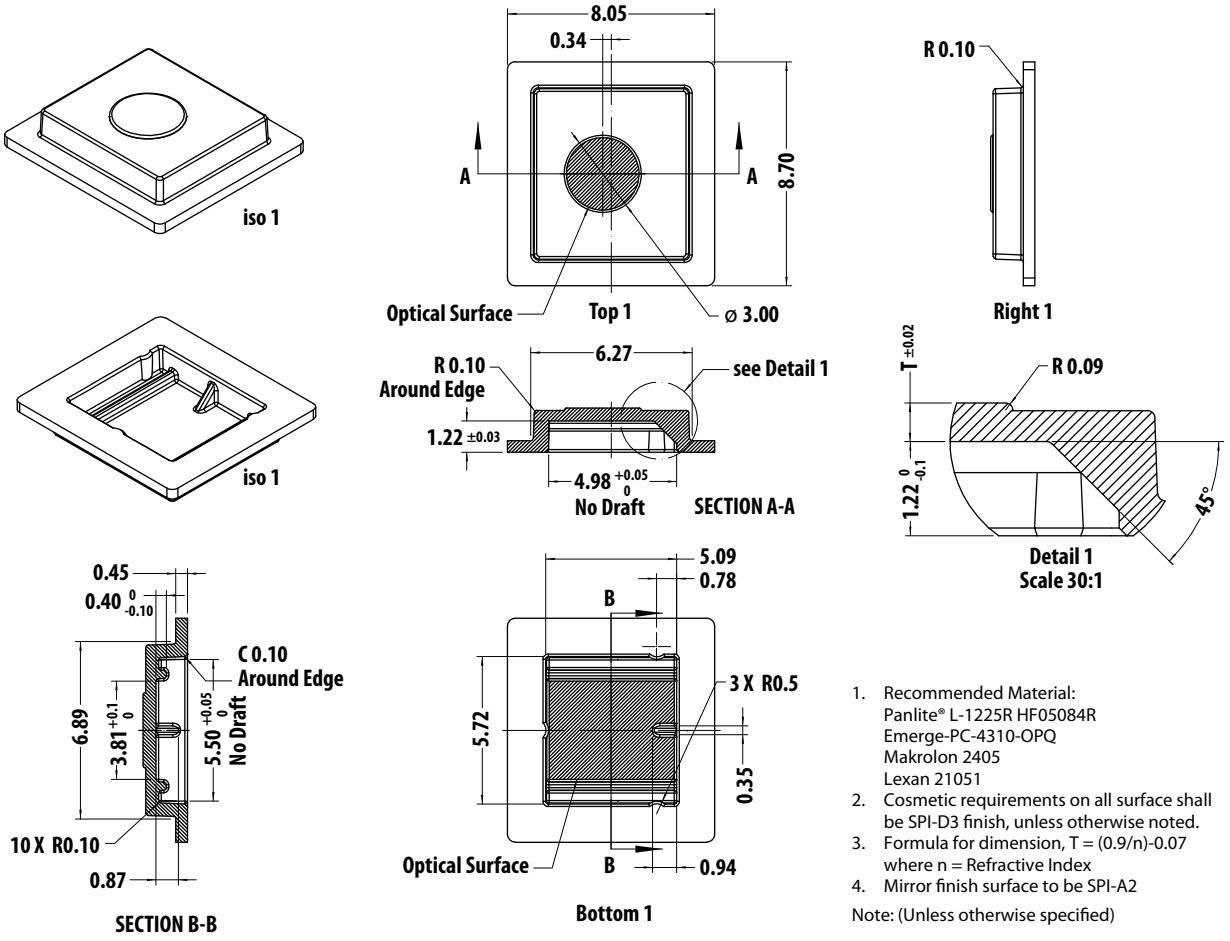


Figure 5b. Exploded Bottom view



1. Recommended Material:
   Panlite® L-1225R HF05084R
   Emerge-PC-4310-OPQ
   Makrolon 2405
   Lexan 21051
2. Cosmetic requirements on all surface shall be SPI-D3 finish, unless otherwise noted.
3. Formula for dimension, T = (0.9/n)-0.07 where n = Refractive Index
4. Mirror finish surface to be SPI-A2

Note: (Unless otherwise specified)

Figure 6a. Top cover drawing design

Important notes for top cover designs:

1. The recommended transmissivity of top cover window is between 86%-92% from 800nm to 940nm with worst case minimum of 80% and maximum of 97% across this range of light spectrum.
2. The Assert/ Deassert thresholds must be recalculated and set in the sensor accordingly during initialization to address variation of surface reflection and transmissivity for custom cover designs. (See OFN firmware application note and OFN mechanical guide application note for further details).

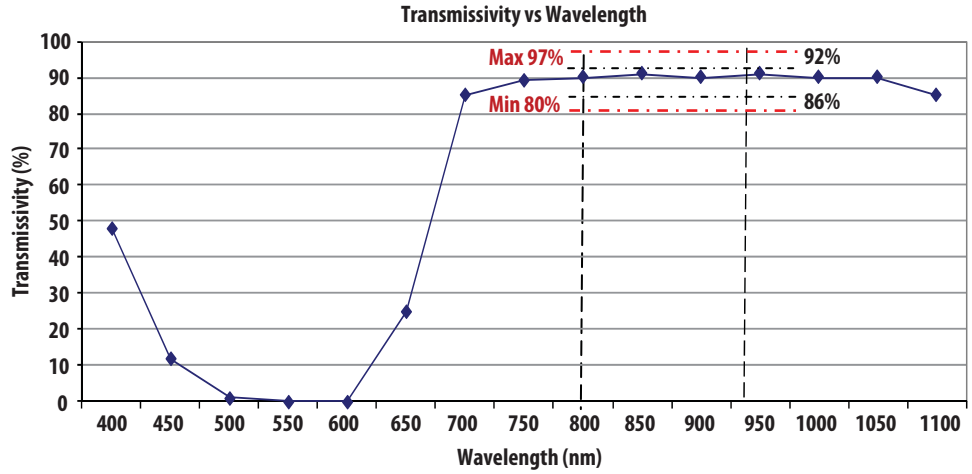
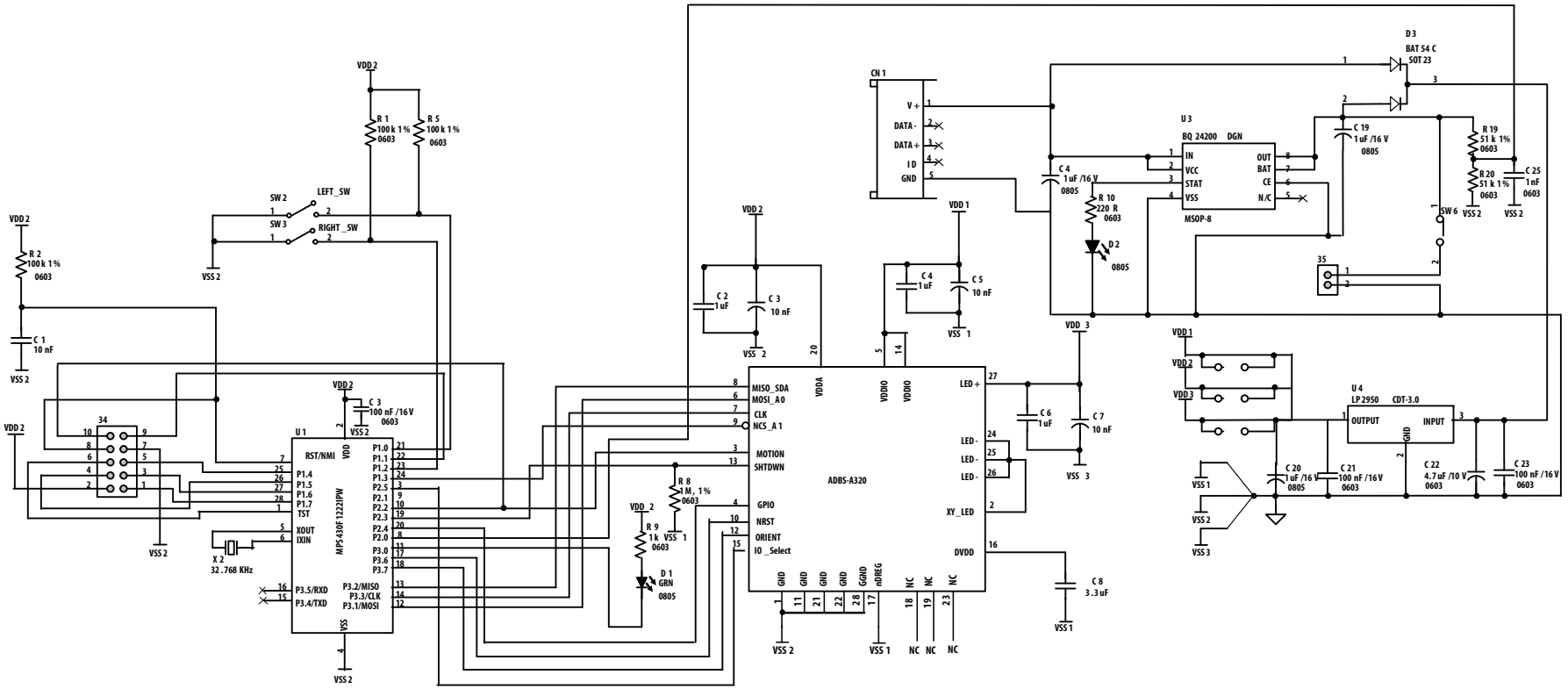
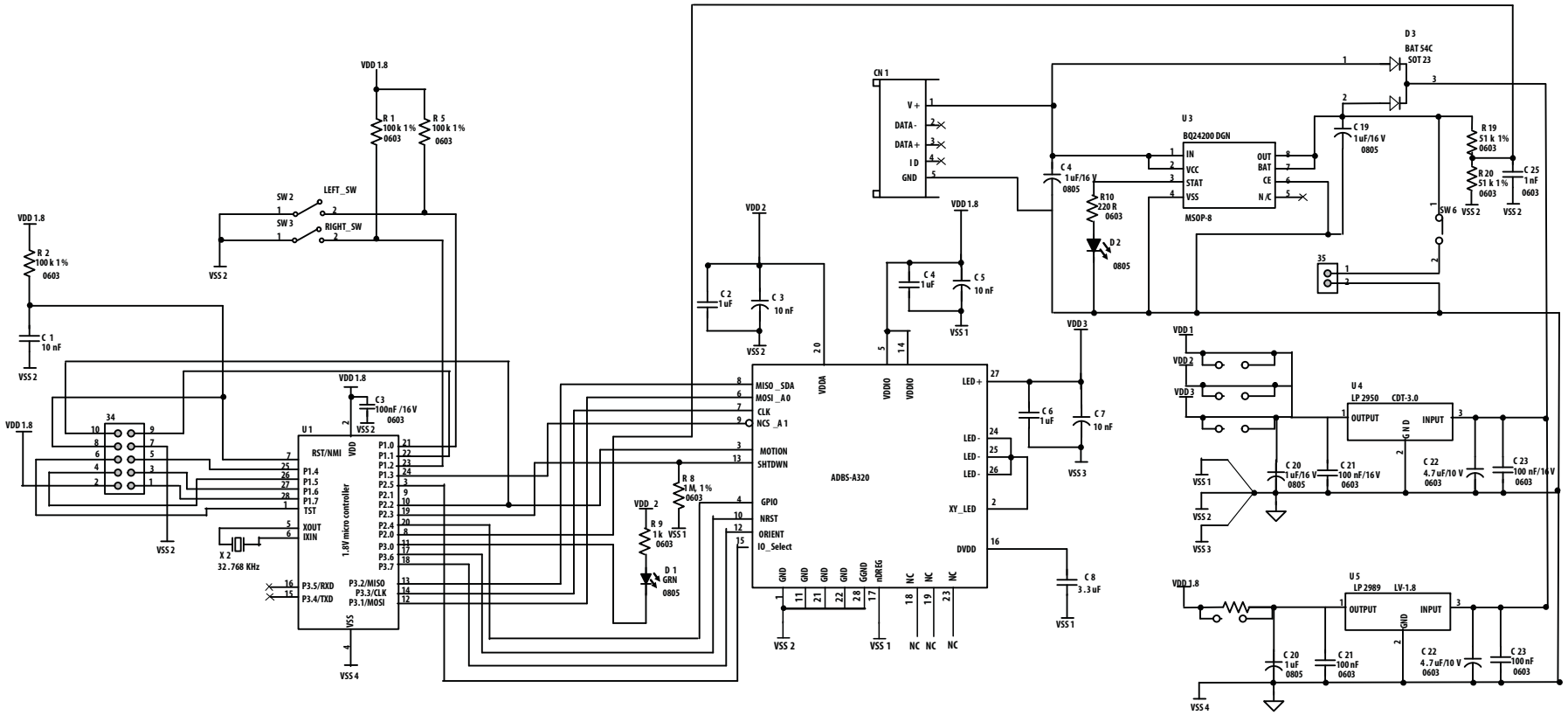


Figure 6b. Example of Transmissivity vs. Wavelength curve for standard Avago cover material



Note :- Dome + must be connected to MCU to detect button change state and Dome – can be connected to GND

Figure 7a. Schematic diagram for interface between ADBS-A320 and 3V microcontroller via SPI with internal Regulator 1.8V enabled



Note :- Dome + must be connected to MCU to detect button change state and Dome – can be connected to GND.

Figure 7b. Schematic diagram for interface between ADBS-A320 and 1.8V microcontroller via SPI with internal Regulator 1.8V enabled

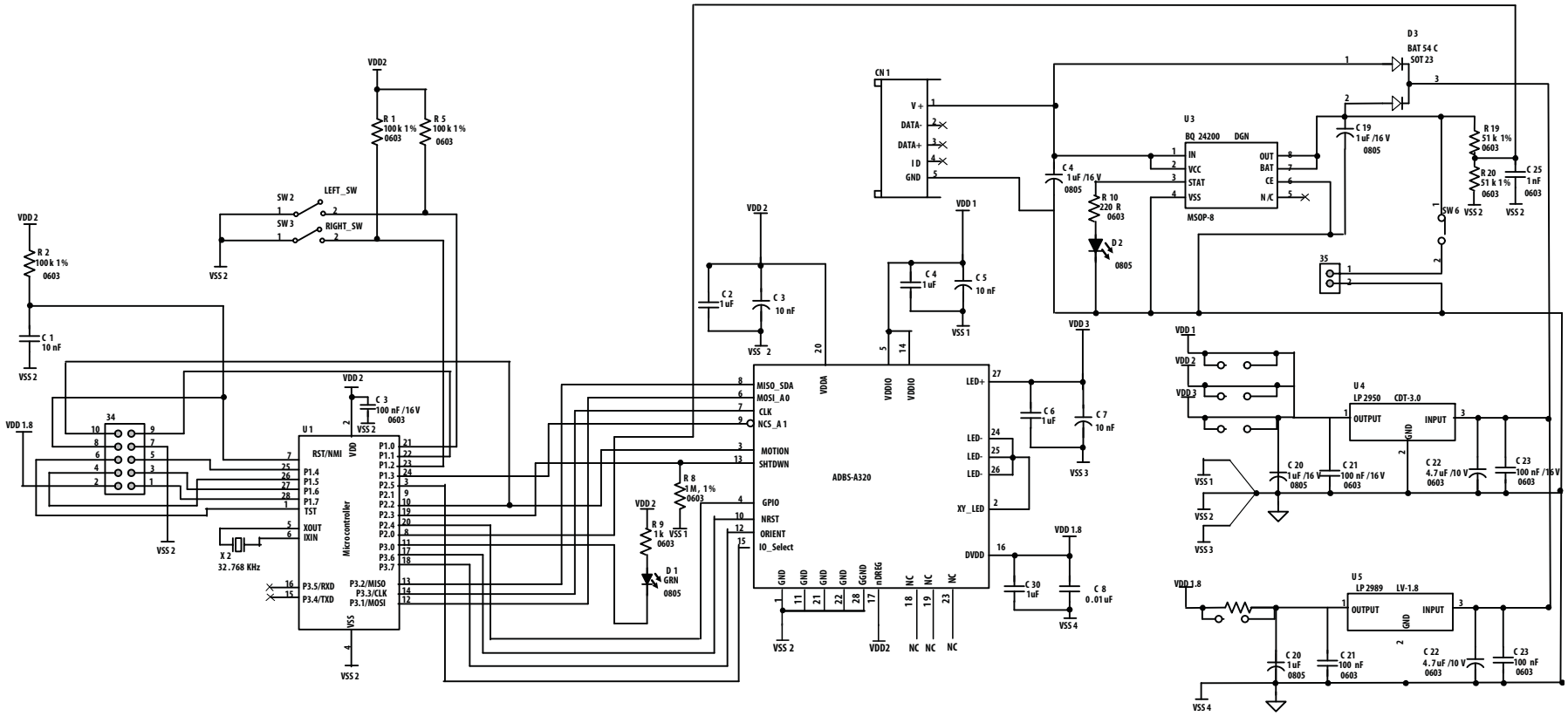
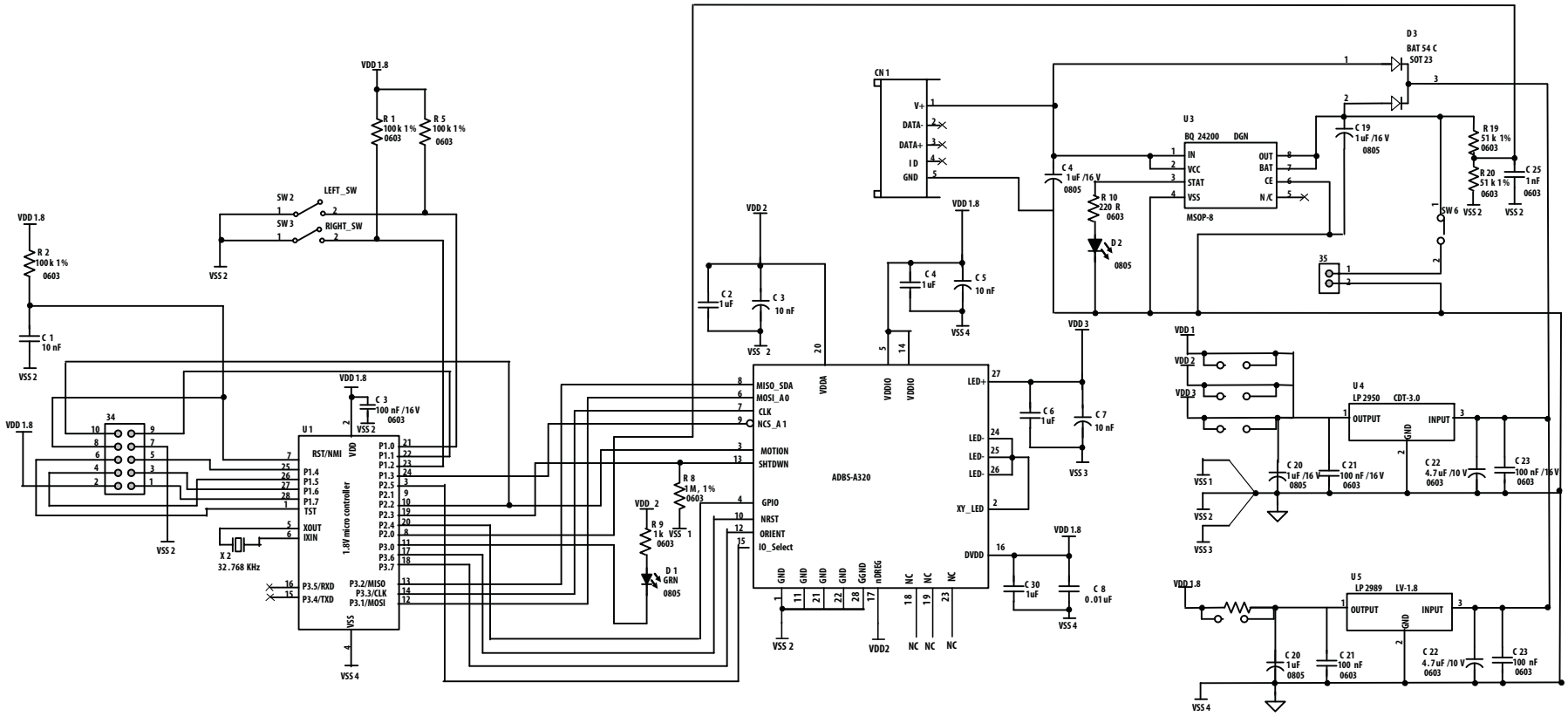


Figure 7c. Schematic diagram for interface between ADBS-A320 and 3V microcontroller via SPI with internal Regulator 1.8V disabled



Note :- Dome + must be connected to MCU to detect button change state and Dome – can be connected to GND.

Figure 7d. Schematic diagram for interface between ADBS-A320 and 1.8V microcontroller via SPI with internal Regulator 1.8V disabled

I/O Voltage options (values listed are typical)

Internal regulator status	nDREG pin	V_{DDA}	DV_{DD}	V_{DDIO}	I/O pin interface voltage	Notes for DV_{DD}	Notes for pin18 & 19 connection
Enabled	GND (Fig 7a)	2.8V	Output 1.8V with bypass capacitor 3.3uF	External 1.8V or V_{DDA}	1.8V or 2.8V	Do not use internal regulator output voltage as supply to other circuits.	MUST be No Connect (NC)
Disabled	V_{DDA} (Fig 7b)	2.8V	Input of 1.8V with 0.01uF and 1uF	External 1.8V or V_{DDA}	1.8V or 2.8V	Require external voltage supply.	Prefer if No Connect. Optional connection to GND allowed

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled following Avago Technologies recommendations.
- Passes IEC-55024 or CISPR 24 radiated susceptibility level when assembled following Avago Technologies recommendations.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Lead Solder Temp			260	°C	For 1.4 seconds
Moisture Sensitivity Level	MSL		1		Referring to JEDEC-J-STD-020.
Analog Supply Voltage	V_{DDA}	-0.5	3.6	V	
I/O Supply Voltage	V_{DDIO}	-0.5	3.6	V	
Digital Supply Voltage	DV_{DD}	-0.5	2	V	
LED supply voltage	V_{LED+}	-0.5	3.6	V	
ESD (sensor only)			2	kV	All pins, human body model JESD22-A114-E
Input Voltage	V_{IN}	-0.5	V_{DDA}+0.5 V_{DDIO}+0.5	V	nDREG_EN pin All pins except nDREG_EN pin
Latchup Current	Iout		20	mA	All Pins

Note - Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated may affect device reliability.

At power up, if DV_{DD} is powered up before V_{DDA}, DV_{DD} should never exceed V_{DDA} by more than 0.7V to avoid high inrush current. If DV_{DD} is powered up before V_{DDA}, then V_{DDA} must ramp up to stable voltage in less than 1.5seconds. In this case high inrush current of up to 180mA can be observed at DV_{DD}.

At power down, if V_{DDA} is powered down before DV_{DD} and V_{DDIO}, then DV_{DD} must ramp down to 0V in less than 1.5seconds. In this case high inrush current of up to 180mA can be observed at DV_{DD}.

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	-20		60	°C	
Analog supply voltage	V_{DDA}	2.6	2.8	3.3	Volts	Including V_{NA} noise.
I/O supply voltage	V_{DDIO}	1.65	1.8 or 2.8	3.3	Volts	Including V_{NA} noise. Sets I/O voltages but not for nDREG_EN. See fig 7a, 7b.
Digital supply voltage	DV_{DD}	1.65	1.8	1.95	Volts	Input voltage supply when nDREG pin is high. Input voltage supply not required when nDREG is GND
LED supply voltage	V_{LED+}	2.6	2.8	3.3	Volts	Including V_{NA} noise.
Power supply rise time	t_{VRT}	0.001		100	ms	0 to 2.8V
Supply noise (Sinusoidal)	V_{NA}			100	mV p-p	10kHz-50MHz
Speed	S			15	in/sec	Using prosthetic finger as surface

AC Electrical Specifications

Electrical Characteristics at 25°C, V_{DDA}=2.8V, DV_{DD}=1.8V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Motion delay after reset	$t_{MOT-RST}$	3.5		23	ms	From Hard or Soft_RESET register write to valid register write/read and motion, assuming motion is present
Shutdown	t_{SHTDWN}			50	ms	From SHTDWN pin active to low current
Wake from shutdown	t_{WAKEUP}	100			ms	From SHTDWN pin inactive to valid motion. Refer to section "Notes on Shutdown", also note $t_{MOT-RST}$
MOTION rise time	$t_{r-MOTION}$		150	300	ns	C_L = 100pF
MOTION fall time	$t_{f-MOTION}$		150	300	ns	C_L = 100pF
SHTDWN pulse width	$t_{P-SHTDWN}$	150			ms	
NRST pulse width	t_{NRST}	20			us	From edge of valid NRST pulse
Reset wait time after stable supply voltage	$t_{VRT-NRST}$	100			ms	
Transient Supply Current	I_{DDT}			75	mA	Max supply current for 500 usec for each supply voltages ramp from 0 to 3.3V

DC Electrical Specifications

Electrical Characteristics at 25°C, V_{DDA}=3.3V, DV_{DD}=1.95V at default LED setting 13mA.

		Internal regulator Enabled		Internal regulator Disabled			
Parameter		**Typical**	**Max**	**Typical**	**Max**	**Units**	**Notes**
DC average supply current in Run mode	I V_{DDA}	1.80	2.50	0.90	1.10	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	IDD_LED+	1.30	1.80	1.30	1.80	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	I DV_{DD}	0	0	0.90	1.40	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	Total	3.10	4.30	3.10	4.30	mA	
DC average supply current in Rest1 mode	I V_{DDA}	0.20	0.30	0.10	0.15	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	IDD_LED+	0.20	0.40	0.20	0.40	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	I DV_{DD}	0	0	0.10	0.15	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	Total	0.40	0.70	0.40	0.70	mA	
DC average supply current in Rest2 mode	I V_{DDA}	0.06	0.12	0.03	0.07	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	IDD_LED+	0.04	0.08	0.04	0.08	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	I DV_{DD}	0	0	0.03	0.05	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	Total	0.10	0.20	0.10	0.20	mA	
DC average supply current in Rest3 mode	I V_{DDA}	0.03	0.12	0.02	0.06	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	IDD_LED+	0.01	0.03	0.01	0.03	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	I DV_{DD}	0	0	0.01	0.06	mA	GPIO=SHTDWN=pull low, IO_MISO=NRST=ORIENT=pull high.
	Total	0.04	0.15	0.04	0.15	mA	
Analog shutdown supply current	$I_{DDSHTDWN}$ V_{DDA}	17	44.3	0	2	µA	GPIO=pull low, SHTDWN= IO_MISO=NRST=ORIENT=pull high.
Analog shutdown supply current	$I_{DDSHTDWN}$ VLED+	0	0.7	0	0.7	µA	GPIO=pull low, SHTDWN= IO_MISO=NRST=ORIENT=pull high.
Digital shutdown supply current	$I_{DDSHTDWN}$ DV_{DD}	0	0	3	15	µA	GPIO=pull low, SHTDWN= IO_MISO=NRST=ORIENT=pull high.

DC Electrical Specifications

Electrical Characteristics at 25°C, V_{DDA}=3.3V, DV_{DD}=1.95V at default LED setting 13mA.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
V_{DDIO} DC Supply Current	I V_{DDIO}			10	uA	Average current V_{DDIO}.
Analog peak supply current	I_{PEAK} V_{DDA}			2.5	mA	At LED register setting of 40mA.
LED+ peak supply current	I_{PEAK} LED+			49.5	mA	At LED register setting of 40mA.
Digital Peak supply current	I_{PEAK} DV_{DD}			1.5	mA	At LED register setting of 40mA.
Input Low Voltage	V_{IL}	-0.05	0	V_{DDIO}*0.35	V	IO_MOSI_A0, IO_CLK, IO_MISO_SDA, IO_NCS_A1, NRST, ORIENT, SHTDWN, IO_SELECT
Input High Voltage	V_{IH}	V_{DDIO} * 0.7	V_{DDIO}	V_{DDIO}+0.05	V	IO_MOSI_A0, IO_CLK, IO_MISO_SDA, IO_NCS_A1, NRST, ORIENT, SHTDWN, IO_SELECT
Input hysteresis	V_{HYS}	100			mV	
Input leakage current	I_{leak}		±1	±10	µA	IO_MOSI_A0, IO_CLK, IO_MISO_SDA, IO_NCS_A1, NRST, ORIENT, SHTDWN, IO_SELECT
Output Low Voltage	V_{OL}			0.2	V	I_{out}=1.2mA
Output High Voltage	V_{OH}	V_{DDIO}-0.2	V_{DDIO}-0.1		V	I_{out}=600uA
Input Capacitance	C_{in}			10	pF	MOSI, NCS, SCLK, SHTDWN

Notes on Power-up

The ADBS-A320 does not perform an internal power up self-reset; the NRST pin must be toggled every time power is applied. The appropriate sequence is as follows:

1. Apply power. See Notes on Power Up sequence below.
2. Set NCS pin high if using SPI. If TWI, then NCS_A1 will follow TWI address. Set Shutdown pin low and Orient. Set IO_Select pin to low (for TWI) or high (for SPI).
3. If in TWI mode, set A0 and A1 according to the Table TWI slave address in datasheet. This step is skipped if SPI mode is used.
4. In TWI, drive NRST low then high. This is optional for SPI. TWI slave address will only be selected after a NRST toggle is applied when A0 and A1 is set.
5. If in SPI mode, wait until sensor valid power up by reading Product ID register. If in TWI mode, skip this step.
6. If in SPI mode, perform soft reset by writing 0x5A to address 0x3a. In TWI mode, this is not required.
7. Write 0xE4 to address 0x60.
8. Set Speed Switching, write 0x62 with 0x12, 0x63 with 0x0E.
9. Check registers 0x64 with 0x08, 0x65 with 0x06, 0x66 with 0x40, 0x67 with 0x08, 0x68 with 0x48, 0x69 with 0x0a, 0x6a with 0x50, 0x6b with 0x48.
10. Check Assert/De-assert registers, 0x6d with 0xc4, 0x6e with 0x34, 0x6f with 0x3c, 0x70 with 0x18, 0x71 with 0x20.
11. Check Finger Presence Detect register, 0x75 with 0x50.
12. IF XY Quantization is used, check 0x73 with 0x99 and 0x74 with 0x02.
13. Write 0x10 to register 0x1C. This will activate burst mode. If burst mode not used then skip this step.
14. Read from registers 0x02, 0x03 and 0x04 (or read these same 3 bytes from burst motion) one time regardless the state of the motion pin.
15. Check 0x1a with 0x00 to set LED drive current to 13mA.
16. At power down, see Notes on Power Down sequence below.

Note on register settings

Please refer to the OFN A320 firmware design guide for tuning best Speed Switching, Assert/Deassert, Finger Presence Detect and XY Quantisation register settings.

Notes on Power Up sequence

When internal regulator is enabled, nDREG_EN = Ground, apply V_{DDA} and V_{DDIO} in any order.

When internal regulator is disabled, nDREG_EN = High, V_{DDA} must be applied prior to DV_{DD}. The sensor must power up from V_{DDA} first to a stable voltage. Then apply DV_{DD}. V_{DDIO} can be applied in any order.

See Absolute Maximum Rating for other condition.

If V_{DDIO} is applied before V_{DDA} in internal regulator enabled or V_{DDIO} is applied before V_{DDA} and DV_{DD} in internal regulator disabled, while all sensor I/O pins are at high or low, then a small leakage current of 1uA can be expected at V_{DDIO}.

If V_{DDIO} is applied before V_{DDA} in internal regulator enabled or V_{DDIO} is applied before V_{DDA} and DV_{DD} in internal regulator disabled, while all sensor I/O pins are floating, then a leakage current of up to 1mA can be expected at V_{DDIO}.

If V_{DDIO} is Grounded, then the TWI line will be pulled down and rendered not operational. V_{DDIO} must be applied for I/O pins to be functional.

Notes on Power Down sequence

During power down and internal regulator disabled, it is a MUST to ramp down DV_{DD} first then followed by V_{DDA} to 0V or all at the same time. Do not power down V_{DDA} before power down DV_{DD}.

If V_{DDA} is powered down before DV_{DD}, DV_{DD} should never exceed V_{DDA} by more than 0.7V to avoid high inrush current.

During power-up there will be a period of time after the power supply is high but before any clocks are available. See power sequence chart below reference to "Notes on Power up" steps.

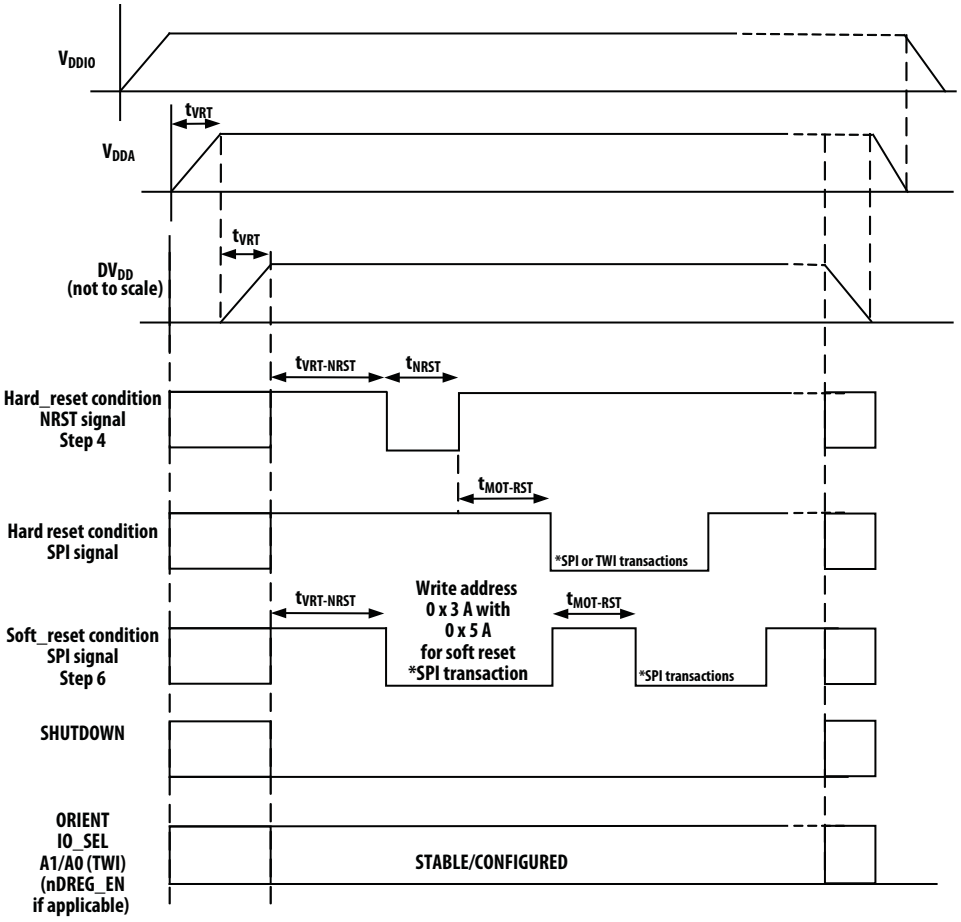


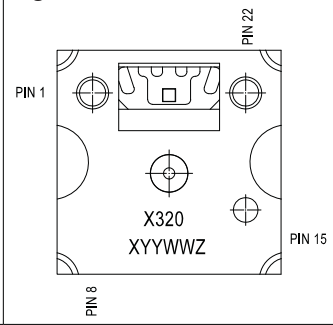
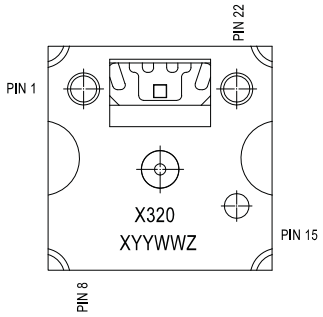
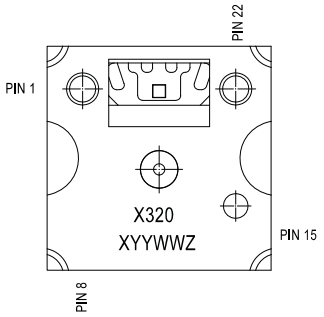
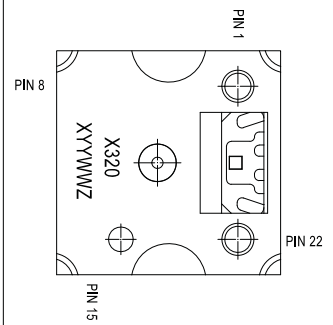
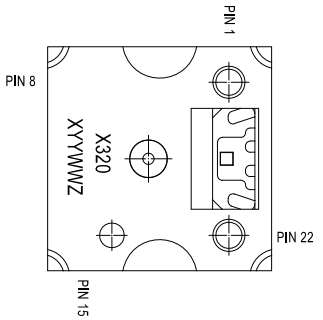
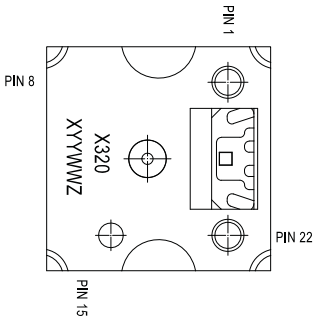
Figure 8. Power up and down sequence

As in step 4, in TWI mode, the sensor must be toggle with hard reset. The hard reset via toggling NRST pin high to low then high again must observe $t_{VRT-NRST}$ and t_{NRST}. Then a time of $t_{MOT-RST}$ must be observed before accessing the sensor registers via SPI or TWI ports. See two graphs for Hard reset condition.

If SPI mode is used, then hard reset is not required. Instead a soft reset can be employed. Note that time $t_{VRT-NRST}$ and $t_{MOT-RST}$ must be observed before accessing SPI ports.

The Shutdown, Orient, IO_Select and TWI ports are stable after proper power up procedures.

The table below shows the state of the various pins during power-up and reset.

State of Signal Pins After V_{DDA} is Valid			
Pin	**NCS high before reset**	**NCS Low before reset**	**After Reset**
NCS	High	Low	Functional
MISO	Undefined	Functional	Depends on NCS
SCLK	Ignored	Functional	Depends on NCS
MOSI	Ignored	Functional	Depends on NCS
XY_LED	Undefined	Undefined	Functional
MOTION	Undefined	Undefined	Functional
SHTDWN	Must be low	Must be low	Functional
NRST	High	High	High
IO_Select	SPI: High, TWI:Low	SPI: High, TWI:Low	SPI: High, TWI:Low
ORIENT Top view	High 	High 	High 
ORIENT Top view	Low 	Low 	Low 
GPIO	Undefined	Undefined	Undefined

Notes on Shutdown and Reset

The ADBS-A320 can be set in Shutdown mode by asserting or setting SHTDWN pin high. During the shutdown state, supply voltages V_{DDIO} and DV_{DD} must be maintained above the minimum level. If these conditions are not met, then the sensor must be restarted by powering down then powering up again for proper operation. Any register settings must then be reloaded.

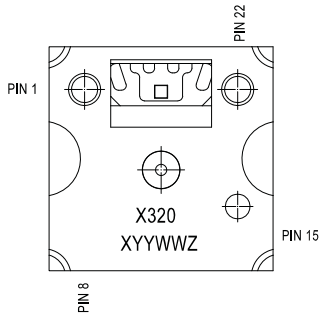
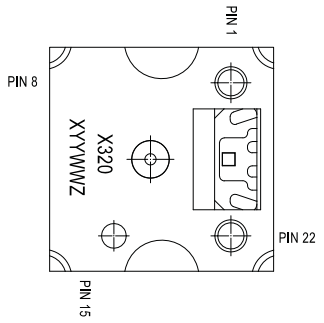
During the shutdown state, supply voltages V_{DDIO} and DV_{DD} must be maintained above the minimum level. For proper operation, SHTDWN pulse width must be at least $t_{P\text{-}SHTDWN}$. Shorter pulse widths may cause the chip to enter an undefined state. In addition, the SPI or TWI port should not be accessed when SHTDWN is asserted. (Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted.) The table below shows the state of various pins during shutdown. After deasserting SHTDWN, wait t_{WAKEUP} before accessing the SPI port. Reinitializing the sensor from shutdown state will retain all register data that were written to the sensor prior to shutdown (see register table page 34 for list of registers). If the internal regulator is disabled and V_{DDA} is removed but DV_{DD} is retained, reinitializing the sensor from shutdown state will retain all register data that were written to the sensor prior to shutdown. See register table page 34 for list of registers.

The reset of the sensor via Soft_RESET register or through the NRST pin would reset all registers to the default value. Any register settings must then be reloaded.

Power management modes

The ADBS-A320 has three power-saving modes. Each mode has a different motion detection period, affecting response time to sensor motion (Response Time). The sensor automatically changes to the appropriate mode, depending on the time since the last reported motion (Downshift Time). The parameters of each mode are shown in the following table.

Mode	Response Time (nominal)	Downshift Time (nominal)
Rest 1	19.5 ms	250 ms
Rest 2	96 ms	9.5 s
Rest 3	482 ms	582 s

Pin	SHTDWN active
NCS	Functional*
MISO	Undefined
SCLK	Undefined
MOSI	Undefined
XY_LED	Low current
MOTION	Undefined
NRST	High
IO_Select	SPI:High, TWI:Low
ORIENT Top view	High 
ORIENT Top view	Low 
GPIO	Undefined

*In Regulator disabled mode, NCS pin must be held to 1 (high) if SPI bus is shared with other devices.

Note: There are long wakeup times from shutdown. These features should not be used for power management during normal sensor motion.

Motion Pin Timing

The motion pin is a level-sensitive output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is data in the Delta_X or Delta_Y registers. Clearing the motion bit (by reading Delta_Y and Delta_X, or writing to the Motion register) will put the motion pin high.

LED Mode

For power savings, the LED will not be continuously on. ADBS-A320 will flash the LED only when needed.

Serial Peripheral Interface (SPI)

AC Electrical Specifications

Electrical Characteristics at 25°C, V_{DDA}=2.8V, DV_{DD}=1.8V.

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Serial Port Clock Frequency	f_{sclk}			1	MHz	Active drive, 50% duty cycle
MISO rise time	tr-MISO		150	300	ns	CL = 100pF
MISO fall time	tf-MISO		150	300	ns	CL = 100pF
MISO delay after SCLK	tDLY-MISO			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO hold time	thold-MISO	0.5		1/fSCLK	µs	Data held until next falling SCLK edge
MOSI hold time	thold-MOSI	200			ns	Amount of time data is valid after SCLK rising edge
MOSI setup time	tsetup-MOSI	120			ns	From data valid to SCLK rising edge
SPI time between write commands	tSWW	30			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte.
SPI time between write and read commands	tSWR	20			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte.
SPI time between read and subsequent commands	tSRW tSRR	500			ns	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command.
SPI read address-data delay	tSRAD	4			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read.
NCS inactive after motion burst	tBEXIT	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK active	tNCS-SCLK	120			ns	From NCS falling edge to first SCLK falling edge
SCLK to NCS inactive (for read operation)	tSCLK-NCS	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS inactive (for write operation)	tSCLK-NCS	20			us	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS to MISO high-Z	tNCS-MISO			500	ns	From NCS rising edge to MISO high-Z state

The synchronous serial port is used to set and read parameters in the ADBS-A320, and to read out the motion information.

The port is a four wire serial port. The host micro-controller always initiates communication; the ADBS-A320 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port:

SCLK: Clock input. It is always generated by the master (the micro-controller).

MOSI: Input data. (Master Out/Slave In)

MISO: Output data. (Master In/Slave Out)

NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Write Operation

Write operation, defined as data going from the micro-controller to the ADBS-A320, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The ADBS-A320 reads MOSI on rising edges of SCLK.

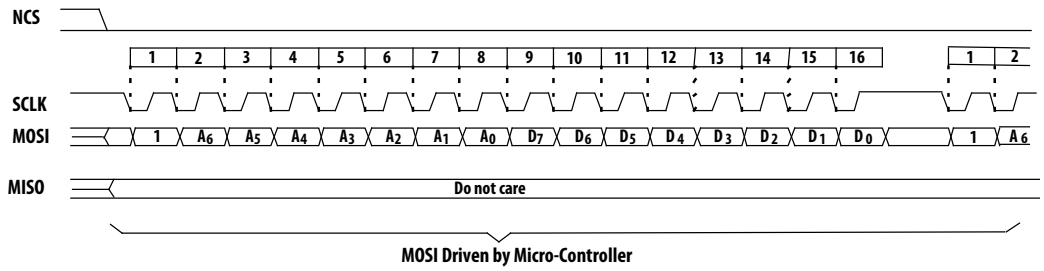


Figure 9. Write Operation

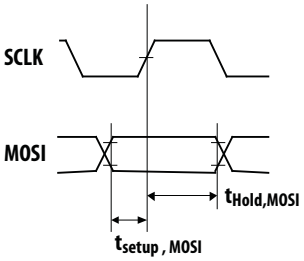


Figure 10. MOSI Setup and Hold Time

Read Operation

A read operation, defined as data going from the ADBS-A320 to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADBS-A320 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

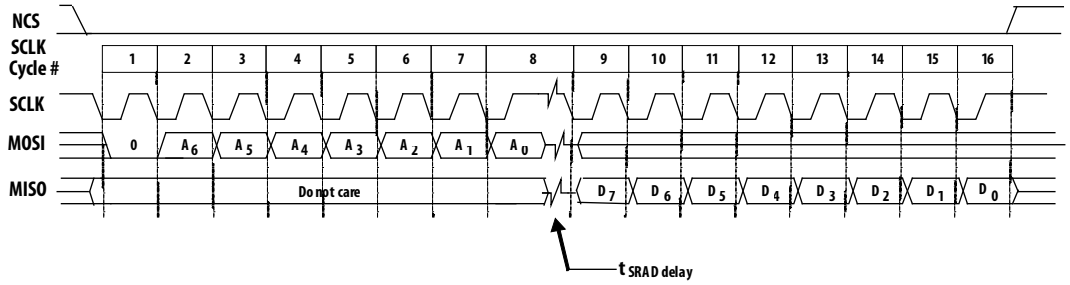
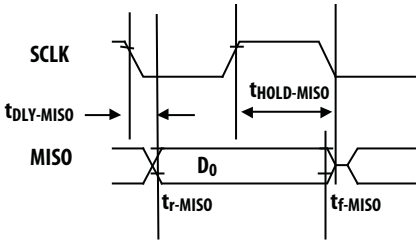


Figure 11. Read Operation



NOTE: The $0.5/f_{SCLK}$ minimum high state of SCLK is also the minimum MISO data hold time of the ADBS-A320. Since the falling edge of SCLK is actually the start of the next read or write command, the ADBS-A320 will hold the state of data on MISO until the falling edge of SCLK.

Figure 12. MISO Delay and Hold Time

Required timing between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.

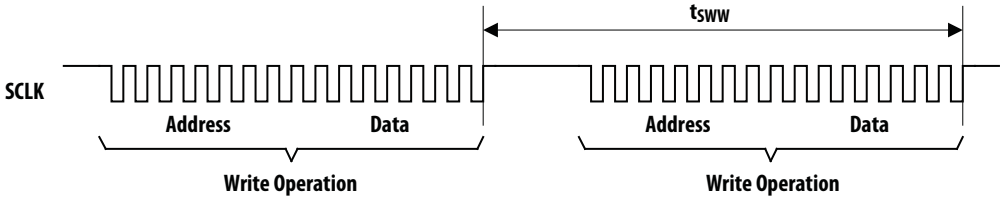


Figure 13. Timing between two write commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.

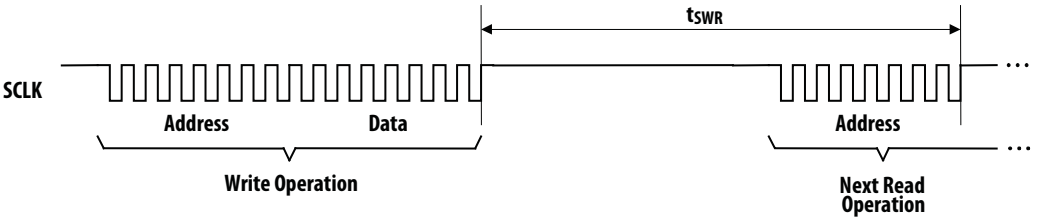


Figure 14. Timing between write and read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.

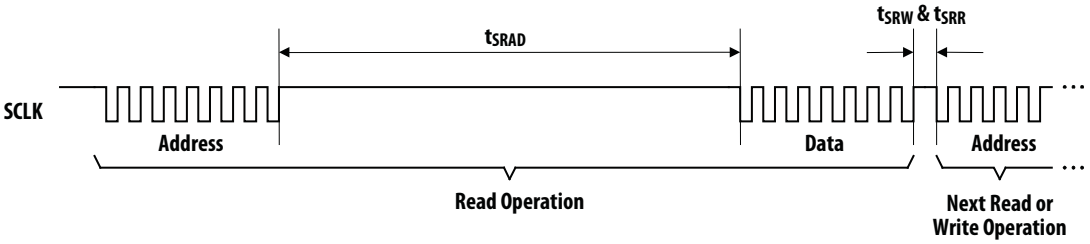


Figure 15. Timing between read and either write or subsequent read commands

During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the ADBS-A320 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation.

Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is activated by writing 0x10 to register 0x1c IO_MODE. Then the burst mode data can be read by reading the Motion register 0x02. The ADBS-A320 will respond with the contents of the Motion, Delta_Y, Delta_X, SQUAL, Shutter_Upper, Shutter_Lower and Maximum_Pixel registers in that order. The burst transaction can be terminated after the first 3 bytes of the sequence are read by bringing the NCS pin high. After sending the register address, the micro-controller must wait t_{SRAD} and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data is latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

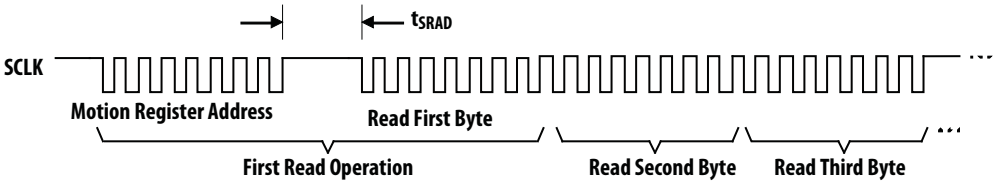


Figure 16. Motion Burst Timing

Two – Wire Interface (TWI)

ADBS-A320 uses a two-wire serial control interface compatible with I2C. The parameters are listed below.

Electrical Characteristics at 25°C, V_{DDA}=2.8V, DV_{DD}=1.8V.

Parameter	Symbol	Minimum	Maximum	Units	Notes
SCL clock frequency	fscl		400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	0.6	–	µs	
LOW period of the SCL clock	t_{LOW}	1.0	–	µs	
HIGH period of the SCL clock	t_{HIGH}	0.6	–	µs	
Set up time for a repeated START condition	$t_{SU;STA}$	0.6	–	µs	
Data hold time	$t_{HD;DAT}$	0(2)	0.9(3)	µs	
Data set-up time	$t_{SU;DAT}$	100	–	ns	
Rise time of both SDA and SCL signals	t_r	20+0.1C_b(4)	300	ns	
Fall time of both SDA and SCL signals	t_f	20+0.1C_b(4)	300	ns	
Set up time for STOP condition	$t_{SU;STO}$	0.6	–	µs	
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	µs	
Capacitive load for each bus line	C_b	–	400	pF	
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 VDDA	–	V	
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 V_{DDA}		V	

Notes:
1. All values referred to V_{IHMIN} and V_{ILMAX} levels.
2. A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum has $t_{HD;DAT}$ only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.
4. C_B = total capacitance of one bus line in pF.

The ADBS-A320 responds to one of the following selectable slave device addresses depending on the IO_A0 and IO_A1 input pin state. These pins should be set to avoid conflict with any other devices that might be sharing the bus.

Table 1. TWI slave address

A0	A1	Slave Address (Hex)
0	0	33
0	1	37
0	NC	3b
1	0	53
1	1	57
1	NC	5b
NC	0	63
NC	1	67
NC	NC	6b

Serial Transfer Clock and Serial Data signals

The serial control interface uses two signals: a serial transfer clock (SCL) signal and a serial data (SDA) signal. Always driven by the master, SCL synchronizes the serial transmission of data bits on SDA. The frequency of SCL may vary throughout a transfer, as long as the timing is greater than the minimum timing.

SDA is bi-directional. The host (master) can read from or write to the ADBS-A320. The host (typically a microcontroller) drives SCL and SDA in a write operation or requesting information from the ADBS-A320. The ADBS-A320 drives the SDA only under two conditions. First, when responding with an acknowledge (ACK) bit after receiving data from the host, or second, when sending data to the host at the host's request. Data is sent in Eight-bit packets.

Start and Stop of Synchronous Operation

The host initiates and terminates all data transfers. Data transfers are initiated by driving SDA from high to low while holding SCL high. Data transfers are terminated by driving SDA from low to high while SCL is held high.

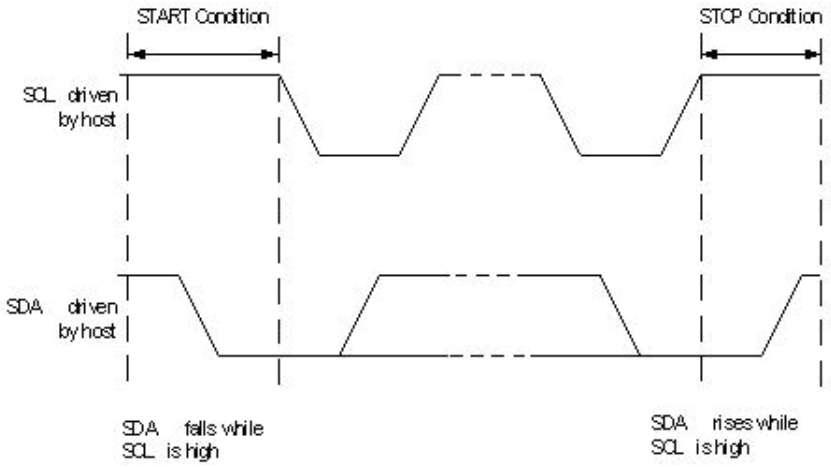


Figure 17. TWI Start and Stop operation

Acknowledge/Not Acknowledge Bit

After a start condition, a single acknowledge/not acknowledge bit follows each Eight-bit data packet. The device receiving the data drives the acknowledge/not acknowledge signal on SDA. Acknowledge (ACK) is defined as 0 and not acknowledge (NAK) is defined as 1.

Packet Formats

Read and write operations between the host and the ADBS-A320 use three types of host driven packets and one type of ADBS-A320 driven packet. All packets are eight bits long with the most significant bit first, followed by an acknowledge bit.

Slave Device Address (DA)

Command packets contain a 7-bit ADBS-A320 device address and an active low read/write bit (R/W).

First bit of packet							Last bit of packet
Device Address							R/$\overline{W}$
DA[6]	DA[5]	DA[4]	DA[3]	DA[2]	DA[1]	DA[0]	Write = 0 Read = 1

Register Address Packets (RA)

The address packets contain an auto-increment (ai) bit and a 7-bit address. If the 'ai' bit is set, the slave will process data from successive addresses in successive bytes. For example, registers 0x01, 0x02, and 0x03 can be written by setting the 'ai' bit to one with address 0x01. The host would send three bytes of data, and the host would terminate with a P condition.

First bit of packet							Last bit of packet
Auto increment	Register Address						
Auto increment=1, No increment=0	RA[6]	RA[5]	RA[4]	RA[3]	RA[2]	RA[1]	RA[0]

Data Packet (DP)

Contains 8 data bits and may be sent by the host or the ADBS-A320.

First bit of packet							Last bit of packet
Data							
DP[7]	DP[6]	DP[5]	DP[4]	DP[3]	DP[2]	DP[1]	DP[0]

Host Driven Packets

The host initiates all data transmission with a START condition. Next, slave address and register address packets are sent. If there is a device address match, the ADBS-A320 then responds to each Eight-bit data transmission with an acknowledge signal (SDA = 0). Data is transmitted with the most significant bit first.

To terminate the transfer of host driven packets, the host follows the ADBS-A320's ACK with a STOP condition. The host can also issue a START condition after the ADBS-A320's ACK if it wants to start a new data transfer.

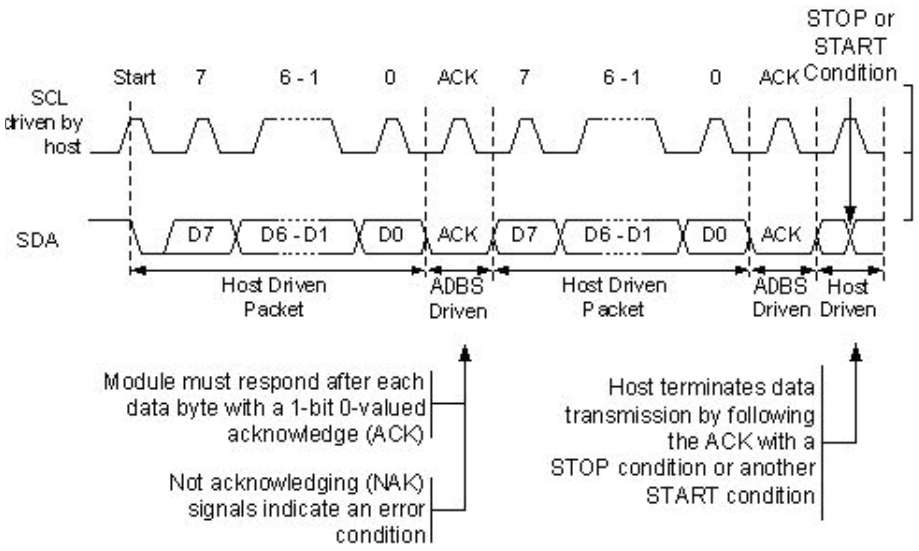


Figure 18. Host packets

ADBS-A320 Driven Packets

By request of the host, the ADBS-A320 acknowledges a read request and then outputs a data byte transmitting the most significant bit (7) first. If the host intends to continue the data transfer, the host acknowledges the ADBS-A320. If the host intends to terminate the transfer, it responds with not acknowledge (SDA = 1), and then drives SDA to generate a STOP condition. The host can also drive a START condition if it wants to begin a new data transfer with the same ADBS-A320.