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ADC1215S series

Single 12-bit ADC; 65 Msps, 80 Msps, 105 Msps or 125 Msps with input buffer; CMOS or LVDS DDR digital outputs

Rev. 03 — 2 July 2012 Product data sheet

1. General description

The ADC1215S is a single channel 12-bit Analog-to-Digital Converter (ADC) optimized for high dynamic performance and low power consumption at sample rates up to 125 Msps. Pipelined architecture and output error correction ensure the ADC1215S is accurate enough to guarantee zero missing codes over the entire operating range. Supplied from a single 3 V source, it can handle output logic levels from 1.8 V to 3.3 V in CMOS mode because of a separate digital output supply.

The ADC1215S supports the Low Voltage Differential Signalling (LVDS) Double Data Rate (DDR) output standard. An integrated Serial Peripheral Interface (SPI) allows the user to easily configure the ADC.

The device also includes a SPI programmable full-scale to allow flexible input voltage range from 1 V to 2 V (peak-to-peak). With excellent dynamic performance from the baseband to input frequencies of 170 MHz or more, the ADC1215S is ideal for use in communications, imaging and medical applications - especially in high Intermediate Frequency (IF) applications because of the integrated input buffer. The input buffer ensures that the input impedance remains constant and low and the performance consistent over a wide frequency range.

2. Features and benefits

- SNR, 70 dBFS / SFDR, 86 dBc
- Sample rate up to 125 Msps
- 12-bit pipelined ADC core
- Clock input divided by 2 for less jitter contribution
- Integrated input buffer
- Flexible input voltage range: 1 V (p-p) to 2 V (p-p)
- CMOS or LVDS DDR digital outputs
- Pin compatible with the ADC1415S series, the ADC1015S series and the ADC1115S125
- Input bandwidth, 600 MHz
- Power dissipation, 635 mW at 80 Msps, including analog input buffer
- SPI
- Duty cycle stabilizer
- Fast OuT-of-Range (OTR) detection
- Offset binary, two's complement, gray code
- Power-down and Sleep modes
- HVQFN40 package

3. Applications

- Wireless and wired broadband communications
- Portable instrumentation
- Imaging systems
- Digital predistortion loop, power amplifier linearization
- Spectral analysis
- Ultrasound equipment
- Software defined radio

4. Ordering information

Table 1. Ordering information

Type number	f_s (Msps)	Package		
		Name	Description	Version
ADC1215S125HN-C1	125	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-6
ADC1215S105HN-C1	105	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-6
ADC1215S080HN-C1	80	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-6
ADC1215S065HN-C1	65	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-6

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5. Block diagram

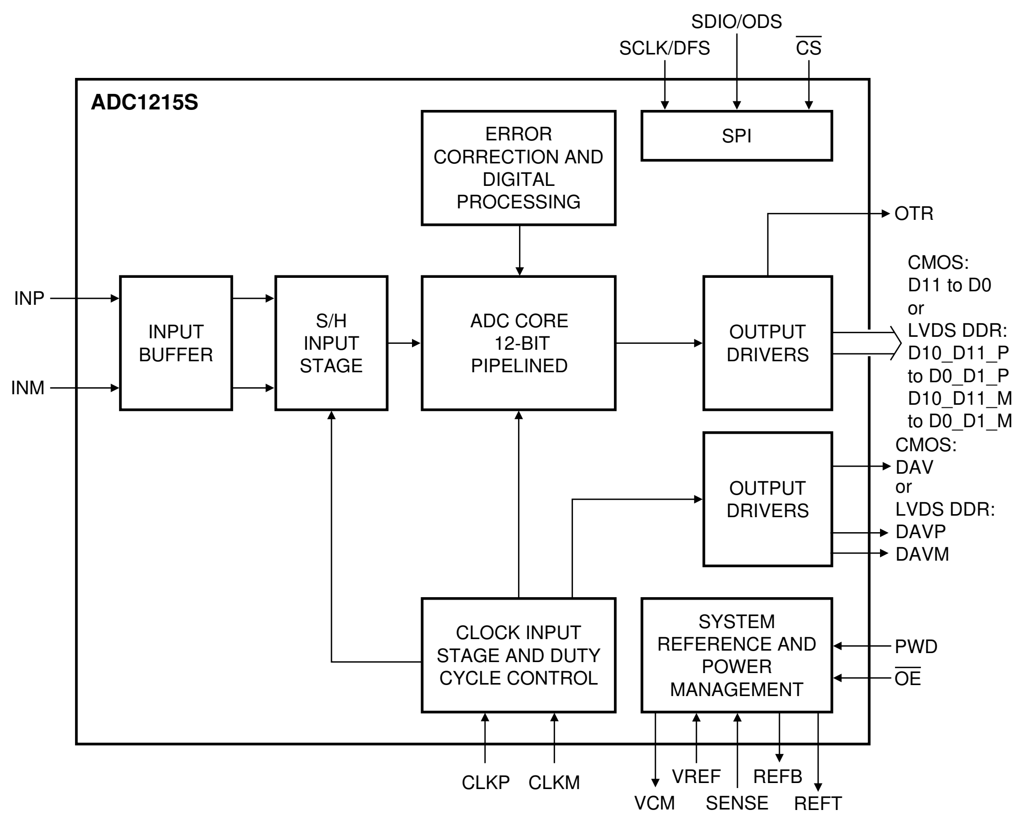

Fig 1. Block diagram

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6. Pinning information

6.1 Pinning

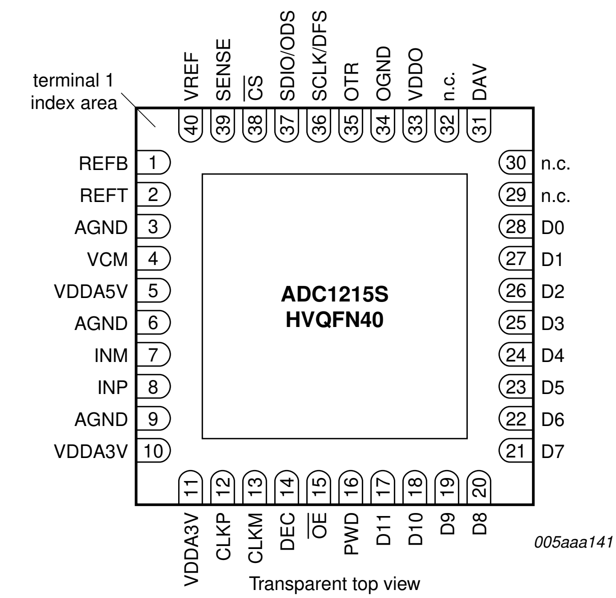

Fig 2. Pin configuration with CMOS digital outputs selected

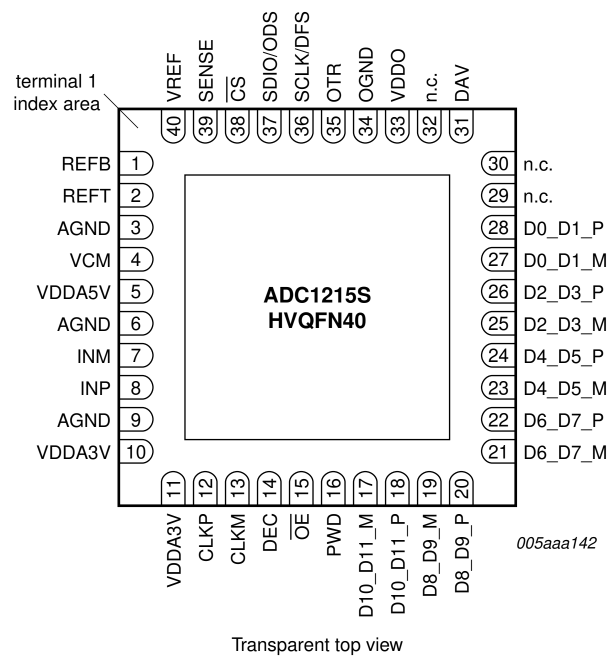

Fig 3. Pin configuration with LVDS/DDR digital outputs selected

6.2 Pin description

Table 2. Pin description (CMOS digital outputs)

Symbol	Pin	Type [1]	Description
REFB	1	O	bottom reference
REFT	2	O	top reference
AGND	3	G	analog ground
VCM	4	O	common-mode output voltage
VDDA5V	5	P	5 V analog power supply
AGND	6	G	analog ground
INM	7	I	complementary analog input
INP	8	I	analog input
AGND	9	G	analog ground
VDDA3V	10	P	3 V analog power supply
VDDA3V	11	P	3 V analog power supply
CLKP	12	I	clock input
CLKM	13	I	complementary clock input
DEC	14	O	regulator decoupling node
$\overline{\text{OE}}$	15	I	output enable, active LOW
PWD	16	I	power down, active HIGH

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Table 2. Pin description (CMOS digital outputs) *…continued*

Symbol	Pin	Type [1]	Description
D11	17	O	data output bit 11 (Most Significant Bit (MSB))
D10	18	O	data output bit 10
D9	19	O	data output bit 9
D8	20	O	data output bit 8
D7	21	O	data output bit 7
D6	22	O	data output bit 6
D5	23	O	data output bit 5
D4	24	O	data output bit 4
D3	25	O	data output bit 3
D2	26	O	data output bit 2
D1	27	O	data output bit 1
D0	28	O	data output bit 0 (Least Significant Bit (LSB))
n.c.	29	-	not connected
n.c.	30	-	not connected
DAV	31	O	data valid output clock
n.c.	32	-	not connected
VDDO	33	P	output power supply
OGND	34	G	output ground
OTR	35	O	out of range
SCLK/DFS	36	I	SPI clock / data format select
SDIO/ODS	37	I/O	SPI data IO / output data standard
$\overline{CS}$	38	I	SPI chip select
SENSE	39	I	reference programming pin
VREF	40	I/O	voltage reference input/output

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

Table 3. Pin description (LVDS/DDR) digital outputs)

Symbol	Pin [1]	Type [2]	Description
D10_D11_M	17	O	differential output data D10 and D11 multiplexed, complement
D10_D11_P	18	O	differential output data D10 and D11 multiplexed, true
D8_D9_M	19	O	differential output data D8 and D9 multiplexed, complement
D8_D9_P	20	O	differential output data D8 and D9 multiplexed, true
D6_D7_M	21	O	differential output data D6 and D7 multiplexed, complement
D6_D7_P	22	O	differential output data D6 and D7 multiplexed, true
D4_D5_M	23	O	differential output data D4 and D5 multiplexed, complement
D4_D5_P	24	O	differential output data D4 and D5 multiplexed, true
D2_D3_M	25	O	differential output data D2 and D3 multiplexed, complement
D2_D3_P	26	O	differential output data D2 and D3 multiplexed, true
D0_D1_M	27	O	differential output data D0 and D1 multiplexed, complement
D0_D1_P	28	O	differential output data D0 and D1 multiplexed, true
n.c.	29	-	not connected

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Table 3. Pin description *...continued* **(LVDS/DDR) digital outputs)**

Symbol	Pin [1]	Type [2]	Description
n.c.	30	-	not connected
DAVM	31	O	data valid output clock, complement
DAVP	32	O	data valid output clock, true

[1] Pins 1 to 16 and pins 33 to 40 are the same for both CMOS and LVDS DDR outputs (see Table 2)

[2] P: power supply; G: ground; I: input; O: output; I/O: input/output.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_O	output voltage	pins D11 to D0 or pins D10_D11_P to D0_D1_P and D10_D11_M to D0_D1_M	−0.4	+3.9	V
$V_{DDA(3V)}$	analog supply voltage 3 V	on pin VDDA3V	−0.5	+4.6	V
$V_{DDA(5V)}$	analog supply voltage 5 V	on pin VDDA5V	−0.5	+6.0	V
V_{DDO}	output supply voltage		−0.5	+4.6	V
T_{stg}	storage temperature		−55	+125	°C
T_{amb}	ambient temperature		−40	+85	°C
T_j	junction temperature		-	125	°C

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	[1]	30.5	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	[1]	13.3	K/W

[1] Value for 6 layers board in still air with a minimum of 25 thermal vias.

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9. Static characteristics

Table 6. Static characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
$V_{DDA(5V)}$	analog supply voltage 5 V		4.75	5.0	5.25	V
$V_{DDA(3V)}$	analog supply voltage 3 V		2.85	3.0	3.4	V
V_{DDO}	output supply voltage	CMOS mode	1.65	1.8	3.6	V
		LVDS DDR mode	2.85	3.0	3.6	V
$I_{DDA(5V)}$	analog supply current 5 V	f_{clk} = 125 Msps; f_i = 70 MHz	-	46	-	mA
$I_{DDA(3V)}$	analog supply current 3 V	f_{clk} = 125 Msps; f_i = 70 MHz	-	205	-	mA
I_{DDO}	output supply current	CMOS mode; f_{clk} = 125 Msps; f_i = 70 MHz	-	12	-	mA
		LVDS DDR mode: f_{clk} = 125 Msps; f_i = 70 MHz	-	39	-	mA
P	power dissipation	ADC1215S125; analog supply only	-	840	-	mW
		ADC1215S105; analog supply only	-	770	-	mW
		ADC1215S080; analog supply only	-	635	-	mW
		ADC1215S065; analog supply only	-	580	-	mW
		Power-down mode	-	2	-	mW
		Standby mode	-	40	-	mW
Clock inputs: pins CLKP and CLKM						
LVPECL						
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	-	1.6	-	V
SINE wave						
$V_{i(clk)dif}$	differential clock input voltage	peak	-	±3.0	-	V
LVCMOS						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDA(3V)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDA(3V)}$	-	-	V
Logic inputs: pins PWD and $\overline{OE}$						
V_{IL}	LOW-level input voltage		0	-	0.8	V
V_{IH}	HIGH-level input voltage		2	-	$V_{DDA(3V)}$	V
I_{IL}	LOW-level input current		-	55	-	µA
I_{IH}	HIGH-level input current		-	65	-	µA
Serial peripheral interface: pins $\overline{CS}$, SDIO/ODS, SCLK/DFS						
V_{IL}	LOW-level input voltage		0	-	$0.3V_{DDA(3V)}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDA(3V)}$	-	$V_{DDA(3V)}$	V

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Table 6. Static characteristics[1] *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{IL}	LOW-level input current		−10	-	+10	μA
I_{IH}	HIGH-level input current		−50	-	+50	μA
C_I	input capacitance		-	4	-	pF
Digital outputs, CMOS mode: pins D11 to D0, OTR, DAV						
Output levels, V_{DDO} = 3 V						
V_{OL}	LOW-level output voltage		OGND	-	$0.2V_{DDO}$	V
V_{OH}	HIGH-level output voltage		$0.8V_{DDO}$	-	V_{DDO}	V
C_O	output capacitance	high impedance; $\overline{OE}$ = HIGH	-	3	-	pF
Output levels, V_{DDO} = 1.8 V						
V_{OL}	LOW-level output voltage		OGND	-	$0.2V_{DDO}$	V
V_{OH}	HIGH-level output voltage		$0.8V_{DDO}$	-	V_{DDO}	V
Digital outputs, LVDS mode: pins D10_D11_P to D0_D1_P, D10_D11_M to D0_D1_M, DAVP and DAVM						
Output levels, V_{DDO} = 3 V only, R_{load} = 100 Ω						
$V_{O(offset)}$	output offset voltage	output buffer current set to 3.5 mA	-	1.2	-	V
$V_{O(dif)}$	differential output voltage	output buffer current set to 3.5 mA	-	350	-	mV
C_O	output capacitance		-	3	-	pF
Analog inputs: pins INP and INM						
I_I	input current		−5	-	+5	μA
R_I	input resistance		-	550	-	Ω
C_I	input capacitance		-	1.3	-	pF
$V_{I(cm)}$	common-mode input voltage	$V_{INP} = V_{INM}$	0.9	1.5	2	V
B_i	input bandwidth		-	600	-	MHz
$V_{I(dif)}$	differential input voltage	peak-to-peak	1	-	2	V
Common mode output voltage: pin VCM						
$V_{O(cm)}$	common-mode output voltage		-	$0.5V_{DDA(3V)}$	-	V
$I_{O(cm)}$	common-mode output current		-	4	-	mA
I/O reference voltage: pin VREF						
V_{VREF}	voltage on pin VREF	output	-	0.5 to 1	-	V
		input	0.5	-	1	V

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Table 6. Static characteristics[1] *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Accuracy						
INL	integral non-linearity		−1.25	±0.25	+1.25	LSB
DNL	differential non-linearity	guaranteed no missing codes	−0.25	±0.12	+0.25	LSB
E_{offset}	offset error		-	±2	-	mV
E_G	gain error		-	±0.5	-	%FS
Supply						
PSRR	power supply rejection ratio	200 mV (p-p) on $V_{DDA(3V)}$	-	−54	-	dBc

[1] Typical values measured at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V; T_{amb} = 25 °C and C_L = 5 pF; minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V, $V_{INP} - V_{INM}$ = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

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10. Dynamic characteristics

10.1 Dynamic characteristics

Table 7. Dynamic characteristics[1]

Symbol	Parameter	Conditions	ADC1215S065			ADC1215S080			ADC1215S105			ADC1215S125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Analog signal processing															
α_{2H}	second harmonic level	f_i = 3 MHz	-	87	-	-	87	-	-	86	-	-	88	-	dBc
		f_i = 30 MHz	-	86	-	-	86	-	-	86	-	-	87	-	dBc
		f_i = 70 MHz	-	85	-	-	85	-	-	84	-	-	85	-	dBc
		f_i = 170 MHz	-	82	-	-	82	-	-	81	-	-	83	-	dBc
α_{3H}	third harmonic level	f_i = 3 MHz	-	86	-	-	86	-	-	85	-	-	87	-	dBc
		f_i = 30 MHz	-	85	-	-	85	-	-	85	-	-	86	-	dBc
		f_i = 70 MHz	-	84	-	-	84	-	-	83	-	-	84	-	dBc
		f_i = 170 MHz	-	81	-	-	81	-	-	80	-	-	82	-	dBc
THD	total harmonic distortion	f_i = 3 MHz	-	83	-	-	83	-	-	82	-	-	84	-	dBc
		f_i = 30 MHz	-	82	-	-	82	-	-	82	-	-	83	-	dBc
		f_i = 70 MHz	-	81	-	-	81	-	-	80	-	-	81	-	dBc
		f_i = 170 MHz	-	78	-	-	78	-	-	77	-	-	79	-	dBc
ENOB	effective number of bits	f_i = 3 MHz	-	11.3	-	-	11.3	-	-	11.3	-	-	11.3	-	bits
		f_i = 30 MHz	-	11.3	-	-	11.3	-	-	11.3	-	-	11.2	-	bits
		f_i = 70 MHz	-	11.2	-	-	11.2	-	-	11.2	-	-	11.2	-	bits
		f_i = 170 MHz	-	11.1	-	-	11.1	-	-	11.1	-	-	11.1	-	bits
SNR	signal-to-noise ratio	f_i = 3 MHz	-	70.0	-	-	69.9	-	-	69.8	-	-	69.6	-	dBFS
		f_i = 30 MHz	-	69.5	-	-	69.5	-	-	69.5	-	-	69.4	-	dBFS
		f_i = 70 MHz	-	69.2	-	-	69.2	-	-	69.1	-	-	69.0	-	dBFS
		f_i = 170 MHz	-	68.8	-	-	68.8	-	-	68.7	-	-	68.6	-	dBFS
SFDR	spurious-free dynamic range	f_i = 3 MHz	-	86	-	-	86	-	-	85	-	-	87	-	dBc
		f_i = 30 MHz	-	85	-	-	85	-	-	85	-	-	86	-	dBc
		f_i = 70 MHz	-	84	-	-	84	-	-	83	-	-	84	-	dBc
		f_i = 170 MHz	-	81	-	-	81	-	-	80	-	-	82	-	dBc

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Table 7. Dynamic characteristics[1] *…continued*

Symbol	Parameter	Conditions	ADC1215S065			ADC1215S080			ADC1215S105			ADC1215S125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IMD	Intermodu-lation distortion	f_i = 3 MHz	-	89	-	-	89	-	-	88	-	-	89	-	dBc
		f_i = 30 MHz	-	88	-	-	88	-	-	88	-	-	88	-	dBc
		f_i = 70 MHz	-	87	-	-	87	-	-	86	-	-	86	-	dBc
		f_i = 170 MHz	-	84	-	-	85	-	-	83	-	-	84	-	dBc

[1] Typical values measured at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V; T_{amb} = 25 °C and C_L = 5 pF; minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V, $V_{INP} - V_{INM}$ = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

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10.2 Clock and digital output timing

Table 8. Clock and digital output timing characteristics[1]

Symbol	Parameter	Conditions	ADC1410S065			ADC1410S080			ADC1410S105			ADC1410S125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock timing input: pins CLKP and CLKM															
f_{clk}	clock frequency		40	-	65	60	-	80	75	-	105	100	-	125	MHz
$t_{lat(data)}$	data latency time		-	13.5	-	-	13.5	-	-	13.5	-	-	13.5	-	clock cycles
δ_{clk}	clock duty cycle	DCS_EN = 1	30	50	70	30	50	70	30	50	70	30	50	70	%
		DCS_EN = 0	45	50	55	45	50	55	45	50	55	45	50	55	%
$t_{d(s)}$	sampling delay time		-	0.8	-	-	0.8	-	-	0.8	-	-	0.8	-	ns
t_{wake}	wake-up time		-	76	-	-	76	-	-	76	-	-	76	-	μs
CMOS Mode timing output: pins D11 to D0 and DAV															
t_{PD}	propagation delay	DATA	13.6	14.9	16.4	11.9	12.9	14.4	8.0	10.8	12.4	8.2	9.7	11.3	ns
		DAV	-	4.2	-	-	3.6	-	-	3.3	-	-	3.4	-	ns
t_{su}	set-up time		-	12.5	-	-	9.8	-	-	6.8	-	-	5.6	-	ns
t_h	hold time		-	3.4	-	-	3.3	-	-	3.1	-	-	2.8	-	ns
t_r	rise time	DATA [2]	0.39	-	2.4	0.39	-	2.4	0.39	-	2.4	0.39	-	2.4	ns
		DAV	0.26	-	2.4	0.26	-	2.4	0.26	-	2.4	0.26	-	2.4	ns
t_f	fall time	DATA [2]	0.19	-	2.4	0.19	-	2.4	0.19	-	2.4	0.19	-	2.4	ns

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Table 8. Clock and digital output timing characteristics[1] *…continued*

Symbol	Parameter	Conditions		ADC1410S065			ADC1410S080			ADC1410S105			ADC1410S125			Unit
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
LVDS DDR mode timing output: pins D10_D11_P to D0_D1_P, D10_D11_M to D0_D1_M, DAVP and DAVM																
t_{PD}	propagation delay	DATA		3.3	5.1	7.6	2.9	4.6	7.1	2.5	4.2	6.8	2.2	4.0	6.6	ns
		DAV		-	2.8	-	-	2.5	-	-	2.3	-	-	2.2	-	ns
t_{su}	set-up time			-	5.4	-	-	4.1	-	-	2.6	-	-	1.9	-	ns
t_h	hold time			-	2.2	-	-	2.0	-	-	1.8	-	-	1.7	-	ns
t_r	rise time	DATA	[3]	0.5	-	5	0.5	-	5	0.5	-	5	0.5	-	5	ns
		DAV		0.18	-	2.4	0.18	-	2.4	0.18	-	2.4	0.18	-	2.4	ns
t_f	fall time	DATA	[3]	0.15	-	1.6	0.15	-	1.6	0.15	-	1.6	0.15	-	1.6	ns

[1] Typical values measured at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V; T_{amb} = 25 °C and C_L = 5 pF; minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V, $V_{INP} - V_{INM}$ = −1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

[2] Measured between 20 % to 80 % of V_{DDO}.

[3] Rise time measured from −50 mV to +50 mV; fall time measured from +50 mV to −50 mV.

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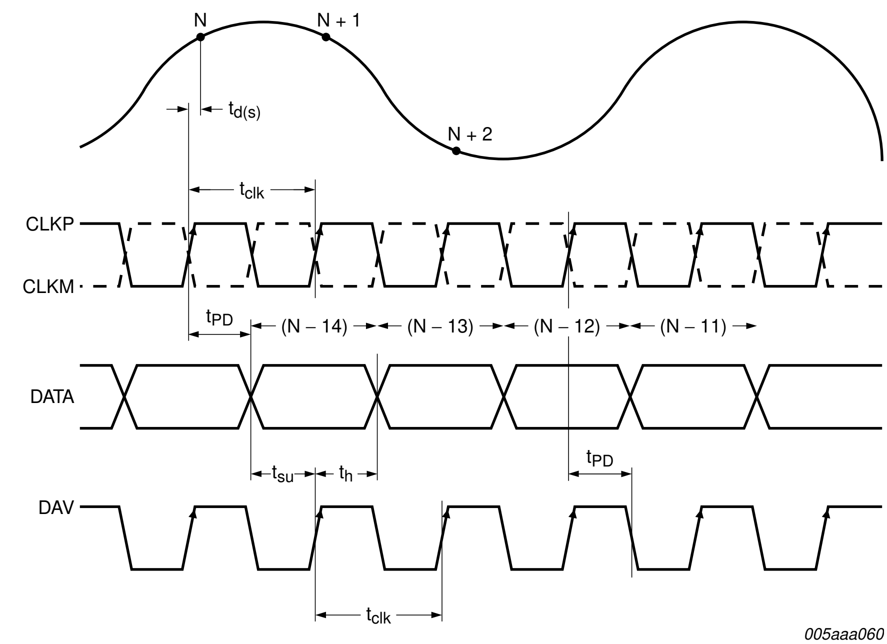

Fig 4. CMOS mode timing

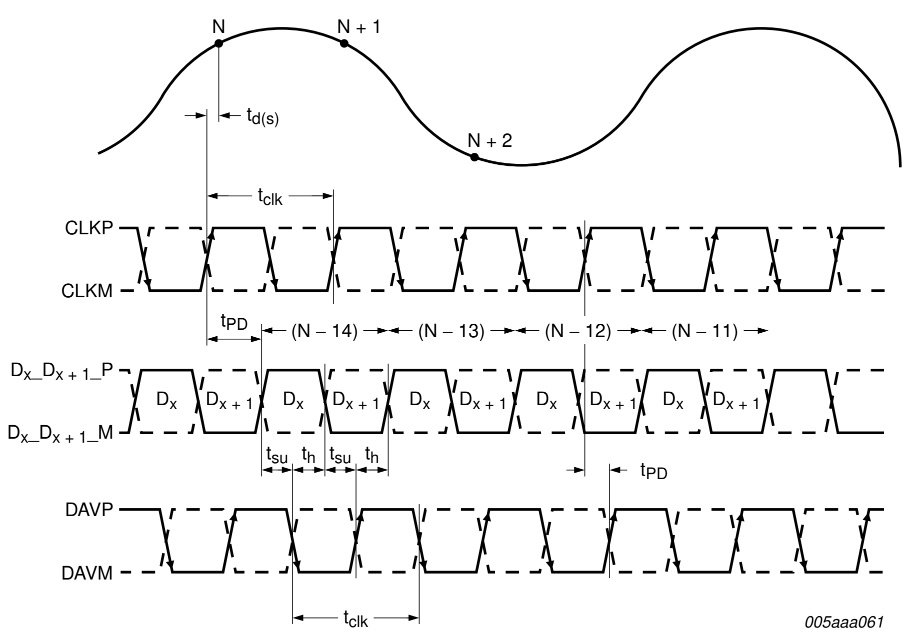

Fig 5. LDVS DDR mode timing

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10.3 SPI timings

Table 9. SPI timings characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCLK)}$	SCLK pulse width		-	40	-	ns
$t_{w(SCLKH)}$	SCLK HIGH pulse width		-	16	-	ns
$t_{w(SCLKL)}$	SCLK LOW pulse width		-	16	-	ns
t_{su}	set-up time	data to SCLK HIGH	-	5	-	ns
		$\overline{CS}$ to SCLK HIGH	-	5	-	ns
t_h	hold time	data to SCLK HIGH	-	2	-	ns
		$\overline{CS}$ to SCLK HIGH	-	2	-	ns
$f_{clk(max)}$	maximum clock frequency		-	25	-	MHz

[1] Typical values measured at $V_{DDA(3V)}$ = 3 V, V_{DDO} = 1.8 V, $V_{DDA(5V)}$ = 5 V, T_{amb} = 25 °C and C_L = 5 pF; minimum and maximum values are across the full temperature range T_{amb} = –40 °C to +85 °C at V_{DDA} = 3 V, V_{DDO} = 1.8 V.

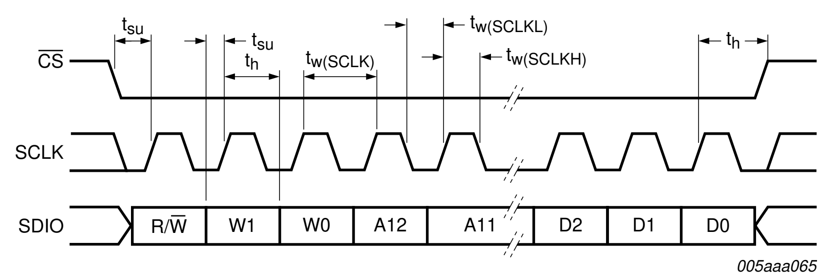

Fig 6. SPI timing

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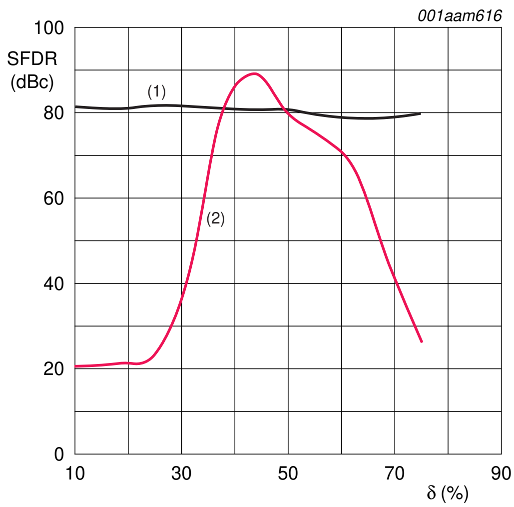
10.4 Typical characteristics

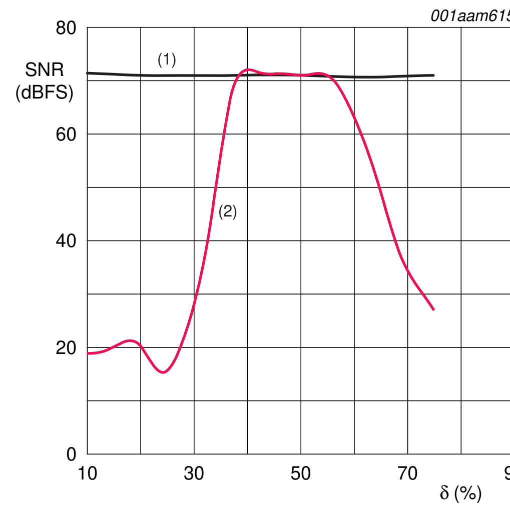


T = 25 °C; V_{DD} = 3 V; f_i = 170 MHz; f_s = 125 Msps

(1) DCS on

(2) DCS off

Fig 7. Spurious-free dynamic range as a function of duty cycle (δ)

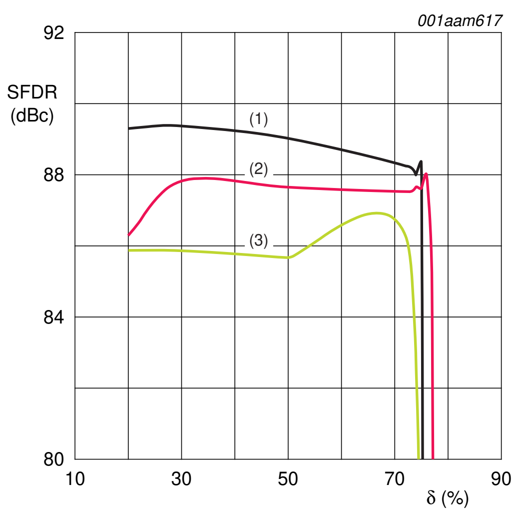


T = 25 °C; V_{DD} = 3 V; f_i = 170 MHz; f_s = 125 Msps

(1) DCS on

(2) DCS off

Fig 8. Signal-to-noise ratio as a function of duty cycle (δ)

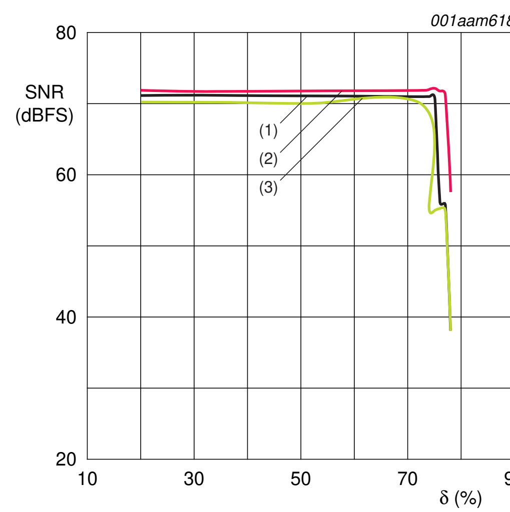


(1) T_{amb} = −40 °C/typical supply voltages

(2) T_{amb} = +25 °C/typical supply voltages

(3) T_{amb} = +90 °C/typical supply voltages

Fig 9. Spurious-free dynamic range as a function of duty cycle (δ)



(1) T_{amb} = −40 °C/typical supply voltages

(2) T_{amb} = +25 °C/typical supply voltages

(3) T_{amb} = +90 °C/typical supply voltages

Fig 10. Signal-to-noise ratio as a function of duty cycle (δ)

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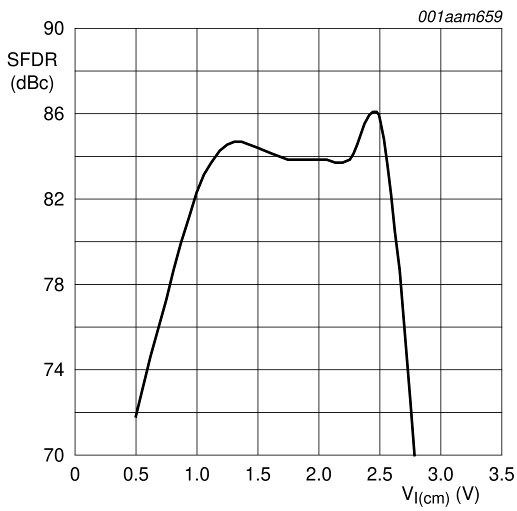

Fig 11. Spurious-free dynamic range as a function of common-mode input voltage ($V_{i(cm)}$)

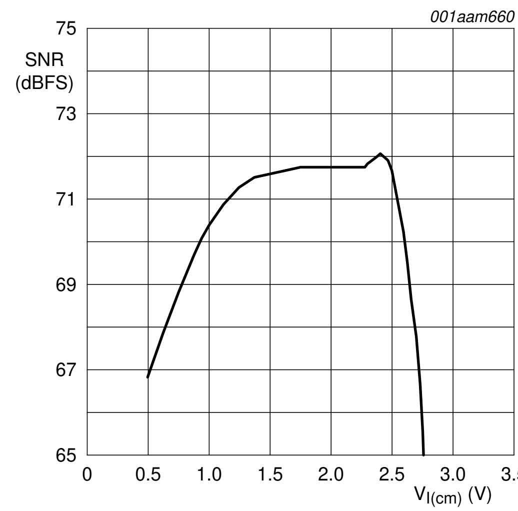

Fig 12. Signal-to-noise ratio as a function of common-mode input voltage ($V_{i(cm)}$)

11. Application information

11.1 Device control

The ADC1215S can be controlled via the Serial Peripheral Interface (SPI control mode) or directly via the I/O pins (Pin control mode).

11.1.1 SPI and Pin control modes

The device enters Pin control mode at power-up, and remains in this mode as long as pin $\overline{CS}$ is held HIGH. In Pin control mode, the SPI pins SDIO, $\overline{CS}$ and SCLK are used as static control pins.

SPI control mode is enabled by forcing pin $\overline{CS}$ LOW. Once SPI control mode has been enabled, the device remains in this mode. The transition from Pin control mode to SPI control mode is illustrated in Figure 13.

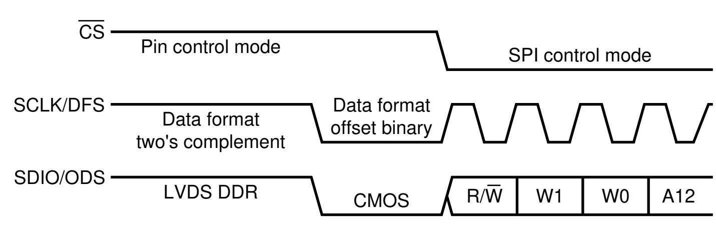

Fig 13. Control mode selection

When the device enters SPI control mode, the output data standard and data format are determined by the level on pin SDIO as soon as a transition is triggered by a falling edge on $\overline{CS}$.

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11.1.2 Operating mode selection

The active ADC1215S operating mode (Power-up, Power-down or Sleep) can be selected via the SPI interface (see Figure 24) or using pins PWD and $\overline{OE}$ in Pin control mode, as described in Table 10.

Table 10. Operating mode selection via pin PWD and $\overline{OE}$

Pin PWD	Pin $\overline{OE}$	Operating mode	Output high-Z
0	0	Power-up	no
0	1	Power-up	yes
1	0	Sleep	yes
1	1	Power-down	yes

11.1.3 Selecting the output data standard

The output data standard (CMOS or LVDS DDR) can be selected via the SPI interface (see Table 23) or using pin ODS in Pin control mode. LVDS DDR is selected when ODS is HIGH, otherwise CMOS is selected.

11.1.4 Selecting the output data format

The output data format can be selected via the SPI interface (offset binary, two's complement or gray code; see Table 23) or using pin DFS in Pin control mode (offset binary or two's complement). Offset binary is selected when DFS is LOW. When DFS is HIGH, two's complement is selected.

11.2 Analog inputs

11.2.1 Input stage

The analog input of the ADC1215S supports a differential or a single-ended input drive. Optimal performance is achieved using differential inputs. The ADC inputs are internally biased and need to be decoupled.

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) via a programmable internal reference (see Section 11.3 and Table 21).

The equivalent circuit of the input buffer followed by the Sample and Hold (S/H) input stage, including ElectroStatic Discharge (ESD) protection and circuit and package parasitics, is shown in Figure 14.

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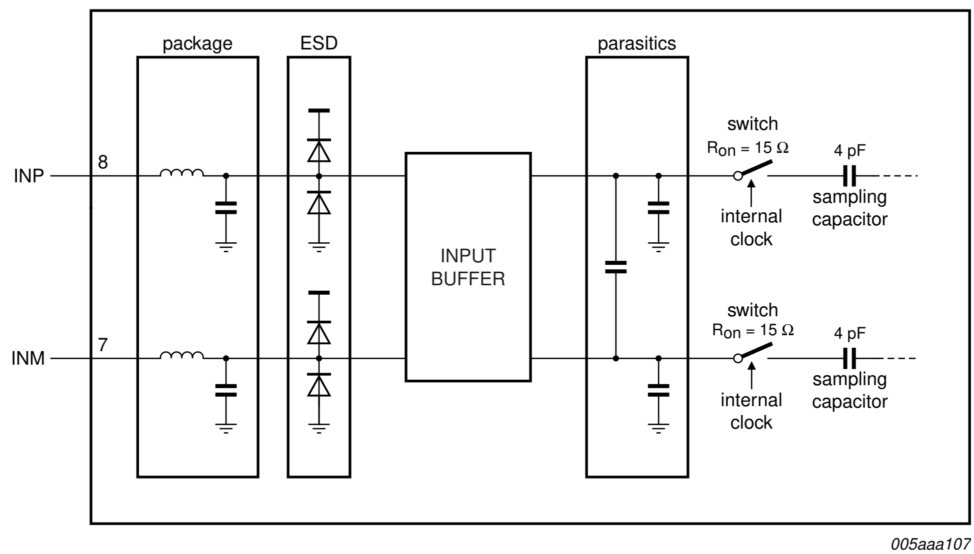

Fig 14. Input sampling circuit and input buffer

The integrated input buffer offers the following advantages:

- The kickback effect is avoided - the charge injection and glitches generated by the S/H input stage are isolated from the input circuitry, so there is no need for additional filtering.
- The input capacitance is very low and constant over a wide frequency range, which makes the ADC1215S easy to drive.

The sample phase occurs when the internal clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the clock signal goes LOW, the stage enters the hold phase and the voltage information is transmitted to the ADC core.

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11.2.2 Transformer

The configuration of the transformer circuit is determined by the input frequency. The configuration shown in Figure 15 would be suitable for a baseband application.

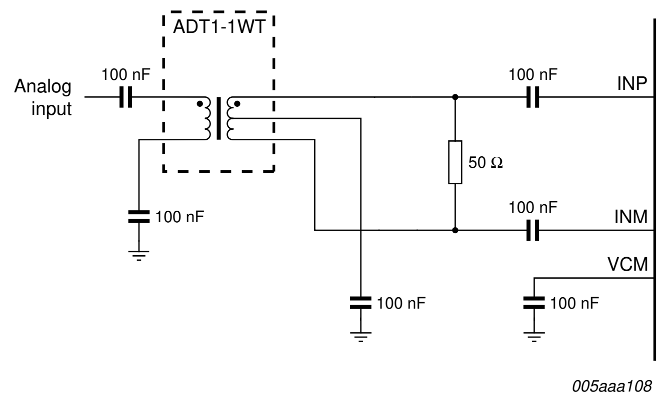

Fig 15. Single transformer configuration suitable for baseband applications

The configuration shown in Figure 16 is recommended for high frequency applications. In both cases, the choice of transformer is a compromise between cost and performance.

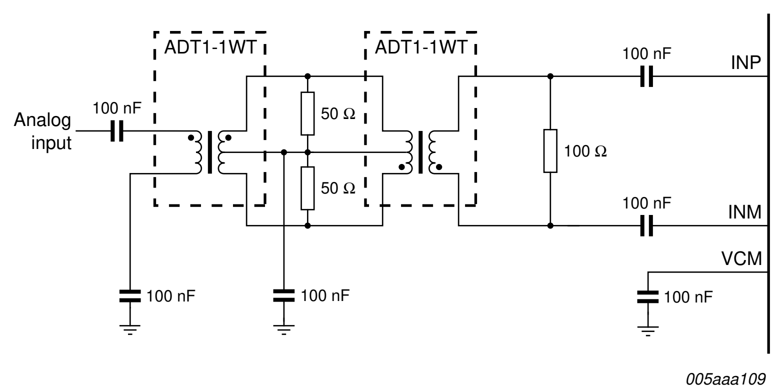

Fig 16. Dual transformer configuration suitable for high intermediate frequency application

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11.3 System reference and power management

11.3.1 Internal/external references

The ADC1215S has a stable and accurate built-in internal reference voltage to adjust the ADC full-scale. This reference voltage can be set internally via SPI or with pins VREF and SENSE (programmable in 1 dB steps between 0 dB and –6 dB via control bits INTREF[2:0] when bit INTREF_EN = logic 1; see Table 21). See Figure 18 to Figure 21. The equivalent reference circuit is shown in Figure 17. External reference is also possible by providing a voltage on pin VREF as described in Figure 20.

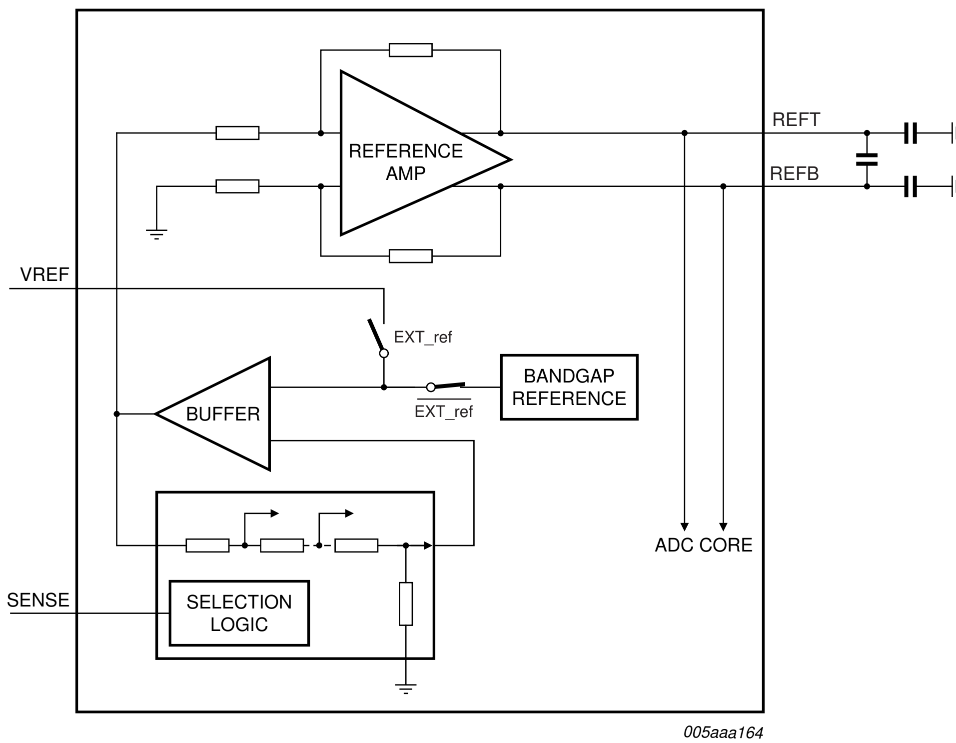

Fig 17. Reference equivalent schematic

If bit INTREF_EN is set to logic 0, the reference voltage is determined either internally or externally as detailed in Table 11.

Table 11. Reference selection

Selection	SPI bit INTREF_EN	SENSE pin	VREF pin	Full-scale (p-p)
internal (Figure 18)	0	AGND	330 pF capacitor to AGND	2 V
internal (Figure 19)	0	pin VREF connected to pin SENSE and via a 330 pF capacitor to AGND		1 V
external (Figure 20)	0	$V_{DDA(3V)}$	external voltage between 0.5 V and 1 V[1]	1 V to 2 V
internal via SPI (Figure 21)	1	pin VREF connected to pin SENSE and via 330 pF capacitor to AGND		1 V to 2 V

[1] The voltage on pin VREF is doubled internally to generate the internal reference voltage.

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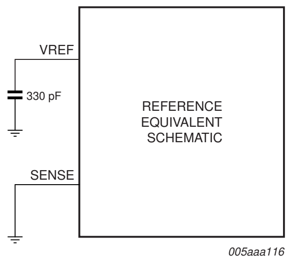

Fig 18. Internal reference, 2 V (p-p) full-scale

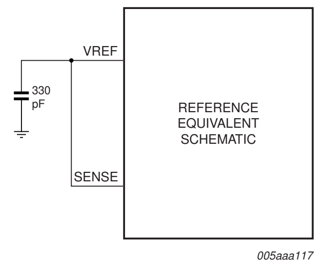

Fig 19. Internal reference, 1 V (p-p) full-scale

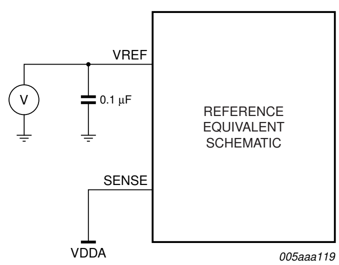

Fig 20. External reference, 1 V (p-p) to 2 V (p-p) full-scale

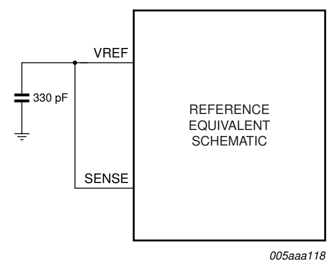

Fig 21. Internal reference via SPI, 1 V (p-p) to 2 V (p-p) full-scale

Figure 18 to Figure 21 illustrate how to connect the SENSE and VREF pins to select the required reference voltage source.

11.3.2 Programmable full-scale

The full-scale is programmable between 1 V (peak-to-peak) to 2 V (peak-to-peak) (see Table 12).

Table 12. Reference SPI gain control

INTREF	Gain	Full-scale (p-p)
000	0 dB	2 V
001	−1 dB	1.78 V
010	−2 dB	1.59 V
011	−3 dB	1.42 V
100	−4 dB	1.26 V
101	−5 dB	1.12 V
110	−6 dB	1 V
111	reserved	x

11.3.3 Common-mode output voltage ($V_{O(cm)}$)

A 0.1 μF filter capacitor should be connected between pin VCM and ground.

11.3.4 Biasing

The common-mode input voltage ($V_{I(cm)}$) on pins INP and INM is set internally. The input buffer bias current can be set to one of three levels (high, medium or low) via the SPI (see Table 22).

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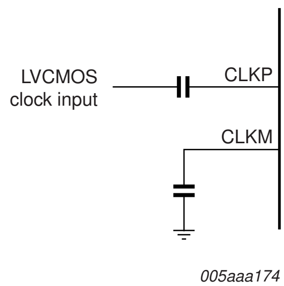
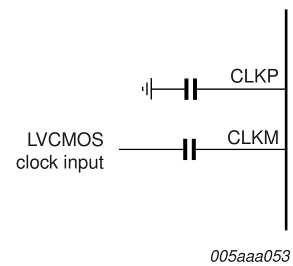
11.4 Clock input

11.4.1 Drive modes

The ADC1215S can be driven differentially (LVPECL). It can also be driven by a single-ended Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) signal connected to pin CLKP (pin CLKM should be connected to ground via a capacitor) or CLKM (pin CLKP should be connected to ground via a capacitor).

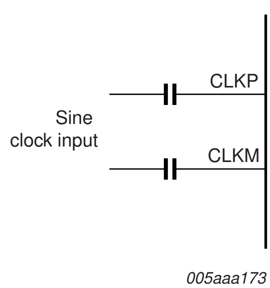


a. Rising edge LVCMOS

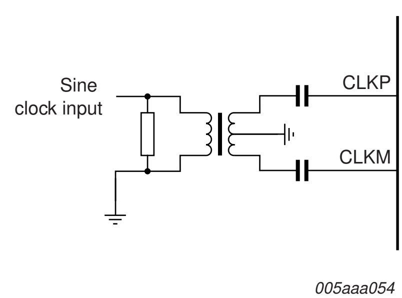


b. Falling edge LVCMOS

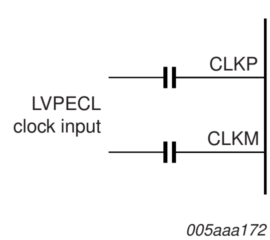
Fig 22. LVCMOS single-ended clock input



a. Sine clock input



b. Sine clock input (with transformer)



c. LVPECL clock input

Fig 23. Differential clock input

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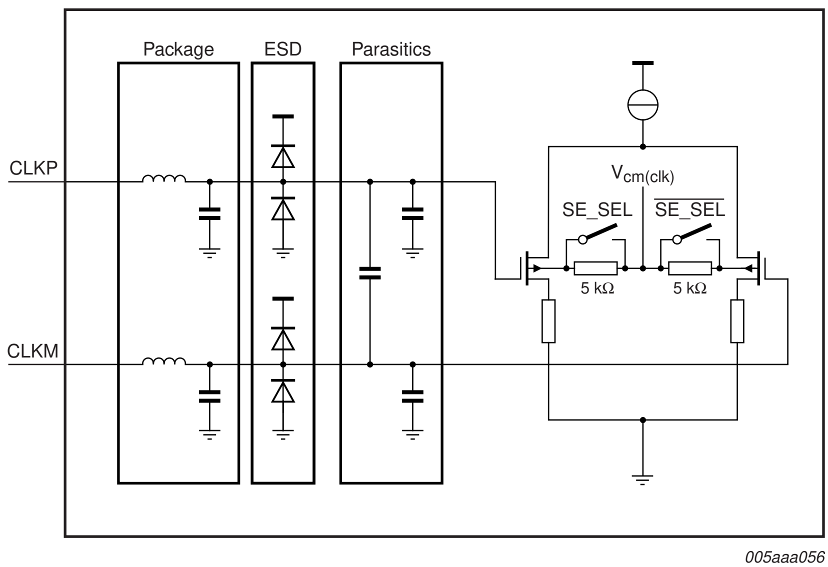
11.4.2 Equivalent input circuit

The equivalent circuit of the input clock buffer is shown in Figure 24. The common-mode voltage of the differential input stage is set via internal 5 kΩ resistors.



$V_{cm(clk)}$ = common-mode voltage of the differential input stage.

Fig 24. Equivalent input circuit

Single-ended or differential clock inputs can be selected via the SPI interface (see Table 20). If single-ended is enabled, the input pin (CLKM or CLKP) is selected via control bit SE_SEL.

If single-ended is implemented without setting bit SE_SEL to the appropriate value, the unused pin should be connected to ground via a capacitor.

11.4.3 Duty cycle stabilizer

The duty cycle stabilizer can improve the overall performances of the ADC by compensating the duty cycle of the input clock signal. When the duty cycle stabilizer is active (bit DCS_EN = logic 1; see Table 20), the circuit can handle signals with duty cycles of between 30 % and 70 % (typical). When the duty cycle stabilizer is disabled (DCS_EN = logic 0), the input clock signal should have a duty cycle of between 45 % and 55 %.

11.4.4 Clock input divider

The ADC1215S contains an input clock divider that divides the incoming clock by a factor of 2 (when bit CLKDIV = logic 1; see Table 20). This feature allows the user to deliver a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

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11.5 Digital outputs

11.5.1 Digital output buffers: CMOS mode

The digital output buffers can be configured as CMOS by setting bit LVDS_CMOS to logic 0 (see Table 23).

Each digital output has a dedicated output buffer. The equivalent circuit of the CMOS digital output buffer is shown in Figure 25. The buffer is powered by a separate OGND/V_{DDO} to ensure 1.8 V to 3.3 V compatibility and is isolated from the ADC core. Each buffer can be loaded by a maximum of 10 pF.

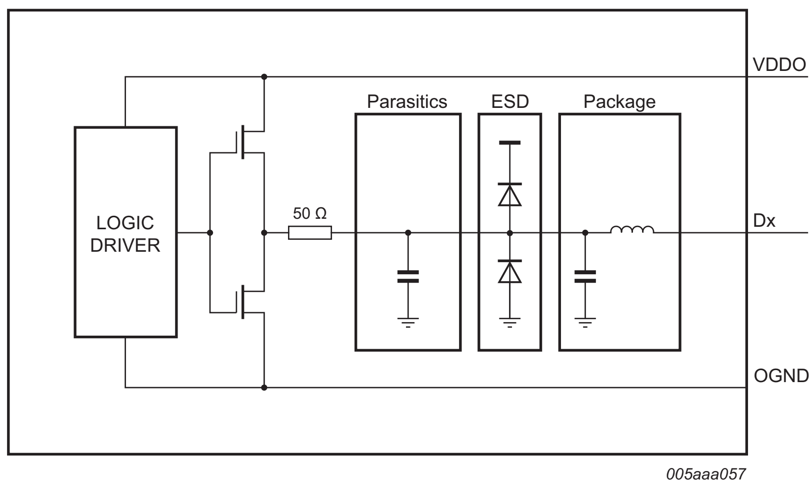

Fig 25. CMOS digital output buffer

The output resistance is 50 Ω and is the combination of the an internal resistor and the equivalent output resistance of the buffer. There is no need for an external damping resistor. The drive strength of both data and DAV buffers can be programmed via the SPI in order to adjust the rise and fall times of the output digital signals (see Table 30):

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