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ADC1453D250

Dual 14-bit ADC; up to 246 Msps; JESD204B serial outputs

Rev. 3.2 — 6 June 2014 Preliminary data sheet

1. General description

The ADC1453D is a dual channel 14-bit Analog-to-Digital Converter (ADC) with JESD204B interface (which is backward compatible with the JESD204A interface) optimized for high dynamic performance and low power consumption at sample rates up to 246 Msps. Pipelined architecture and output error correction guarantee zero missing codes over the entire operating range.

The ADC1453D has JESD204B serial outputs over a configurable number of lanes (1 or 2). Multiple Device Synchronization (MDS) allows sample-accurate synchronization of the data outputs of multiple ADC devices. It guarantees a maximum skew of one clock period between as many as 16 output lanes from up to eight ADC1453D devices.

An integrated Serial Peripheral Interface (SPI) allows easy configuration of the ADC. The device also includes a programmable full-scale to allow a flexible input voltage range of 1 V (p-p) to 2 V (p-p).

The ADC1453D is available in an VFQFPN56 package (8 mm × 8 mm outline). It is supported with customer demo boards.

2. Features and benefits

- Dual channel 14-bit resolution ADC
- Sampling rate up to 246 Msps
- JESD204B Device Subclass 0, 1 and 2 with harmonic clocking and deterministic latency support
- ADC Multiple Device Synchronization (MDS)
- Offset binary, two's complement and Gray output data
- Two JESD204B serial output lanes, up to 5 Gbps
- Flexible input voltage range from 1 V (p-p) to 2 V (p-p) by 1 dB steps
- Clock input divider from 1 to 8 supports harmonic clocking
- Duty Cycle Stabilizer (DCS)
- SNR = 70.1 dBFS; fs = 246 Msps; fi = 190 MHz
- SFDR = 80 dBc; f_s = 246 Msps; f_i = 190 MHz
- IMD3 = 86 dBc; f_s = 246 Msps; f_{i1} = 188.5 MHz; f_{i2} = 191.5 MHz
- Analog input bandwidth of 1 GHz (typical)
- Pin to pin compatible with ADC1413D and ADC1443D series
- Typical power dissipation = 1.4 W; f_s = 246 Msps
- Industrial temperature range from −40 °C to +85 °C
- Serial Peripheral Interface (SPI) for configuration control and status monitoring
- VFQFPN56 package; 8 × 8 mm

3. Applications

- Wireless infrastructure: LTE, TD-LTE, WiMAX, MC-GSM, CDMA, WCDMA, TD-SCDMA
- Software defined radio
- Medical non-invasive scanners
- Scientific particle detectors
- Microwave backhaul transceivers
- Aerospace and defense communications and radar systems
- Industrial signal analysis instruments
- General-purpose high-speed applications

4. Ordering information

Table 1. Ordering information

Type number	f_s (Msps)	Package		
		Name	Description	Version
ADC1453D250NGG	246	VFQFPN	plastic thermal enhanced low profile quad flat package; no leads; 56 terminals; resin based; body 8 × 8 × 1.35 mm	PSC-4449

5. Block diagram

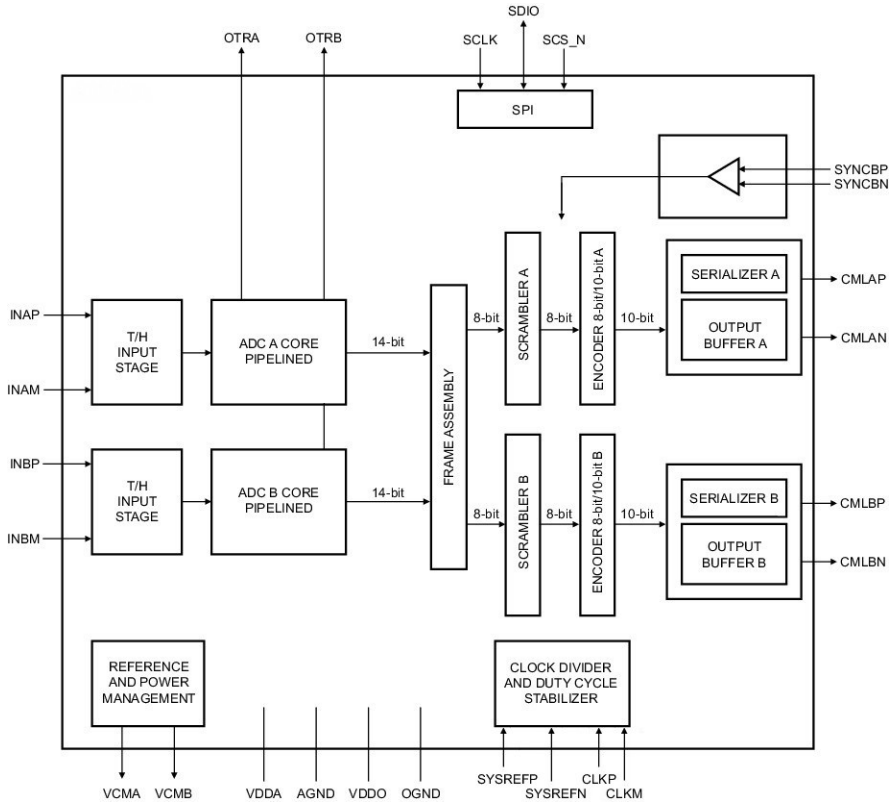


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

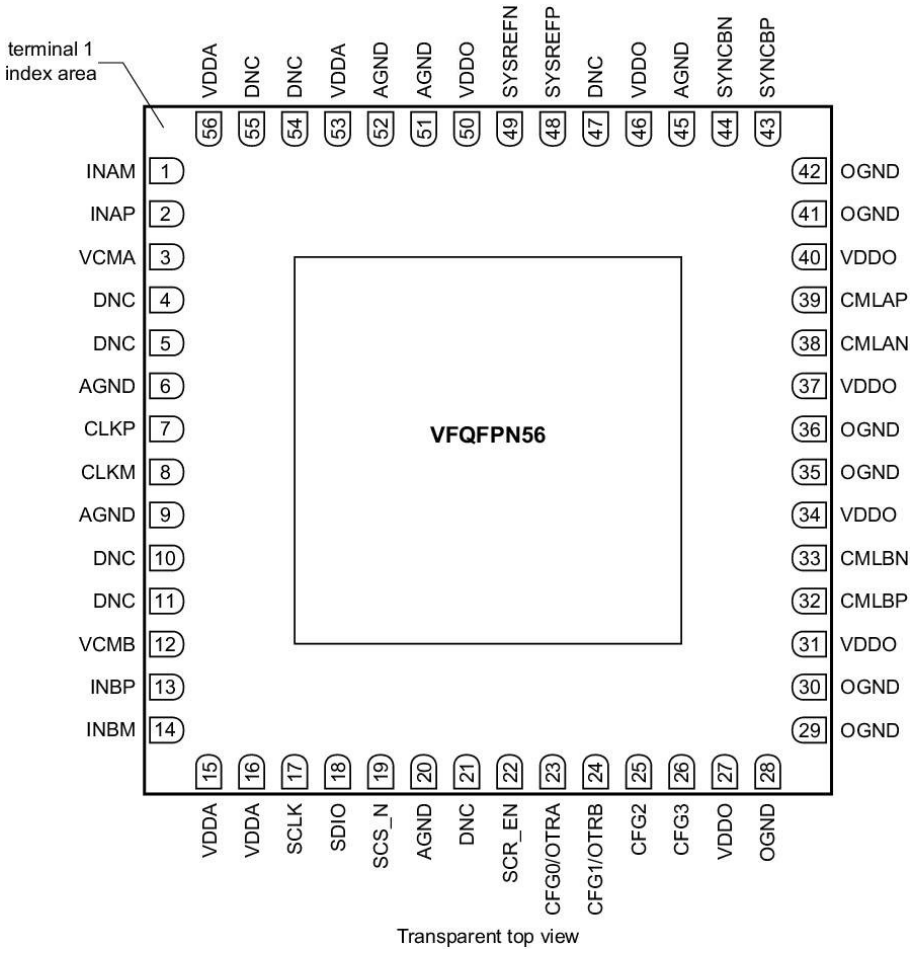


Fig 2. Pin configuration (PSC-4449)

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type[1]	Description
INAM	1	I	channel A complementary analog input
INAP	2	I	channel A analog input
VCMA	3	O	channel A output common voltage
DNC	4	-	do not connect
DNC	5	-	do not connect
AGND	6	G	analog ground
CLKP	7	I	clock input
CLKN	8	I	complementary clock input
AGND	9	G	analog ground
DNC	10	-	do not connect
DNC	11	-	do not connect
VCMB	12	O	channel B output common voltage
INBP	13	I	channel B analog input
INBM	14	I	channel B complementary analog input
VDDA	15	P	analog power supply
VDDA	16	P	analog power supply
SCLK	17	I	SPI clock (50 kΩ internal pull-dow)
SDIO	18	I/O	SPI data IO (50 kΩ internal pull-dow)
SCS_N	19	I	SPI chip select (50 kΩ internal pull-up)
AGND	20	G	analog ground
DNC	21	-	do not connect
SCR_EN	22	I	scrambler enable (50 kΩ internal pull-up)
CFG0/OTRA	23	I/O	configuration pin 0/OuT of Range A (OTRA) (50 kΩ internal pull-down)
CFG1/OTRB	24	I/O	configuration pin 1/OuT of Range B (OTRB) (50 kΩ internal pull-down)
CFG2	25	I/O	configuration pin 2 (50 kΩ internal pull-down)
CFG3	26	I/O	configuration pin 3 (50 kΩ internal pull-down)
VDDO	27	P	digital output power supply
AGND	28	G	analog ground
OGND	29	G	digital output ground
OGND	30	G	digital output ground
VDDO	31	P	digital output power supply
CMLBP	32	O	channel B output
CMLBN	33	O	channel B complementary output
VDDO	34	P	digital output power supply
OGND	35	G	digital output ground
OGND	36	G	digital output ground
VDDO	37	P	digital output power supply
CMLAN	38	O	channel A complementary output

Table 2. Pin description *…continued*

Symbol	Pin	Type[1]	Description
CMLAP	39	O	channel A output
VDDO	40	P	digital output power supply
OGND	41	G	digital output ground
OGND	42	G	digital output ground
SYNCBP	43	I	JESD204B SYNC synchronization signal from receiver
SYNCBN	44	I	complementary SYNC from receiver
AGND	45	G	analog ground
VDDO	46	P	digital output power supply
DNC	47	-	do not connect
SYSREFP	48	I	positive clock synchronization
SYSREFN	49	I	negative clock synchronization
VDDO	50	P	digital output power supply
AGND	51	G	analog ground
AGND	52	G	analog ground
VDDA	53	P	analog power supply
DNC	54	-	do not connect
DNC	55	-	do not connect
VDDA	56	P	analog power supply
AGND	EXP	G	Expose PAD

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

6.2.1 Start-up Configuration

Because the maximum sampling clock of the ADC1453D is 246 Msps, care should be taken in case of harmonic clocking. If the input clock frequency is higher than 246 MHz, the clock divider must be set before providing the clock.

In order to avoid any issue, it is recommended to start the device in power-down mode by setting the configuration pins to logic level ’1’ (see Table 19). This can be done by adding for example a 1 kΩ pull-up resistor on CFG0, CFG1, CFG2 and CFG3.

When the power supplies are set, the divider can be programmed by the use of the SPI registers. Then the device is powered on and the JESD204B configuration is set by the use of the SPI registers (bits CFG_SETUP[3:0] in Table 43).

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		–0.3	+2.1	V
V_{DDO}	output supply voltage		–0.3	+2.1	V
ΔV_{DD}	supply voltage difference	$V_{DDA} - V_{DDO}$	–0.8	+0.8	V
V_I	input voltage	pins INP, INM, CLKP and CLKM; referenced to AGND	–0.3	V_{DDA} + 0.3	V
		pins OTR, SCS_N, SDIO, SCLK, CFG, SCR_EN, SYSREFP, SYSREFN, SYNCBP, and SYNCBN; referenced to AGND	–0.3	V_{DDO} + 0.3	V
V_O	output voltage	pin VCM; referenced to AGND	–0.3	V_{DDA} + 0.3	V
		pins CMLP, and CMLN; referenced to OGND	–0.3	V_{DDO} + 0.3	V
T_{stg}	storage temperature		–55	+125	°C
T_{amb}	ambient temperature		–40	+85	°C
T_j	junction temperature		-	125	°C

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	66 vias	[1]	22.7	K/W
$R_{th(j-c)}$	thermal resistance from junction to case	66 vias	[1]	9.3	K/W

[1] In compliance with JEDEC test board, in free air.

9. Static characteristics

Table 5. Static characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDA}	analog supply voltage		1.7	1.8	1.9	V
V_{DDO}	output supply voltage	serial link up to 4 Gbps	1.7	1.8	1.9	V
		serial link from 4 to 5 Gbps	1.8	1.85	1.9	V
I_{DDA}	analog supply current	f_s = 246 Msps; f_i = 190 MHz	-	407	<tbd>	mA
I_{DDO}	output supply current	f_s = 246 Msps; f_i = 190 MHz	-	345	<tbd>	mA

Table 5. Static characteristics[1] *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_{tot}	total power dissipation	f_i = 190 MHz				
		f_s = 246 Msps	-	1.4	<tbd>	W
		Power-down mode	-	10	-	mW
		Sleep mode	-	115	-	mW
Clock inputs: pins CLKP and CLKM (AC-coupled; peak-to-peak)						
$V_{i(clk)}$	clock input voltage	LVPECL	-	±0.8	-	V
		LVDS	-	±0.35	-	V
		SINE differential	±0.5	±1.25	-	V
		LVCMOS single	-	±0.6	-	V
C_I	input capacitance		-	1.2	-	pF
Logic inputs						
I_{IL}	LOW-level input current	absolute value	-	30	-	µA
I_{IH}	HIGH-level input current	absolute value	-	70	-	µA
C_I	input capacitance		-	1.2	-	pF
pins SYSREFP, SYSREFN, SYNCBP, and SYNCBN (differential pins)						
$V_{i(cm)}$	common-mode input voltage		0.925	1.2	1.475	V
$V_{i(dif)}$	differential input voltage		0.2	0.7	-	V
pins SCS_N, SDIO, SCLK, SCR_EN ,CFG, SYNCBP and SYSREFP (Single Ended)						
V_{IL}	LOW-level input voltage		0	-	$0.3V_{DDO}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDO}$	-	V_{DDO}	V
Logic output: pins OTRA, OTRB and SDIO						
V_{OL}	LOW-level output voltage		0	-	0.2	V
V_{OH}	HIGH-level output voltage		V_{DDO}-0.2	-	V_{DDO}	V
Digital outputs: pins CMLAP, CMLAN, CMLBP, and CMLBN						
$V_{O(cm)}$	common-mode output voltage	default current	-	1.4	-	V
$V_{O(dif)}$	differential output voltage	default current; peak-to-peak	-	800	-	mV
Analog inputs: pins INP and INM						
I_I	input current		-	±5	-	µA
R_I	input resistance	f_i = 190 MHz	-	400	-	Ω
C_I	input capacitance	f_i = 190 MHz	-	5	-	pF
$V_{I(cm)}$	common-mode input voltage	$V_{INP} = V_{INM}$;T_{amb} = 25 °C	0.8	0.9	1.0	V
B_i	input bandwidth		-	1	-	GHz
$V_{I(dif)}$	differential input voltage	peak-to-peak; full-scale	1	-	2	V
Common-mode output voltage: pins VCMA and VCMB						
$V_{O(cm)}$	common-mode output voltage	$I_{O(cm)}$=1mA	-	0.9	-	V
$I_{O(cm)}$	common-mode output current	T_{amb} = 25 °C	-	-	1	mA
Accuracy						
INL	integral non-linearity	f_s = 246 Msps; f_i = 4.43 MHz	-	±2.1	±6.62	LSB

Table 5. Static characteristics[1] *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DNL	differential non-linearity	f_s = 246 Msps; f_i = 4.43 MHz; guaranteed no missing codes				
		negative DNL	-0.88	–0.71	-	LSB
		positive DNL	-	+0.87	+1.22	LSB
E_{offset}	offset error		–20	-	+20	mV
E_G	gain error	full-scale	-	4.1	-	%
$M_{G(CTC)}$	channel-to-channel gain matching		-	2.5	-	%
OS	Offset Spur	measured at fs/2 with fs = 246Msps		-80		dBc
Supply						
PSRR	power supply rejection ratio	100 mV (p-p) on V_{DDA}, 0.5 to 2MHz	-	-35	-	dB

[1] Typical values measured at V_{DDA} = 1.8 V; V_{DDO} = 1.85 V; T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = –40 °C to +85 °C at V_{DDA} = 1.8 V; V_{DDO} = 1.85 V; $V_{I(dif)}$ = 2 V; $V_{INP} – V_{INM}$ = –1.5 dBFS; unless otherwise specified.

10. Dynamic characteristics

10.1 Dynamic characteristics

Table 6. Dynamic characteristics[1]

Symbol	Parameter	Conditions	f_s = 246Msps			Unit
			Min	Typ	Max	
α_{2H}	second harmonic level	f_i = 70 MHz	-	-89	-	dBc
		f_i = 140 MHz	-	-83	-	dBc
		f_i = 190 MHz	-	-85	-	dBc
		f_i = 230 MHz	-	-82	-	dBc
		f_i = 310 MHz	-	-79	-	dBc
α_{3H}	third harmonic level	f_i = 70 MHz	-	-81	-	dBc
		f_i = 140 MHz	-	-86	-	dBc
		f_i = 190 MHz	-	-80	-	dBc
		f_i = 230 MHz	-	-87	-	dBc
		f_i = 310 MHz	-	-80	-	dBc
SFDR	spurious-free dynamic range	f_i = 70 MHz	-	81	-	dBc
		f_i = 140 MHz	-	82	-	dBc
		f_i = 190 MHz	-	80	-	dBc
		f_i = 230 MHz	-	81	-	dBc
		f_i = 310 MHz	-	79	-	dBc
THD	total harmonic distortion	f_i = 70 MHz	-	-79	-	dBc
		f_i = 140 MHz	-	-80	-	dBc
		f_i = 190 MHz	-	-78	-	dBc
		f_i = 230 MHz	-	-79	-	dBc
		f_i = 310 MHz	-	-76	-	dBc
IMD3	third-order intermodulation distortion	f_{i1} = 68.5 MHz; f_{i2} = 71.5 MHz	-	90	-	dBc
		f_{i1} = 138.5 MHz; f_{i2} = 141.5 MHz	-	88	-	dBc
		f_{i1} = 188.5 MHz; f_{i2} = 191.5 MHz	-	90	-	dBc
		f_{i1} = 228.5 MHz; f_{i2} = 231.5 MHz	-	86	-	dBc
		f_{i1} = 308.5 MHz; f_{i2} = 311.5 MHz	-	88	-	dBc
SNR	signal-to-noise ratio	f_i = 70 MHz	-	70.6	-	dBFS
		f_i = 140 MHz	-	70.5	-	dBFS
		f_i = 190 MHz	-	70.1	-	dBFS
		f_i = 230 MHz	-	69.8	-	dBFS
		f_i = 310 MHz	-	69.3	-	dBFS

Table 6. Dynamic characteristics[1] *…continued*

Symbol	Parameter	Conditions	f_s = 246Msps			Unit
			Min	Typ	Max	
ENOB	effective number of bits	f_i = 70 MHz	-	11.1	-	bit
		f_i = 140 MHz	-	11.1	-	bit
		f_i = 190 MHz	-	11	-	bit
		f_i = 230 MHz	-	11	-	bit
		f_i = 310 MHz	-	10.9	-	bit
$\alpha_{ct(ch)}$	channel crosstalk	f_i = 140 MHz	-	83	-	dBc
		f_i = 230 MHz	-	82	-	dBc

[1] Typical values measured at V_{DDA} = 1.8 V; V_{DDO} = 1.85 V; T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 1.8 V; V_{DDO} = 1.85 V; $V_{I(dif)}$ = 2 V; $V_{INP} - V_{INM}$ = −1.5 dBFS; unless otherwise specified.

10.2 Timing

10.2.1 Clock timing

Table 7. Clock and digital output timing characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{lat(data)}$	data latency time	F = 1	54	-	55	clock cycles
		F = 2	45.5	-	46	clock cycles
		F = 4	41	-	41.25	clock cycles
t_{wake}	wake-up time	from Power-down mode	-	60	-	µs
		from Sleep mode	-	54	-	µs
Clock timing						
f_s	sampling rate		180	-	246	MHz
f_{clk}	clock frequency		60	-	1000	MHz
δ_{clk}	clock duty cycle		40	-	60	%

[1] Typical values measured at V_{DDA} = 1.8 V; V_{DDO} = 1.85 V; T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = −40 °C to 85 °C at V_{DDA} = 1.8 V; V_{DDO} = 1.85 V; $V_{I(dif)}$ = 2 V; $V_{INP} - V_{INM}$ = −1.5 dBFS; unless otherwise specified.

10.2.2 SYSREFP/N and SYNCBP/N timings

Table 8. SYSREF timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	set-up time		0.5	-	-	ns
t_h	hold time		(tclk/2) -0.5	-	-	ns

Table 9. SYNCB timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{su}	set-up time		0.75	-	-	ns
t_h	hold time		(tclk/2) -0.25	-	-	ns

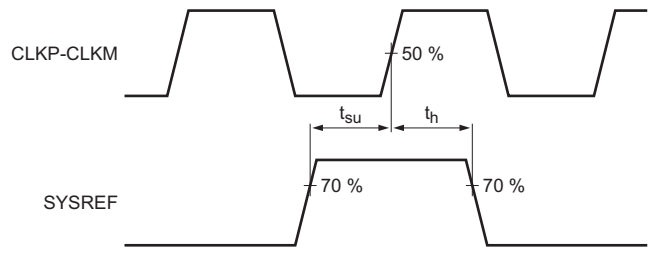


Fig 3. SYSREF timing

10.2.3 SPI timing

Table 10. SPI timing characteristics [1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCLK)}$	SCLK pulse width		40	-	-	ns
$t_{w(SCLKH)}$	SCLK HIGH pulse width		16	-	-	ns
$t_{w(SCLKL)}$	SCLK LOW pulse width		16	-	-	ns
t_{su}	set-up time	SDIO to SCLK HIGH	5	-	-	ns
		SCS_N to SCLK HIGH	5	-	-	ns
t_h	hold time	SDIO to SCLK HIGH	2	-	-	ns
		SCS_N to SCLK HIGH	2	-	-	ns
f_{clk}	clock frequency		-	-	25	MHz

[1] Typical values measured at V_{DDA} = 1.8 V; V_{DDO} = 1.85 V; T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 1.8 V; V_{DDO} = 1.85 V

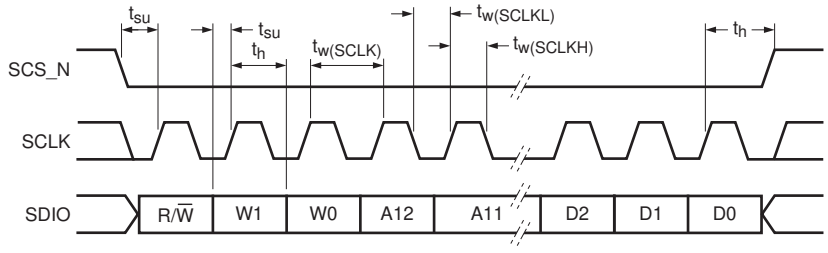


Fig 4. SPI timing

10.3 Typical dynamic performances[1]

10.3.1 Typical FFT at 246 Msps

TBD

Fig 5. 1-tone FFT: –1.5 dBFS; f_i =65 MHz; f_s = 246Msps

TBD

Fig 6. 1-tone FFT: –1.5 dBFS; f_i = 190 MHz; f_s = 246 Msps

TBD

Fig 7. 1-tone FFT: –14 dBFS; f_i = 190 MHz; f_s = 246 Msps

TBD

Fig 8. 2-tone FFT: –7.5 dBFS; f_{i1} = 188.5 MHz; f_{i2} = 191.5 MHz; f_s = 246 Msps

1. Typical values measured at V_{DDA} = 1.8 V; V_{DDO} = 1.85 V; T_{amb} = 25 °C

10.3.2 Typical performances

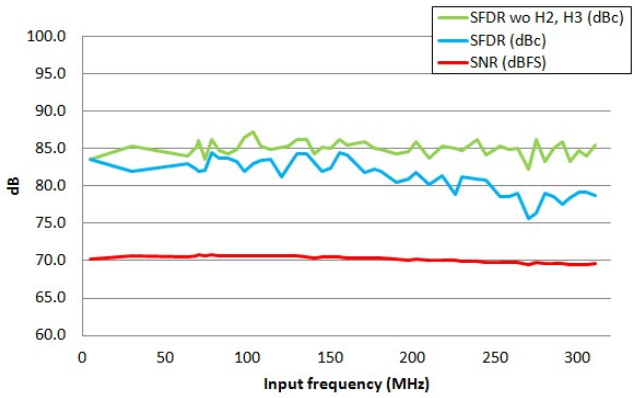


Fig 9. SNR and SFDR as a function of input frequency; −1.5 dBFS

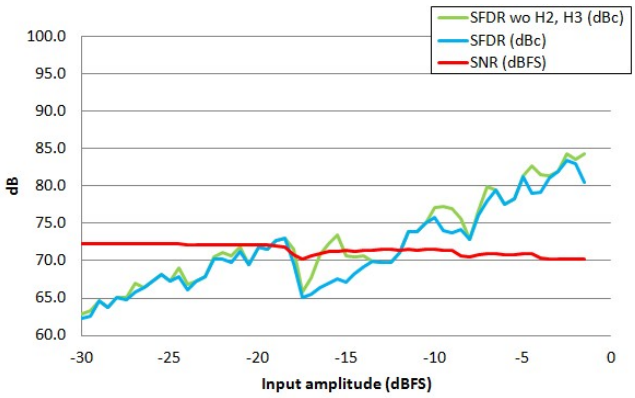


Fig 10. SNR and SFDR as a function of input amplitude; $V_{I(dif)}$ = 2 V

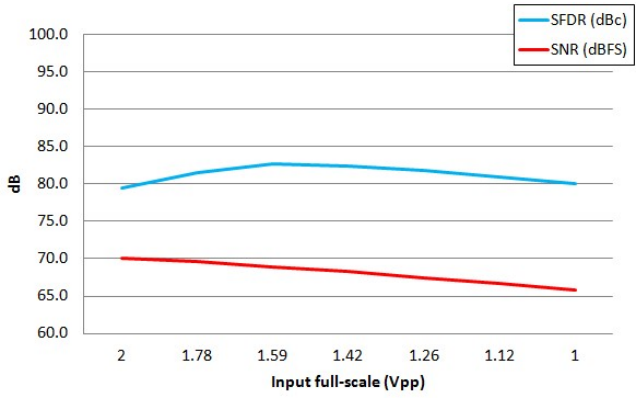


Fig 11. SNR and SFDR as a function of full-scale amplitude; −1.5 dBFS

TBD

Fig 12. tbd

11. Application information

11.1 Analog inputs

11.1.1 Input stage

The analog input of the ADC1453D supports a differential or a single-ended input drive. Optimal performance is achieved using differential inputs with respect to the common-mode input voltage ($V_{I(cm)}$) on pins INP and INM.

The equivalent circuit of the sample and hold input stage, including ElectroStatic Discharge (ESD) protection circuit and package parasitics, is shown in Figure 13.

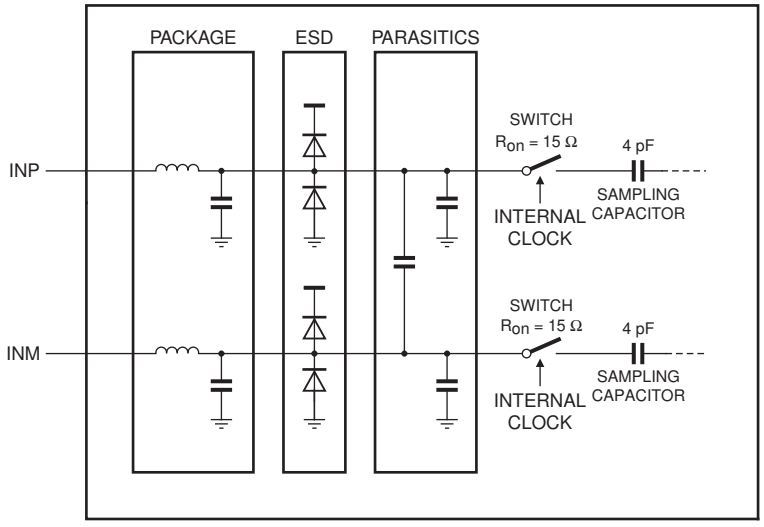


Fig 13. Input sampling circuit

The sample phase occurs when the internal sampling clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the sampling clock signal becomes LOW, the device enters the hold phase and the voltage information is transmitted to the ADC core.

11.1.2 Common-mode input voltage ($V_{I(cm)}$)

Set the common-mode input voltage ($V_{I(cm)}$) on pins INP and INM externally to 0.9 V for optimal performance.

11.1.3 Pin VCM

When the input stage is AC-coupled, pin VCM can be used to set the common-mode reference for the analog inputs, for instance, via a transformer middle point. Connect a 0.1 μF filter capacitor between pin VCM and ground to ensure a low-noise common-mode output voltage.

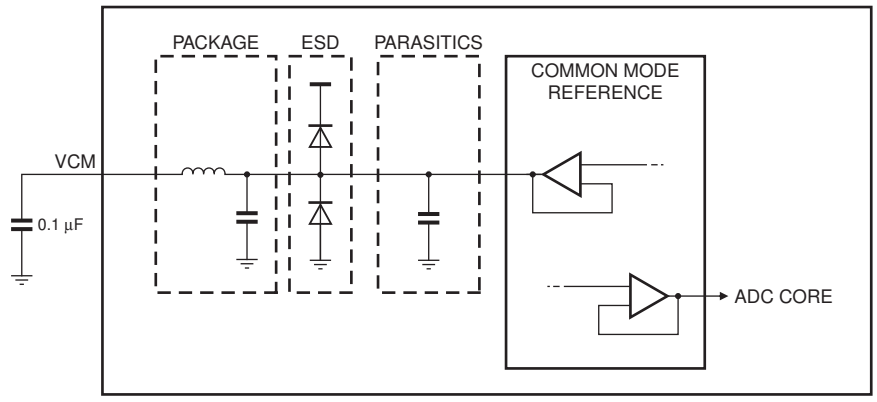


Fig 14. Equivalent schematic of the common-mode reference circuit

11.1.4 Programmable full-scale

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) by programming internal reference gain between 0 dB and −6 dB in 1 dB steps. The full-scale range can be set independently via bits INTREF[2:0] of the SPI local registers (see Table 11 and Table 30).

Table 11. Reference gain control

Default values are shown highlighted.

INTREF[2:0]	Level (dB)	Full-scale (V (p-p))
000	**0**	**2**
001	−1	1.78
010	−2	1.59
011	−3	1.42
100	−4	1.26
101	−5	1.12
110	−6	1
111	reserved	x

11.1.5 Anti-kickback circuitry

An anti-kickback circuitry (RC-filter in Figure 15) is required to counteract the effects of the charge injection generated by the sampling capacitance.

The RC-filter is also used to filter noise from the signal before it reaches the sampling stage. It is recommended that the capacitor has a value that maximizes noise attenuation without degrading the settling time excessively.

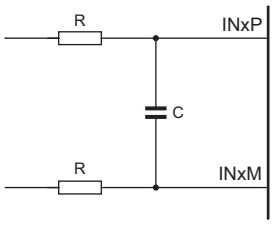


Fig 15. Anti-kickback circuit

The input frequency determines the component values. Select values that do not affect the input bandwidth. The values given in the following table are advised for 50Ω impedance system.

Table 12. RC coupling versus input frequency; typical values

Input frequency range (MHz)	R (Ω)	C (pF)
0 to 50	25	12
50 to 200	10	3.9
200 to 300	5	0.5

11.1.6 Transformer

The input frequency determines the configuration of the transformer circuit. The configuration shown in Figure 16 is suitable for a baseband application.

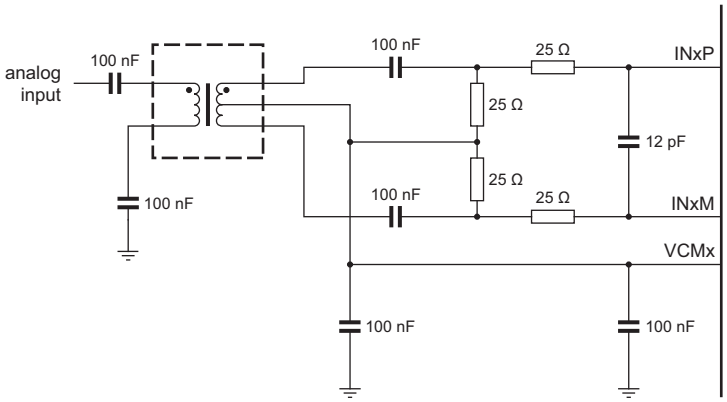


Fig 16. Single transformer configuration (baseband)

The configuration shown in Figure 17 is recommended for high-frequency applications. In both cases, the choice of transformer is a compromise between cost and performance.

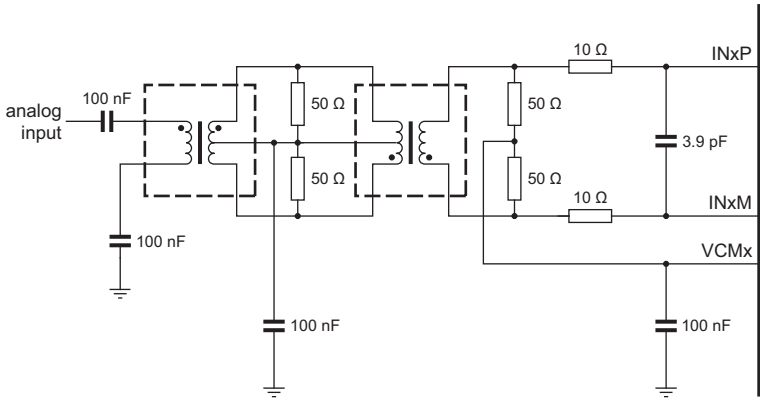


Fig 17. Dual transformer configuration (high IF)

11.2 Clock input

11.2.1 Drive modes

The ADC1453D series can be driven differentially (LVPECL, LVDS or SINE). A single-ended LVCMOS signal connected to either pin CLKP or pin CLKM can also drive the device (connect the complementary pin to ground using a capacitor). The LVPECL is recommended for an optimal performance.

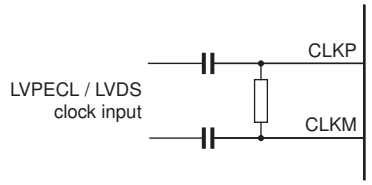
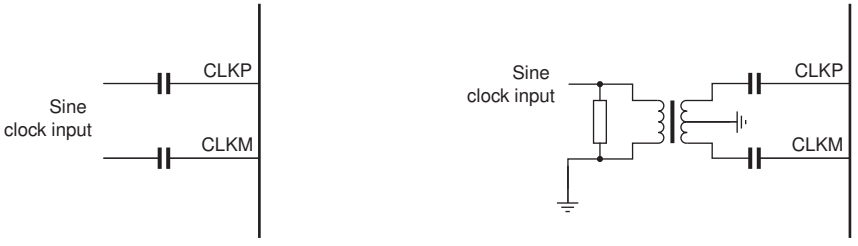


Fig 18. LVPECL/LVDS differential clock input



a. Differential sine clock input

b. Single-ended sine clock input (with transformer)

Fig 19. Sine clock input

a. Rising edge LVCMOS b. Falling edge LVCMOS

Fig 20. LVCMOS single-ended clock input

Single-ended or differential clock inputs can be selected via bit DIFF_SE of SPI. If single-ended is enabled, the input pin (pin CLKM or pin CLKP) is selected using control bit SE_SEL (see Table 29).

11.2.2 Equivalent input circuit

Figure 21 shows the equivalent circuit of the input clock buffer. The input signal must be AC-coupled and the common-mode voltage of the differential input stage is set via internal 5 kΩ resistors.

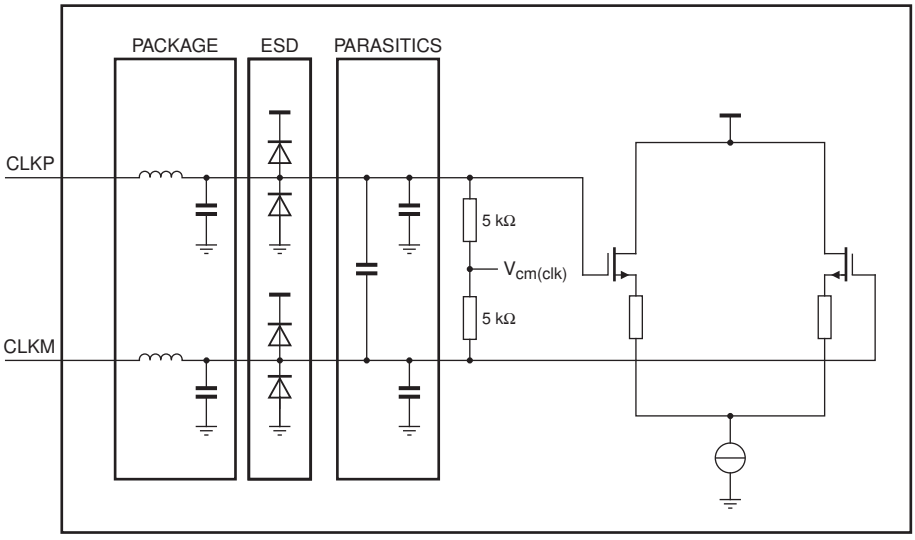


Fig 21. Equivalent input circuit

11.2.3 JESD204B harmonic clocking

The ADC1453D embeds an input clock divider that divides the incoming clock (clock frequency fclk) by a factor of 1 to 8. The output of this divider is then used as sampling clock (sampling frequency fs) (see bits CLK_DIV[2:0] in Table 29).

Caution must be taken to, first power the ADC1453D in «Power Down» mode by setting the CFG Pins to «1111» see Table 19, second, program the clock divider to the wanted value (see bits CLK_DIV[1:0] in Table 29) and finally, set the ADC using the SPI register IP_CFG_SETUP Table 43, to the wanted configuration.

11.2.4 JESD204B Deterministic Latency (pins SYSREFN and SYSREFP or SYNCBP and SYNCBN)

In the JESD204B standard 3 subclasses have been defined.
Subclass 0: No deterministic latency is required (equivalent to the JESD204A)

Subclass 1: Deterministic latency is required and is realized through the dedicated SYSREFP/N pins.

The deterministic latency can be controlled with a single-ended or a differential SYSREF signal.

When SYSREF is active (High by default), it resets the clock divider phase registers. In a multi-device application and when the clock divider factor is higher than 1, all sampling clock edges for multiple ADC1453D will be aligned (see Table 8 and Figure 3).

On top of this, the SYSREFP/N pins initiates an internal LMFC clock (Local Multi-frame Clock), with a period of a multi-frame F*K (F: number of octets per frame, K: number of frames per multi-frame). See table Table 19 for examples.

A single pulse of SYSREF is needed for both clock divider reset and LMFC initialization. Because the SYSREF processing doesn't stop the data transmission, the signal can also be sent periodically at an harmonic frequency of the LMFC in order to change the alignment. In case of a periodic SYSREF not correlated to the LMFC, the user can program the LMFC to take into account only the first SYSREF pulse (see bit LMFC_periodic_rst in Table 48).

At a SYNC request from the receiver (on pins SYNCBP/N), K28.5 comma characters are sent over the serial lanes. When the receiver releases the SYNC request, then the Initial Lane Alignment (ILA) will start at an edge of the LMFC

At the receiver side, the different lanes are aligned using the ILA start of frame characters and fetched at the next LMFC boundary.

This operation ensures a deterministic latency. See the JESD204B JEDEC standard for more information.

Subclass2: Behavior is similar to Subclass1, but, instead of using a dedicated SYSREF signal, the SYNCBP/N is used for both SYNC request and deterministic latency.

The rising edge of the SYNCBP/N start the LMFC, while the falling edge set the SYNC request and hence start the Initial Lane Alignment according to the JEDEC JESD204B standard.

Below is an example of a Subclass1 ADC1453D registers programming:

Table 13. Subclass1 path activation

Register	value	Comment
DCS_CTRL (@0x043)	0xC7	Choose the SYSREFP/N on rising edge as DCS Reset
JESD204B_CTRL1 (@810)	0xC0	Enable an LMFC periodic reset
JESD204B_CTRL2 (@811)	0x40	Enable a one shot DCS reset
JESD204B_CTRL3 (@812)	0x0A	Activate a Sync fetch at LMFC boundary
SYSREF_CFG (@81E)	0x08	Enable SYSREFP/N on differential mode

11.2.5 Clock Group Delay

The ADC1453D has the ability to delay the sampling clock when derived from a harmonic clock within the range of a complete sampling clock period and with half harmonic clock period step

The delay can be adjusted over 2 × N steps, where N is the clock divider ratio (bits CLK_DELAY[3:0] in Table 38).

As an example: for a device clock of 500 Mhz and a clock division by 2 (fs = 250 Msps), the sampling clock can be delayed over 4 steps of 1/(2*500 Mhz)= 1 ns.

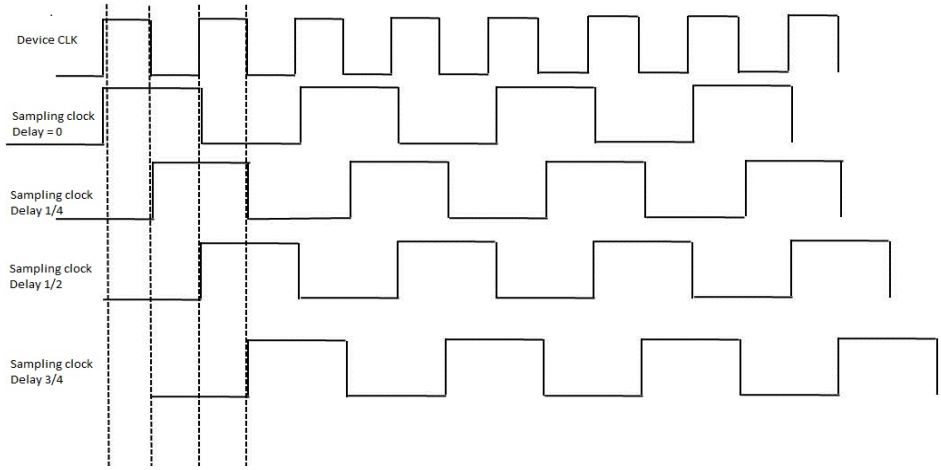


Fig 22. Sampling clock with 4 different clock delay for a 4 clock division

11.3 Digital outputs

11.3.1 Digital output buffers

The JESD204B standard specifies that both the receiver and the transmitter must share the same supply if they are connected in DC-coupling.

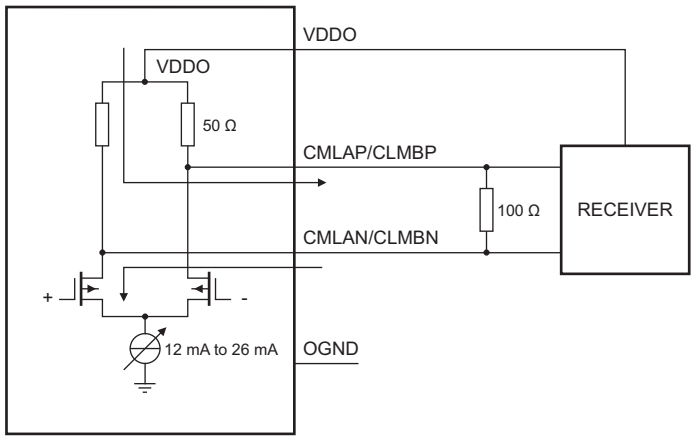


Fig 23. JESD204B serial output - DC-coupled

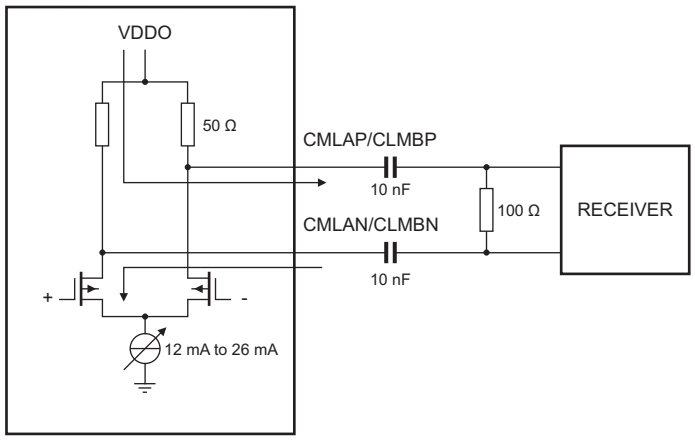


Fig 24. JESD204B serial output - AC-coupled

11.3.2 JESD204B serializer

11.3.2.1 Digital JESD204B formatter

The block placed after the ADC1453D cores implements all the JESD204B standard functionalities. This ensures signal integrity and guarantees the clock and the data recovery at the receiver side.

The block is highly configurable in various ways depending on the sampling frequency and the number of lanes used. All the processing and transmission are done with MSB first.

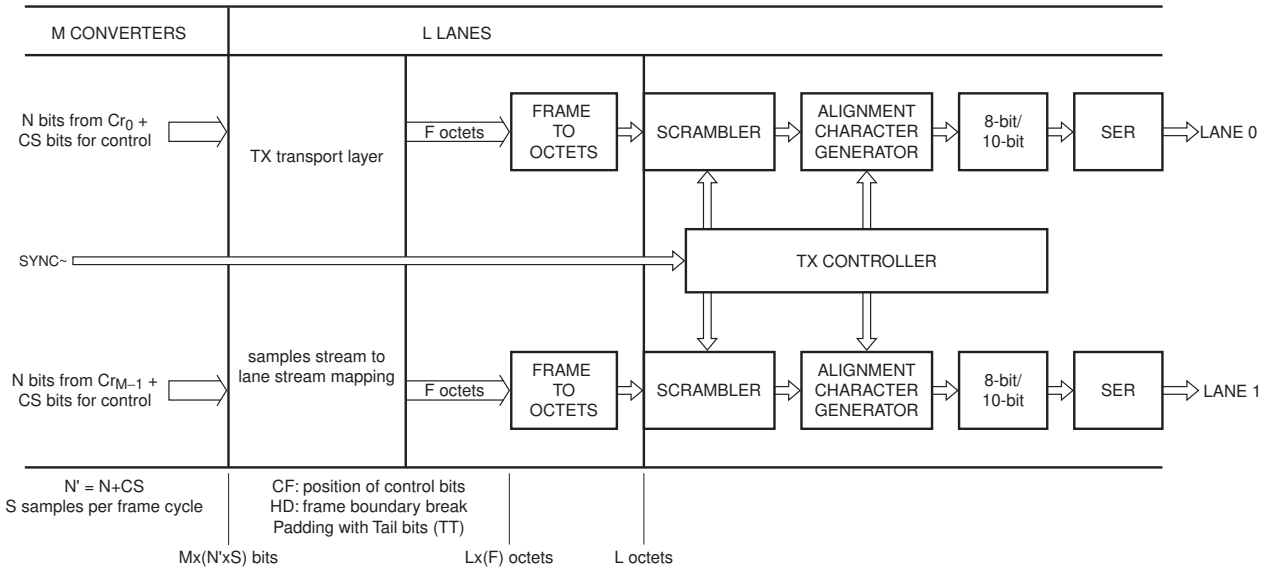


Fig 25. General overview of the JESD204B serializer

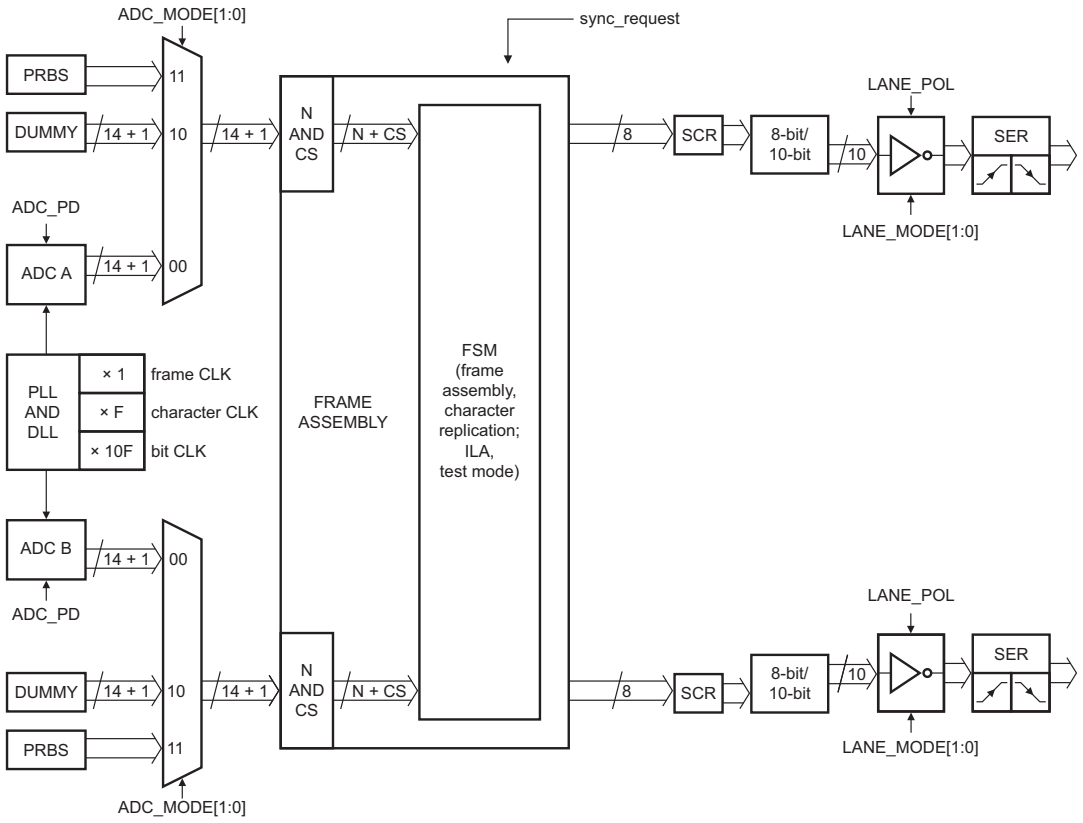


Fig 26. Detailed view of the JESD204B serializer with debug functionalities

11.3.2.2 Scrambler (SCR_EN)

The main purpose of scrambling is to avoid the spectral peaks that would be produced when the same data octet repeats from frame to frame. In general, scrambling makes the spectrum data-independent, so that possible frequency-selective effects on the electrical interface will not cause data-dependent errors. However, all digital operations in converters (including scrambling) cause some amount of switching noise, so there may be applications where it is of advantage to disable the scrambling.

The scrambler can be selected via the pin SCR_EN or the SPI registers (bit SCR_EN in Table 58).

Table 14. Scrambler configuration

Pin SCR_EN	Scrambler
HIGH	enabled
LOW	disabled

An internal pull-up resistor (50 kΩ) sets pin SCR_EN to HIGH when no signal is connected to it. The pin SCR_EN is active only at start-up or after a JESD204B reset (bit SCR_EN in Table 42).

11.3.3 OuT-of-Range (OTR)

An out-of-range signal is provided on pins OTRA and OTRB. The OTR signal goes logic level HIGH when the input signal exceeds the maximum full scale range.

The latency of OTR is 31 clock cycles. The OTR response can be speeded up by enabling fast OTR using SPI local registers (bit FAST_OTR in Table 37). In this mode, the latency of OTR is reduced to only 11 clock cycles. The fast OTR detection threshold (below full-scale) can be programmed using the SPI local registers (bits FAST_OTR_DET[2:0] in Table 37).

Table 15. Fast OTR register threshold

FAST_OTR_DET[2:0]	Detection level (dB)
000	−18.06
001	−14.54
010	−12.04
011	−8.52
100	**−6.02**
101	−4.08
110	−2.5
111	−1.16

11.3.4 Digital offset

By default, the ADC1453D delivers an output code that corresponds to the analog input. However, it is possible to add a digital offset to the output code using the SPI local registers (bits DIG_OFFSET[5:0] in see Table 16 and Table 33). The digital offset adjustment is coded in two's complement.

Table 16. Digital offset adjustment
Default values are shown highlighted.

DIG_OFFSET[5:0]	Digital offset adjustment (LSB)
10 0000	−32
10 0001	−31
...	...
11 1111	−1
00 0000	**0**
00 0001	+1
...	...
01 1110	+30
01 1111	+31

11.3.5 Test patterns

The ADC1453D can be configured to transmit a number of predefined test patterns using the SPI local registers (bits TEST_PAT_SEL[2:0] in Table 17 and Table 34). The selected test pattern is transmitted regardless of the analog input.

Table 17. Digital test pattern selection
Default values are shown highlighted.

TEST_PAT_SEL[2:0]	Digital test pattern
000	**Off**
001	Mid code
010	Min code
011	Max code
100	Toggle '1111..1111'/'0000..0000'
101	Custom test pattern
110	'0101..0101'
111	'1010..1010'

A custom test pattern can be defined using the SPI local registers (bits TEST_PAT_USER[13:6] in Table 35 and bits TEST_PAT_USER[5:0] in Table 36).

11.3.6 Output data format selection

The ADC1453D output data format can be selected (offset binary, two's complement or gray code) using the SPI local registers (bits DATA_FORMAT[1:0] in Table 32).

11.3.7 Output codes versus input voltage

Table 18. Output codes

$V_{INP} - V_{INM}$	Offset binary	Two's complement	Gray code	OTR
< –1	00 0000 0000 0000	10 0000 0000 0000	00 0000 0000 0000	1
–1	00 0000 0000 0000	10 0000 0000 0000	00 0000 0000 0000	0
–0.99987793	00 0000 0000 0001	10 0000 0000 0001	00 0000 0000 0001	0
–0.99975586	00 0000 0000 0010	00 0000 0000 0010	00 0000 0000 0011	0
...	...	...	...	0
–0.00024414	01 1111 1111 1110	11 1111 1111 1110	01 0000 0000 0001	0
–0.00012207	01 1111 1111 1111	11 1111 1111 1111	01 0000 0000 0000	0
+0.00012207	10 0000 0000 0000	00 0000 0000 0000	11 0000 0000 0000	0
+0.0.00024414	10 0000 0000 0001	00 0000 0000 0001	11 0000 0000 0001	0
...	...	...	...	0
+0.99975586	11 1111 1111 1101	01 1111 1111 1101	10 0000 0000 0011	0
+0.99987793	11 1111 1111 1110	01 1111 1111 1110	10 0000 0000 0001	0
+1	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000	0
> +1	11 1111 1111 1111	01 1111 1111 1111	10 0000 0000 0000	1