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# ADC1610S series

Single 16-bit ADC; 65 Msps, 80 Msps, 105 Msps or 125 Msps;  
CMOS or LVDS DDR digital outputs

Rev. 3 — 25 January 2011

Product data sheet

## 1. General description

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The ADC1610S is a single-channel 16-bit Analog-to-Digital Converter (ADC) optimized for high dynamic performance and low power consumption at sample rates up to 125 Msps. Pipelined architecture and output error correction ensure the ADC1610S is accurate enough to guarantee zero missing codes over the entire operating range. Supplied from a single 3 V source, it can handle output logic levels from 1.8 V to 3.3 V in CMOS mode, because of a separate digital output supply. It supports the Low Voltage Differential Signaling (LVDS) Double Data Rate (DDR) output standard. An integrated Serial Peripheral Interface (SPI) allows the user to easily configure the ADC. The device also includes a programmable full-scale SPI to allow a flexible input voltage range from 1 V to 2 V (peak-to-peak). With excellent dynamic performance from the baseband to input frequencies of 170 MHz or more, the ADC1610S is ideal for use in communications, imaging and medical applications.

## 2. Features and benefits

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- SNR, 72.5 dBFS; SFDR, 88 dBc
- Sample rate up to 125 Msps
- 16-bit pipelined ADC core
- Clock input divided by 2 for less jitter
- Single 3 V supply
- Flexible input voltage range: 1 V (p-p) to 2 V (p-p)
- CMOS or LVDS DDR digital outputs
- HVQFN40 package
- Input bandwidth, 600 MHz
- Power dissipation, 430 mW at 80 Msps
- Serial Peripheral Interface (SPI)
- Duty cycle stabilizer
- Fast Out-of-Range (OTR) detection
- Offset binary, two's complement, gray code
- Power-down and Sleep modes

## 3. Applications

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- Wireless and wired broadband communications
- Spectral analysis
- Ultrasound equipment
- Portable instrumentation
- Imaging systems
- Software defined radio



### 4. Ordering information

Table 1. Ordering information

Type number	f <sub>s</sub> (MSPS)	Package		Version
		Name	Description	
ADC1610S125HN/C1	125	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1
ADC1610S105HN/C1	105	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1
ADC1610S080HN/C1	80	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1
ADC1610S065HN/C1	65	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1

### 5. Block diagram

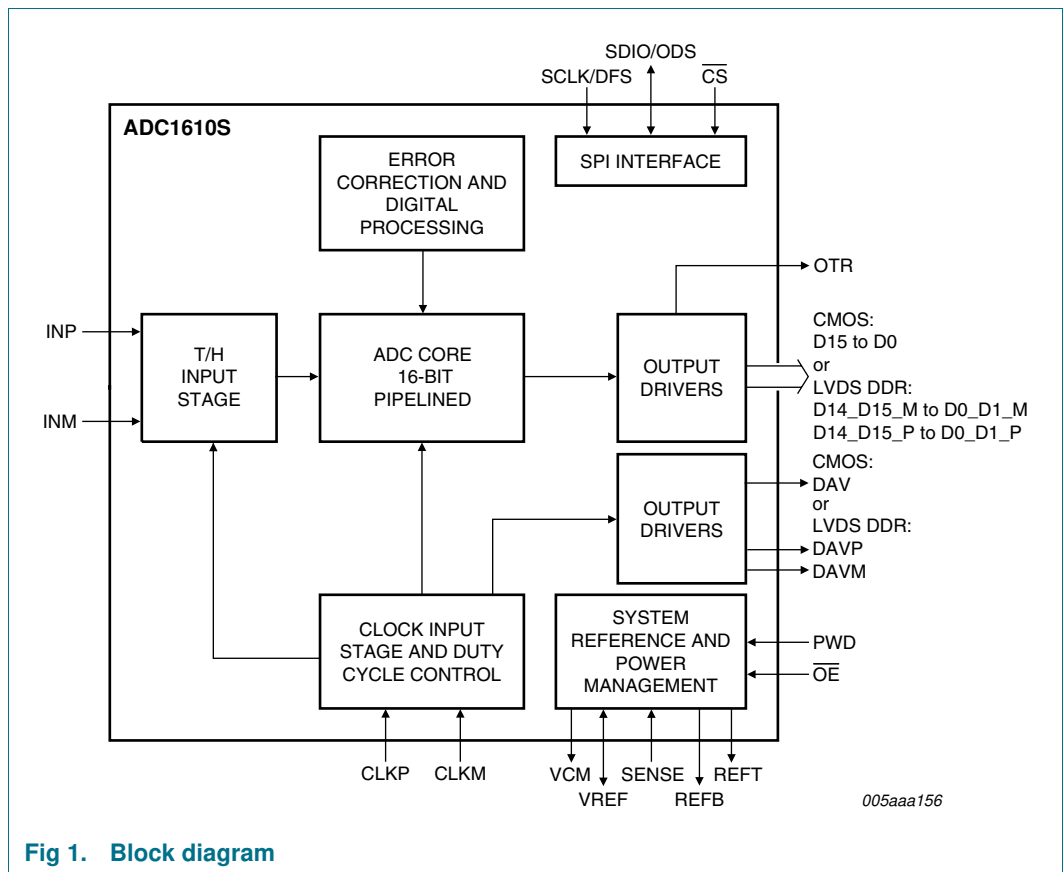
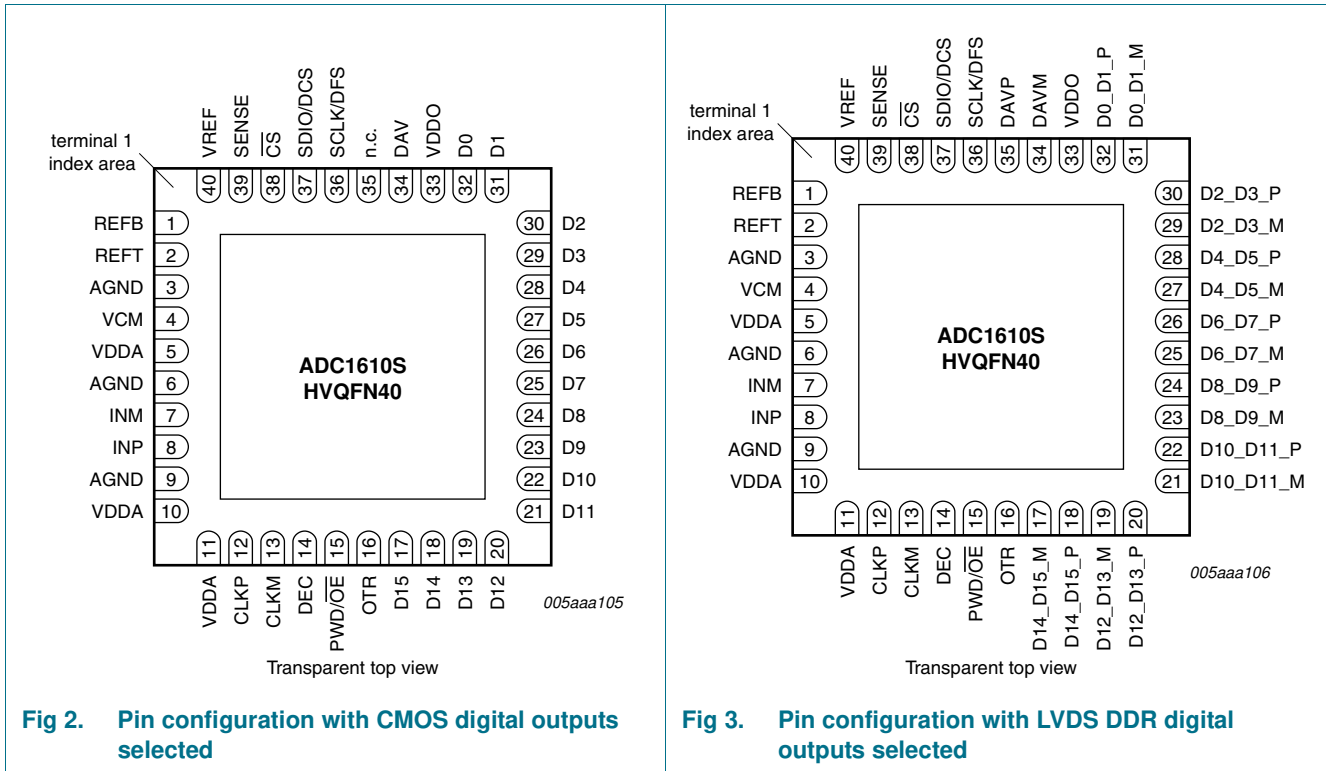


Fig 1. Block diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 2. Pin description (CMOS digital outputs)

Symbol	Pin	Type <sup>[1]</sup>	Description
REFB	1	O	bottom reference
REFT	2	O	top reference
AGND	3	G	analog ground
VCM	4	O	common-mode output voltage
VDDA	5	P	analog power supply
AGND	6	G	analog ground
INM	7	I	complementary analog input
INP	8	I	analog input
AGND	9	G	analog ground
VDDA	10	P	analog power supply
VDDA	11	P	analog power supply
CLKP	12	I	clock input
CLKM	13	I	complementary clock input
DEC	14	O	regulator decoupling node
PWD/ $\overline{\text{OE}}$	15	I	power down, active HIGH; output enable, active LOW
OTR	16	O	out of range

Table 2. Pin description (CMOS digital outputs) ...continued

Symbol	Pin	Type <sup>[1]</sup>	Description
D15	17	O	data output bit 15 (Most Significant Bit (MSB))
D14	18	O	data output bit 14
D13	19	O	data output bit 13
D12	20	O	data output bit 12
D11	21	O	data output bit 11
D10	22	O	data output bit 10
D9	23	O	data output bit 9
D8	24	O	data output bit 8
D7	25	O	data output bit 7
D6	26	O	data output bit 6
D5	27	O	data output bit 5
D4	28	O	data output bit 4
D3	29	O	data output bit 3
D2	30	O	data output bit 2
D1	31	O	data output bit 1
D0	32	O	data output bit 0 (Least Significant Bit (LSB))
VDDO	33	P	output power supply
DAV	34	O	data valid output clock
n.c.	35	-	not connected
SCLK/DFS	36	I	SPI clock; data format select
SDIO/ODS	37	I/O	SPI data IO; output data standard
$\overline{\text{CS}}$	38	I	SPI chip select
SENSE	39	I	reference programming pin
VREF	40	I/O	voltage reference input/output

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

**Table 3. Pin description (LVDS DDR) digital outputs)**

Symbol	Pin <sup>[1]</sup>	Type <sup>[2]</sup>	Description
D14_D15_M	17	O	differential output data D14 and D15 multiplexed, complement
D14_D15_P	18	O	differential output data D14 and D15 multiplexed, true
D12_D13_M	19	O	differential output data D12 and D13 multiplexed, complement
D12_D13_P	20	O	differential output data D12 and D13 multiplexed, true
D10_D11_M	21	O	differential output data D10 and D11 multiplexed, complement
D10_D11_P	22	O	differential output data D10 and D11 multiplexed, true
D8_D9_M	23	O	differential output data D8 and D9 multiplexed, complement
D8_D9_P	24	O	differential output data D8 and D9 multiplexed, true
D6_D7_M	25	O	differential output data D6 and D7 multiplexed, complement
D6_D7_P	26	O	differential output data D6 and D7 multiplexed, true
D4_D5_M	27	O	differential output data D4 and D5 multiplexed, complement
D4_D5_P	28	O	differential output data D4 and D5 multiplexed, true
D2_D3_M	29	O	differential output data D2 and D3 multiplexed, complement
D2_D3_P	30	O	differential output data D2 and D3 multiplexed, true
D0_D1_M	31	O	differential output data D0 and D1 multiplexed, complement
D0_D1_P	32	O	differential output data D0 and D1 multiplexed, true
DAVM	34	O	data valid output clock, complement
DAVP	35	O	data valid output clock, true

[1] Pins 1 to 16 and pins 36 to 40 are the same for both CMOS and LVDS DDR outputs (see [Table 2](#)).

[2] P: power supply; G: ground; I: input; O: output; I/O: input/output.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_O$	output voltage	pins D15 to D0; pins D14_D15_P to D0_D1_P; pins D14_D15_M to D0_D1_M	-0.4	+3.9	V
$V_{DDA}$	analog supply voltage		-0.4	+3.9	V
$V_{DDO}$	output supply voltage		-0.4	+3.9	V
$T_{stg}$	storage temperature		-55	+125	°C
$T_{amb}$	ambient temperature		-40	+85	°C
$T_j$	junction temperature		-	125	°C

## 8. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		<a href="#">[1]</a> 22.5	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		<a href="#">[1]</a> 11.7	K/W

[1] Value for six layers board in still air with a minimum of 25 thermal vias.

## 9. Static characteristics

Table 6. Static characteristics<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supplies</b>						
V <sub>DDA</sub>	analog supply voltage		2.85	3.0	3.4	V
V <sub>DDO</sub>	output supply voltage	CMOS mode	1.65	1.8	3.6	V
		LVDS DDR mode	2.85	3.0	3.6	V
I <sub>DDA</sub>	analog supply current	f <sub>clk</sub> = 125 Msps; f <sub>i</sub> = 70 MHz	-	210	-	mA
I <sub>DDO</sub>	output supply current	CMOS mode; f <sub>clk</sub> = 125 Msps; f <sub>i</sub> = 70 MHz	-	14	-	mA
		LVDS DDR mode: f <sub>clk</sub> = 125 Msps; f <sub>i</sub> = 70 MHz	-	43	-	mA
P	power dissipation	ADC1610S125; analog supply only	-	630	-	mW
		ADC1610S105; analog supply only	-	550	-	mW
		ADC1610S080; analog supply only	-	430	-	mW
		ADC1610S065; analog supply only	-	380	-	mW
		Power-down mode	-	2	-	mW
		Sleep mode	-	40	-	mW
<b>Clock inputs: pins CLKP and CLKM</b>						
<b>Low-Voltage Positive Emitter-Coupled Logic (LVPECL)</b>						
V <sub>i(clk)dif</sub>	differential clock input voltage	peak-to-peak	-	1.6	-	V
<b>SINE</b>						
V <sub>i(clk)dif</sub>	differential clock input voltage	peak	-	±3.0	-	V
<b>Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)</b>						
V <sub>IL</sub>	LOW-level input voltage		-	-	0.3V <sub>DDA</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DDA</sub>	-	-	V
<b>Logic inputs, Power-down: pin PWD/OE</b>						
V <sub>IL</sub>	LOW-level input voltage	LOW-medium level	-	0.3V <sub>DDA</sub>	-	V
		Medium-HIGH level	-	0.6V <sub>DDA</sub>	-	V
			-	0	-	V
V <sub>IH</sub>	HIGH-level input voltage		-	V <sub>DDA</sub>	-	V
I <sub>IL</sub>	LOW-level input current		-	55	-	μA
I <sub>IH</sub>	HIGH-level input current		-	65	-	μA
<b>Serial peripheral interface: pins CS, SDIO/ODS, SCLK/DFS</b>						
V <sub>IL</sub>	LOW-level input voltage		0	-	0.3V <sub>DDA</sub>	V
V <sub>IH</sub>	HIGH-level input voltage		0.7V <sub>DDA</sub>	-	V <sub>DDA</sub>	V
I <sub>IL</sub>	LOW-level input current		-10	-	+10	μA
I <sub>IH</sub>	HIGH-level input current		-50	-	+50	μA
C <sub>i</sub>	input capacitance		-	4	-	pF

Table 6. Static characteristics<sup>[1]</sup> ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Digital outputs, CMOS mode: pins D15 to D0, OTR, DAV</b>						
Output levels, $V_{DDO} = 3\text{ V}$						
$V_{OL}$	LOW-level output voltage		OGND	-	$0.2V_{DDO}$	V
$V_{OH}$	HIGH-level output voltage		$0.8V_{DDO}$	-	$V_{DDO}$	V
$C_O$	output capacitance	high impedance; $\overline{OE} = \text{HIGH}$	-	3	-	pF
Output levels, $V_{DDO} = 1.8\text{ V}$						
$V_{OL}$	LOW-level output voltage		OGND	-	$0.2V_{DDO}$	V
$V_{OH}$	HIGH-level output voltage		$0.8V_{DDO}$	-	$V_{DDO}$	V
<b>Digital outputs, LVDS mode: pins D14_D15_P to D0_D1_P, D14_D15_M to D0_D1_M, DAVP and DAVM</b>						
Output levels, $V_{DDO} = 3\text{ V}$ only, $R_L = 100\ \Omega$						
$V_{O(\text{offset})}$	output offset voltage	output buffer current set to 3.5 mA	-	1.2	-	V
$V_{O(\text{dif})}$	differential output voltage	output buffer current set to 3.5 mA	-	350	-	mV
$C_O$	output capacitance		-	3	-	pF
<b>Analog inputs: pins INP and INM</b>						
$I_I$	input current		-5	-	+5	$\mu\text{A}$
$R_{i(\text{dif})}$	differential input resistance		-	19.8	-	k $\Omega$
$C_{i(\text{dif})}$	differential input capacitance		-	2.8	-	pF
$V_{I(\text{cm})}$	common-mode input voltage	$V_{INP} = V_{INM}$	1.1	1.5	2.5	V
$B_i$	input bandwidth		-	650	-	MHz
$V_{I(\text{dif})}$	differential input voltage	peak-to-peak	1	-	2	V
<b>Common-mode output voltage: pin VCM</b>						
$V_{O(\text{cm})}$	common-mode output voltage		-	$V_{DDA} / 2$	-	V
$I_{O(\text{cm})}$	common-mode output current		-	4	-	mA
<b>I/O reference voltage: pin VREF</b>						
$V_{VREF}$	voltage on pin VREF	output	0.5	-	1	V
		input	0.5	-	1	V
<b>Accuracy</b>						
INL	integral non-linearity		-	$\pm 4$	-	LSB
DNL	differential non-linearity	guaranteed no missing codes	-0.95	$\pm 0.5$	+0.95	LSB
$E_{\text{offset}}$	offset error		-	$\pm 2$	-	mV
$E_G$	gain error	full-scale	-	$\pm 0.5$	-	%



**Table 6. Static characteristics**<sup>[1]</sup> ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Supply</b>						
PSRR	power supply rejection ratio	200 mV (p-p) on $V_{DDA}$ ; $f_i = DC$	-	-54	-	dB

[1] Typical values measured at  $V_{DDA} = 3 V$ ,  $V_{DDO} = 1.8 V$ ,  $T_{amb} = 25 °C$  and  $C_L = 5 pF$ ; minimum and maximum values are across the full temperature range  $T_{amb} = -40 °C$  to  $+85 °C$  at  $V_{DDA} = 3 V$ ,  $V_{DDO} = 1.8 V$ ;  $V_{INP} - V_{INM} = -1 dBFS$ ; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

## 10. Dynamic characteristics

### 10.1 Dynamic characteristics

Table 7. Dynamic characteristics

Symbol	Parameter	Conditions	ADC1610S065			ADC1610S080			ADC1610S105			ADC1610S125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>Analog signal processing</b>															
$\alpha_{2H}$	second harmonic level	$f_i = 3$ MHz	-	89	-	-	89	-	-	88	-	-	90	-	dBc
		$f_i = 30$ MHz	-	88	-	-	88	-	-	88	-	-	89	-	dBc
		$f_i = 70$ MHz	-	87	-	-	87	-	-	86	-	-	87	-	dBc
		$f_i = 170$ MHz	-	84	-	-	84	-	-	83	-	-	85	-	dBc
$\alpha_{3H}$	third harmonic level	$f_i = 3$ MHz	-	88	-	-	88	-	-	87	-	-	89	-	dBc
		$f_i = 30$ MHz	-	87	-	-	87	-	-	87	-	-	88	-	dBc
		$f_i = 70$ MHz	-	86	-	-	86	-	-	85	-	-	86	-	dBc
		$f_i = 170$ MHz	-	83	-	-	83	-	-	82	-	-	84	-	dBc
THD	total harmonic distortion	$f_i = 3$ MHz	-	85	-	-	85	-	-	84	-	-	86	-	dBc
		$f_i = 30$ MHz	-	84	-	-	84	-	-	84	-	-	85	-	dBc
		$f_i = 70$ MHz	-	83	-	-	83	-	-	82	-	-	83	-	dBc
		$f_i = 170$ MHz	-	80	-	-	80	-	-	79	-	-	81	-	dBc
ENOB	effective number of bits	$f_i = 3$ MHz	-	11.7	-	-	11.7	-	-	11.7	-	-	11.6	-	bits
		$f_i = 30$ MHz	-	11.6	-	-	11.6	-	-	11.6	-	-	11.6	-	bits
		$f_i = 70$ MHz	-	11.5	-	-	11.5	-	-	11.5	-	-	11.5	-	bits
		$f_i = 170$ MHz	-	11.4	-	-	11.4	-	-	11.4	-	-	11.4	-	bits
SNR	signal-to-noise ratio	$f_i = 3$ MHz	-	72.3	-	-	72.2	-	-	72.0	-	-	71.6	-	dBFS
		$f_i = 30$ MHz	-	71.5	-	-	71.4	-	-	71.4	-	-	71.3	-	dBFS
		$f_i = 70$ MHz	-	70.9	-	-	70.9	-	-	70.8	-	-	70.7	-	dBFS
		$f_i = 170$ MHz	-	70.4	-	-	70.3	-	-	70.2	-	-	70.1	-	dBFS
SFDR	spurious-free dynamic range	$f_i = 3$ MHz	-	88	-	-	88	-	-	87	-	-	89	-	dBc
		$f_i = 30$ MHz	-	87	-	-	87	-	-	87	-	-	88	-	dBc
		$f_i = 70$ MHz	-	86	-	-	86	-	-	85	-	-	86	-	dBc
		$f_i = 170$ MHz	-	83	-	-	83	-	-	82	-	-	84	-	dBc

**Table 7. Dynamic characteristics ...continued**

Symbol	Parameter	Conditions	ADC1610S065			ADC1610S080			ADC1610S105			ADC1610S125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IMD	intermodulation distortion	$f_i = 3 \text{ MHz}$	-	89	-	-	89	-	-	88	-	-	89	-	dBc
		$f_i = 30 \text{ MHz}$	-	88	-	-	88	-	-	88	-	-	88	-	dBc
		$f_i = 70 \text{ MHz}$	-	87	-	-	87	-	-	86	-	-	86	-	dBc
		$f_i = 170 \text{ MHz}$	-	84	-	-	85	-	-	83	-	-	84	-	dBc

[1] Typical values measured at  $V_{DDA} = 3 \text{ V}$ ,  $V_{DDO} = 1.8 \text{ V}$ ,  $T_{amb} = 25 \text{ }^\circ\text{C}$  and  $C_L = 5 \text{ pF}$ ; minimum and maximum values are across the full temperature range  $T_{amb} = -40 \text{ }^\circ\text{C}$  to  $+85 \text{ }^\circ\text{C}$  at  $V_{DDA} = 3 \text{ V}$ ,  $V_{DDO} = 1.8 \text{ V}$ ;  $V_{INP} - V_{INM} = -1 \text{ dBFS}$ ; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

## 10.2 Clock and digital output timing

**Table 8. Clock and digital output timing characteristics[1]**

Symbol	Parameter	Conditions	ADC1610S065			ADC1610S080			ADC1610S105			ADC1610S125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	

### Clock timing input: pins CLKP and CLKM

$f_{clk}$	clock frequency		40	-	65	60	-	80	75	-	105	100	-	125	MHz
$t_{lat(data)}$	data latency time		-	13.5	-	-	13.5	-	-	13.5	-	-	13.5	-	clock cycles
$\delta_{clk}$	clock duty cycle	DCS_EN = logic 1	30	50	70	30	50	70	30	50	70	30	50	70	%
		DCS_EN = logic 0	45	50	55	45	50	55	45	50	55	45	50	55	%
$t_{d(s)}$	sampling delay time		-	0.8	-	-	0.8	-	-	0.8	-	-	0.8	-	ns
$t_{wake}$	wake-up time		-	76	-	-	76	-	-	76	-	-	76	-	$\mu\text{s}$

### CMOS Mode timing output: pins D15 to D0 and DAV

$t_{PD}$	propagation delay	DATA	13.6	14.9	16.4	11.9	12.9	14.4	8.0	10.8	12.4	8.2	9.7	11.3	ns
		DAV	-	4.2	-	-	3.6	-	-	3.3	-	-	3.4	-	ns
$t_{su}$	set-up time		-	12.5	-	-	9.8	-	-	6.8	-	-	5.6	-	ns
$t_h$	hold time		-	3.4	-	-	3.3	-	-	3.1	-	-	2.8	-	ns
$t_r$	rise time	DATA	<a href="#">2</a> 0.39	-	2.4	0.39	-	2.4	0.39	-	2.4	0.39	-	2.4	ns
		DAV	0.26	-	2.4	0.26	-	2.4	0.26	-	2.4	0.26	-	2.4	ns
$t_f$	fall time	DATA	<a href="#">2</a> 0.19	-	2.4	0.19	-	2.4	0.19	-	2.4	0.19	-	2.4	ns

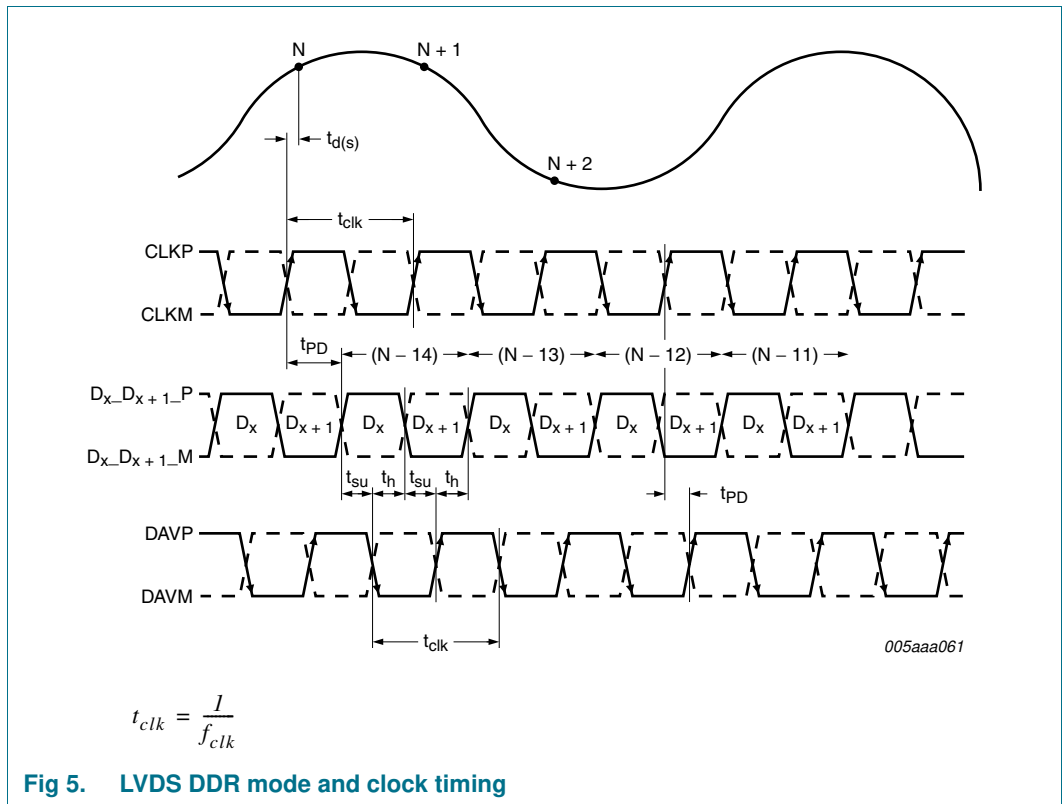
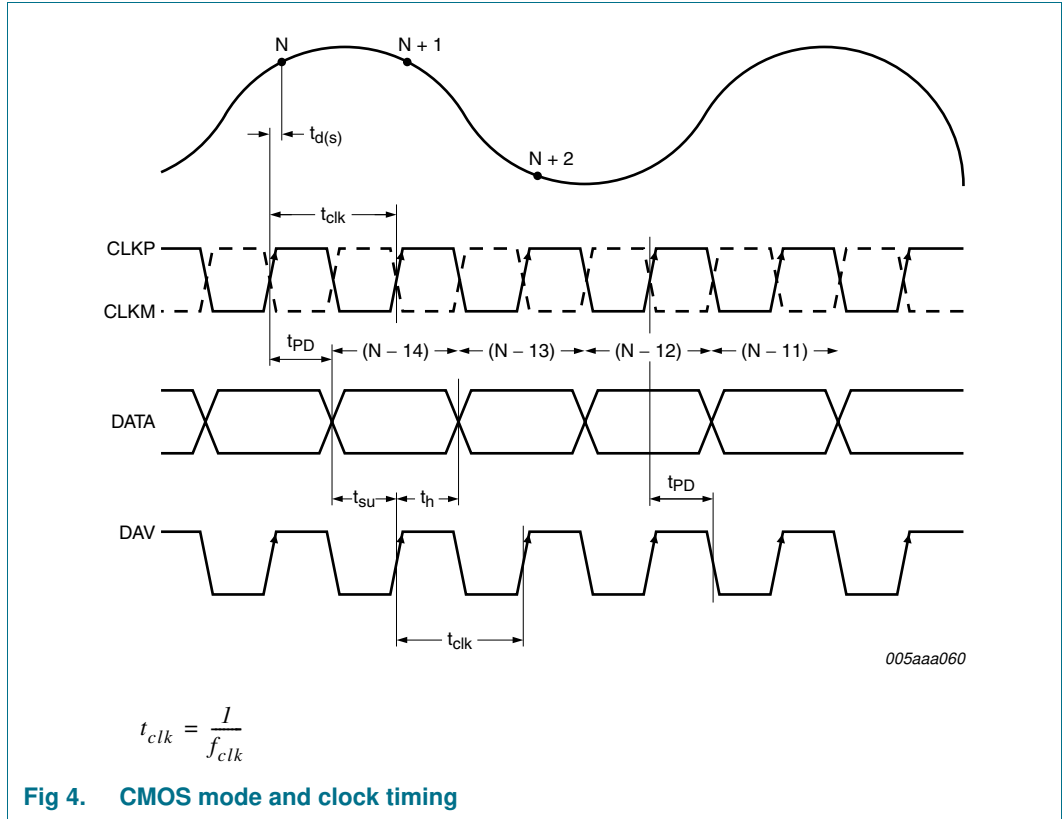
Table 8. Clock and digital output timing characteristics<sup>[1]</sup> ...continued

Symbol	Parameter	Conditions	ADC1610S065			ADC1610S080			ADC1610S105			ADC1610S125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
<b>LVDS DDR mode timing output: pins D14_D15_P to D0_D1_P, D14_D15_M to D0_D1_M, DAVP and DAVM</b>															
t <sub>PD</sub>	propagation delay	DATA	3.3	5.1	7.6	2.9	4.6	7.1	2.5	4.2	6.8	2.2	4.0	6.6	ns
		DAV	-	2.8	-	-	2.5	-	-	2.3	-	-	2.2	-	ns
t <sub>su</sub>	set-up time		-	5.4	-	-	4.1	-	-	2.6	-	-	1.9	-	ns
t <sub>h</sub>	hold time		-	2.2	-	-	2.0	-	-	1.8	-	-	1.7	-	ns
t <sub>r</sub>	rise time	DATA <sup>[3]</sup>	0.5	-	5	0.5	-	5	0.5	-	5	0.5	-	5	ns
		DAV	0.18	-	2.4	0.18	-	2.4	0.18	-	2.4	0.18	-	2.4	ns
t <sub>f</sub>	fall time	DATA <sup>[3]</sup>	0.15	-	1.6	0.15	-	1.6	0.15	-	1.6	0.15	-	1.6	ns

[1] Typical values measured at V<sub>DDA</sub> = 3 V, V<sub>DDO</sub> = 1.8 V, T<sub>amb</sub> = 25 °C and C<sub>L</sub> = 5 pF; minimum and maximum values are across the full temperature range T<sub>amb</sub> = -40 °C to +85 °C at V<sub>DDA</sub> = 3 V, V<sub>DDO</sub> = 1.8 V; V<sub>INP</sub> - V<sub>INM</sub> = -1 dBFS; internal reference mode; applied to CMOS and LVDS interface; unless otherwise specified.

[2] Measured between 20 % to 80 % of V<sub>DDO</sub>.

[3] Rise time measured from -50 mV to +50 mV; fall time measured from +50 mV to -50 mV.



10.3 SPI timings

Table 9. SPI timings characteristics<sup>[1]</sup>

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCLK)}$	SCLK pulse width		-	40	-	ns
$t_{w(SCLKH)}$	SCLK HIGH pulse width		-	16	-	ns
$t_{w(SCLKL)}$	SCLK LOW pulse width		-	16	-	ns
$t_{su}$	set-up time	data to SCLK HIGH	-	5	-	ns
		$\overline{CS}$ to SCLK HIGH	-	5	-	ns
$t_h$	hold time	data to SCLK HIGH	-	2	-	ns
		$\overline{CS}$ to SCLK HIGH	-	2	-	ns
$f_{clk(max)}$	maximum clock frequency		-	25	-	MHz

[1] Typical values measured at  $V_{DDA} = 3\text{ V}$ ,  $V_{DDO} = 1.8\text{ V}$ ,  $T_{amb} = 25\text{ }^\circ\text{C}$  and  $C_L = 5\text{ pF}$ ; minimum and maximum values are across the full temperature range  $T_{amb} = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  at  $V_{DDA} = 3\text{ V}$ ,  $V_{DDO} = 1.8\text{ V}$ .

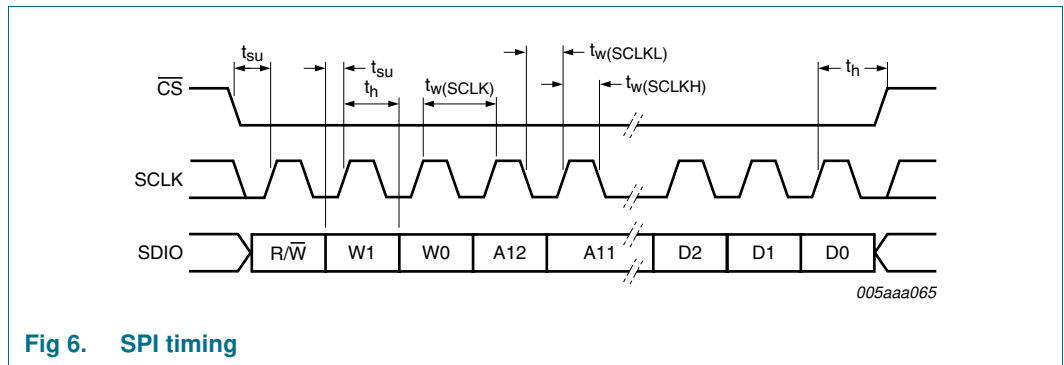


Fig 6. SPI timing

10.4 Typical characteristics

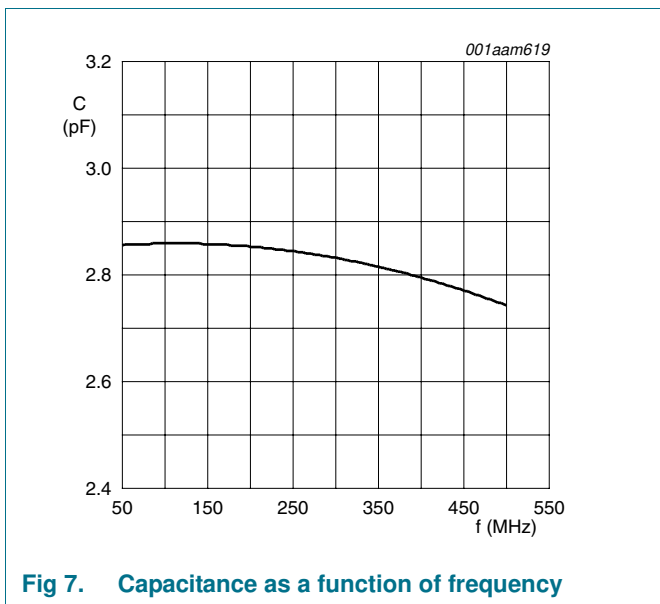


Fig 7. Capacitance as a function of frequency

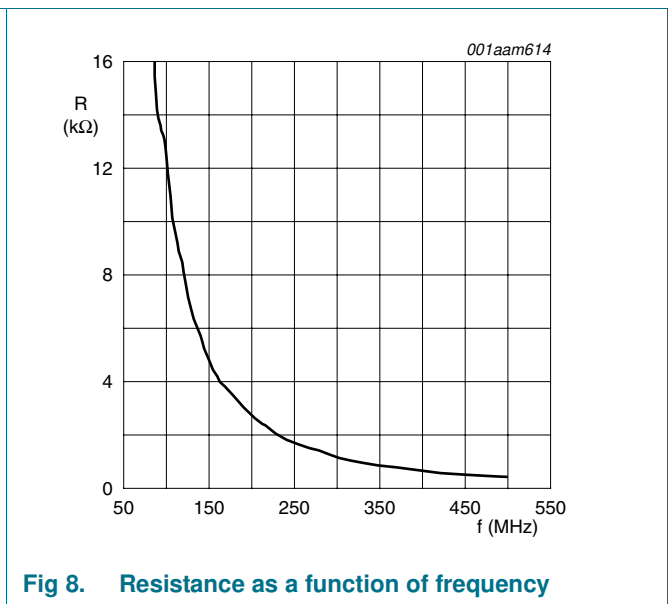
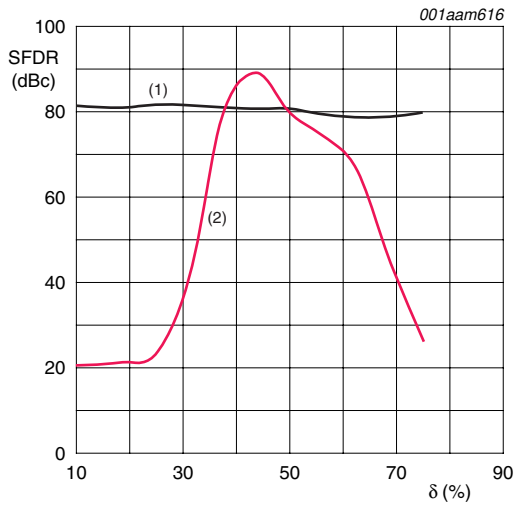
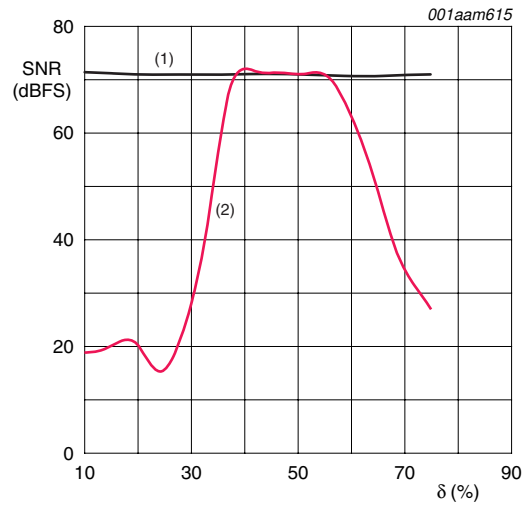


Fig 8. Resistance as a function of frequency



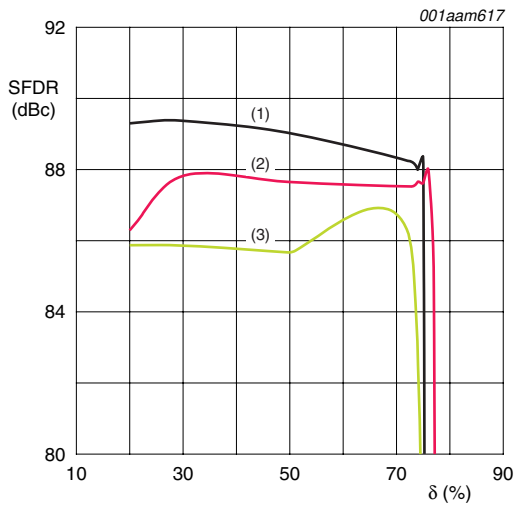
$T = 25\text{ }^\circ\text{C}$ ;  $V_{DD} = 3\text{ V}$ ;  $f_i = 170\text{ MHz}$ ;  $f_s = 125\text{ Mpsps}$ .  
 (1) DCS on.  
 (2) DCS off.

**Fig 9. SFDR as a function of duty cycle ( $\delta$ )**



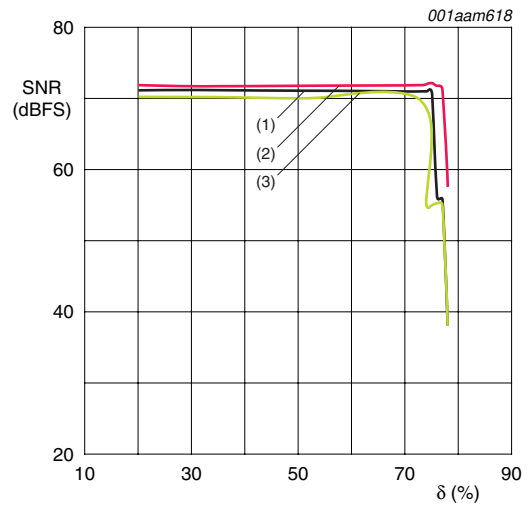
$T = 25\text{ }^\circ\text{C}$ ;  $V_{DD} = 3\text{ V}$ ;  $f_i = 170\text{ MHz}$ ;  $f_s = 125\text{ Mpsps}$ .  
 (1) DCS on.  
 (2) DCS off.

**Fig 10. SNR as a function of duty cycle ( $\delta$ )**



(1)  $T_{amb} = -40\text{ }^\circ\text{C}$ /typical supply voltages.  
 (2)  $T_{amb} = +25\text{ }^\circ\text{C}$ /typical supply voltages.  
 (3)  $T_{amb} = +90\text{ }^\circ\text{C}$ /typical supply voltages.

**Fig 11. SFDR as a function of duty cycle ( $\delta$ )**



(1)  $T_{amb} = -40\text{ }^\circ\text{C}$ /typical supply voltages.  
 (2)  $T_{amb} = +25\text{ }^\circ\text{C}$ /typical supply voltages.  
 (3)  $T_{amb} = +90\text{ }^\circ\text{C}$ /typical supply voltages.

**Fig 12. SNR as a function of duty cycle ( $\delta$ )**

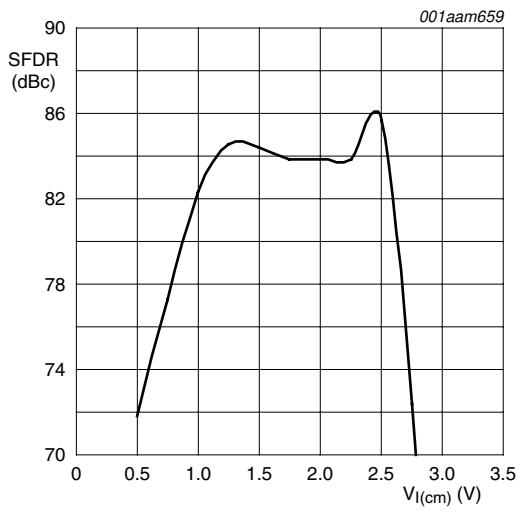


Fig 13. SFDR as a function of common-mode input voltage ( $V_{I(cm)}$ )

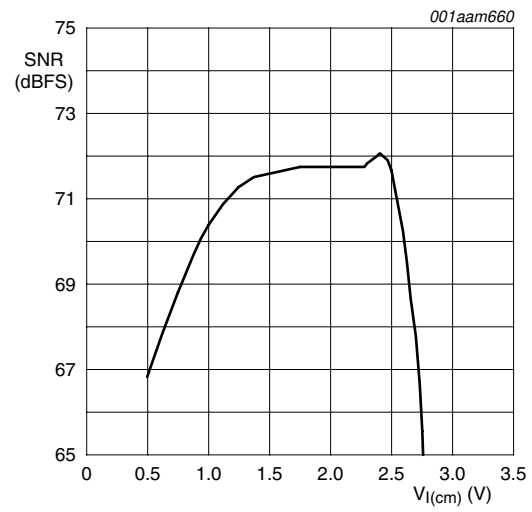


Fig 14. SNR as a function of common-mode input voltage ( $V_{I(cm)}$ )



## 11. Application information

### 11.1 Device control

The ADC1610S can be controlled via SPI or directly via the I/O pins (Pin control mode).

#### 11.1.1 SPI and Pin control modes

The device enters Pin control mode at power-up, and remains in this mode as long as pin  $\overline{CS}$  is held HIGH. In Pin control mode, the SPI pins SDIO,  $\overline{CS}$  and SCLK are used as static control pins.

SPI control mode is enabled by forcing pin  $\overline{CS}$  LOW. Once SPI control mode has been enabled, the device remains in this mode. The transition from Pin control mode to SPI control mode is illustrated in [Figure 15](#).

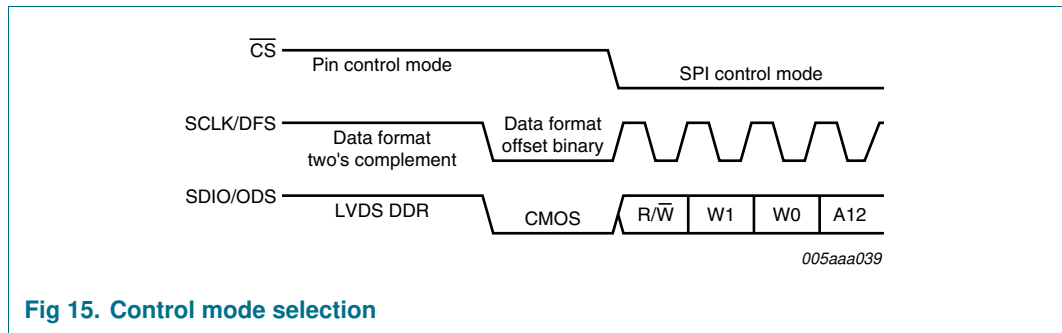


Fig 15. Control mode selection

When the device enters SPI control mode, the output data standard and data format are determined by the level on pin SDIO when a transition is triggered by a falling edge on pin  $\overline{CS}$ .

#### 11.1.2 Operating mode selection

The active ADC1610S operating mode (Power-up, Power-down or Sleep) can be selected using bits OP\_MODE[1:0] of the Reset and operating mode register (see [Table 20](#)) or using pins PWD and  $\overline{OE}$  in Pin control mode, as described in [Table 10](#).

Table 10. Operating mode selection pin PWD/ $\overline{OE}$

Pin PWD/ $\overline{OE}$	Power mode	Output high-Z
GND	Power-down	yes
1/3 V <sub>DDA</sub>	Sleep	yes
2/3 V <sub>DDA</sub>	Power-up	yes
V <sub>DDA</sub>	Power-up	no

#### 11.1.3 Selecting the output data standard

The output data standard (CMOS or LVDS DDR) can be selected via the SPI interface (see [Table 23](#)) or using pin ODS in Pin control mode. LVDS DDR is selected when ODS is HIGH, otherwise CMOS is selected.

11.1.4 Selecting the output data format

The output data format can be selected via the SPI interface (offset binary, two's complement or gray code; see [Table 23](#)) or using pin DFS in Pin control mode (offset binary or two's complement). Offset binary is selected when DFS is LOW. When DFS is HIGH, two's complement is selected.

11.2 Analog inputs

11.2.1 Input stage

The analog input of the ADC1610S supports a differential or a single-ended input drive. Optimal performance is achieved using differential inputs with the common-mode input voltage ( $V_{I(cm)}$ ) on pins INP and INM set to  $0.5V_{DDA}$ .

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) via a programmable internal reference (see [Section 11.3](#) and [Table 22](#)).

The equivalent circuit of the sample and hold input stage, including Electrostatic Discharge (ESD) protection and circuit and package parasitics, is shown in [Figure 16](#).

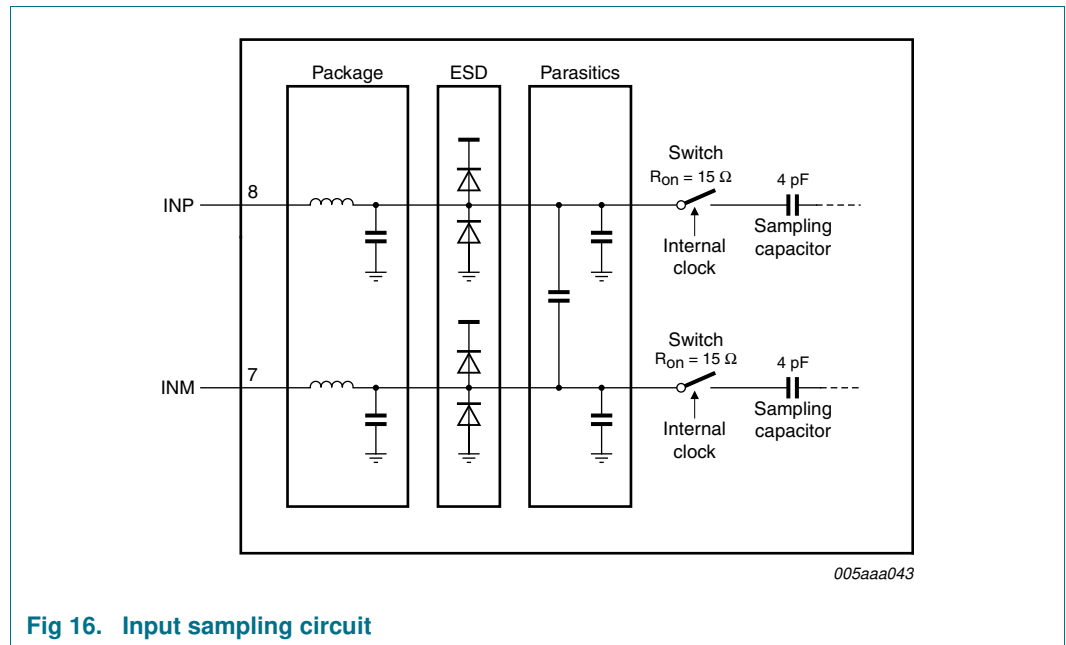


Fig 16. Input sampling circuit

The sample phase occurs when the internal clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the clock signal goes LOW, the stage enters the hold phase and the voltage information is transmitted to the ADC core.

11.2.2 Anti-kickback circuitry

Anti-kickback circuitry (R-C filter in [Figure 17](#)) is needed to counteract the effects of a charge injection generated by the sampling capacitance.

The RC filter is also used to filter noise from the signal before it reaches the sampling stage. The value of the capacitor should be chosen to maximize noise attenuation without degrading the settling time excessively.

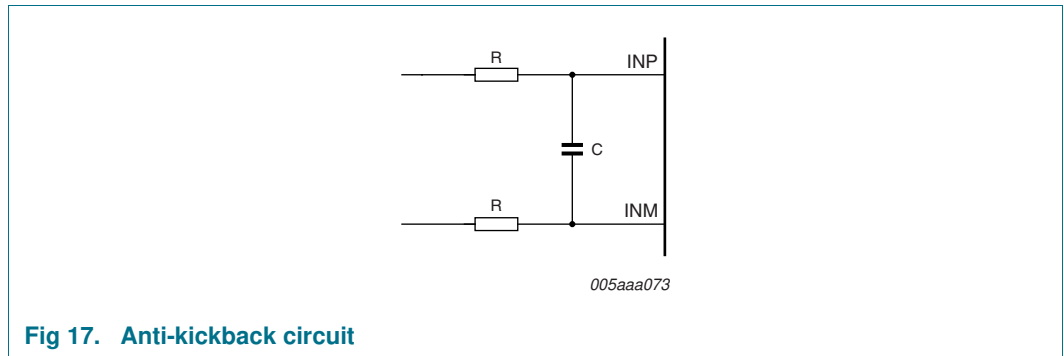


Fig 17. Anti-kickback circuit

The component values are determined by the input frequency and should be selected so as not to affect the input bandwidth.

Table 11. RC coupling versus input frequency, typical values

Input frequency (MHz)	Resistance ( $\Omega$ )	Capacitance (pF)
3 MHz	25 $\Omega$	12 pF
70 MHz	12 $\Omega$	8 pF
170 MHz	12 $\Omega$	8 pF

11.2.3 Transformer

The configuration of the transformer circuit is determined by the input frequency. The configuration shown in [Figure 18](#) would be suitable for a baseband application.

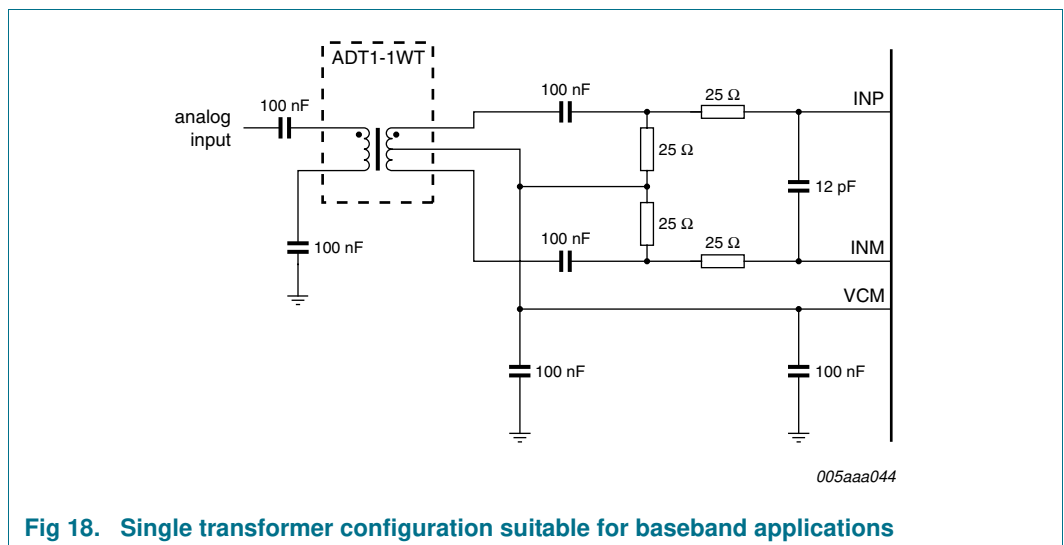
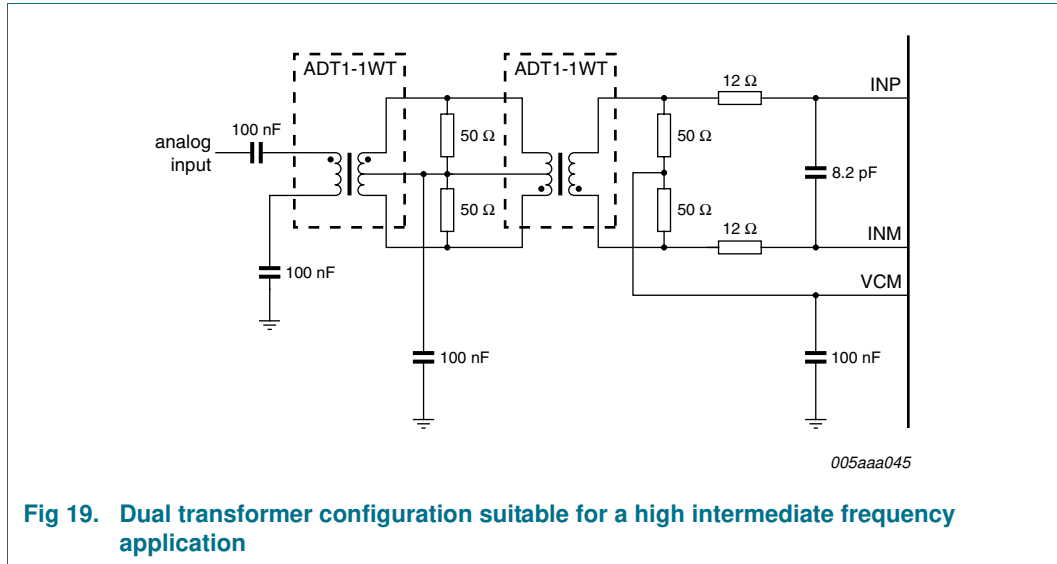


Fig 18. Single transformer configuration suitable for baseband applications

The configuration shown in [Figure 19](#) is recommended for high frequency applications. In both cases, the choice of transformer is a compromise between cost and performance.



### 11.3 System reference and power management

#### 11.3.1 Internal/external references

The ADC1610S has a stable and accurate built-in internal reference voltage to adjust the ADC full-scale. This reference voltage can be set internally via SPI or with pins VREF and SENSE (programmable in 1 dB steps between 0 dB and -6 dB via control bits INTREF[2:0] when bit INTREF\_EN = logic 1; see [Table 22](#)). See [Figure 21](#) to [Figure 24](#). The equivalent reference circuit is shown in [Figure 20](#). An external reference is also possible by providing a voltage on pin VREF as described in [Figure 23](#).

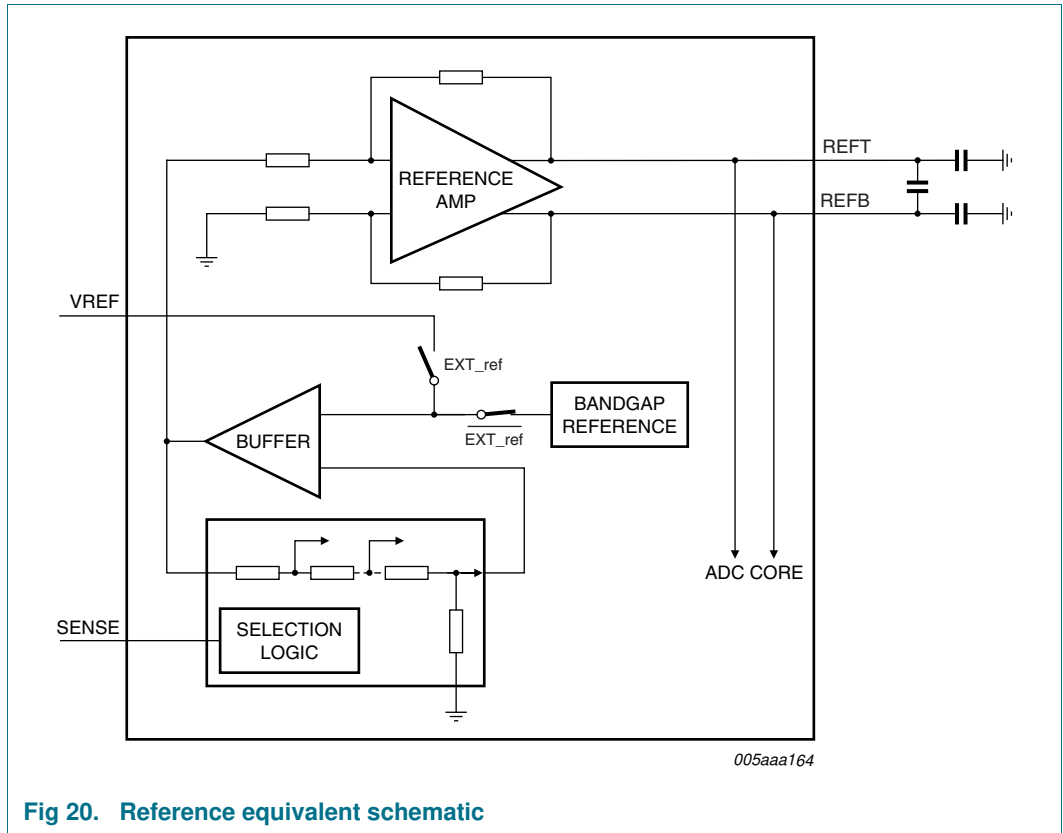


Fig 20. Reference equivalent schematic

If bit INTREF\_EN is set to logic 0, the reference voltage is determined either internally or externally as detailed in Table 12.

Table 12. Reference selection

Selection	SPI bit INTREF_EN	SENSE pin	VREF pin	Full-scale (p-p)
internal (Figure 21)	0	AGND	330 pF capacitor to AGND	2 V
internal (Figure 22)	0	pin VREF connected to pin SENSE and via a 330 pF capacitor to AGND		1 V
external (Figure 23)	0	V <sub>DDA</sub>	external voltage between 0.5 V and 1 V <sup>[1]</sup>	1 V to 2 V
internal via SPI (Figure 24)	1	pin VREF connected to pin SENSE and via 330 pF capacitor to AGND		1 V to 2 V

[1] The voltage on pin VREF is doubled internally to generate the internal reference voltage.

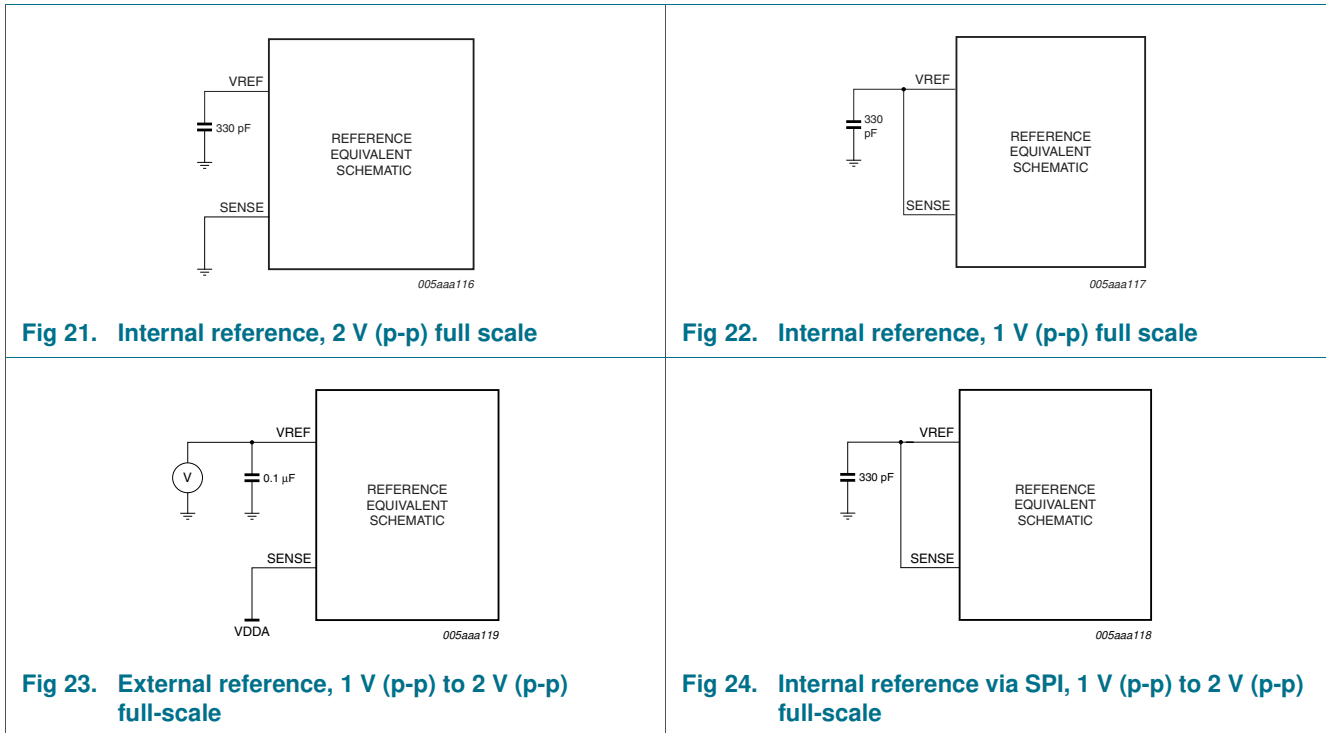


Figure 21 to Figure 24 illustrate how to connect the SENSE and VREF pins to select the required reference voltage source.

**11.3.2 Programmable full-scale**

The full-scale is programmable between 1 V (p-p) to 2 V (p-p) (see Table 13).

**Table 13. Reference SPI gain control**

INTREF[2:0]	Gain (dB)	Full-scale (V (p-p))
000	0	2
001	-1	1.78
010	-2	1.59
011	-3	1.42
100	-4	1.26
101	-5	1.12
110	-6	1
111	reserved	x

11.3.3 Common-mode output voltage ( $V_{O(cm)}$ )

A 0.1  $\mu\text{F}$  filter capacitor should be connected between pin VCM and ground to ensure a low-noise common-mode output voltage. When AC-coupled, pin VCM can be used to set the common-mode reference for the analog inputs, for instance via a transformer middle point.

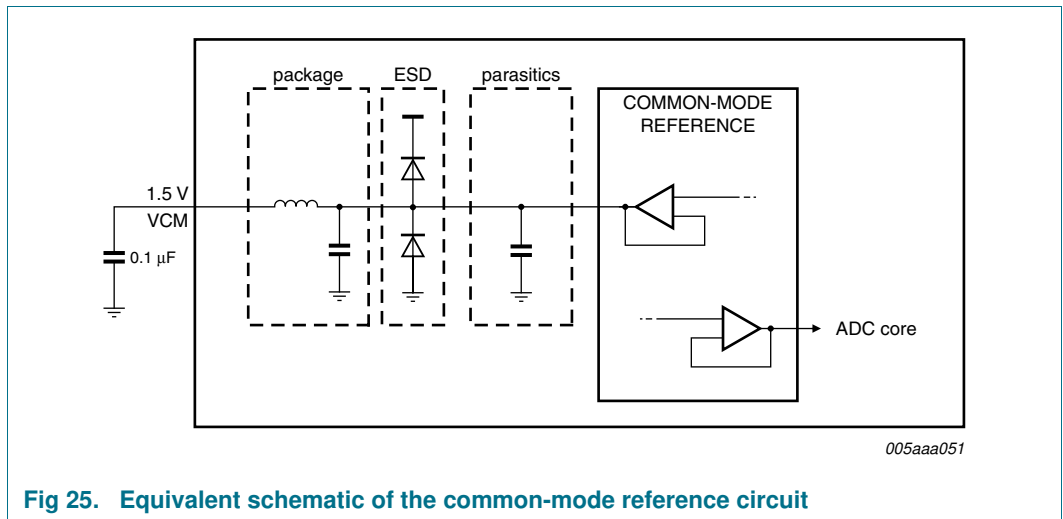


Fig 25. Equivalent schematic of the common-mode reference circuit

11.3.4 Biasing

The common-mode input voltage ( $V_{I(cm)}$ ) on pins INP and INM should be set externally to  $0.5V_{DDA}$  for optimal performance and should always be between 0.9 V and 2 V.

11.4 Clock input

11.4.1 Drive modes

The ADC1610S can be driven differentially (LVPECL). It can also be driven by a single-ended Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS) signal connected to pin CLKP (pin CLKM should be connected to ground via a capacitor) or pin CLKM (pin CLKP should be connected to ground via a capacitor).

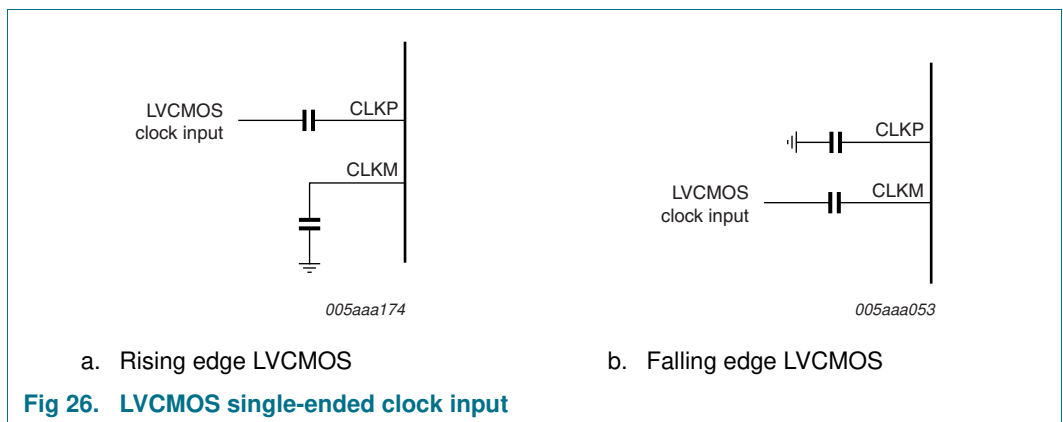
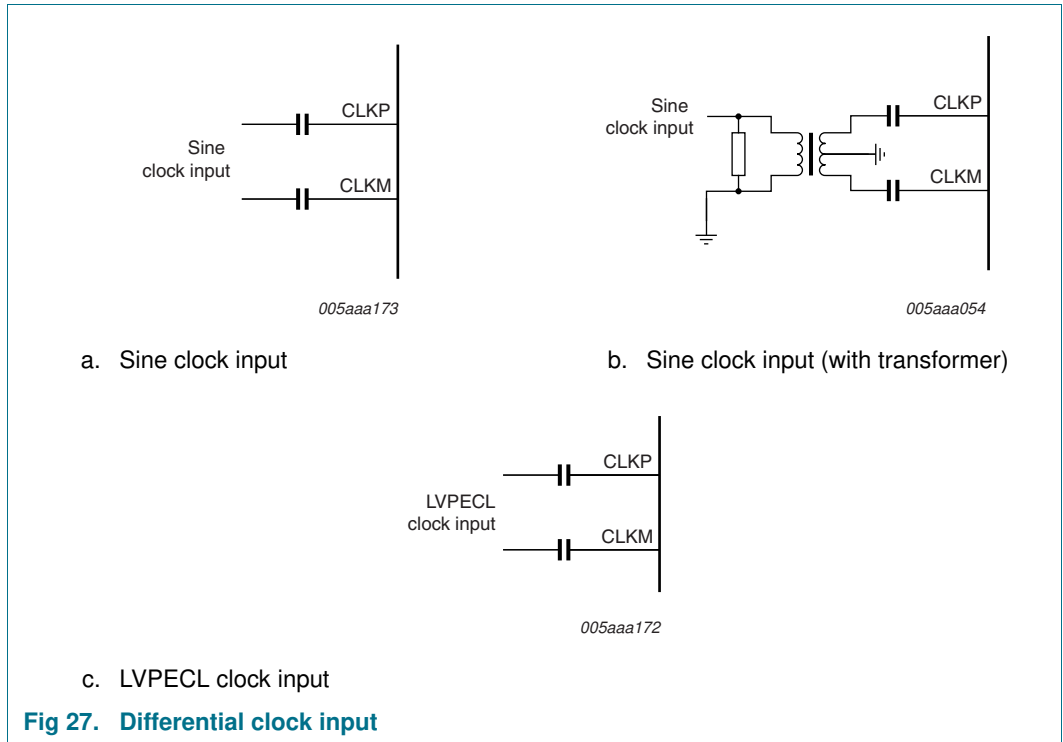
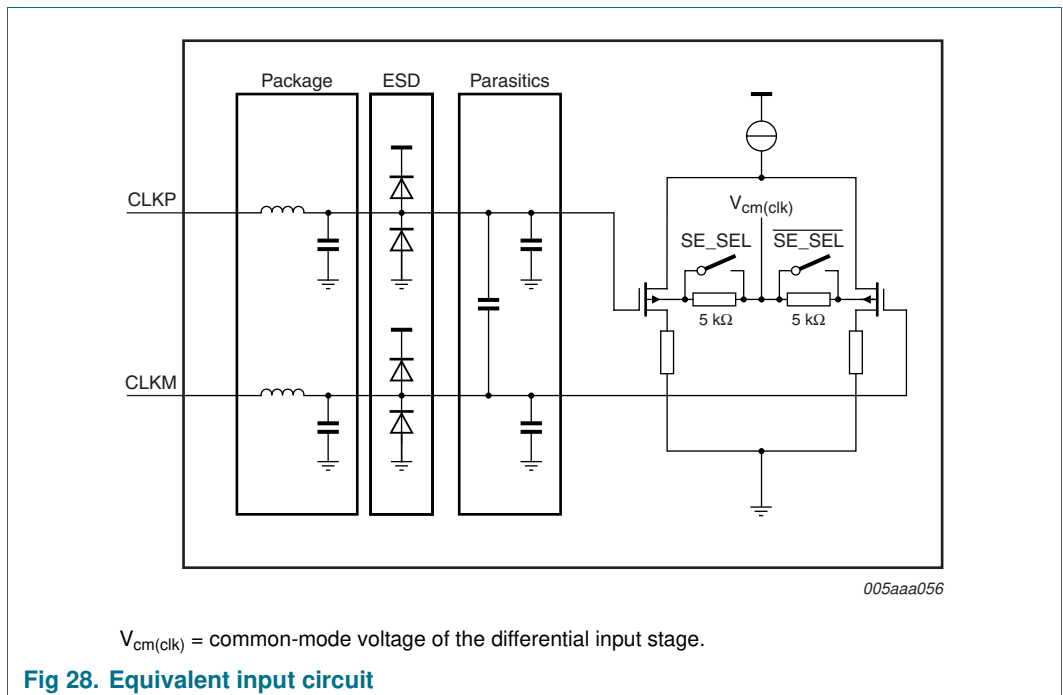


Fig 26. LVCMOS single-ended clock input



11.4.2 Equivalent input circuit

The equivalent circuit of the input clock buffer is shown in Figure 29. The common-mode voltage of the differential input stage is set via internal 5 kΩ resistors.





Single-ended or differential clock inputs can be selected via the SPI interface (see [Table 21](#)). If single-ended is enabled, the input pin (CLKM or CLKP) is selected via control bit SE\_SEL.

If single-ended is implemented without setting bit SE\_SEL to the appropriate value, the unused pin should be connected to ground via a capacitor.

**11.4.3 Duty cycle stabilizer**

The duty cycle stabilizer can improve the overall performance of the ADC by compensating the duty cycle of the input clock signal. When the duty cycle stabilizer is active (bit DCS\_EN = logic 1; see [Table 21](#)), the circuit can handle signals with duty cycles of between 30 % and 70 % (typical). When the duty cycle stabilizer is disabled (DCS\_EN = logic 0), the input clock signal should have a duty cycle of between 45 % and 55 %.

**11.4.4 Clock input divider**

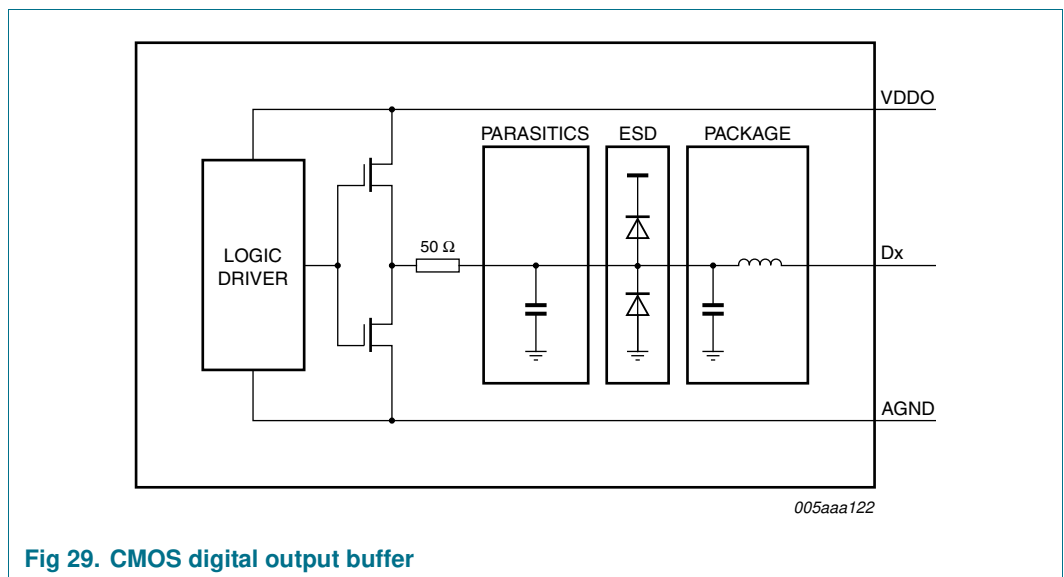
The ADC1610S contains an input clock divider that divides the incoming clock by a factor of 2 (when bit CLKDIV = logic 1; see [Table 21](#)). This feature allows the user to deliver a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

**11.5 Digital outputs**

**11.5.1 Digital output buffers: CMOS mode**

The digital output buffers can be configured as CMOS by setting bit LVDS\_CMOS to logic 0 (see [Table 23](#)).

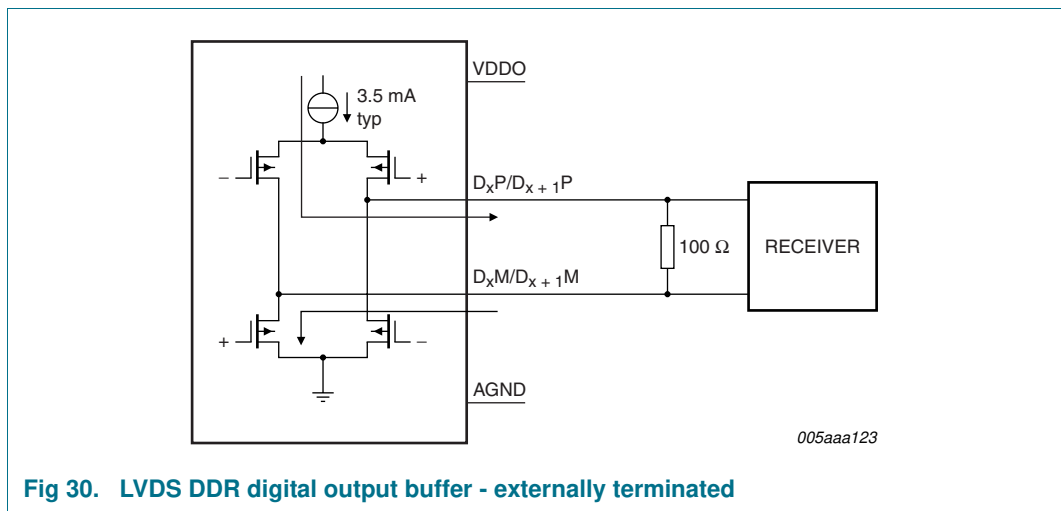
Each digital output has a dedicated output buffer. The equivalent circuit of the CMOS digital output buffer is shown in [Figure 30](#). The buffer is powered by a separate power supply, pins OGND and VDDO, to ensure 1.8 V to 3.3 V compatibility and is isolated from the ADC core. Each buffer can be loaded by a maximum of 10 pF.



The output resistance is 50 Ω and is the combination of an internal resistor and the equivalent output resistance of the buffer. There is no need for an external damping resistor. The drive strength of both data and DAV buffers can be programmed via the SPI in order to adjust the rise and fall times of the output digital signals (see [Table 30](#)):

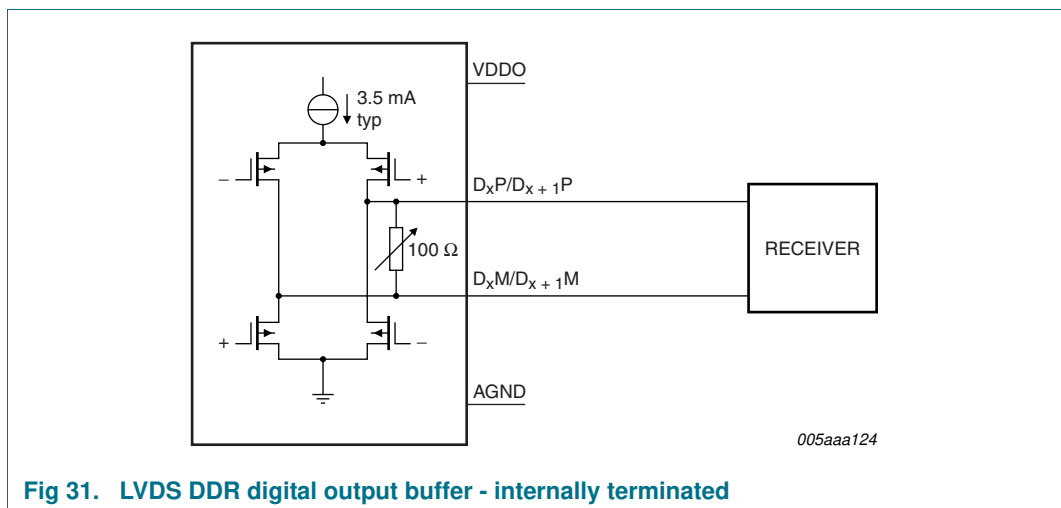
**11.5.2 Digital output buffers: LVDS DDR mode**

The digital output buffers can be configured as LVDS DDR by setting bit LVDS\_CMOS to logic 1 (see [Table 23](#)).



**Fig 30. LVDS DDR digital output buffer - externally terminated**

Each output should be terminated externally with a 100 Ω resistor (typical) at the receiver side ([Figure 31](#)) or internally via SPI control bits LVDS\_INT\_TER[2:0] (see [Figure 32](#) and [Table 32](#)).



**Fig 31. LVDS DDR digital output buffer - internally terminated**

The default LVDS DDR output buffer current is set to 3.5 mA. It can be programmed via the SPI (bits DAVI[1:0] and DATAI[1:0]; see [Table 31](#)) in order to adjust the output logic voltage levels.