Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ADC1613D series

Dual 16-bit ADC; 65 Msps, 80 Msps, 105 Msps or 125 Msps; serial JESD204A interface

Rev. 04 — 2 July 2012 Product data sheet

1. General description

The ADC1613D is a dual-channel 16-bit Analog-to-Digital Converter (ADC) optimized for high dynamic performance and low power at sample rates up to 125 Msps. Pipelined architecture and output error correction ensure the ADC1613D is accurate enough to guarantee zero missing codes over the entire operating range. Supplied from a 3.3 V source for analog and a 1.8 V source for the output driver, it embeds two serial outputs. Each lane is differential and complies with the JESD204A standard. An integrated Serial Peripheral Interface (SPI) allows the user to easily configure the ADC. A set of IC configurations is also available via the binary level control pins taken, which are used at power-up. The device also includes a programmable full-scale SPI to allow a flexible input voltage range of 1 V to 2 V (peak-to-peak).

Excellent dynamic performance is maintained from the baseband to input frequencies of 170 MHz or more, making the ADC1613D ideal for use in communications, imaging, and medical applications.

2. Features and benefits

- SNR, 72.5 dBFS; SFDR, 88 dBc
- Sample rate up to 125 Msps
- Clock input divided by 2 for less jitter contribution
- 3 V, 1.8 V single supplies
- Flexible input voltage range: 1 V (p-p) to 2 V (p-p)
- Two configurable serial outputs
- Compliant with JESD204A serial transmission standard
- Pin compatible with the ADC1413D series, the ADC1213D series and the ADC1113D125
- Input bandwidth, 600 MHz
- Power dissipation, 995 mW at 80 Msps
- SPI register programming
- Duty Cycle Stabilizer (DCS)
- High IF capability
- Offset binary, two’s complement, gray code
- Power-down mode and Sleep mode
- HVQFN56 package

3. Applications

- Wireless and wired broadband communications
- Spectral analysis
- Ultrasound equipment
- Portable instrumentation
- Imaging systems
- Software defined radio

4. Ordering information

Table 1. Ordering information

Type number	Sampling frequency (Msps)	Package		
		Name	Description	Version
ADC1613D125HN-C1	125	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm	SOT684-7
ADC1613D105HN-C1	105	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm	SOT684-7
ADC1613D080HN-C1	80	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm	SOT684-7
ADC1613D065HN-C1	65	HVQFN56	plastic thermal enhanced very thin quad flat package; no leads; 56 terminals; body 8 × 8 × 0.85 mm	SOT684-7

5. Block diagram

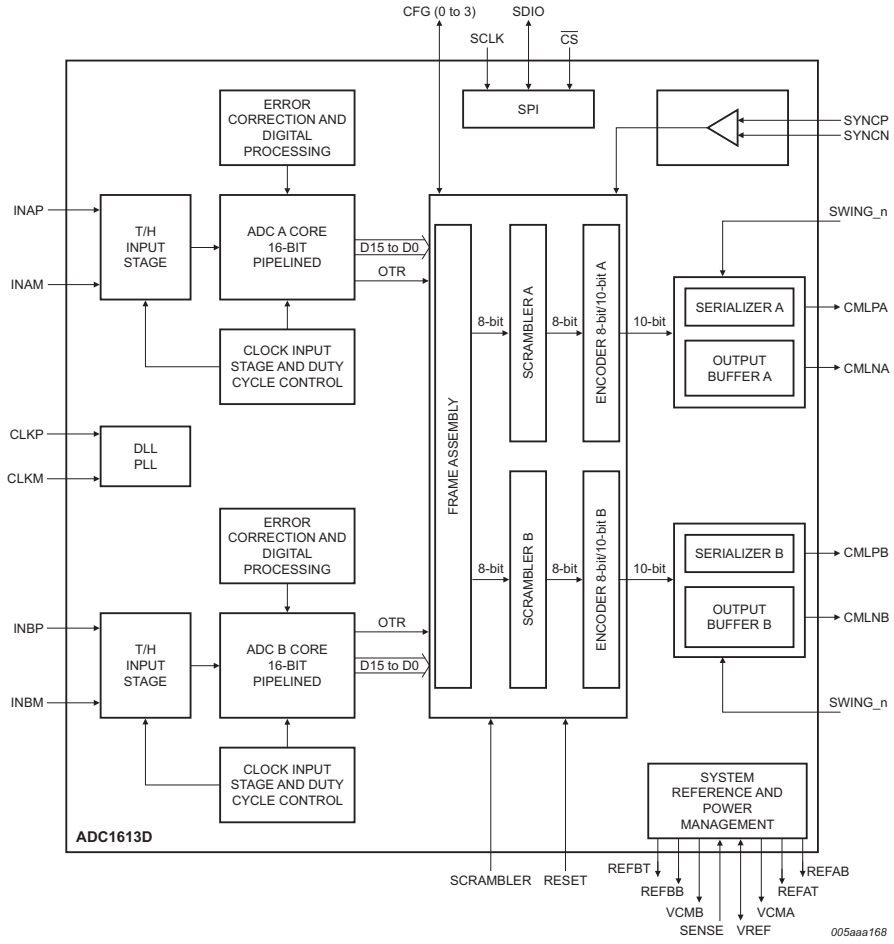


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

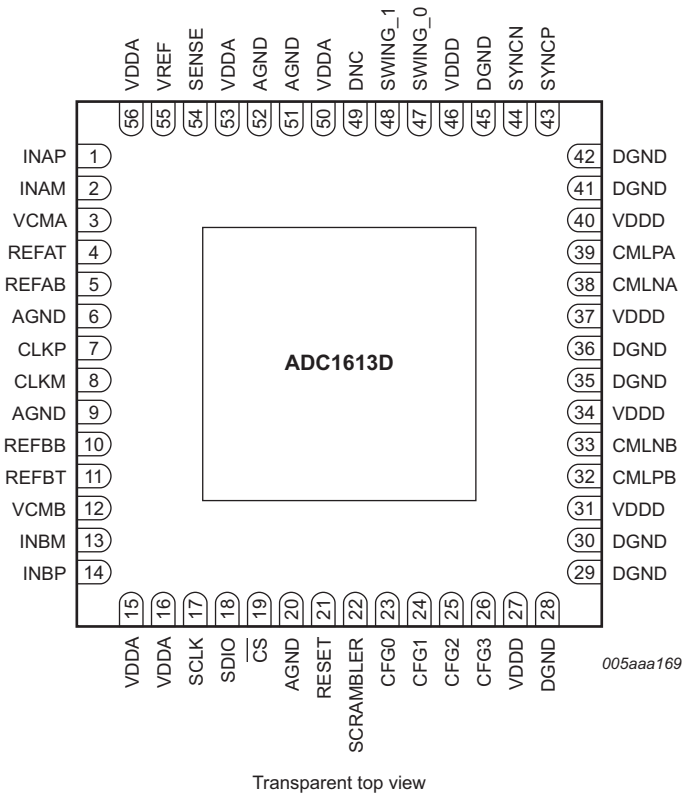


Fig 2. Pinning diagram

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Type [1]	Description
INAP	1	I	channel A analog input
INAM	2	I	channel A complementary analog input
VCMA	3	O	channel A output common voltage
REFAT	4	O	channel A top reference
REFAB	5	O	channel A bottom reference
AGND	6	G	analog ground
CLKP	7	I	clock input
CLKM	8	I	complementary clock input
AGND	9	G	analog ground
REFBB	10	O	channel B bottom reference
REFBT	11	O	channel B top reference
VCMB	12	O	channel B output common voltage
INBM	13	I	channel B complementary analog input

Table 2. Pin description *...continued*

Symbol	Pin	Type [1]	Description
INBP	14	I	channel B analog input
VDDA	15	P	analog power supply 3 V
VDDA	16	P	analog power supply 3 V
SCLK	17	I	SPI clock
SDIO	18	I/O	SPI data IO
$\overline{CS}$	19	I	chip select
AGND	20	G	analog ground
RESET	21	I	JEDEC digital IP reset
SCRAMBLER	22	I	scrambler enable and disable
CFG0	23	I/O	Table 30 (input) or OTRA (output)[2]
CFG1	24	I/O	Table 30 (input) or OTRB (output)[2]
CFG2	25	I/O	Table 30 (input)
CFG3	26	I/O	Table 30 (input)
VDDD	27	P	digital power supply 1.8 V
DGND	28	G	digital ground
DGND	29	G	digital ground
DGND	30	G	digital ground
VDDD	31	P	digital power supply 1.8 V
CMLPB	32	O	channel B output
CMLNB	33	O	channel B complementary output
VDDD	34	P	digital power supply 1.8 V
DGND	35	G	digital ground
DGND	36	G	digital ground
VDDD	37	P	digital power supply 1.8 V
CMLNA	38	O	channel A complementary output
CMLPA	39	O	channel A output
VDDD	40	P	digital power supply 1.8 V
DGND	41	G	digital ground
DGND	42	G	digital ground
SYNCP	43	I	synchronization from FPGA
SYNCN	44	I	synchronization from FPGA
DGND	45	G	digital ground
VDDD	46	P	digital power supply 1.8 V
SWING_0	47	I	JESD204 serial buffer programmable output swing
SWING_1	48	I	JESD204 serial buffer programmable output swing
DNC	49	O	do not connect
VDDA	50	P	analog power supply 3 V
AGND	51	G	analog ground
AGND	52	G	analog ground

Table 2. Pin description *...continued*

Symbol	Pin	Type [1]	Description
VDDA	53	P	analog power supply 3 V
SENSE	54	I	reference programming pin
VREF	55	I/O	voltage reference input/output
VDDA	56	P	analog power supply 3 V

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

[2] OTRA stands for “OuT of Range” A. OTRB stands for “OuT of Range” B.

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DDA}	analog supply voltage		−0.4	+4.6	V
V_{DDD}	digital supply voltage		−0.4	+2.5	V
T_{stg}	storage temperature		−55	+125	°C
T_{amb}	ambient temperature		−40	+85	°C
T_j	junction temperature		-	125	°C

8. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1]	17.8	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[1]	6.8	K/W

[1] Value for six layers board in still air with a minimum of 25 thermal vias.

9. Static characteristics

Table 5. Static characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DDA}	analog supply voltage		2.85	3.0	3.4	V
V_{DDD}	digital supply voltage		1.65	1.8	1.95	V
I_{DDA}	analog supply current	f_{clk} = 125 Msps; f_i = 70 MHz	-	343	-	mA
I_{DDD}	digital supply current	f_{clk} = 125 Msps; f_i = 70 MHz	-	150	-	mA
P_{tot}	total power dissipation	f_{clk} = 125 Msps	-	1270	-	mW
		f_{clk} = 105 Msps	-	1150	-	mW
		f_{clk} = 80 Msps	-	995	-	mW
		f_{clk} = 65 Msps	-	885	-	mW
P	power dissipation	Power-down mode	-	30	-	mW
		Standby mode	-	200	-	mW
Clock inputs: pins CLKP and CLKM, AC coupled						
Low-Voltage Positive Emitter-Coupled Logic (LVPECL)						
$V_{i(clk)dif}$	differential clock input voltage	peak-to-peak	-	1.6	-	V
SINE						
$V_{i(clk)dif}$	differential clock input voltage	peak	-	±3.0	-	V
Low Voltage Complementary Metal Oxide Semiconductor (LVCMOS)						
V_{IL}	LOW-level input voltage		-	-	$0.3V_{DDA}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDA}$	-	-	V
Logic inputs, Power-down: pins CFG0 to CFG3, SCRAMBLER, SWING_0, SWING_1, and RESET						
V_{IL}	LOW-level input voltage		-	0	-	V
V_{IH}	HIGH-level input voltage		-	$0.66V_{DDD}$	-	V
I_{IL}	LOW-level input current		−6	-	+6	μA
I_{IH}	HIGH-level input current		−30	-	+30	μA
SPI: pins $\overline{CS}$, SDIO, and SCLK						
V_{IL}	LOW-level input voltage		0	-	$0.3V_{DDA}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDA}$	-	V_{DDA}	V
I_{IL}	LOW-level input current		−10	-	+10	μA
I_{IH}	HIGH-level input current		−50	-	+50	μA
C_I	input capacitance		-	4	-	pF

Table 5. Static characteristics[1] *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Analog inputs: pins INAP, INAM, INBP, and INBM						
I_I	input current	track mode	−5	-	+5	μA
R_I	input resistance	track mode	-	15	-	Ω
C_I	input capacitance	track mode	-	5	-	pF
$V_{I(cm)}$	common-mode input voltage	track mode	0.9	1.5	2	V
B_i	input bandwidth		-	600	-	MHz
$V_{I(dif)}$	differential input voltage	peak-to-peak	1	-	2	V
Voltage controlled regulator output: pins VCMA and VCMB						
$V_{O(cm)}$	common-mode output voltage		-	V_{DDA} / 2	-	V
$I_{O(cm)}$	common-mode output current		-	4	-	mA
Reference voltage input/output: pin VREF						
V_{VREF}	voltage on pin VREF	output	0.5	-	1	V
		input	0.5	-	1	V
Reference mode selection: pin SENSE						
V_{SENSE}	voltage on pin SENSE		-	pin AGND; V_{VREF}; V_{DDA}	-	V
Data outputs: pins CMLPA, CMLNA						
Output levels, V_{DDD} = 1.8 V; SWING_SEL[2:0] = 000						
V_{OL}	LOW-level output voltage	DC coupled; output	-	1.5	-	V
		AC coupled	-	1.35	-	V
V_{OH}	HIGH-level output voltage	DC coupled; output	-	1.8	-	V
		AC coupled	-	1.65	-	V
Output levels, V_{DDD} = 1.8 V; SWING_SEL[2:0] = 001						
V_{OL}	LOW-level output voltage	DC coupled; output	-	1.45	-	V
		AC coupled	-	1.275	-	V
V_{OH}	HIGH-level output voltage	DC coupled; output	-	1.8	-	V
		AC coupled	-	1.625	-	V
Output levels, V_{DDD} = 1.8 V; SWING_SEL[2:0] = 010						
V_{OL}	LOW-level output voltage	DC coupled; output	-	1.4	-	V
		AC coupled	-	1.2	-	V
V_{OH}	HIGH-level output voltage	DC coupled; output	-	1.8	-	V
		AC coupled	-	1.6	-	V
Output levels, V_{DDD} = 1.8 V; SWING_SEL[2:0] = 011						
V_{OL}	LOW-level output voltage	DC coupled; output	-	1.35	-	V
		AC coupled	-	1.125	-	V
V_{OH}	HIGH-level output voltage	DC coupled; output	-	1.8	-	V
		AC coupled	-	1.575	-	V

Table 5. Static characteristics[1] *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Output levels, V_{DDD} = 1.8 V; SWING_SEL[2:0] = 100						
V_{OL}	LOW-level output voltage	DC coupled; output	-	1.3	-	V
		AC coupled	-	1.05	-	V
V_{OH}	HIGH-level output voltage	DC coupled; output	-	1.8	-	V
		AC coupled	-	1.55	-	V
Serial configuration: pins SYNCCP, SYNCCN						
V_{IL}	LOW-level input voltage	differential; input	-	0.95	-	V
V_{IH}	HIGH-level input voltage	differential; input	-	1.47	-	V
Accuracy						
INL	integral non-linearity		-	±5	-	LSB
DNL	differential non-linearity	no missing codes guaranteed	–0.95	±0.5	+0.95	LSB
E_{offset}	offset error		-	±2	-	mV
E_G	gain error	full-scale	-	± 0.5	-	%
$M_{G(CTC)}$	channel-to-channel gain matching		-	1.1	-	%
Supply						
PSRR	power supply rejection ratio	200 mV (p-p) on pin VDDA; f_i = DC	-	–54	-	dB

[1] Typical values measured at V_{DDA} = 3 V, V_{DDD} = 1.8 V, T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = –40 °C to +85 °C at V_{DDA} = 3 V, V_{DDD} = 1.8 V; V_I (INAP, INBP) – V_I (INAM, INBM) = –1 dBFS; internal reference mode; 100 Ω differential applied to serial outputs; unless otherwise specified.

10. Dynamic characteristics

10.1 Dynamic characteristics

Table 6. Dynamic characteristics[1]

Symbol	Parameter	Conditions	ADC1613D065			ADC1613D080			ADC1613D105			ADC1613D125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Analog signal processing															
α_{2H}	second harmonic level	f_i = 3 MHz	-	89	-	-	89	-	-	88	-	-	90	-	dBc
		f_i = 30 MHz	-	88	-	-	88	-	-	88	-	-	89	-	dBc
		f_i = 70 MHz	-	87	-	-	87	-	-	86	-	-	87	-	dBc
		f_i = 170 MHz	-	84	-	-	84	-	-	83	-	-	85	-	dBc
α_{3H}	third harmonic level	f_i = 3 MHz	-	88	-	-	88	-	-	87	-	-	89	-	dBc
		f_i = 30 MHz	-	87	-	-	87	-	-	87	-	-	88	-	dBc
		f_i = 70 MHz	-	86	-	-	86	-	-	85	-	-	86	-	dBc
		f_i = 170 MHz	-	83	-	-	83	-	-	82	-	-	84	-	dBc
THD	total harmonic distortion	f_i = 3 MHz	-	85	-	-	85	-	-	84	-	-	86	-	dBc
		f_i = 30 MHz	-	84	-	-	84	-	-	84	-	-	85	-	dBc
		f_i = 70 MHz	-	83	-	-	83	-	-	82	-	-	83	-	dBc
		f_i = 170 MHz	-	80	-	-	80	-	-	79	-	-	81	-	dBc
ENOB	effective number of bits	f_i = 3 MHz	-	11.7	-	-	11.7	-	-	11.7	-	-	11.6	-	bits
		f_i = 30 MHz	-	11.6	-	-	11.6	-	-	11.6	-	-	11.6	-	bits
		f_i = 70 MHz	-	11.5	-	-	11.5	-	-	11.5	-	-	11.5	-	bits
		f_i = 170 MHz	-	11.4	-	-	11.4	-	-	11.4	-	-	11.4	-	bits
SNR	signal-to-noise ratio	f_i = 3 MHz	-	72.3	-	-	72.2	-	-	72.0	-	-	71.6	-	dBFS
		f_i = 30 MHz	-	71.5	-	-	71.4	-	-	71.4	-	-	71.3	-	dBFS
		f_i = 70 MHz	-	70.9	-	-	70.9	-	-	70.8	-	-	70.7	-	dBFS
		f_i = 170 MHz	-	70.4	-	-	70.3	-	-	70.2	-	-	70.1	-	dBFS
SFDR	spurious-free dynamic range	f_i = 3 MHz	-	88	-	-	88	-	-	87	-	-	89	-	dBc
		f_i = 30 MHz	-	87	-	-	87	-	-	87	-	-	88	-	dBc
		f_i = 70 MHz	-	86	-	-	86	-	-	85	-	-	86	-	dBc
		f_i = 170 MHz	-	83	-	-	83	-	-	82	-	-	84	-	dBc

Table 6. Dynamic characteristics[1] …continued

Symbol	Parameter	Conditions	ADC1613D065			ADC1613D080			ADC1613D105			ADC1613D125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
IMD	intermodulation distortion	f_i = 3 MHz	-	89	-	-	89	-	-	88	-	-	89	-	dBc
		f_i = 30 MHz	-	88	-	-	88	-	-	88	-	-	88	-	dBc
		f_i = 70 MHz	-	87	-	-	87	-	-	86	-	-	86	-	dBc
		f_i = 170 MHz	-	84	-	-	85	-	-	83	-	-	84	-	dBc
$\alpha_{ct(ch)}$	channel crosstalk	f_i = 70 MHz	-	100	-	-	100	-	-	100	-	-	100	-	dBc

[1] Typical values measured at V_{DDA} = 3 V, V_{DDD} = 1.8 V, T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDD} = 1.8 V; V_I (INAP, INBP) − V_I (INAM, INBM) = −1 dBFS; internal reference mode; 100 Ω differential applied to serial outputs; unless otherwise specified.

10.2 Clock and digital output timing

Table 7. Clock and digital output timing characteristics[1]

Symbol	Parameter	Conditions	ADC1613D065			ADC1613D080			ADC1613D105			ADC1613D125			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Clock timing input: pins CLKP and CLKM															
f_{clk}	clock frequency		40	-	65	60	-	80	75	-	105	100	-	125	Msps
$t_{lat(data)}$	data latency time		17	-	20	17	-	20	17	-	20	17	-	20	clock cycle
δ_{clk}	clock duty cycle	DCS_EN = 1: en	30	50	70	30	50	70	30	50	70	30	50	70	%
		DCS_EN = 0: dis	45	50	55	45	50	55	45	50	55	45	50	55	%
$t_{d(s)}$	sampling delay time		-	0.8	-	-	0.8	-	-	0.8	-	-	0.8	-	ns
t_{wake}	wake-up time		-	76	-	-	76	-	-	76	-	-	76	-	µs

[1] Typical values measured at V_{DDA} = 3 V, V_{DDD} = 1.8 V, T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDD} = 1.8 V; V_I (INAP, INBP) − V_I (INAM, INBM) = −1 dBFS; internal reference mode; 100 Ω differential applied to serial outputs; unless otherwise specified.

10.3 Serial output timing

The eye diagram of the serial output is shown in Figure 3 and Figure 4. Test conditions are:

- 3.125 Gbps data rate
- T_{amb} = 25 °C
- DC coupling with two different receiver common-mode voltages

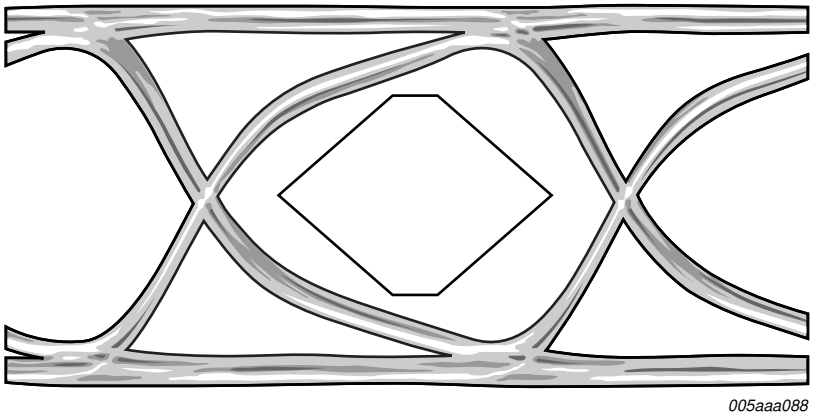


Fig 3. Eye diagram at 1 V receiver common-mode

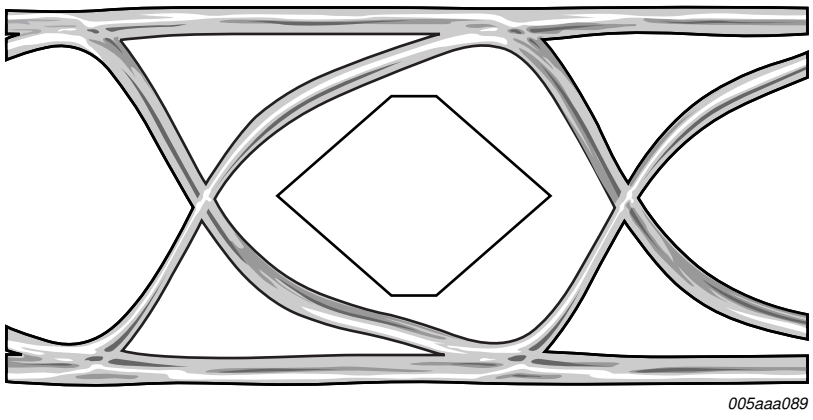


Fig 4. Eye diagram at 2 V receiver common-mode

10.4 SPI timing

Table 8. SPI timing characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(SCLK)}$	SCLK pulse width		-	40	-	ns
$t_{w(SCLKH)}$	SCLK HIGH pulse width		-	16	-	ns
$t_{w(SCLKL)}$	SCLK LOW pulse width		-	16	-	ns
t_{su}	set-up time	data to SCLK H	-	5	-	ns
		$\overline{CS}$ to SCLK H	-	5	-	ns
t_h	hold time	data to SCLK H	-	2	-	ns
		$\overline{CS}$ to SCLK H	-	2	-	ns
$f_{clk(max)}$	maximum clock frequency		-	25	-	MHz

[1] Typical values measured at V_{DDA} = 3 V, V_{DDD} = 1.8 V, T_{amb} = 25 °C. Minimum and maximum values are across the full temperature range T_{amb} = −40 °C to +85 °C at V_{DDA} = 3 V, V_{DDD} = 1.8 V; V_I (INAP, INBP) − V_I (INAM,INBM) = −1 dBFS; internal reference mode; 100 Ω differential applied to serial outputs; unless otherwise specified.

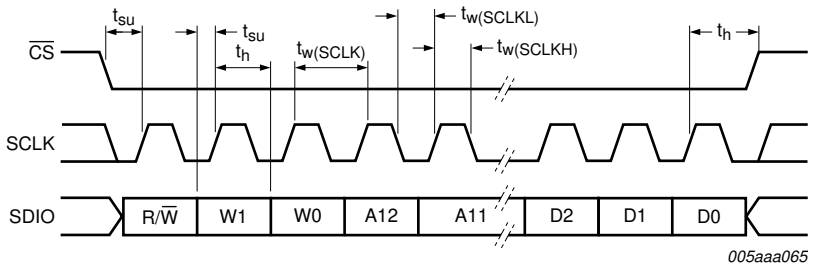


Fig 5. SPI timing

11. Application information

11.1 Analog inputs

11.1.1 Input stage description

The analog input of the ADC1613D supports a differential or a single-ended input drive. Optimal performance is achieved using differential inputs with the common-mode input voltage ($V_{I(cm)}$) on pins INP and INM set to $0.5V_{DDA}$.

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) via a programmable internal reference (see Section 11.2 and Table 21).

Figure 6 shows the equivalent circuit of the sample-and-hold input stage, including ElectroStatic Discharge (ESD) protection and circuit and package parasitics.

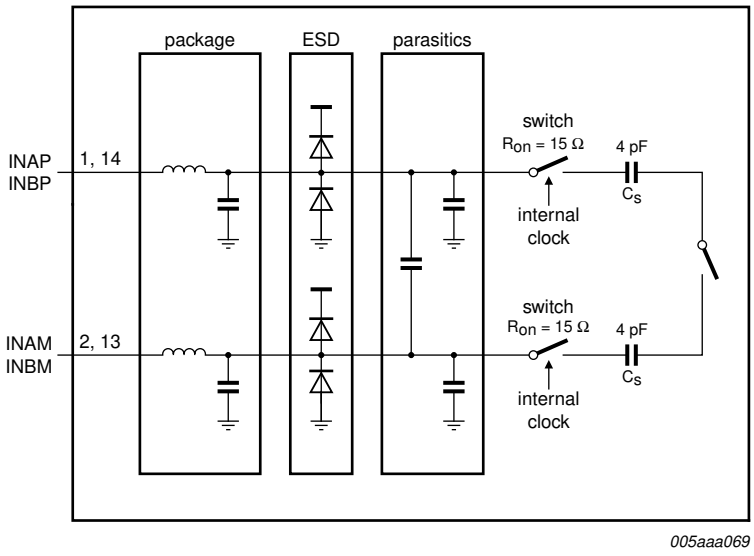


Fig 6. Input sampling circuit

The sample phase occurs when the internal clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the clock signal goes LOW, the stage enters the hold phase and the voltage information is transmitted to the ADC core.

11.1.2 Anti-kickback circuitry

Anti-kickback circuitry (Figure 7) is needed to counteract the effects of a charge injection generated by the sampling capacitance.

The RC filter is also used to filter noise from the signal before it reaches the sampling stage. The value of the capacitor should be chosen to maximize noise attenuation without degrading the settling time excessively.

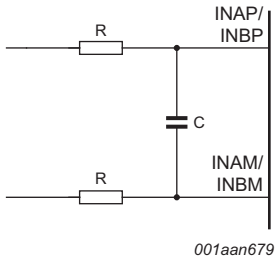


Fig 7. Anti-kickback circuit

The component values are determined by the input frequency and should be selected so as not to affect the input bandwidth.

Table 9. RC coupling versus input frequency - typical values

Input frequency (MHz)	Resistance (Ω)	Capacitance (pF)
3	25	12
70	12	8
170	12	8

11.1.3 Transformer

The configuration of the transformer circuit is determined by the input frequency. The configuration shown in Figure 8 would be suitable for a baseband application.

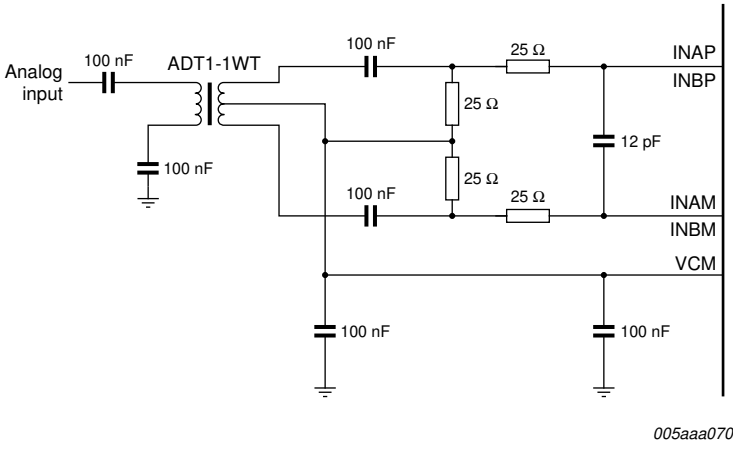


Fig 8. Single transformer configuration

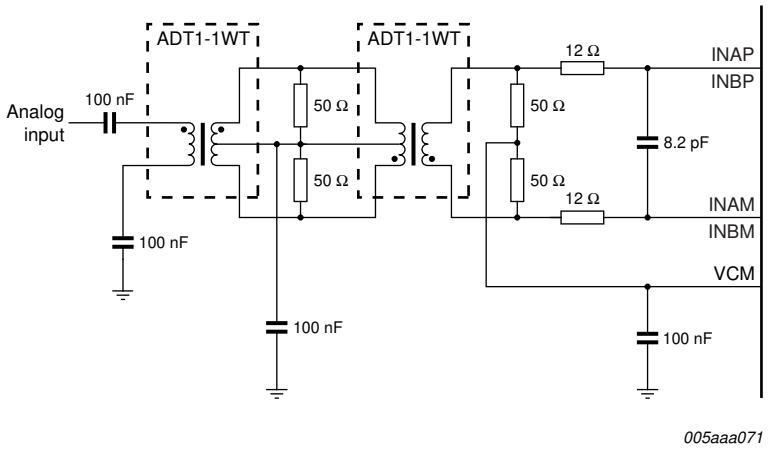


Fig 9. Dual transformer configuration

The configuration shown in Figure 9 is recommended for high frequency applications. In both cases, the choice of transformer is a compromise between cost and performance.

11.2 System reference and power management

11.2.1 Internal/external reference

The ADC1613D has a stable and accurate built-in internal reference voltage to adjust the ADC full-scale. This reference voltage can be set internally via SPI or with pins VREF and SENSE (see Figure 11 to Figure 14), in 1 dB steps between 0 dB and −6 dB, via SPI control bits INTREF[2:0] (when bit INTREF_EN = logic 1; see Table 21). The equivalent reference circuit is shown in Figure 10. An external reference is also possible by providing a voltage on pin VREF as described in Figure 13.

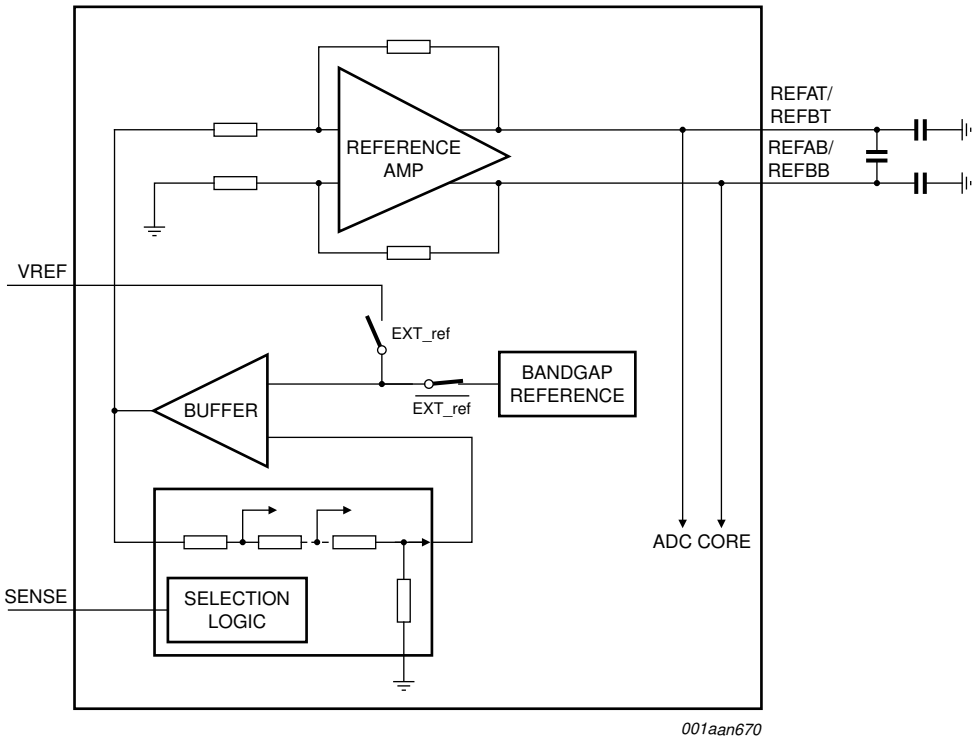


Fig 10. Reference equivalent schematic

If bit INTREF_EN is set to logic 0, the reference voltage is determined either internally or externally as detailed in Table 10.

Table 10. Reference modes

Mode	SPI bit, "Internal reference"	SENSE pin	VREF pin	Full-scale (V (p-p))
Internal (Figure 11)	0	GND	330 pF capacitor to GND	2
Internal (Figure 12)	0	VREF pin = SENSE pin and 330 pF capacitor to GND		1
External (Figure 13)	0	V_{DDA}	external voltage from 0.5 V to 1 V	1 to 2
Internal, SPI mode (Figure 14)	1	VREF pin = SENSE pin and 330 pF capacitor to GND		1 to 2

Figure 11 to Figure 14 illustrate how to connect the SENSE and VREF pins to select the required reference voltage source.

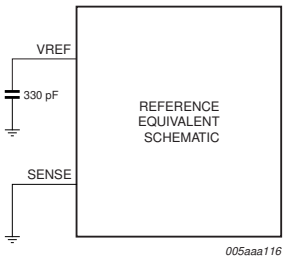


Fig 11. Internal reference, 2 V (p-p) full-scale

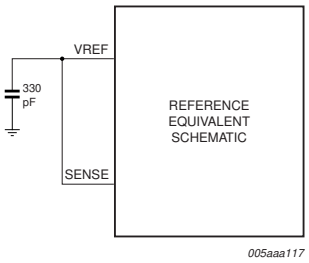


Fig 12. Internal reference, 1 V (p-p) full-scale

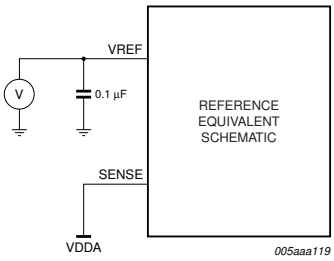


Fig 13. External reference, 1 V (p-p) to 2 V (p-p) full-scale

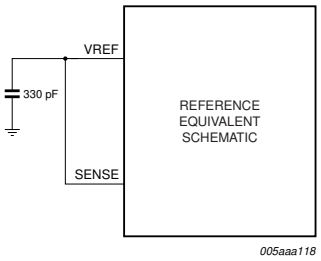


Fig 14. Internal reference via SPI, 1 V (p-p) to 2 V (p-p) full-scale

11.2.2 Programmable full-scale

The full-scale is programmable between 1 V (p-p) to 2 V (p-p) (see Table 11).

Table 11. Reference SPI gain control

INTREF[2:0]	Level (dB)	Full-scale (V (p-p))
000	0	2
001	−1	1.78
010	−2	1.59
011	−3	1.42
100	−4	1.26
101	−5	1.12
110	−6	1
111	not used	x

11.2.3 Common-mode output voltage ($V_{O(cm)}$)

An 0.1 μF filter capacitor should be connected between the pins VCMA and VCMB and ground to ensure a low-noise common-mode output voltage. When AC-coupled, these pins can be used to set the common-mode reference for the analog inputs, for instance via a transformer middle point.

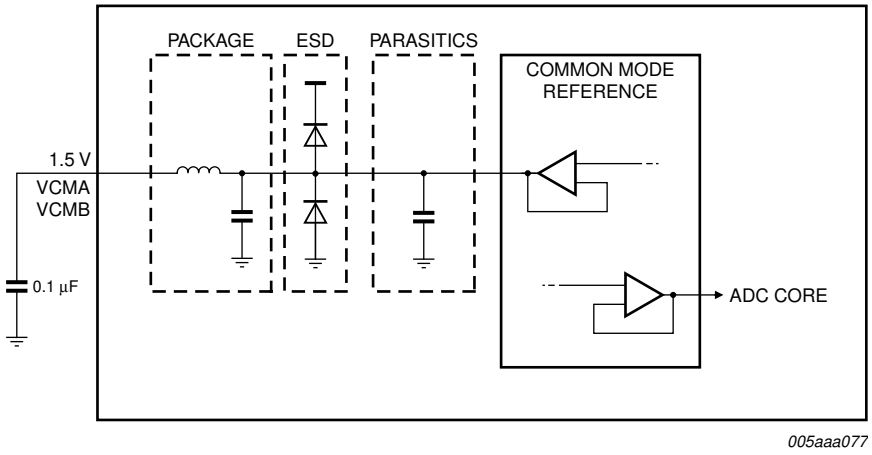


Fig 15. Reference equivalent schematic

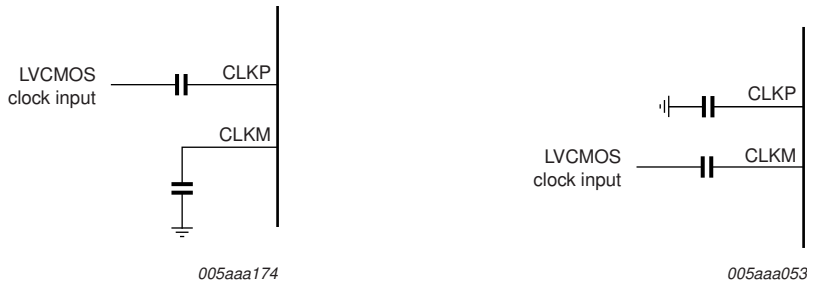
11.2.4 Biasing

The common-mode input voltage, $V_{I(cm)}$, at the inputs to the sample-and-hold stage (pins INAM, INBM, INAP, and INBP) must be between 0.9 V and 2 V for optimal performance.

11.3 Clock input

11.3.1 Drive modes

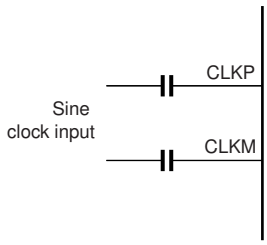
The ADC1613D can be driven differentially (LVPECL). It can also be driven by a single-ended LVCMOS signal connected to pin CLKP (pin CLKM should be connected to ground via a capacitor) or pin CLKM (pin CLKP should be connected to ground via a capacitor).



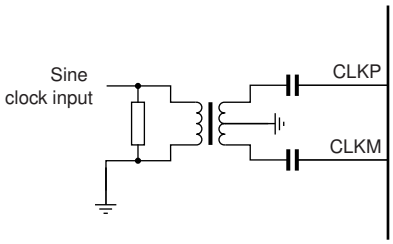
a. Rising edge LVCMOS

b. Falling edge LVCMOS

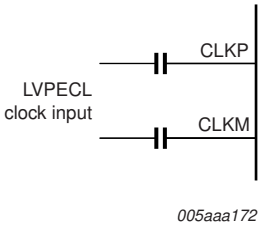
Fig 16. LVCMOS single-ended clock input



a. Sine clock input



b. Sine clock input (with transformer)

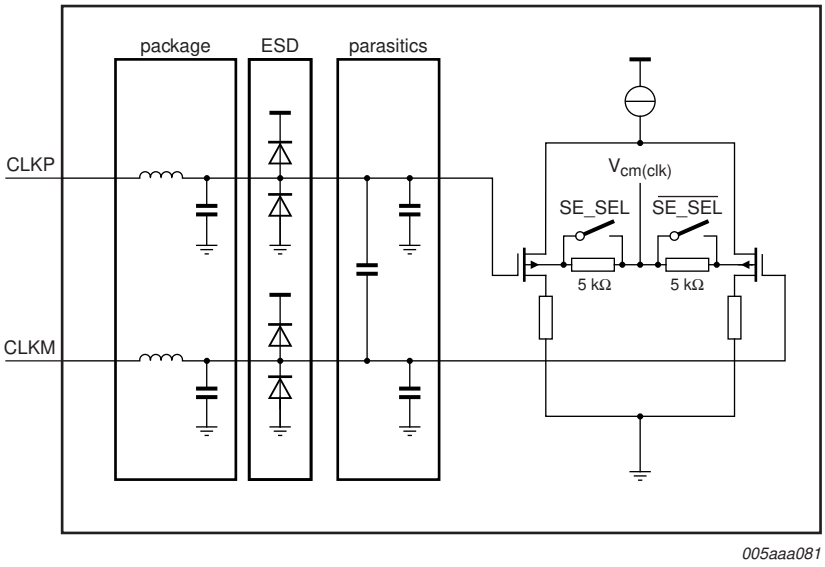


c. LVPECL clock input

Fig 17. Differential clock input

11.3.2 Equivalent input circuit

The equivalent circuit of the input clock buffer is shown in Figure 18. The common-mode voltage of the differential input stage is set via 5 kΩ internal resistors.



$V_{cm(clk)}$ = common-mode voltage of the differential input stage.

Fig 18. Equivalent input circuit

Single-ended or differential clock inputs can be selected via the SPI (see Table 20). If single-ended is selected, the input pin (CLKM or CLKP) is selected via control bit SE_SEL.

If single-ended is implemented without setting bit SE_SEL accordingly, the unused pin should be connected to ground via a capacitor.

11.3.3 Clock input divider

The ADC1613D contains an input clock divider that divides the incoming clock by a factor of 2 (when bit CLKDIV2_SEL = logic 1; see Table 20). This feature allows the user to deliver a higher clock frequency with better jitter performance, leading to a better SNR result once acquisition has been performed.

11.3.4 Duty cycle stabilizer

The duty cycle stabilizer can improve the overall performances of the ADC by compensating the input clock signal duty cycle. When the duty cycle stabilizer is active (bit DCS_EN = logic 1; see Table 20), the circuit can handle signals with duty cycles of between 30 % and 70 % (typical). When the duty cycle stabilizer is disabled (DCS_EN = logic 0), the input clock signal should have a duty cycle of between 45 % and 55 %.

Table 12. Duty cycle stabilizer

Bit DCS_EN	Description
0	duty cycle stabilizer disable
1	duty cycle stabilizer enable

11.4 Digital outputs

11.4.1 Serial output equivalent circuit

The JESD204A standard specifies that if the receiver and the transmitter are DC-coupled, both must be fed from the same supply.

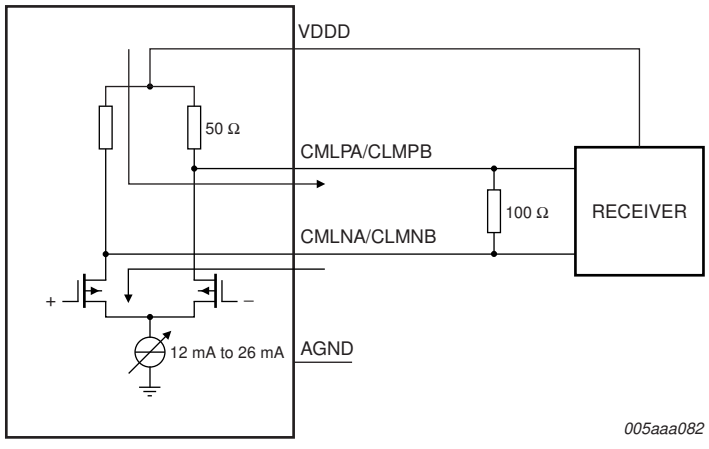


Fig 19. CML output connection to the receiver (DC-coupled)

The output should be terminated when 100 Ω (typical) is reached at the receiver side.

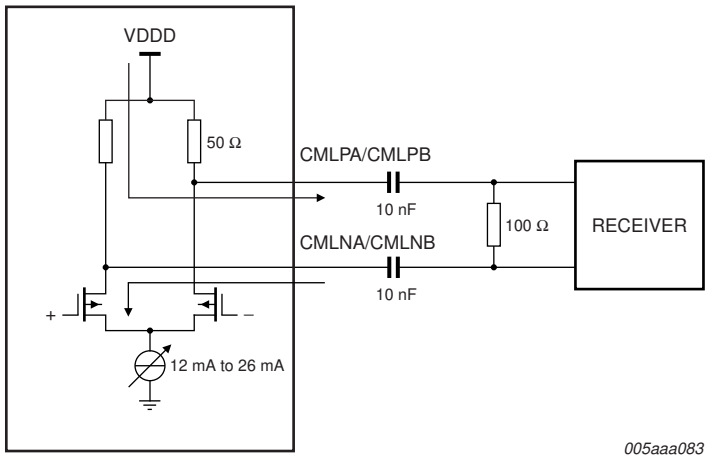


Fig 20. CML output connection to the receiver (AC-coupled)

11.5 JESD204A serializer

For more information about the JESD204A standard refer to the JEDEC web site.

11.5.1 Digital JESD204A formatter

The block placed after the ADC cores is used to implement all functionalities of the JESD204A standard. This ensures signal integrity and guarantees the clock and the data recovery at the receiver side.

The block is highly parameterized and can be configured in various ways depending on the sampling frequency and the number of lanes used.

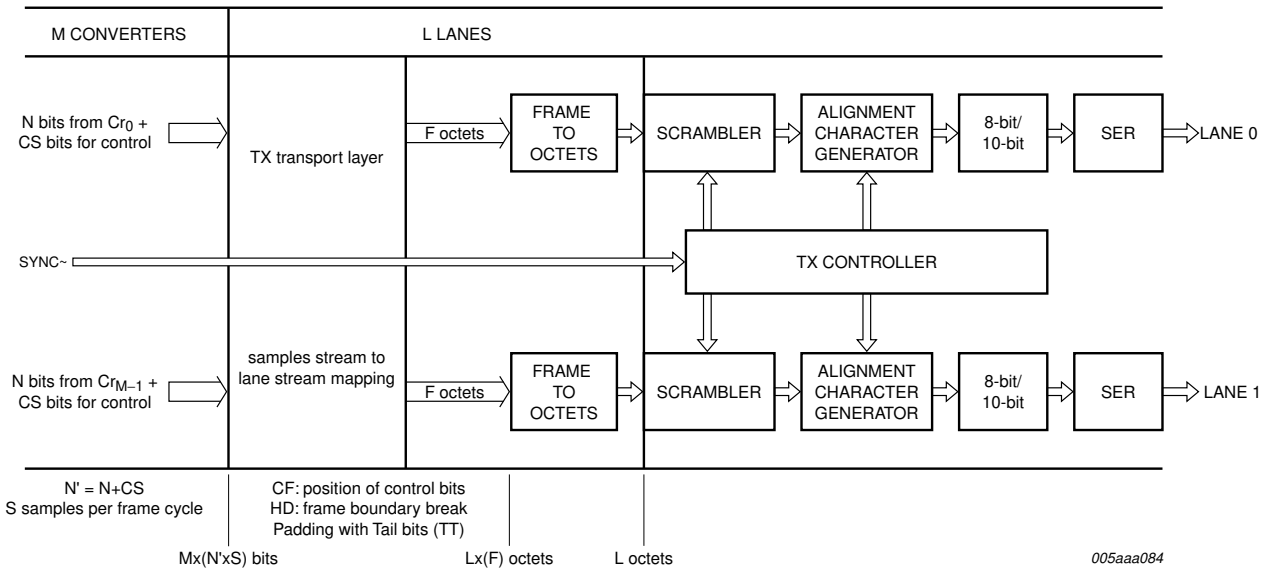


Fig 21. General overview of the JESD204A serializer

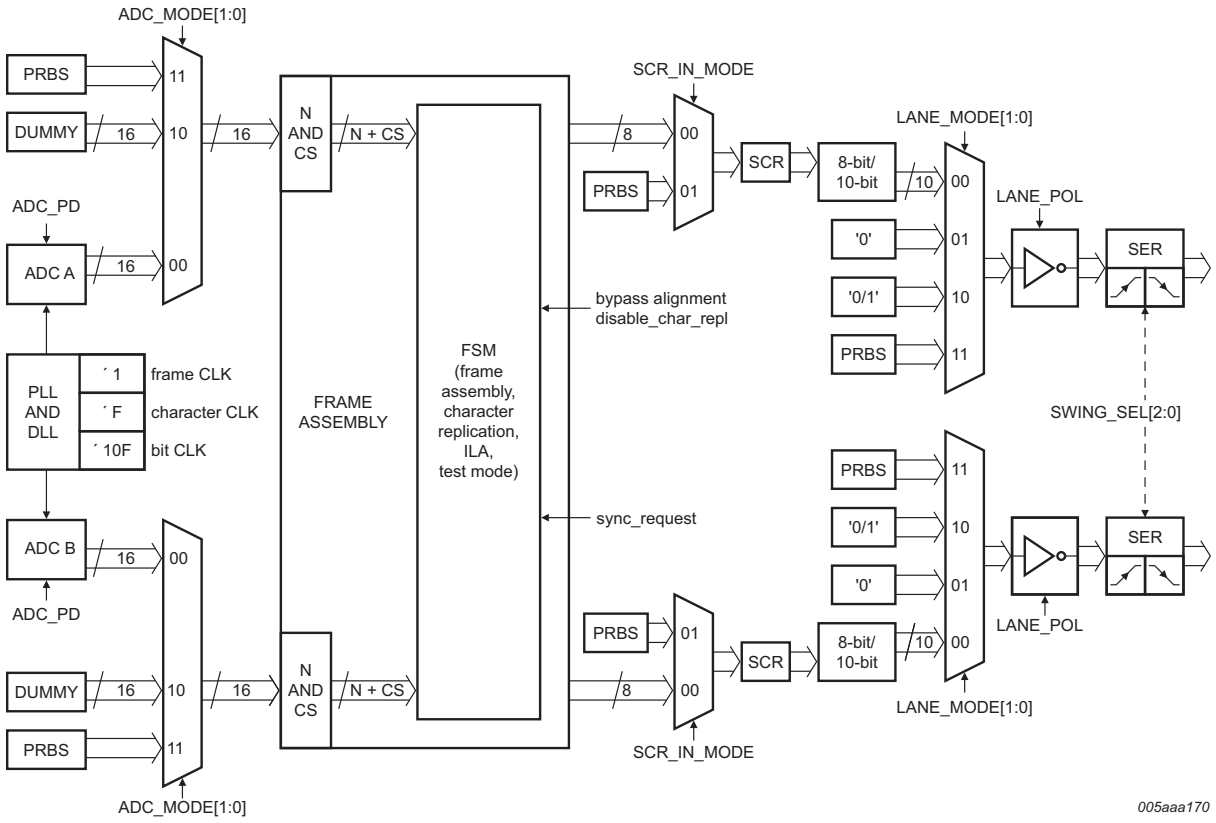


Fig 22. Detailed view of the JESD204A serializer with debug functionality

11.5.2 ADC core output codes versus input voltage

Table 13 shows the data output codes for a given analog input voltage.

Table 13. Output codes versus input voltage

INP − INM (V)	Offset binary	Two's complement	OTR
< −1	0000 0000 0000 0000	1000 0000 0000 0000	1
−1	0000 0000 0000 0000	1000 0000 0000 0000	0
−0.99996948	0000 0000 0000 0001	1000 0000 0000 0001	0
−0.99993896	0000 0000 0000 0010	1000 0000 0000 0010	0
−0.99990845	0000 0000 0000 0011	1000 0000 0000 0011	0
−0.99987793	0000 0000 0000 0100	1000 0000 0000 0100	0
....	....	....	0
−0.00006104	0111 1111 1111 1110	1111 1111 1111 1110	0
−0.00003052	0111 1111 1111 1111	1111 1111 1111 1111	0
0	1000 0000 0000 0000	0000 0000 0000 0000	0
+0.00003052	1000 0000 0000 0001	0000 0000 0000 0001	0
+0.00006104	1000 0000 0000 0010	0000 0000 0000 0010	0
....	....	....	0
+0.99987793	1111 1111 1111 1011	0111 1111 1111 1011	0

Table 13. Output codes versus input voltage *...continued*

INP − INM (V)	Offset binary	Two's complement	OTR
+0.99990845	1111 1111 1111 1100	0111 1111 1111 1100	0
+0.99993896	1111 1111 1111 1101	0111 1111 1111 1101	0
+0.99996948	1111 1111 1111 1110	0111 1111 1111 1110	0
+1	1111 1111 1111 1111	0111 1111 1111 1111	0
> +1	1111 1111 1111 1111	0111 1111 1111 1111	1

11.6 Serial Peripheral Interface (SPI)

11.6.1 Register description

The ADC1613D serial interface is a synchronous serial communications port allowing for easy interfacing with many industry microprocessors. It provides access to the registers that control the operation of the chip in both read and write modes.

This interface is configured as a 3-wire type (SDIO as bidirectional pin).

Pin SCLK acts as the serial clock, and pin $\overline{CS}$ acts as the serial chip select.

Each read/write operation is sequenced by the $\overline{CS}$ signal and enabled by a LOW level to to drive the chip with 2 bytes to 5 bytes, depending on the content of the instruction byte (see Table 14).

Table 14. SPI instruction bytes

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/W[1]	W1	W0	A12	A11	A10	A9	A8
	A7	A6	A5	A4	A3	A2	A1	A0

[1] R/W indicates whether a read (logic 1) or write (logic 0) transfer occurs after the instruction byte

Table 15. Read or Write mode access description

R/W[1]	Description
0	Write mode operation
1	Read mode operation

[1] Bits W1 and W0 indicate the number of bytes transferred after the instruction byte.

Table 16. Number of bytes to be transferred

W1	W0	Number of bytes transferred
0	0	1 byte
0	1	2 bytes
1	0	3 bytes
1	1	4 or more bytes

Bits A12 to A0 indicate the address of the register being accessed. In the case of a multiple byte transfer, this address is the first register to be accessed. An address counter is incremented to access subsequent addresses.

The steps for a data transfer:

1. A falling edge on pin $\overline{CS}$ in combination with a rising edge on pin SCLK determine the start of communications.
2. The first phase is the transfer of the 2-byte instruction.
3. The second phase is the transfer of the data which can vary in length but always a multiple of 8 bits. The MSB is always sent first (for instruction and data bytes)
4. A rising edge on pin $\overline{CS}$ indicates the end of data transmission.

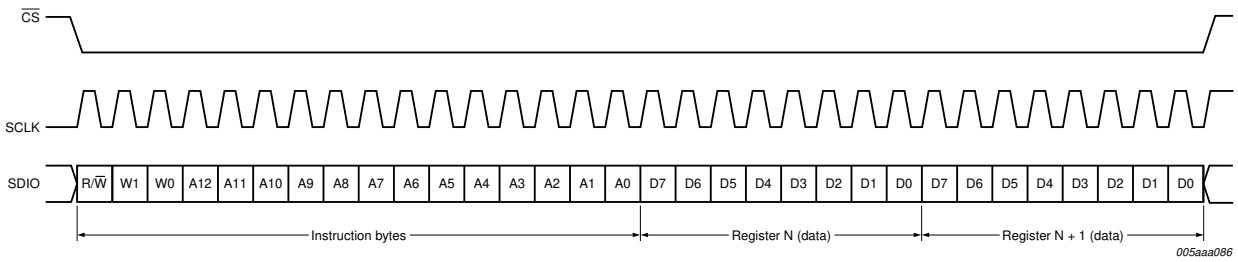


Fig 23. Transfer diagram for two data bytes (3-wire type)

11.6.2 Channel control

The two ADC channels can be configured at the same time or separately. By using the register “Channel index”, the user can choose which ADC channel receives the next SPI-instruction. By default the channel A and B receives the same instructions in write mode. In read mode only A is active.