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## FEATURES

**Fully specified rail to rail at  $V_{CC1} = 2.5\text{ V}$  to  $5.5\text{ V}$**   
**Input common-mode voltage from  $-0.2\text{ V}$  to  $V_{CC1} + 0.2\text{ V}$**   
**CML-compatible output stage**  
**1.25 ns propagation delay**  
**50 mW at 2.5 V power supply**  
**Shutdown pin**  
**Single-pin control for programmable hysteresis and latch**  
 (ADCMP607 only)  
**Power supply rejection > 60 dB**  
 **$-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  operation**

## APPLICATIONS

**High speed instrumentation**  
**Clock and data signal restoration**  
**Logic level shifting or translation**  
**Pulse spectroscopy**  
**High speed line receivers**  
**Threshold detection**  
**Peak and zero-crossing detectors**  
**High speed trigger circuitry**  
**Pulse-width modulators**  
**Current-/voltage-controlled oscillators**  
**Automatic test equipment (ATE)**

## GENERAL DESCRIPTION

The ADCMP606 and ADCMP607 are very fast comparators fabricated on XFCB2, an Analog Devices, Inc., proprietary process. These comparators are exceptionally versatile and easy to use. Features include an input range from  $V_{EE} - 0.5\text{ V}$  to  $V_{CC1} + 0.2\text{ V}$ , low noise, CML-compatible output drivers, and TTL-/CMOS-compatible latch inputs with adjustable hysteresis and/or shutdown inputs.

The devices offer 1.25 ns propagation delay with 2.5 ps rms random jitter (RJ). Overdrive and slew rate dispersion are typically less than 50 ps.

A flexible power supply scheme allows the devices to operate with a single +2.5 V positive supply and a  $-0.5\text{ V}$  to  $+2.7\text{ V}$  input signal range up to a +5.5 V positive supply with a  $-0.5\text{ V}$  to  $+5.7\text{ V}$  input signal range. The ADCMP607 features split input/output supplies with no sequencing restrictions to support a wide input signal range with independent output swing control and power savings.

The CML-compatible output stage is fully back-matched for superior performance. The comparator input stage offers robust protection against large input overdrive, and the outputs do not phase reverse when the valid input signal range is exceeded. On the ADCMP607, latch and programmable hysteresis features are also provided with a unique single-pin control option.

The ADCMP606 is available in a 6-lead SC70 package and the ADCMP607 is available in a 12-lead LFCSP package.

## FUNCTIONAL BLOCK DIAGRAM

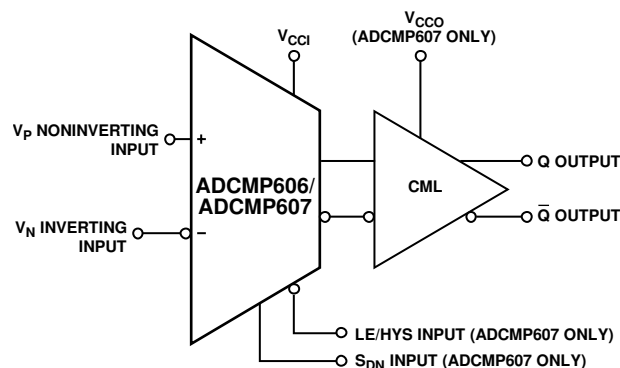


Figure 1.

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**REVISION HISTORY**

**4/16—Rev. B to Rev. C**

Changes to Figure 4 and Table 6 .....	7
Updated Outline Dimensions .....	14
Changes to Ordering Guide .....	14

**11/14—Rev. A to Rev. B**

Changes to Figure 4 and Table 6 .....	7
Changes to Figure 12 and Figure 13 .....	9
Changes to Comparator Hysteresis Section .....	11
Updated Outline Dimensions .....	14
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**8/07—Rev. 0 to Rev. A**

Changes to Specifications Section .....	3
Changes to Table 3 .....	6
Changes to Ordering Guide .....	14

**10/06—Revision 0: Initial Version**

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC0} = 2.5\text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ , typical at  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>DC INPUT CHARACTERISTICS</b>						
Voltage Range	$V_P, V_N$	$V_{CC1} = 2.5\text{ V to } 5.5\text{ V}$	-0.5		$V_{CC1} + 0.2$	V
Common-Mode Range		$V_{CC1} = 2.5\text{ V to } 5.5\text{ V}$	-0.2		$V_{CC1} + 0.2$	V
Differential Voltage		$V_{CC1} = 2.5\text{ V to } 5.5\text{ V}$			$V_{CC1}$	V
Offset Voltage	$V_{OS}$		-5.0		+5.0	mV
Bias Current	$I_P, I_N$		-5.0	$\pm 2$	+5.0	$\mu\text{A}$
Offset Current			-2.0		2.0	$\mu\text{A}$
Capacitance	$C_P, C_N$			1		pF
Resistance, Differential Mode		-0.1 V to $V_{CC1}$	200	700		k $\Omega$
Resistance, Common Mode		-0.5 V to $V_{CC1} + 0.5\text{ V}$	100	350		k $\Omega$
Active Gain	$A_V$			85		dB
Common-Mode Rejection Ratio	CMRR	$V_{CC1} = 2.5\text{ V}, V_{CC0} = 2.5\text{ V},$ $V_{CM} = -0.2\text{ V to } +2.7\text{ V}$	50			dB
		$V_{CC1} = 2.5\text{ V}, V_{CC0} = 5.5\text{ V}$	50			dB
Hysteresis		$R_{HYS} = \infty$		<0.1		mV
<b>LATCH ENABLE PIN CHARACTERISTICS (ADCMP607 Only)</b>						
$V_{IH}$		Hysteresis is shut off	2.0		$V_{CC0}$	V
$V_{IL}$		Latch mode guaranteed	-0.2	+0.4	+0.8	V
$I_{IH}$		$V_{IH} = V_{CC0}$	-6		+6	$\mu\text{A}$
$I_{IL}$		$V_{IL} = 0.4\text{ V}$	-0.1		+0.1	mA
<b>HYSTERESIS MODE AND TIMING</b>						
Hysteresis Mode Bias Voltage		Current sink 0 $\mu\text{A}$	1.145	1.25	1.35	V
Minimum Resistor Value		Hysteresis = 120 mV	55	75	110	k $\Omega$
Latch Setup Time	$t_S$	$V_{OD} = 50\text{ mV}$		-1.5		ns
Latch Hold Time	$t_H$	$V_{OD} = 50\text{ mV}$		2.3		ns
Latch-to-Output Delay	$t_{PLOH}, t_{PLOL}$	$V_{OD} = 50\text{ mV}$		30		ns
Latch Minimum Pulse Width	$t_{PL}$	$V_{OD} = 50\text{ mV}$		25		ns
<b>SHUTDOWN PIN CHARACTERISTICS (ADCMP607 Only)</b>						
$V_{IH}$		Comparator is operating	2.0		$V_{CC0}$	V
$V_{IL}$		Shutdown guaranteed	-0.2	+0.4	+0.6	V
$I_{IH}$		$V_{IH} = V_{CC0}$	-6		+6	$\mu\text{A}$
$I_{IL}$		$V_{IL} = 0\text{ V}$			-0.1	mA
Sleep Time	$t_{SD}$	10% output swing		<1		ns
Wake-Up Time	$t_H$	$V_{OD} = 100\text{ mV}$ , output valid		35		ns
<b>DC OUTPUT CHARACTERISTICS</b>						
Output Voltage High Level	$V_{OH}$	$V_{CC0} = 2.5\text{ V to } 5.5\text{ V}$ 50 $\Omega$ terminate to $V_{CC0}$	$V_{CC0} - 0.1$	$V_{CC0} - 0.05$	$V_{CC0}$	V
Output Voltage Low Level	$V_{OL}$	50 $\Omega$ terminate to $V_{CC0}$	$V_{CC0} - 0.6$	$V_{CC0} - 0.45$	$V_{CC0} - 0.3$	V
Output Voltage Differential		50 $\Omega$ terminate to $V_{CC0}$	300	400	500	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>AC PERFORMANCE<sup>1</sup></b>						
Rise Time/Fall time	$t_{r}/t_{f}$	10% to 90%, $V_{CCI} = V_{CCO} = 2.5\text{ V to }5.5\text{ V}$		160		ps
Propagation Delay	$t_{PD}$	$V_{CCI} = V_{CCO} = 2.5\text{ V to }5.5\text{ V}$ , $V_{OD} = 50\text{ mV}$		1.2		ns
		$V_{CCI} = V_{CCO} = 2.5\text{ V}$ , $V_{OD} = 10\text{ mV}$		2.1		ns
Propagation Delay Skew—Rising to Falling Transition	$T_{PINSKEW}$	$V_{OD} = 50\text{ mV}$		40		ps
Overdrive Dispersion		$10\text{ mV} < V_{OD} < 125\text{ mV}$		2.3		ns
Common-Mode Dispersion		$-0.2\text{ V} < V_{CM} < V_{CC} + 0.2\text{ V}$		150		ps
Input Stage Bandwidth				750		MHz
RMS Random Jitter	RJ	$V_{OD} = 200\text{ mV}$ , $0.5\text{ V/ns}$		2		ps
Minimum Pulse Width	$PW_{MIN}$	$V_{CCI} = V_{CCO} = 5.5\text{ V}$ , $PW_{OUT} = 90\%$ of $PW_{IN}$		1.1		ns
Output Skew Q to $\bar{Q}$	$T_{DIFFSKEW}$	50%		20		ps
<b>POWER SUPPLY</b>						
Input Supply Voltage Range	$V_{CCI}$		2.5		5.5	V
Output Supply Voltage Range	$V_{CCO}$		2.5		5.5	V
Positive Supply Differential (ADCMP607)	$V_{CCI} - V_{CCO}$	Operating	-3.0		+3.0	V
		Nonoperating	-6		+6	V
Positive Supply Current (ADCMP606)	$I_{VCCI/VCCO}$	$V_{CCI} = V_{CCO} = 2.5\text{ V}$	11	17.5	21	mA
		$V_{CCI} = V_{CCO} = 5.5\text{ V}$	16	20.5	26	mA
Input Section Supply Current (ADCMP607)	$I_{VCCI}$	$V_{CCI} = 2.5\text{ V}$	0.5	1.1	1.5	mA
Output Section Supply Current (ADCMP607)	$I_{VCCO}$	$V_{CCO} = 2.5\text{ V}$	10	15.8	18	mA
		$V_{CCO} = 5.5\text{ V}$	16	18	25	mA
Power Dissipation	$P_D$	$V_{CCI} = V_{CCO} = 2.5\text{ V}$	30	46	55	mW
		$V_{CCI} = V_{CCO} = 5.5\text{ V}$	90	110	150	mW
Power Supply Rejection Ratio	PSRR	$V_{CCI} = 2.5\text{ V to }5\text{ V}$	-50			dB
Shutdown Mode $I_{CCI}$		$V_{CCI} = V_{CCO} = 2.5\text{ V to }5\text{ V}$	200	240	800	$\mu\text{A}$
Shutdown Mode $I_{CCO}$		$V_{CCI} = V_{CCO} = 2.5\text{ V to }5\text{ V}$	-30		30	$\mu\text{A}$

<sup>1</sup>  $V_{IN} = 100\text{ mV}$  square input at 50 MHz,  $V_{CM} = 2.5\text{ V}$ ,  $V_{CCI} = V_{CCO} = 2.5\text{ V}$ , unless otherwise noted.

**TIMING INFORMATION**

Figure 2 illustrates the ADCMP606/ADCMP607 latch timing relationships. Table 2 provides definitions of the terms shown in Figure 2.

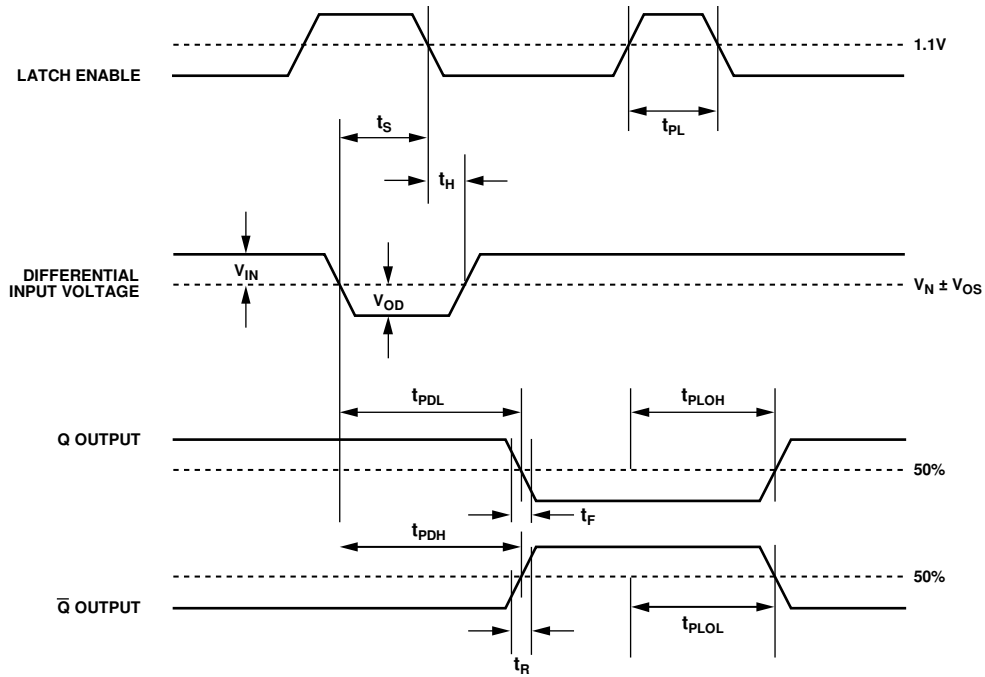


Figure 2. System Timing Diagram

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**Table 2. Timing Descriptions**

Symbol	Symbol Description	Timing Description
$t_F$	Output fall time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points.
$t_H$	Minimum hold time	Minimum time after the negative transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs.
$t_{PDH}$	Input to output high delay	Propagation delay measured from the time the input signal crosses the reference ( $\pm$ the input offset voltage) to the 50% point of an output low-to-high transition.
$t_{PDL}$	Input to output low delay	Propagation delay measured from the time the input signal crosses the reference ( $\pm$ the input offset voltage) to the 50% point of an output high-to-low transition.
$t_{PL}$	Minimum latch enable pulse width	Minimum time that the latch enable signal must be high to acquire an input signal change.
$t_{PLOH}$	Latch enable to output high delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition.
$t_{PLOL}$	Latch enable to output low delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition.
$t_R$	Output rise time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points.
$t_S$	Minimum setup time	Minimum time before the negative transition of the latch enable signal occurs that an input signal change must be present to be acquired and held at the outputs.
$V_{OD}$	Voltage overdrive	Difference between the input voltages $V_A$ and $V_B$ .

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltages	
Input Supply Voltage ( $V_{CCI}$ to GND)	–0.5 V to +6.0 V
Output Supply Voltage ( $V_{CCO}$ to GND)	–0.5 V to +6.0 V
Positive Supply Differential ( $V_{CCI} - V_{CCO}$ )	–6.0 V to +6.0 V
Input Voltages	
Input Voltage	–0.5 V to $V_{CCI} + 0.5$ V
Differential Input Voltage	$\pm(V_{CCI} + 0.5$ V)
Maximum Input/Output Current	$\pm 50$ mA
Shutdown Control Pin	
Applied Voltage ( $S_{DN}$ to GND)	–0.5 V to $V_{CCO} + 0.5$ V
Maximum Input/Output Current	$\pm 50$ mA
Latch/Hysteresis Control Pin	
Applied Voltage (HYS to GND)	–0.5 V to $V_{CCO} + 0.5$ V
Maximum Input/Output Current	$\pm 50$ mA
Output Current	$\pm 50$ mA
Temperature	
Operating Temperature, Ambient	–40°C to +125°C
Operating Temperature, Junction	150°C
Storage Temperature Range	–65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$ <sup>1</sup>	Unit
ADCMP606 6-Lead SC70	426	°C/W
ADCMP607 12-Lead LFCSP	62	°C/W

<sup>1</sup> Measurement in still air.

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

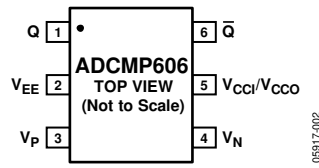
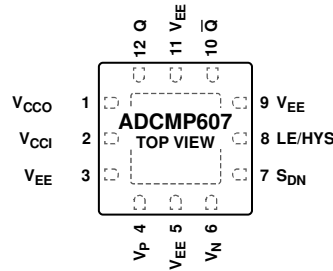


Figure 3. ADCMP606 Pin Configuration

Table 5. ADCMP606 (6-Lead SC70) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, $V_P$ , is greater than the analog voltage at the inverting input, $V_N$ .
2	$V_{EE}$	Negative Supply Voltage.
3	$V_P$	Noninverting Analog Input.
4	$V_N$	Inverting Analog Input.
5	$V_{CCI}/V_{CCO}$	Input Section Supply/Output Section Supply. Shared pin.
6	$\bar{Q}$	Inverting Output. $\bar{Q}$ is at logic low if the analog voltage at the noninverting input, $V_P$ , is greater than the analog voltage at the inverting input, $V_{IN}$ .



**NOTES**

1. EXPOSED PAD. IF CONNECTED, THE EPAD MUST BE CONNECTED TO  $V_{EE}$ . THE METALLIC BACK SURFACE OF THE PACKAGE IS ELECTRICALLY CONNECTED TO  $V_{EE}$ . IT CAN BE LEFT FLOATING BECAUSE PIN 3, PIN 5, PIN 9, AND PIN 11 PROVIDE ADEQUATE ELECTRICAL CONNECTION. IT CAN ALSO BE SOLDERED TO THE APPLICATION BOARD IF IMPROVED THERMAL AND/OR MECHANICAL STABILITY IS DESIRED.

Figure 4. ADCMP607 Pin Configuration

Table 6. ADCMP607 (12-Lead LFCSP) Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{CCO}$	Output Section Supply.
2	$V_{CCI}$	Input Section Supply.
3, 5, 9, 11	$V_{EE}$	Negative Supply Voltage.
4	$V_P$	Noninverting Analog Input.
6	$V_N$	Inverting Analog Input.
7	$S_{DN}$	Shutdown. Drive this pin low to shut down the device.
8	LE/HYS	Latch/Hysteresis Control. Bias with resistor or current for hysteresis adjustment; drive low to latch.
10	$\bar{Q}$	Inverting Output. $\bar{Q}$ is at logic low if the analog voltage at the noninverting input, $V_P$ , is greater than the analog voltage at the inverting input, $V_N$ , if the comparator is in compare mode.
12	Q	Noninverting Output. Q is at logic high if the analog voltage at the noninverting input, $V_P$ , is greater than the analog voltage at the inverting input, $V_N$ , if the comparator is in compare mode.
	EPAD	Exposed Pad. If connected, the EPAD must be connected to $V_{EE}$ . The metallic back surface of the package is electrically connected to $V_{EE}$ . It can be left floating because Pin 3, Pin 5, Pin 9, and Pin 11 provide adequate electrical connection. It can also be soldered to the application board if improved thermal and/or mechanical stability is desired.

TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CCI} = V_{CCO} = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

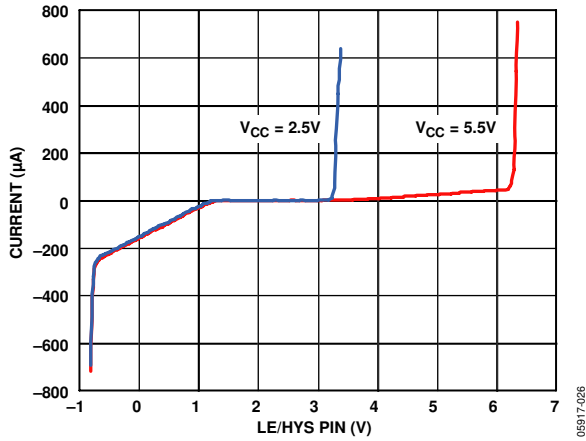


Figure 5. LE/HYS Pin Current vs. Voltage

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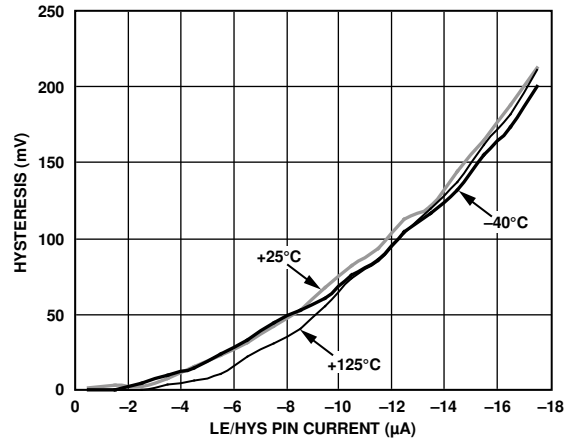


Figure 8. Hysteresis vs. LE/HYS Pin Current

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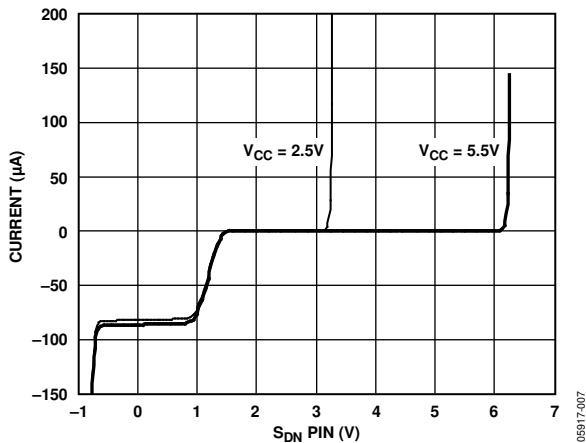


Figure 6.  $S_{DN}$  Pin Current vs. Voltage

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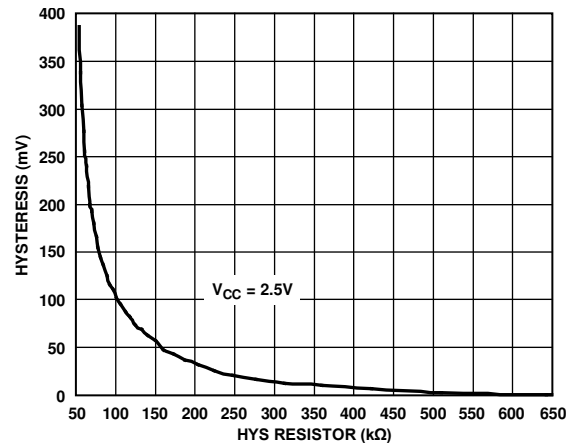


Figure 9. Hysteresis vs. Hysteresis Resistor

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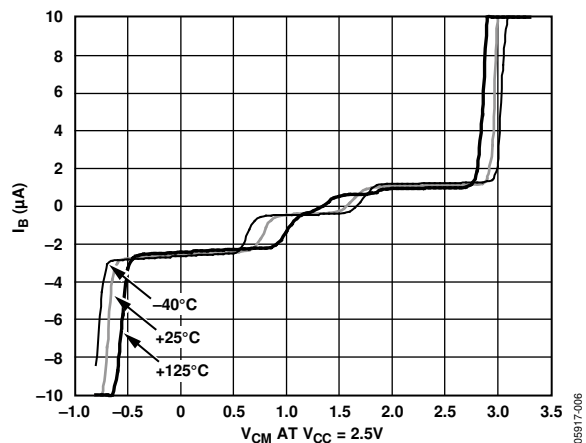


Figure 7. Input Bias Current vs. Input Common-Mode Voltage

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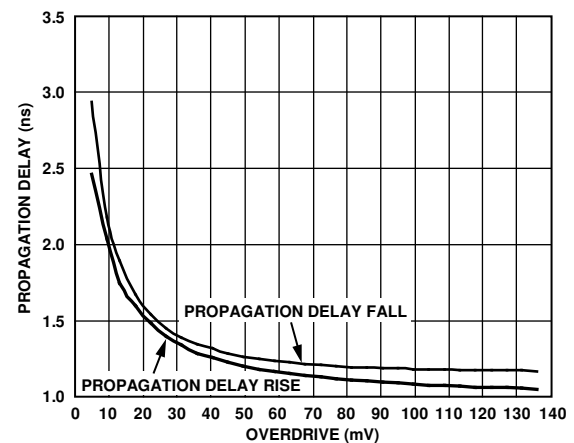


Figure 10. Propagation Delay vs. Input Overdrive

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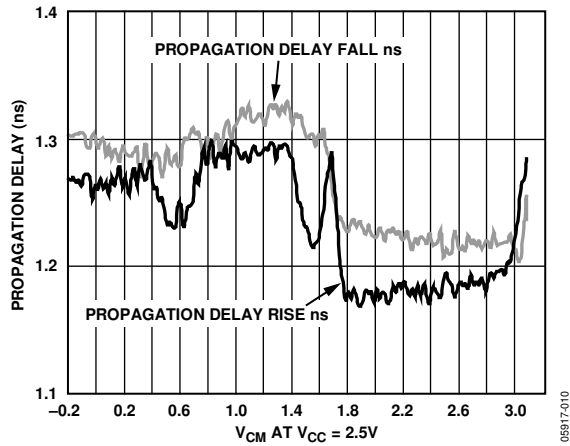


Figure 11. Propagation Delay vs. Input Common-Mode Voltage

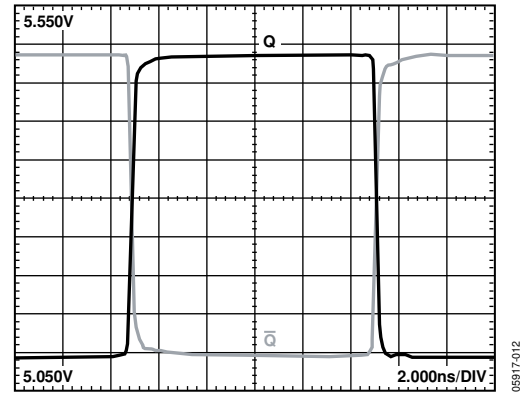


Figure 13. Output Waveform at  $V_{CC} = 5.5V$

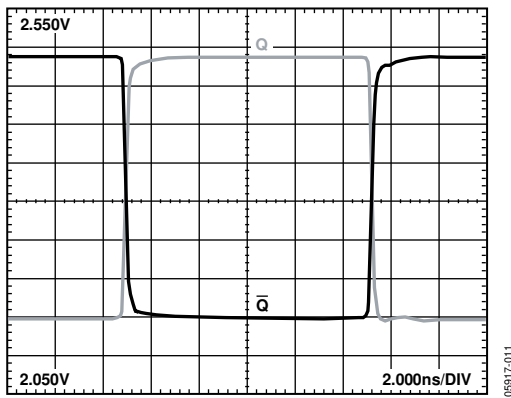


Figure 12. Output Waveform at  $V_{CC} = 2.5V$

## APPLICATIONS INFORMATION

### POWER/GROUND LAYOUT AND BYPASSING

The ADCMP606/ADCMP607 comparators are very high speed devices. Despite the low noise output stage, it is essential to use proper high speed design techniques to achieve the specified performance. Because comparators are uncompensated amplifiers, feedback in any phase relationship is likely to cause oscillations or undesired hysteresis. Of critical importance is the use of low impedance supply planes, particularly the output supply plane ( $V_{CCO}$ ) and the ground plane (GND). Individual supply planes are recommended as part of a multilayer board. Providing the lowest inductance return path for switching currents ensures the best possible performance in the target application.

It is also important to adequately bypass the input and output supplies. Multiple high quality 0.01  $\mu\text{F}$  bypass capacitors should be placed as close as possible to each of the  $V_{CCI}$  and  $V_{CCO}$  supply pins and should be connected to the GND plane with redundant vias. At least one of these should be placed to provide a physically short return path for output currents flowing back from ground to the  $V_{CCI}$  and  $V_{CCO}$  pins. High frequency bypass capacitors should be carefully selected for minimum inductance and ESR. Parasitic layout inductance should also be strictly controlled to maximize the effectiveness of the bypass at high frequencies.

### CML-COMPATIBLE OUTPUT STAGE

Specified propagation delay dispersion performance can be achieved by using proper transmission line terminations. The outputs of the ADCMP606 and ADCMP607 are designed to drive 400 mV directly into a 50  $\Omega$  cable or into transmission lines terminated using either microstrip or strip line techniques with 50  $\Omega$  referenced to  $V_{CCO}$ . The CML output stage is shown in the simplified schematic diagram in Figure 14. Each output is back terminated with 50  $\Omega$  for best transmission line matching.

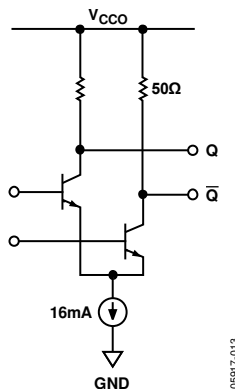


Figure 14. Simplified Schematic Diagram of CML-Compatible Output Stage

If these high speed signals must be routed more than a centimeter, then either microstrip or strip line techniques are required to ensure proper transition times and to prevent excessive output ringing and pulse width dependent propagation delay dispersion.

It is also possible to operate the outputs with the internal termination only if greater output swing is desired. This can be especially useful for driving inputs on CMOS devices intended for full swing ECL and PECL, or for generating pseudo PECL levels. To avoid deep saturation of the outputs and resulting pulse dispersion,  $V_{CCO}$  must be kept above the specified minimum output low level (see the Electrical Characteristics section). The line length driven should be kept as short as possible.

### USING/DISABLING THE LATCH FEATURE

The latch input is designed for maximum versatility. It can safely be left floating or it can be driven low by any standard TTL/CMOS device as a high speed latch.

In addition, the pin can be operated as a hysteresis control pin with a bias voltage of 1.25 V nominal and an input resistance of approximately 70 k $\Omega$ . This allows the comparator hysteresis to be easily controlled by either a resistor or an inexpensive CMOS DAC. Driving this pin high or floating the pin removes all hysteresis.

Hysteresis control and latch mode can be used together if an open-drain, an open-collector, or a three-state driver is connected parallel to the hysteresis control resistor or current source.

Due to the programmable hysteresis feature, the logic threshold of the latch pin is approximately 1.1 V regardless of  $V_{CCO}$ .

### OPTIMIZING PERFORMANCE

As with any high speed comparator, proper design and layout techniques are essential for obtaining the specified performance. Stray capacitance, inductance, inductive power and ground impedances, or other layout issues can severely limit performance and often cause oscillation. Large discontinuities along input and output transmission lines can also limit the specified pulse width dispersion performance. The source impedance should be minimized as much as is practicable. High source impedance, in combination with the parasitic input capacitance of the comparator, causes an undesirable degradation in bandwidth at the input, thus degrading the overall response. Thermal noise from large resistances can easily cause extra jitter with slowly slewing input signals; higher impedances encourage undesired coupling.

**COMPARATOR PROPAGATION DELAY DISPERSION**

The ADCMP606/ADCMP607 comparators are designed to reduce propagation delay dispersion over a wide input overdrive range of 5 mV to  $V_{CCI} - 1$  V. Propagation delay dispersion is the variation in propagation delay that results from a change in the degree of overdrive or slew rate (that is, how far or how fast the input signal exceeds the switching threshold).

Propagation delay dispersion is a specification that becomes important in high speed, time-critical applications, such as data communication, automatic test and measurement, and instrumentation. It is also important in event-driven applications, such as pulse spectroscopy, nuclear instrumentation, and medical imaging. Dispersion is defined as the variation in propagation delay as the input overdrive conditions are changed (Figure 15 and Figure 16).

The device dispersion is typically 2.3 ns as the overdrive varies from 10 mV to 125 mV. This specification applies to both positive and negative signals because each device has very closely matched delays for positive-going and negative-going inputs as well as very low output skews.

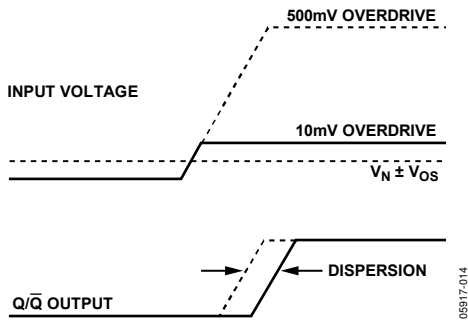


Figure 15. Propagation Delay—Overdrive Dispersion

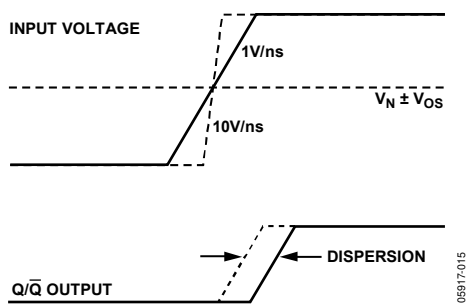


Figure 16. Propagation Delay—Slew Rate Dispersion

**COMPARATOR HYSTERESIS**

The addition of hysteresis to a comparator is often desirable in a noisy environment, or when the differential input amplitudes are relatively small or slow moving. Figure 17 shows the transfer function for a comparator with hysteresis. As the input voltage approaches the threshold (0 V, in this example) from below the threshold region in a positive direction, the comparator switches from low to high when the input crosses  $+V_H/2$ , and the new switching threshold becomes  $-V_H/2$ . The comparator remains in

the high state until the new threshold,  $-V_H/2$ , is crossed from below the threshold region in a negative direction. In this manner, noise or feedback output signals centered on 0 V input cannot cause the comparator to switch states unless it exceeds the region bounded by  $\pm V_H/2$ .

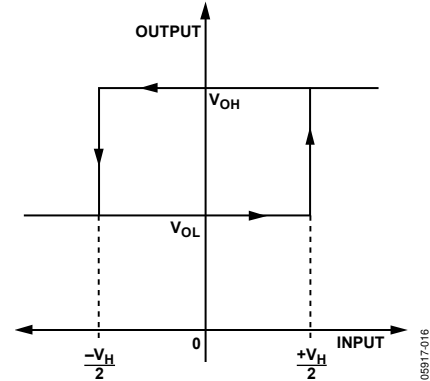


Figure 17. Comparator Hysteresis Transfer Function

The customary technique for introducing hysteresis into a comparator uses positive feedback from the output back to the input. One limitation of this approach is that the amount of hysteresis varies with the output logic levels, resulting in hysteresis that is not symmetric about the threshold. The external feedback network can also introduce significant parasitics that reduce high speed performance and induce oscillation in some cases.

This ADCMP607 comparator offers a programmable hysteresis feature that can significantly improve accuracy and stability. Connecting an external pull-down resistor or a current source from the LE/HYS pin to GND, varies the amount of hysteresis in a predictable, stable manner. Leaving the LE/HYS pin disconnected or driving this pin high removes hysteresis. The maximum hysteresis that can be applied using this pin is approximately 160 mV. Figure 18 illustrates typical hysteresis applied as a function of the external resistor value, and Figure 8 illustrates typical hysteresis as a function of the current.

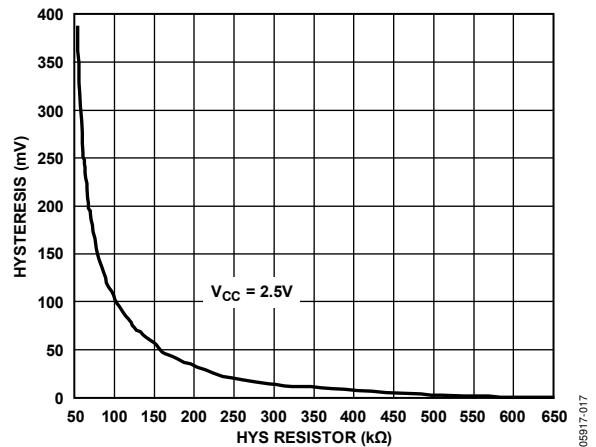


Figure 18. Hysteresis vs.  $R_{HYS}$  Control Resistor

The hysteresis control pin appears as a 1.25 V bias voltage seen through a series resistance of  $70\text{ k}\Omega \pm 20\%$  throughout the hysteresis control range. The advantages of applying hysteresis in this manner are improved accuracy, improved stability, reduced component count, and maximum versatility. An external bypass capacitor is not recommended on the LE/HYS pin because it impairs the latch function and often degrades the jitter performance of the device. As described in the Using/Disabling the Latch Feature section, hysteresis control need not compromise the latch function.

### CROSSOVER BIAS POINTS

In both op amps and comparators, rail-to-rail inputs of this type have a dual front-end design. Certain devices are active near the  $V_{CCI}$  rail and others are active near the  $V_{EE}$  rail. At some pre-terminated point in the common-mode range, a crossover occurs. At this point, normally  $V_{CCI}/2$ , the direction of the bias current reverses and the measured offset voltages and currents change.

The ADCMP606/ADCMP607 comparators slightly elaborate on this scheme. Crossover points are found at approximately 0.6 V and 1.6 V common mode.

### MINIMUM INPUT SLEW RATE REQUIREMENT

With the rated load capacitance and normal good PCB design practice, as discussed in the Optimizing Performance section, these comparators should be stable at any input slew rate with no hysteresis. Broadband noise from the input stage is observed in place of the violent chattering seen with most other high speed comparators. With additional capacitive loading or poor bypassing, oscillation is observed. This oscillation is due to the high gain bandwidth of the comparator in combination with feedback parasitics in the package and PC board. In many applications, chattering is not harmful.

TYPICAL APPLICATION CIRCUITS

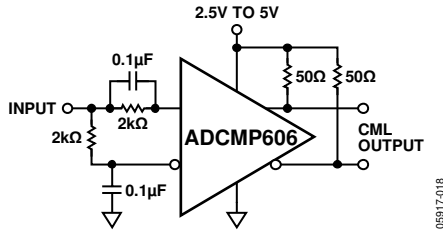


Figure 19. Self-Biased, 50% Slicer on the ADCMP606

05917-018

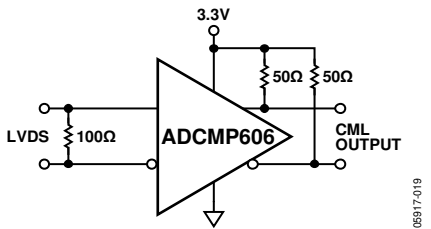


Figure 20. LVDS to CML on the ADCMP606

05917-019

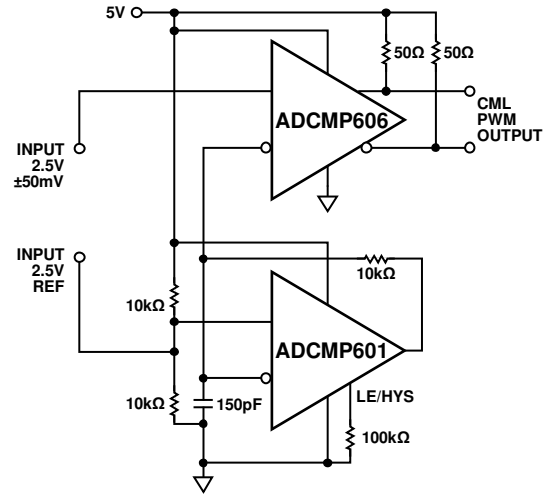


Figure 23. Oscillator and Pulse-Width Modulator on the ADCMP601 and ADCMP606

05917-022

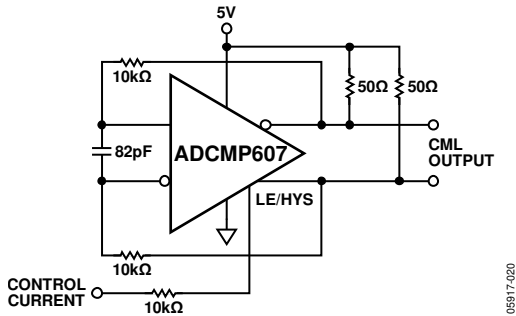


Figure 21. Current-Controlled Oscillator on the ADCMP607

05917-020

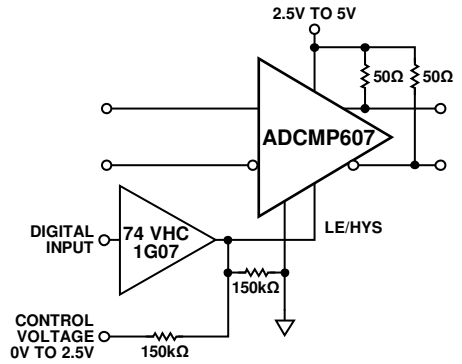


Figure 24. Hysteresis Adjustment with Latch on the ADCMP607

05917-023

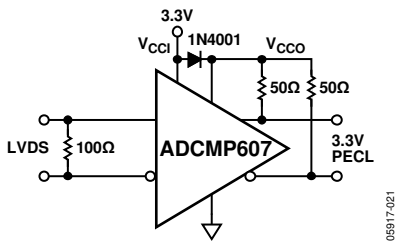


Figure 22. Fake PECL Levels Using a Series Diode on the ADCMP607

05917-021

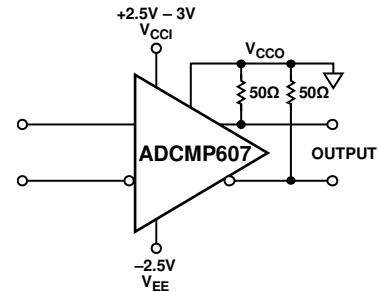
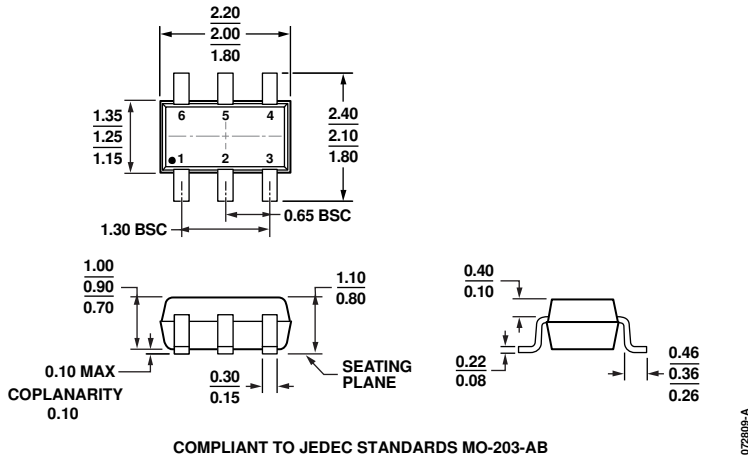


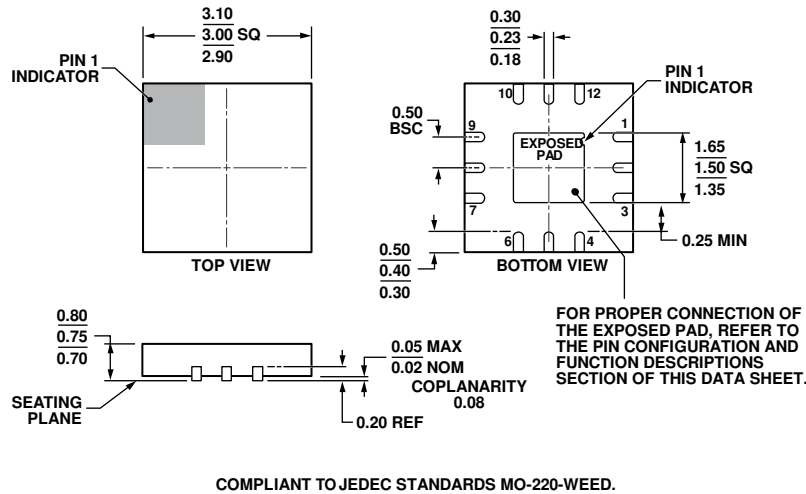
Figure 25. Ground-Referenced CML with ±3V Input Range on the ADCMP607

05917-024

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-203-AB  
 Figure 26. 6-Lead Thin Shrink Small Outline Transistor Package [SC70] (KS-6)  
 Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WEED.  
 Figure 27. 12-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm x 3 mm and 0.75 mm Package Height (CP-12-5)  
 Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
ADCMP606BKSZ-R2	-40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	G0S
ADCMP606BKSZ-REEL7	-40°C to +125°C	6-Lead Thin Shrink Small Outline Transistor Package [SC70]	KS-6	G0S
EVAL-ADCMP606BKSZ		Evaluation Board		
ADCMP607BCPZ-R2	-40°C to +125°C	12-Lead Lead Frame Chip Scale Package [LFCSP]	CP-12-5	G0H
ADCMP607BCPZ-R7	-40°C to +125°C	12-Lead Lead Frame Chip Scale Package [LFCSP]	CP-12-5	G0H
ADCMP607BCPZ-WP	-40°C to +125°C	12-Lead Lead Frame Chip Scale Package [LFCSP]	CP-12-5	G0H
EVAL-ADCMP607BCPZ		Evaluation Board		

<sup>1</sup> Z = RoHS Compliant Part.