

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



# Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China









# Quad-Channel, 16-Bit CCD Signal Processor with *Precision Timing* Core

Data Sheet ADDI7015

#### **FEATURES**

4 independent AFE channels

1.8 V analog and digital core supply voltage

Complete on-chip ISATG timing generator with 16 XV outputs and 4 general-purpose outputs (GPO)

Differential analog inputs

CDS or SHA (CDS bypass) with 7 gain settings

0 dB to 36 dB, 10-bit variable gain amplifier (VGA)

16-bit, 65 MSPS analog-to-digital converter (ADC)

Precision Timing core with 240 ps resolution at 65 MHz

8 programmable H-clock outputs

On-chip sync generator with external sync input

8 mm × 8 mm CSP\_BGA package with 0.65 pitch

#### **APPLICATIONS**

Industrial cameras
Surveillance cameras
Medical imaging
Professional photography

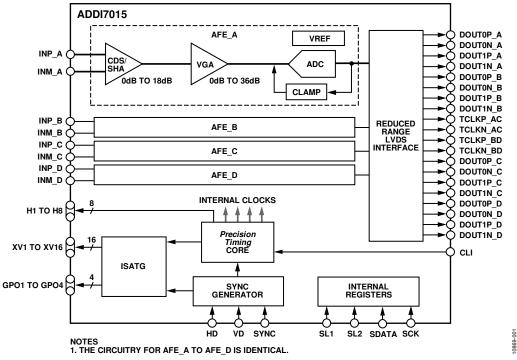
#### **GENERAL DESCRIPTION**

The ADDI7015 is a highly integrated, quad-channel, CCD signal processor for high speed digital imaging applications. Each channel is specified at pixel rates of up to 65 MHz and consists of a complete analog front end (AFE) with analog-to-digital conversion. The *Precision Timing*\* core allows adjustment of the correlated double sampler (CDS) and sample-and-hold amplifier (SHA) clocks with 240 ps resolution at 65 MHz operation. There are eight independent horizontal clock outputs to support a variety of CCD timing requirements. The ADDI7015 also features a programmable ISATG for vertical timing generation.

Each analog front end includes black level clamping, a CDS, a VGA, and a 65 MSPS, 16-bit analog-to-digital converter (ADC). Operation is programmed using a 4-wire serial interface.

Packaged in a space-saving, 8 mm  $\times$  8 mm, CSP\_BGA, the ADDI7015 is specified over an operating temperature range of  $-25^{\circ}$ C to  $+85^{\circ}$ C.

#### **FUNCTIONAL BLOCK DIAGRAM**



Fiaure 1.

For more information on the ADDI7015, email Analog Devices, Inc., at afe.ccd@analog.

# ADDI7015\* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

## COMPARABLE PARTS 🖵

View a parametric search of comparable parts.

## **DOCUMENTATION**

#### **Data Sheet**

 ADDI7015: Quad-Channel, 16-Bit CCD Signal Processor with Precision Timing Core Data Sheet

## **DESIGN RESOURCES**

- · ADDI7015 Material Declaration
- · PCN-PDN Information
- · Quality And Reliability
- Symbols and Footprints

## **DISCUSSIONS**

View all ADDI7015 EngineerZone Discussions.

## SAMPLE AND BUY 🖵

Visit the product page to see pricing options.

## TECHNICAL SUPPORT 🖳

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK 🖳

Submit feedback for this data sheet.

This page is dynamically generated by Analog Devices, Inc., and inserted into this data sheet. A dynamic change to the content on this page will not trigger a change to either the revision number or the content of the product data sheet. This dynamic page may be frequently modified.

ADDI7015 Data Sheet

**NOTES**