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# Single-Phase Energy Measurement IC with 8052 MCU, RTC, and LCD Driver

Data Sheet **ADE5166/ADE5169/ADE5566/ADE5569**

## GENERAL FEATURES

- Wide supply voltage operation: 2.4 V to 3.7 V
- Internal bipolar switch between regulated and battery inputs
- Ultralow power operation with power saving modes (PSM)
  - Full operation: 4.4 mA to 1.6 mA (PLL clock dependent)
  - Battery mode: 3.3 mA to 400 µA (PLL clock dependent)
  - Sleep mode
    - Real-time clock (RTC) mode: 1.7 µA
    - RTC and LCD mode: 38 µA (LCD charge pump enabled)
- Reference: 1.2 V ± 0.1% (10 ppm/°C drift)
- 64-lead, low profile quad flat, RoHS-compliant package (LQFP)
- Operating temperature range: −40°C to +85°C

## ENERGY MEASUREMENT FEATURES

- Proprietary analog-to-digital converters (ADCs) and digital signal processing (DSP) provide high accuracy active (watt), reactive (var), and apparent energy (volt-ampere (VA)) measurement
  - <0.1% error on active energy over a dynamic range of 1000 to 1 @ 25°C
  - <0.5% error on reactive energy over a dynamic range of 1000 to 1 @ 25°C (ADE5169 and ADE5569 only)
  - <0.5% error on root mean square (rms) measurements over a dynamic range of 500 to 1 for current ($I_{rms}$) and 100 to 1 for voltage ($V_{rms}$) @ 25°C
  - Supports IEC 62053-21; IEC 62053-22; IEC 62053-23; EN 50470-3 Class A, Class B, and Class C; and ANSI C12-16
- Differential input with programmable gain amplifiers (PGAs) supports shunts, current transformers, and di/dt current sensors (ADE5169 and ADE5569 only)
- 2 current inputs for antitamper detection in the ADE5166/ADE5169
- High frequency outputs proportional to $I_{rms}$, active, reactive, or apparent power (AP)

Table 1. Features Available on Each Part

| Part No. | Antitamper | Watt, VA, $I_{rms}$, $V_{rms}$ | Var | di/dt Sensor | Memory Size |
|---|---|---|---|---|---|
| ADE5166 | Yes | Yes | No | No | 62kB |
| ADE5169 | Yes | Yes | Yes | Yes | 32kB or 62kB |
| ADE5566 | No | Yes | No | No | 62kB |
| ADE5569 | No | Yes | Yes | Yes | 62kB |

## MICROPROCESSOR FEATURES

- 8052-based core
  - Single-cycle 4 MIPS 8052 core
  - 8052-compatible instruction set
  - 32.768 kHz external crystal with on-chip PLL
  - 2 external interrupt sources
  - External reset pin
- Low power battery mode
  - Wake-up from I/O, temperature change, alarm, and universal asynchronous receiver/transmitter (UART)
  - LCD driver operation with automatic scrolling
  - Temperature measurement
- Real-time clock (RTC)
  - Counter for seconds, minutes, hours, days, months, and years
  - Date counter, including leap year compensation
  - Automatic battery switchover for RTC backup
  - Operation down to 2.4 V
  - Ultralow battery supply current: 1.7 µA
  - Selectable output frequency: 1 Hz to 16 kHz
  - Embedded digital crystal frequency compensation for calibration and temperature variation of 2 ppm resolution
- Integrated LCD driver
  - 108-segment driver for the ADE5566 and ADE5569
  - 104-segment driver for the ADE5166 and ADE5169
  - 2×, 3×, or 4× multiplexing
  - 4 LCD memory banks for screen scrolling
  - LCD voltages generated internally or with external resistors
  - Internal adjustable drive voltages up to 5 V independent of power supply level
- On-chip peripherals
  - 2 independent UART interfaces
  - SPI or $I^2C$
  - Watchdog timer
- Power supply management with user-selectable levels
- Memory: 62 kB flash memory, 2.256 kB RAM
- Development tools
  - Single-pin emulation
  - IDE-based assembly and C source debugging

Rev. D


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## GENERAL DESCRIPTION

The ADE5166/ADE5169/ADE5566/ADE5569[1] integrate the Analog Devices, Inc., energy (ADE) metering IC analog front end and fixed function DSP solution with an enhanced 8052 MCU core, a full RTC, an LCD driver, and all the peripherals to make an electronic energy meter with an LCD display in a single part.

The ADE measurement core includes active, reactive, and apparent energy calculations, as well as voltage and current rms measurements. This information is accessible for energy billing by using the built-in energy scalars. Many power line supervisory features such as SAG, peak, and zero crossing are included in the energy measurement DSP to simplify energy meter design.

The microprocessor functionality includes a single-cycle 8052 core, a full RTC with a power supply backup pin, an SPI or I²C interface, and two independent UART interfaces. The ready-to-use information from the ADE core reduces the requirement for program memory size, making it easy to integrate complicated design into 62 kB of flash memory.

[1] Patents pending.

The ADE5166/ADE5169 include a 104-segment LCD driver and the ADE5566/ADE5569 include a 108-segment LCD driver, each with the capability to store up to four LCD screens in memory. This driver generates voltages capable of driving LCDs up to 5 V.

## 32 KB FLASH OPTION

A reduced memory version of the ADE5169 is available with 32 kB of flash memory. A description of the flash memory organization of this model is provided in the Flash Memory Organization for the 32 kB Model section. All other features and functionality are identical between the models and no reference is made in the remainder of this data sheet to the 32 kB model. If using the 32 kB model, 32 kB should therefore be substituted in any references to 62 kB of flash memory.

## FUNCTIONAL BLOCK DIAGRAMS

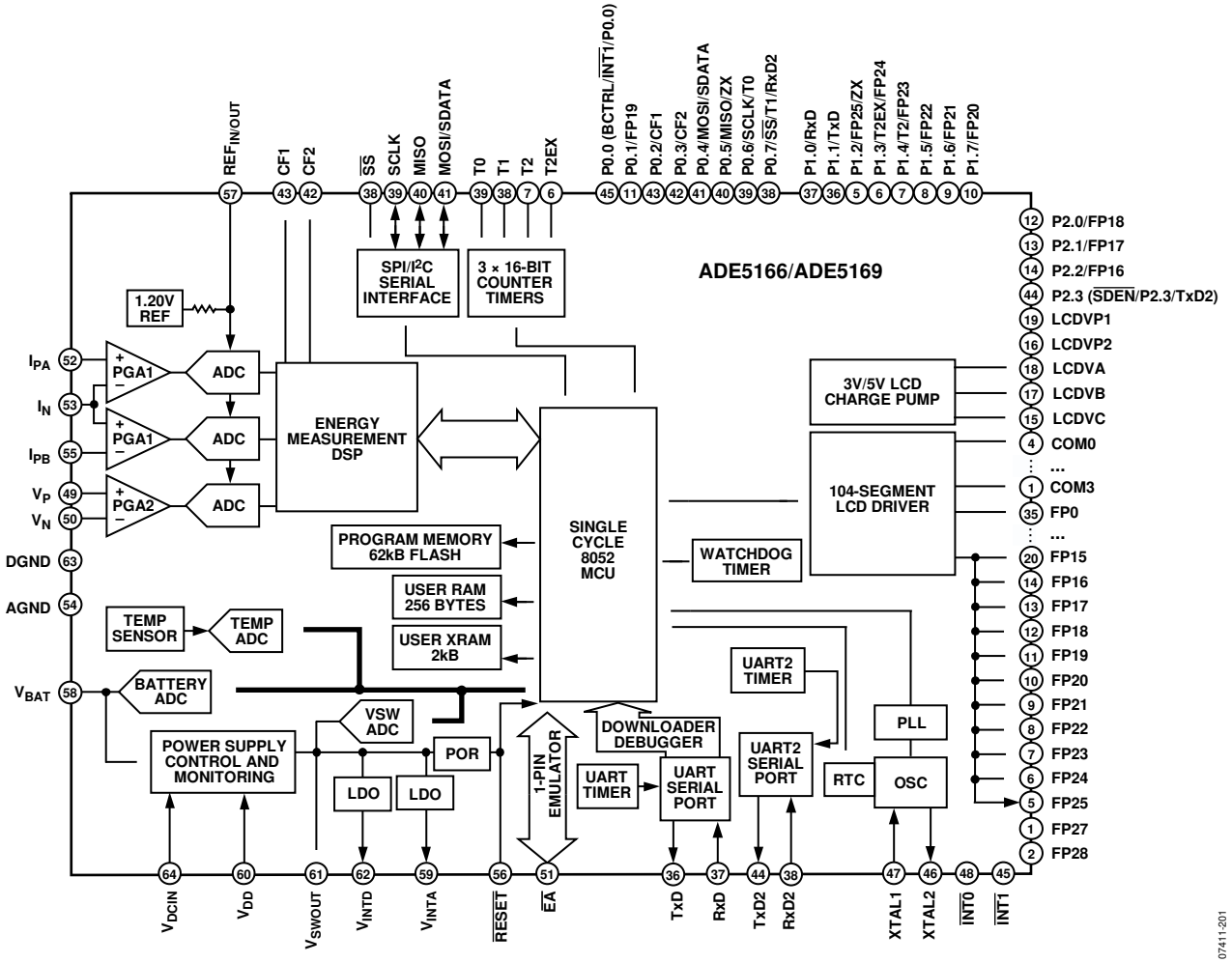


*Figure 1. ADE5166/ADE5169 Functional Block Diagram*

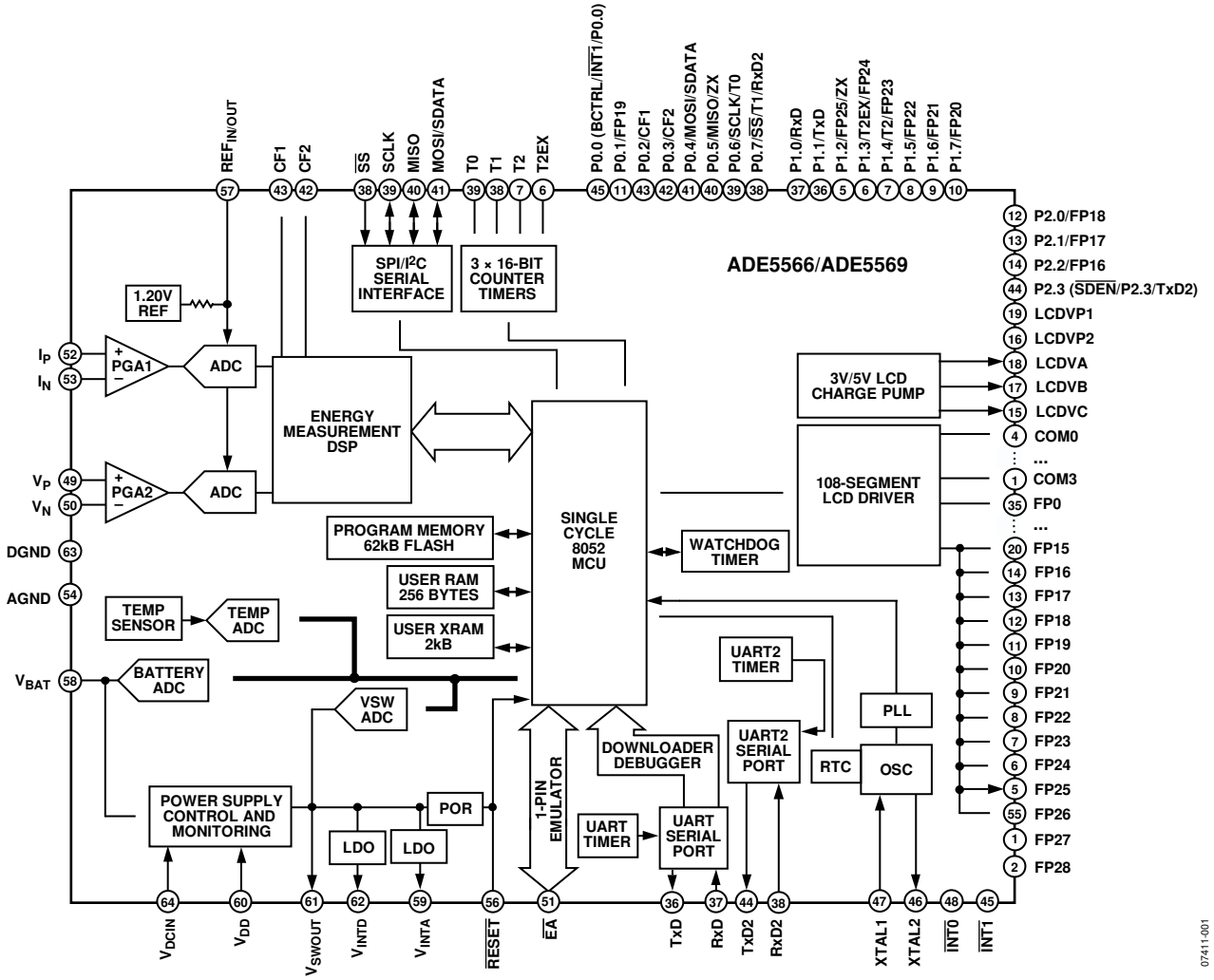


*Figure 2. ADE5566/ADE5569 Functional Block Diagram*

# SPECIFICATIONS

$V_{DD}$ = 3.3 V ± 5%, AGND = DGND = 0 V, on-chip reference XTALx = 32.768 kHz, $T_{MIN}$ to $T_{MAX}$ = −40°C to +85°C, unless otherwise noted.

## ENERGY METERING

**Table 2.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| MEASUREMENT ACCURACY[1] | | | | | |
| Phase Error Between Channels | | | | | |
| PF = 0.8 Capacitive | | ±0.05 | | Degrees | Phase lead: 37° |
| PF = 0.5 Inductive | | ±0.05 | | Degrees | Phase lag: 60° |
| Active Energy Measurement Error[2] | | 0.1 | | % of reading | Over a dynamic range of 1000 to 1 at 25°C |
| AC Power Supply Rejection[2] | | | | | $V_{DD}$ = 3.3 V + 100 mV rms/120 Hz |
| Output Frequency Variation | | 0.01 | | % | $I_{Px} = V_P$ = ±100 mV rms |
| DC Power Supply Rejection[2] | | | | | $V_{DD}$ = 3.3 V ± 117 mV dc |
| Output Frequency Variation | | 0.01 | | % | |
| Active Energy Measurement Bandwidth[1] | | 8 | | kHz | |
| Reactive Energy Measurement Error[2] | | 0.5 | | % of reading | Over a dynamic range of 1000 to 1 at 25°C |
| $V_{rms}$ Measurement Error[2] | | 0.5 | | % of reading | Over a dynamic range of 100 to 1 at 25°C |
| $V_{rms}$ Measurement Bandwidth[1] | | 63.7 | | Hz | Fundamental only, mean absolute measurement |
| $I_{rms}$ Measurement Error[2] | | 0.5 | | % of reading | Over a dynamic range of 500 to 1 at 25°C |
| $I_{rms}$ Measurement Bandwidth[1] | | 3.9 | | kHz | |
| ANALOG INPUTS | | | | | |
| Maximum Signal Levels | | | ±500 | mV peak | $V_P - V_N$ differential input |
| ADE5166/ADE5169 | | | ±500 | mV peak | $I_{PA} - I_N$ and $I_{PB} - I_N$ differential inputs |
| ADE5566/ADE5569 | | | ±500 | mV peak | $I_P - I_N$ |
| Input Impedance (DC) | | 770 | | kΩ | |
| ADC Offset Error[2] | | ±10 | | mV | PGA1 = PGA2 = 1 |
| | | ±1 | | mV | PGA1 = 16 |
| Gain Error[2] | | | | | |
| Current Channel | | ±3 | | % | $I_{PA} = I_{PB}$ = 0.5 V dc or $I_P$ = 0.5 V dc |
| Voltage Channel | | ±3 | | % | $V_P - V_N$ = 0.5 V dc |
| Gain Error Match | | ±0.2 | | % | |
| CF1 AND CF2 PULSE OUTPUT | | | | | |
| Maximum Output Frequency | | 21.6 | | kHz | $V_P - V_N$ = 500 mV peak; $I_{PA} - I_N$ = 500 mV for the ADE5166/ADE5169; $I_P - I_N$ = 500 mV for the ADE5566/ADE5569 |
| Duty Cycle | | 50 | | % | If the CF1 or CF2 frequency > 5.55 Hz |
| Active High Pulse Width | | 90 | | ms | If the CF1 or CF2 frequency < 5.55 Hz |
| FAULT DETECTION[3] | | | | | |
| Fault Detection Threshold | | | | | |
| Inactive Input ≠ Active Input | | 6.25 | | % of active | $I_{PA}$ or $I_{PB}$ active |
| Input Swap Threshold | | | | | |
| Inactive Input > Active Input | | 6.25 | | % of active | $I_{PA}$ or $I_{PB}$ active |
| Accuracy Fault Mode Operation | | | | | |
| $I_{PA}$ Active, $I_{PB}$ = AGND | | 0.1 | | % of reading | Over a dynamic range of 500 to 1 |
| $I_{PB}$ Active, $I_{PA}$ = AGND | | 0.1 | | % of reading | Over a dynamic range of 500 to 1 |
| Fault Detection Delay | | 3 | | Seconds | |
| Swap Delay | | 3 | | Seconds | |

[1] These specifications are not production tested but are guaranteed by design and/or characterization data on production release.
[2] See the Terminology section for definition.
[3] Available only in the ADE5166/ADE5169.

## ANALOG PERIPHERALS

**Table 3.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| INTERNAL ADCs (BATTERY, TEMPERATURE, $V_{DCIN}$) | | | | | |
| Power Supply Operating Range | 2.4 | | 3.7 | V | Measured on $V_{SWOUT}$ |
| No Missing Codes[1] | 8 | | | Bits | |
| Conversion Delay[2] | | 38 | | µs | |
| ADC Gain | | | | | |
| $V_{DCIN}$ Measurement | | 15.3 | | mV/LSB | |
| $V_{BAT}$ Measurement | | 14.6 | | mV/LSB | |
| Temperature Measurement | | 0.83 | | °C/LSB | |
| ADC Offset | | | | | |
| $V_{DCIN}$ Measurement at 3 V | | 200 | | LSB | |
| $V_{BAT}$ Measurement at 3.7 V | | 246 | | LSB | |
| Temperature Measurement at 25°C | | 123 | | LSB | |
| $V_{DCIN}$ Analog Input | | | | | |
| Maximum Signal Levels | 0 | | 3.3 | V | |
| Input Impedance (DC) | 1 | | | MΩ | |
| Low $V_{DCIN}$ Detection Threshold | 1.09 | 1.2 | 1.27 | V | |
| POWER-ON RESET (POR) | | | | | |
| $V_{DD}$ POR | | | | | |
| Detection Threshold | 2.5 | | 2.95 | V | |
| POR Active Timeout Period | | 33 | | ms | |
| $V_{SWOUT}$ POR | | | | | |
| Detection Threshold | 1.8 | | 2.2 | V | |
| POR Active Timeout Period | | 20 | | ms | |
| $V_{INTD}$ POR | | | | | |
| Detection Threshold | 2.0 | | 2.25 | V | |
| POR Active Timeout Period | | 16 | | ms | |
| $V_{INTA}$ POR | | | | | |
| Detection Threshold | 2.0 | | 2.25 | V | |
| POR Active Timeout Period | | 120 | | ms | |
| BATTERY SWITCHOVER | | | | | |
| Voltage Operating Range ($V_{SWOUT}$) | 2.4 | | 3.7 | V | |
| $V_{DD}$ to $V_{BAT}$ Switching | | | | | |
| Switching Threshold ($V_{DD}$) | 2.5 | | 2.95 | V | |
| Switching Delay | | 10 | | ns | When $V_{DD}$ to $V_{BAT}$ switch is activated by $V_{DD}$ |
| | | 30 | | ms | When $V_{DD}$ to $V_{BAT}$ switch is activated by $V_{DCIN}$ |
| $V_{BAT}$ to $V_{DD}$ Switching | | | | | |
| Switching Threshold ($V_{DD}$) | 2.5 | | 2.95 | V | |
| Switching Delay | | 30 | | ms | Based on $V_{DD}$ > 2.75 V |
| $V_{SWOUT}$ to $V_{BAT}$ Leakage Current | | 10 | | nA | $V_{BAT}$ = 0 V, $V_{SWOUT}$ = 3.43 V, $T_A$ = 25°C |
| LCD, CHARGE PUMP ACTIVE | | | | | |
| Charge Pump Capacitance Between LCDVP1 and LCDVP2 | 100 | | | nF | |
| LCDVA, LCDVB, LCDVC Decoupling Capacitance | 470 | | | nF | |
| LCDVA | 0 | | 1.9 | V | |
| LCDVB | 0 | | 3.8 | V | 1/3 bias mode |
| LCDVC | 0 | | 5.8 | V | 1/3 bias mode |
| V1 Segment Line Voltage | LCDVA – 0.1 | | LCDVA | V | Current on segment line = −2 µA |
| V2 Segment Line Voltage | LCDVB – 0.1 | | LCDVB | V | Current on segment line = −2 µA |
| V3 Segment Line Voltage | LCDVC – 0.1 | | LCDVC | V | Current on segment line = −2 µA |
| DC Voltage Across Segment and COMx Pin | | | 50 | mV | LCDVC – LCDVB, LCDVC – LCDVA, or LCDVB – LCDVA |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| LCD, RESISTOR LADDER ACTIVE | | | | | |
| Leakage Current | | ±20 | | nA | 1/2 and 1/3 bias modes, no load |
| V1 Segment Line Voltage | LCDVA − 0.1 | | LCDVA | V | Current on segment line = −2 µA |
| V2 Segment Line Voltage | LCDVB − 0.1 | | LCDVB | V | Current on segment line = −2 µA |
| V3 Segment Line Voltage | LCDVC − 0.1 | | LCDVC | V | Current on segment line = −2 µA |
| ON-CHIP REFERENCE | | | | | Nominal 1.2035 V |
| Reference Error | −2.2 | | +2.2 | mV | $T_A$ = 25°C, $f_{CORE}$ = 1.024 MHz |
| Power Supply Rejection | | 80 | | dB | |
| Temperature Coefficient[1] | | 10 | 50 | ppm/°C | $f_{CORE}$ = 1.024 MHz |

[1] These specifications are not production tested but are guaranteed by design and/or characterization data on production release.
[2] Delay between ADC conversion request and interrupt set.

## DIGITAL INTERFACE

**Table 4.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| LOGIC INPUTS[1] | | | | | |
| All Inputs Except XTAL1, XTAL2, BCTRL, $\overline{INT0}$, $\overline{INT1}$, $\overline{RESET}$ | | | | | |
| Input High Voltage, $V_{INH}$ | 2.0 | | | V | |
| Input Low Voltage, $V_{INL}$ | | | 0.8 | V | |
| BCTRL, $\overline{INT0}$, $\overline{INT1}$, $\overline{RESET}$ | | | | | |
| Input High Voltage, $V_{INH}$ | 1.3 | | | V | |
| Input Low Voltage, $V_{INL}$ | | | 0.8 | V | |
| Input Currents | | | | | |
| $\overline{RESET}$ | | | 100 | nA | $\overline{RESET}$ = $V_{SWOUT}$ = 3.3 V |
| Port 0, Port 1, Port 2 | | | ±100 | nA | Internal pull-up disabled, input = 0 V or $V_{SWOUT}$ |
| | −3.75 | | −8.5 | µA | Internal pull-up enabled, input = 0 V, $V_{SWOUT}$ = 3.3 V |
| Input Capacitance | | 10 | | pF | All digital inputs |
| FLASH MEMORY | | | | | |
| Endurance[2] | 20,000 | | | Cycles | At 25°C |
| Data Retention[3] | 20 | | | Years | $T_J$ = 85°C |
| CRYSTAL OSCILLATOR[4] | | | | | |
| Crystal Equivalent Series Resistance | 30 | | 50 | kΩ | |
| Crystal Frequency | 32 | 32.768 | 33.5 | kHz | |
| XTAL1 Input Capacitance | | 12 | | pF | |
| XTAL2 Output Capacitance | | 12 | | pF | |
| MCU CLOCK RATE ($f_{CORE}$) | | 4.096 | | MHz | Crystal = 32.768 kHz and CD bits = 0b000 |
| | | 32 | | kHz | Crystal = 32.768 kHz and CD bits = 0b111 |
| LOGIC OUTPUTS | | | | | |
| Output High Voltage, $V_{OH}$ | 2.4 | | | V | $V_{DD}$ = 3.3 V ± 5% |
| $I_{SOURCE}$ | | | 80 | µA | |
| Output Low Voltage, $V_{OL}$[5] | | | 0.4 | V | $V_{DD}$ = 3.3 V ± 5% |
| $I_{SINK}$ | | | 2 | mA | |
| START-UP TIME[6] | | | | | |
| PSM0 Power-On Time | | 880 | | ms | $V_{DD}$ at 2.75 V to PSM0 code execution |
| From Power Saving Mode 1 (PSM1) | | | | | |
| PSM1 to PSM0 | | 130 | | ms | $V_{DD}$ at 2.75 V to PSM0 code execution |
| From Power Saving Mode 2 (PSM2) | | | | | |
| PSM2 to PSM1 | | 48 | | ms | Wake-up event to PSM1 code execution |
| PSM2 to PSM0 | | 186 | | ms | $V_{DD}$ at 2.75 V to PSM0 code execution |

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| POWER SUPPLY INPUTS | | | | | |
| $V_{DD}$ | 3.13 | 3.3 | 3.46 | V | |
| $V_{BAT}$ | 2.4 | 3.3 | 3.7 | V | |
| INTERNAL POWER SUPPLY SWITCH ($V_{SWOUT}$) | | | | | |
| $V_{BAT}$ to $V_{SWOUT}$ On Resistance | | | 12 | Ω | $V_{BAT}$ = 2.4 V |
| $V_{DD}$ to $V_{SWOUT}$ On Resistance | | | 9 | Ω | $V_{DD}$ = 3.13 V |
| $V_{BAT}$ to/from $V_{DD}$ Switching Open Time | | 40 | | ns | |
| BCTRL State Change and Switch Delay | | 18 | | µs | |
| $V_{SWOUT}$ Output Current Drive | | | 6 | mA | |
| POWER SUPPLY OUTPUTS | | | | | |
| $V_{INTA}$ | 2.3 | | 2.70 | V | |
| $V_{INTD}$ | 2.3 | | 2.70 | V | |
| $V_{INTA}$ Power Supply Rejection | | 60 | | dB | |
| $V_{INTD}$ Power Supply Rejection | | 50 | | dB | |
| POWER SUPPLY CURRENTS | | | | | |
| Current in Normal Mode (PSM0) | | 4.4 | 5.3 | mA | $f_{CORE}$ = 4.096 MHz, LCD and meter active |
| | | 2.2 | | mA | $f_{CORE}$ = 1.024 MHz, LCD and meter active |
| | | 1.6 | | mA | $f_{CORE}$ = 32.768 kHz, LCD and meter active |
| | | 3 | 3.9 | mA | $f_{CORE}$ = 4.096 MHz; metering ADC and DSP, powered down |
| Current in Battery Mode (PSM1) | | 3.3 | 5.05 | mA | $f_{CORE}$ = 4.096 MHz, LCD active, $V_{BAT}$ = 3.7 V |
| | | 1 | | mA | $f_{CORE}$ = 1.024 MHz, LCD active |
| Current in Sleep Mode (PSM2) | | 38 | | µA | LCD active with charge pump at 3.3 V + RTC, $V_{BAT}$ = 3.3 V |
| | | 1.7 | | µA | RTC only, $T_A$ = 25°C, $V_{BAT}$ = 3.3 V |

[1] Specifications guaranteed by design.
[2] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[3] Retention lifetime equivalent at junction temperature ($T_J$) = 85°C as per JEDEC Standard 22 Method A117. Retention lifetime derates with junction temperature.
[4] Recommended crystal specifications.
[5] Test carried out with all the I/Os set to a low output level.
[6] Delay between power supply valid and execution of first instruction by 8052 core.

## TIMING SPECIFICATIONS

AC inputs during testing were driven at $V_{SWOUT}$ − 0.5 V for Logic 1 and at 0.45 V for Logic 0. Timing measurements were made at $V_{IH}$ minimum for Logic 1 and at $V_{IL}$ maximum for Logic 0, as shown in Figure 3.

For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded $V_{OH}/V_{OL}$ level occurs, as shown in Figure 3.

$C_{LOAD}$ = 80 pF for all outputs, unless otherwise noted. $V_{DD}$ = 2.7 V to 3.6 V; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

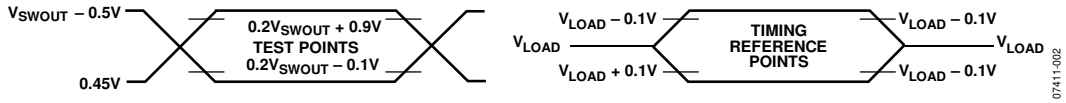


*Figure 3. Timing Waveform Characteristics*

**Table 5. Clock Input (External Clock Driven XTAL1) Parameters**

| | | 32.768 kHz External Crystal | | | |
|---|---|---|---|---|---|
| **Parameter** | **Description** | **Min** | **Typ** | **Max** | **Unit** |
| $t_{CK}$ | XTAL1 period | | 30.52 | | µs |
| $t_{CKL}$ | XTAL1 width low | | 6.26 | | µs |
| $t_{CKH}$ | XTAL1 width high | | 6.26 | | µs |
| $t_{CKR}$ | XTAL1 rise time | | 9 | | ns |
| $t_{CKF}$ | XTAL1 fall time | | 9 | | ns |
| $1/t_{CORE}$ | Core clock frequency[1] | | 1.024 | | MHz |

[1] The ADE5166/ADE5169/ADE5566/ADE5569 internal PLL locks onto a multiple (512×) of the 32.768 kHz external crystal frequency to provide a stable 4.096 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple defined by the CD bits of the POWCON SFR, Address 0xC5[2:0] (see Table 26).

**Table 6. I²C-Compatible Interface Timing Parameters (400 kHz)**

| **Parameter** | **Description** | **Typ** | **Unit** |
|---|---|---|---|
| $t_{BUF}$ | Bus-free time between stop condition and start condition | 1.3 | µs |
| $t_L$ | SCLK low pulse width | 1.36 | µs |
| $t_H$ | SCLK high pulse width | 1.14 | µs |
| $t_{SHD}$ | Start condition hold time | 251.35 | µs |
| $t_{DSU}$ | Data setup time | 740 | ns |
| $t_{DHD}$ | Data hold time | 400 | ns |
| $t_{RSU}$ | Setup time for repeated start | 12.5 | ns |
| $t_{PSU}$ | Stop condition setup time | 400 | ns |
| $t_R$ | Rise time of both SCLK and SDATA | 200 | ns |
| $t_F$ | Fall time of both SCLK and SDATA | 300 | ns |
| $t_{SUP}$[1] | Pulse width of spike suppressed | 50 | ns |

[1] Input filtering on both the SCLK and SDATA suppresses noise spikes of <50 ns.

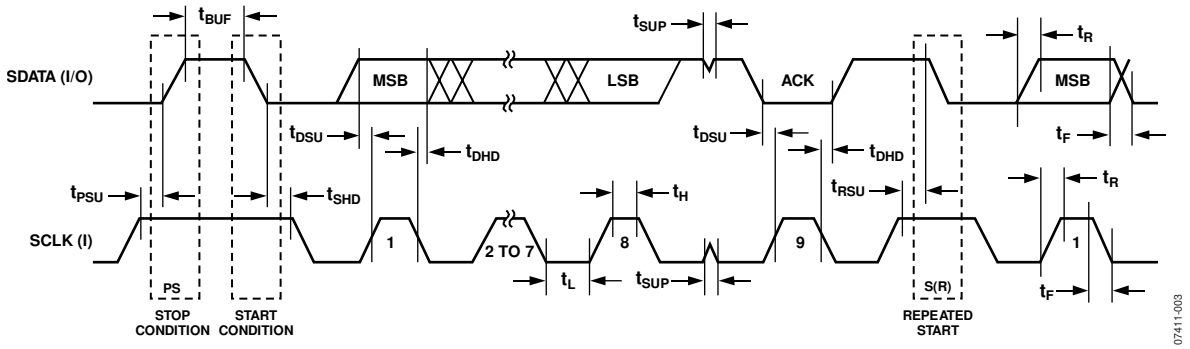


*Figure 4. I²C-Compatible Interface Timing*

**Table 7. SPI Master Mode Timing Parameters (SPICPHA = 1)**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SL}$ | SCLK low pulse width | $2^{SPIR} \times t_{CORE}$[1] | | | ns |
| $t_{SH}$ | SCLK high pulse width | $2^{SPIR} \times t_{CORE}$[1] | | | ns |
| $t_{DAV}$ | Data output valid after SCLK edge | | | $3 \times t_{CORE}$[1] | ns |
| $t_{DSU}$ | Data input setup time before SCLK edge | 0 | | | ns |
| $t_{DHD}$ | Data input hold time after SCLK edge | $t_{CORE}$[1] | | | ns |
| $t_{DF}$ | Data output fall time | | 19 | | ns |
| $t_{DR}$ | Data output rise time | | 19 | | ns |
| $t_{SR}$ | SCLK rise time | | 19 | | ns |
| $t_{SF}$ | SCLK fall time | | 19 | | ns |

[1] $t_{CORE}$ depends on the clock divider or the CD bits of the POWCON SFR, Address 0xC5[2:0] (see Table 26); $t_{CORE} = 2^{CD}/4.096$ MHz.

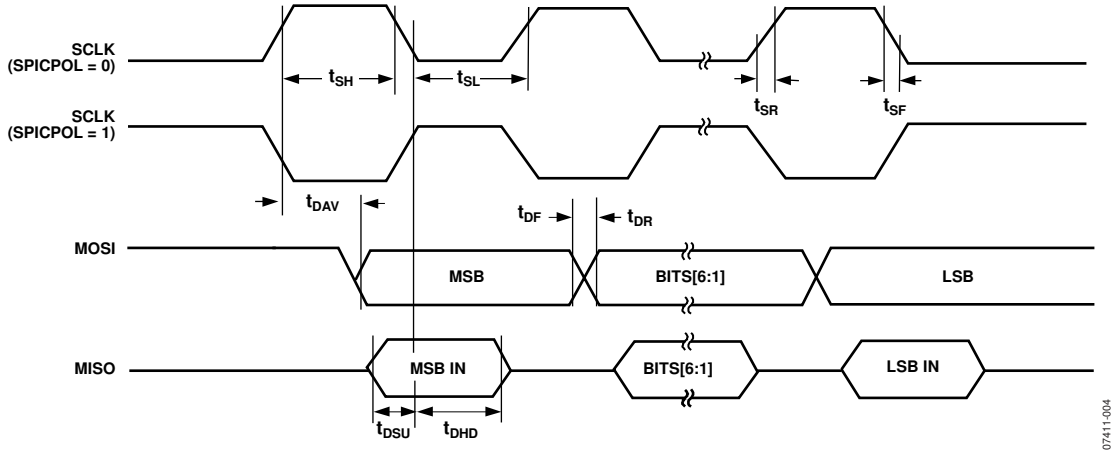


*Figure 5. SPI Master Mode Timing (SPICPHA = 1)*

**Table 8. SPI Master Mode Timing Parameters (SPICPHA = 0)**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{SL}$ | SCLK low pulse width | $2^{SPIR} \times t_{CORE}$[1] | (SPIR + 1) × $t_{CORE}$[1] | | ns |
| $t_{SH}$ | SCLK high pulse width | $2^{SPIR} \times t_{CORE}$[1] | (SPIR + 1) × $t_{CORE}$[1] | | ns |
| $t_{DAV}$ | Data output valid after SCLK edge | | | 3 × $t_{CORE}$[1] | ns |
| $t_{DOSU}$ | Data output setup before SCLK edge | | | 75 | ns |
| $t_{DSU}$ | Data input setup time before SCLK edge | 0 | | | ns |
| $t_{DHD}$ | Data input hold time after SCLK edge | $t_{CORE}$[1] | | | ns |
| $t_{DF}$ | Data output fall time | | 19 | | ns |
| $t_{DR}$ | Data output rise time | | 19 | | ns |
| $t_{SR}$ | SCLK rise time | | 19 | | ns |
| $t_{SF}$ | SCLK fall time | | 19 | | ns |

[1] $t_{CORE}$ depends on the clock divider or the CD bits of the POWCON SFR, Address 0xC5[2:0] (see Table 26); $t_{CORE} = 2^{CD}/4.096$ MHz.

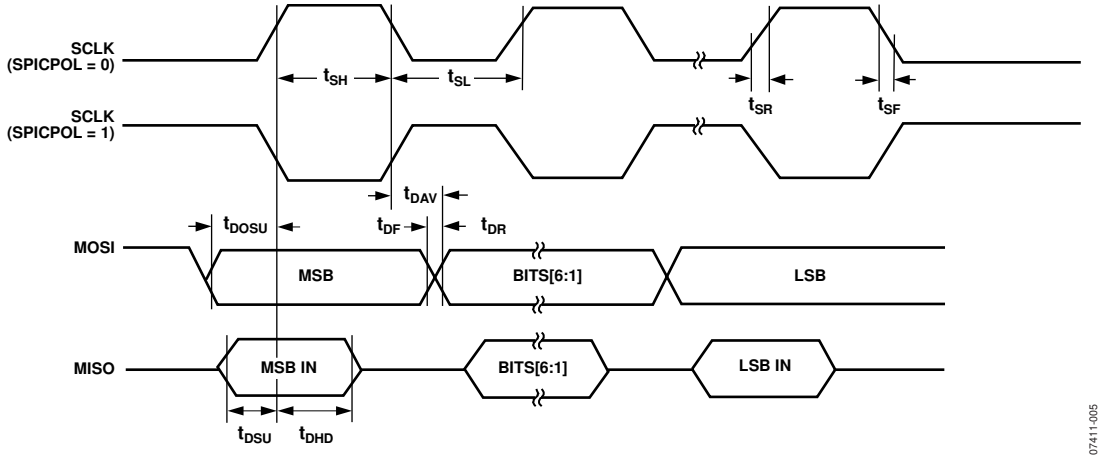


*Figure 6. SPI Master Mode Timing (SPICPHA = 0)*

**Table 9. SPI Slave Mode Timing Parameters (SPICPHA = 1)**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{\overline{SS}}$ | $\overline{SS}$ to SCLK edge | 145 | | | ns |
| $t_{SL}$ | SCLK low pulse width | $6 \times t_{CORE}$[1] | | | ns |
| $t_{SH}$ | SCLK high pulse width | $6 \times t_{CORE}$[1] | | | ns |
| $t_{DAV}$ | Data output valid after SCLK edge | | | 25 | ns |
| $t_{DSU}$ | Data input setup time before SCLK edge | 0 | | | ns |
| $t_{DHD}$ | Data input hold time after SCLK edge | $2 \times t_{CORE}$[1] + 0.5 | | | µs |
| $t_{DF}$ | Data output fall time | | 19 | | ns |
| $t_{DR}$ | Data output rise time | | 19 | | ns |
| $t_{SR}$ | SCLK rise time | | 19 | | ns |
| $t_{SF}$ | SCLK fall time | | 19 | | ns |
| $t_{SFS}$ | $\overline{SS}$ high after SCLK edge | 0 | | | ns |

[1] $t_{CORE}$ depends on the clock divider or the CD bits of the POWCON SFR, Address 0xC5[2:0] (see Table 26); $t_{CORE} = 2^{CD}/4.096$ MHz.

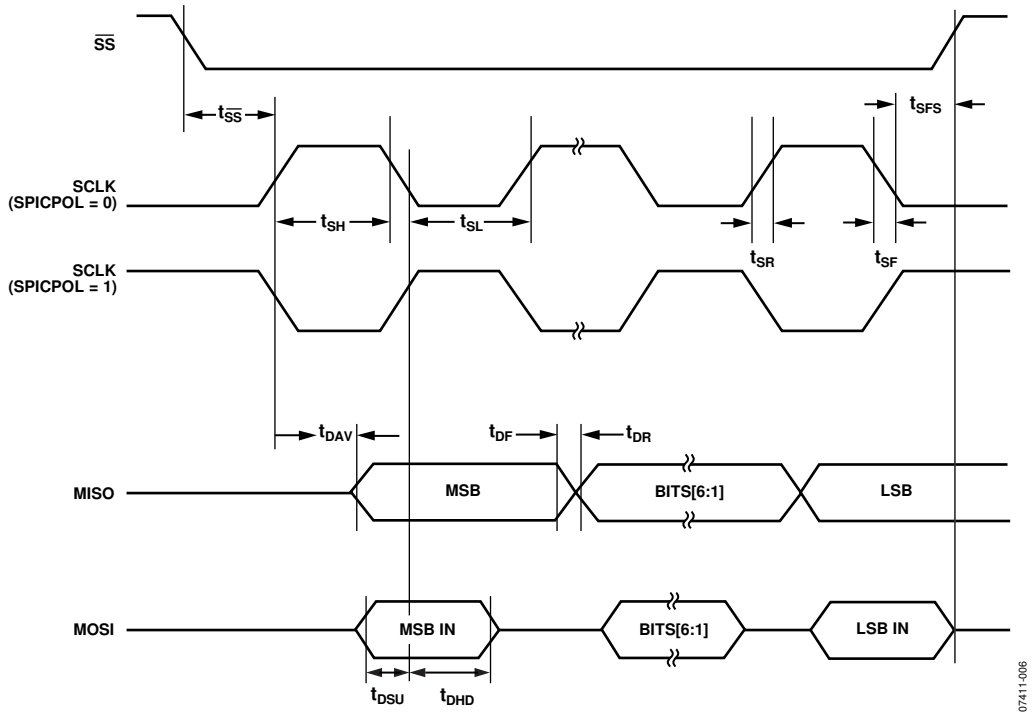


*Figure 7. SPI Slave Mode Timing (SPICPHA = 1)*

**Table 10. SPI Slave Mode Timing Parameters (SPICPHA = 0)**

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{\overline{SS}}$ | $\overline{SS}$ to SCLK edge | 145 | | | ns |
| $t_{SL}$ | SCLK low pulse width | $6 \times t_{CORE}$[1] | | | ns |
| $t_{SH}$ | SCLK high pulse width | $6 \times t_{CORE}$[1] | | | ns |
| $t_{DAV}$ | Data output valid after SCLK edge | | | 25 | ns |
| $t_{DSU}$ | Data input setup time before SCLK edge | 0 | | | ns |
| $t_{DHD}$ | Data input hold time after SCLK edge | $2 \times t_{CORE}$[1] + 0.5 | | | µs |
| $t_{DF}$ | Data output fall time | | 19 | | ns |
| $t_{DR}$ | Data output rise time | | 19 | | ns |
| $t_{SR}$ | SCLK rise time | | 19 | | ns |
| $t_{SF}$ | SCLK fall time | | 19 | | ns |
| $t_{DOSS}$ | Data output valid after $\overline{SS}$ edge | 0 | | | ns |
| $t_{SFS}$ | $\overline{SS}$ high after SCLK edge | 0 | | | ns |

[1] $t_{CORE}$ depends on the clock divider or the CD bits of the POWCON SFR, Address 0xC5[2:0] (see Table 26); $t_{CORE} = 2^{CD}/4.096$ MHz.

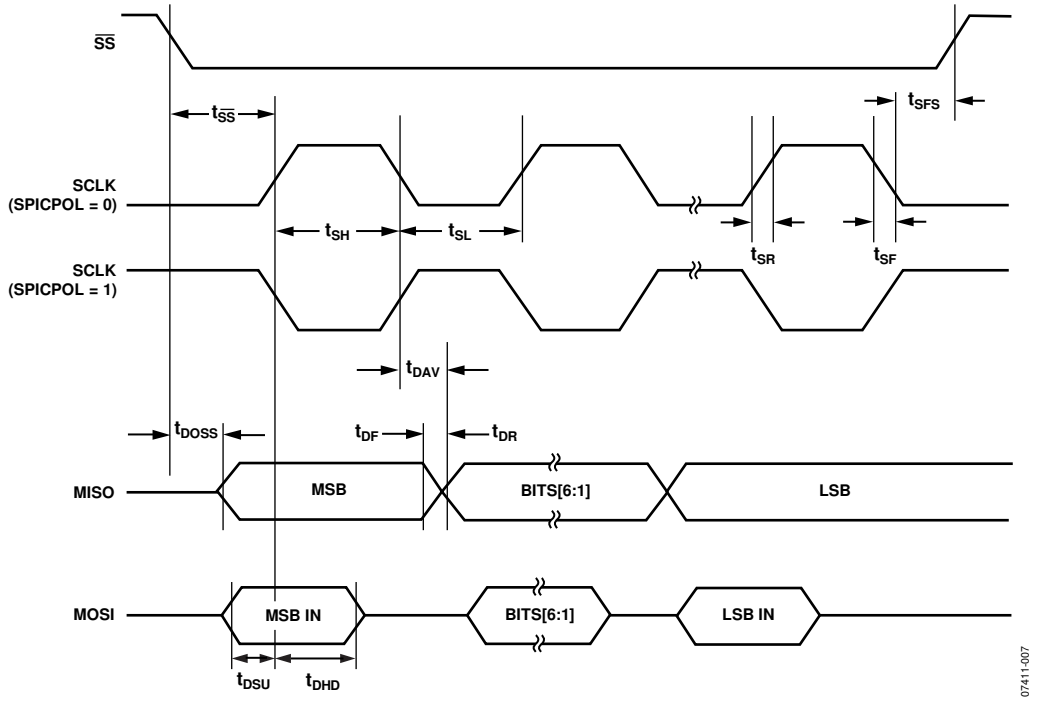


*Figure 8. SPI Slave Mode Timing (SPICPHA = 0)*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 11.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to DGND | −0.3 V to +3.7 V |
| $V_{BAT}$ to DGND | −0.3 V to +3.7 V |
| $V_{DCIN}$ to DGND | −0.3 V to $V_{SWOUT}$ + 0.3 V |
| Input LCD Voltage to AGND, LCDVA, LCDVB, LCDVC[1] | −0.3 V to $V_{SWOUT}$ + 0.3 V |
| Analog Input Voltage to AGND, $V_P$, $V_N$, $I_P$/$I_{PA}$, $I_{PB}$, and $I_N$ | −2 V to +2 V |
| Digital Input Voltage to DGND | −0.3 V to $V_{SWOUT}$ + 0.3 V |
| Digital Output Voltage to DGND | −0.3 V to $V_{SWOUT}$ + 0.3 V |
| Operating Temperature Range (Industrial) | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| 64-Lead LQFP, Power Dissipation | |
| Lead Temperature (Soldering, 30 sec) | 300°C |

[1] When used with external resistor divider.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified for the worst-case condition, that is, a device soldered in a circuit board for surface-mount packages.

**Table 12. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 64-Lead LQFP | 60 | 20.5 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

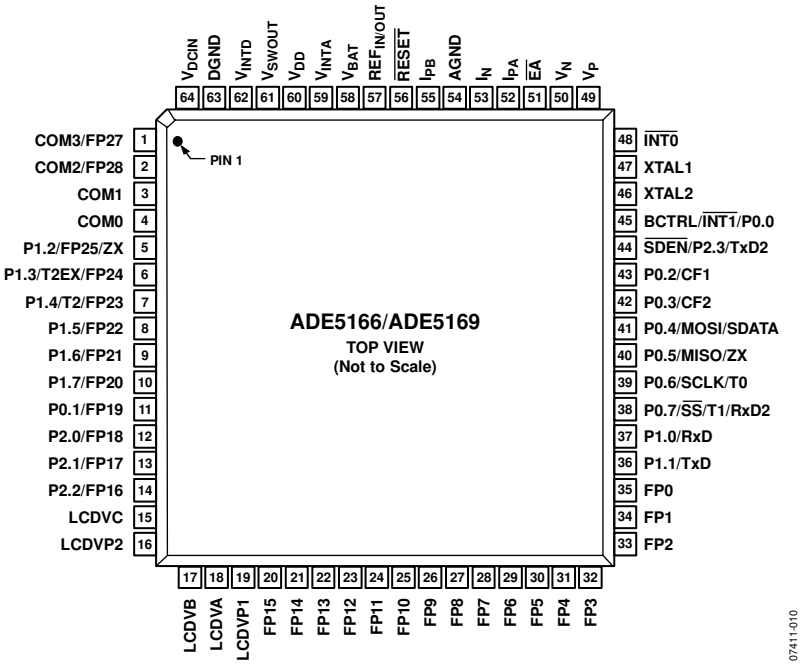


*Figure 9. ADE5166/ADE5169 Pin Configuration*

**Table 13. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | COM3/FP27 | Common Output 3/LCD Segment Output 27. COM3 is used for the LCD backplane. |
| 2 | COM2/FP28 | Common Output 2/LCD Segment Output 28. COM2 is used for the LCD backplane. |
| 3 | COM1 | Common Output 1. COM1 is used for the LCD backplane. |
| 4 | COM0 | Common Output 0. COM0 is used for the LCD backplane. |
| 5 | P1.2/FP25/ZX | General-Purpose Digital I/O Port 1.2/LCD Segment Output 25/ZX Output. |
| 6 | P1.3/T2EX/FP24 | General-Purpose Digital I/O Port 1.3/Timer 2 Control Input/LCD Segment Output 24. |
| 7 | P1.4/T2/FP23 | General-Purpose Digital I/O Port 1.4/Timer 2 Input/LCD Segment Output 23. |
| 8 | P1.5/FP22 | General-Purpose Digital I/O Port 1.5/LCD Segment Output 22. |
| 9 | P1.6/FP21 | General-Purpose Digital I/O Port 1.6/LCD Segment Output 21. |
| 10 | P1.7/FP20 | General-Purpose Digital I/O Port 1.7/LCD Segment Output 20. |
| 11 | P0.1/FP19 | General-Purpose Digital I/O Port 0.1/LCD Segment Output 19. |
| 12 | P2.0/FP18 | General-Purpose Digital I/O Port 2.0/LCD Segment Output 18. |
| 13 | P2.1/FP17 | General-Purpose Digital I/O Port 2.1/LCD Segment Output 17. |
| 14 | P2.2/FP16 | General-Purpose Digital I/O Port 2.2/LCD Segment Output 16. |
| 15 | LCDVC | Output Port for LCD Levels. This pin should be decoupled with a 470 nF capacitor. |
| 16 | LCDVP2 | Analog Output. A 100 nF capacitor should be connected between this pin and LCDVP1 for the internal LCD charge pump device. |
| 17, 18 | LCDVB, LCDVA | Output Ports for LCD Levels. These pins should be decoupled with a 470 nF capacitor. |
| 19 | LCDVP1 | Analog Output. A 100 nF capacitor should be connected between this pin and LCDVP2 for the internal LCD charge pump device. |
| 20 to 35 | FP15 to FP0 | LCD Segment Output 15 to LCD Segment Output 0. |
| 36 | P1.1/TxD | General-Purpose Digital I/O Port 1.1/Transmitter Data Output (Asynchronous). |
| 37 | P1.0/RxD | General-Purpose Digital I/O Port 1.0/Receive Data Input (Asynchronous). |
| 38 | P0.7/SS/T1/RxD2 | General-Purpose Digital I/O Port 0.7/Slave Select When SPI Is in Slave Mode/Timer 1 Input/Receive Data Input 2 (Asynchronous). |
| 39 | P0.6/SCLK/T0 | General-Purpose Digital I/O Port 0.6/Clock Output for I²C or SPI Port/Timer 0 Input. |
| 40 | P0.5/MISO/ZX | General-Purpose Digital I/O Port 0.5/Data Input for SPI Port/ZX Output. |
| 41 | P0.4/MOSI/SDATA | General-Purpose Digital I/O Port 0.4/Data Output for SPI Port/I²C-Compatible Data Line. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 42 | P0.3/CF2 | General-Purpose Digital I/O Port 0.3/Calibration Frequency Logic Output 2. The CF2 logic output gives instantaneous active, reactive, or apparent power or $I_{rms}$ information. |
| 43 | P0.2/CF1 | General-Purpose Digital I/O Port 0.2/Calibration Frequency Logic Output 1. The CF1 logic output gives instantaneous active, reactive, or apparent power or $I_{rms}$ information. |
| 44 | $\overline{\text{SDEN}}$/P2.3/TxD2 | Serial Download Mode Enable/General-Purpose Digital Output Port 2.3/Transmitter Data Output 2 (Asynchronous). This pin is used to enable serial download mode through a resistor when pulled low on power-up or reset. On reset, this pin momentarily becomes an input, and the status of the pin is sampled. If there is no pull-down resistor in place, the pin momentarily goes high, and then user code is executed. If the pin is pulled down on reset, the embedded serial download/debug kernel executes, and this pin remains low during the internal program execution. After reset, this pin can be used as a digital output port pin (P2.3) or as Transmitter Data Output 2 (asynchronous). |
| 45 | BCTRL/$\overline{\text{INT1}}$/P0.0 | Digital Input for Battery Control/External Interrupt Input 1/General-Purpose Digital I/O Port 0.0. This logic input connects $V_{DD}$ or $V_{BAT}$ to $V_{SWOUT}$ internally when set to logic high or logic low, respectively. When left open, the connection between $V_{DD}$ or $V_{BAT}$ and $V_{SWOUT}$ is selected internally. |
| 46 | XTAL2 | A crystal can be connected across this pin and XTAL1 (see the XTAL1 pin description) to provide a clock source. The XTAL2 pin can drive one CMOS load when an external clock is supplied at XTAL1 or by the gate oscillator circuit. An internal 6 pF capacitor is connected to this pin. |
| 47 | XTAL1 | An external clock can be provided at this logic input. Alternatively, a tuning fork crystal can be connected across XTAL1 and XTAL2 to provide a clock source. The clock frequency for specified operation is 32.768 kHz. An internal 6 pF capacitor is connected to this pin. |
| 48 | $\overline{\text{INT0}}$ | External Interrupt Input 0. |
| 49, 50 | $V_P$, $V_N$ | Analog Inputs for Voltage Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±500 mV for specified operation. This channel also has an internal PGA. |
| 51 | $\overline{\text{EA}}$ | Input for Emulation. When held high, this input enables the device to fetch code from internal program memory locations. The ADE5166/ADE5169 do not support external code memory. This pin should not be left floating. |
| 52, 53 | $I_{PA}$, $I_N$ | Analog Inputs for Current Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±500 mV for specified operation. This channel also has an internal PGA. |
| 54 | AGND | Ground Reference for Analog Circuitry. |
| 55 | $I_{PB}$ | Analog Input for Second Current Channel. This input is fully differential with a maximum differential level of ±500 mV, referred to $I_N$ for specified operation. This channel also has an internal PGA. |
| 56 | $\overline{\text{RESET}}$ | Reset Input, Active Low. |
| 57 | $REF_{IN/OUT}$ | Access to On-Chip Voltage Reference. The on-chip reference has a nominal value of 1.2 V ± 0.1% and a typical temperature coefficient of 50 ppm/°C maximum. This pin should be decoupled with a 1 µF capacitor in parallel with a ceramic 100 nF capacitor. |
| 58 | $V_{BAT}$ | Power Supply Input from the Battery with a 2.4 V to 3.7 V Range. This pin is connected internally to $V_{DD}$ when the battery is selected as the power supply. |
| 59 | $V_{INTA}$ | Access to On-Chip 2.5 V Analog LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. |
| 60 | $V_{DD}$ | 3.3 V Power Supply Input from the Regulator. This pin is connected internally to $V_{SWOUT}$ when the regulator is selected as the power supply. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. |
| 61 | $V_{SWOUT}$ | 3.3 V Power Supply Output. This pin provides the supply voltage for the LDOs and the internal circuitry. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. |
| 62 | $V_{INTD}$ | Access to On-Chip 2.5 V Digital LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. |
| 63 | DGND | Ground Reference for Digital Circuitry. |
| 64 | $V_{DCIN}$ | Analog Input for DC Voltage Monitoring. The maximum input voltage on this pin is $V_{SWOUT}$ with respect to AGND. This pin is used to monitor the preregulated dc voltage. |

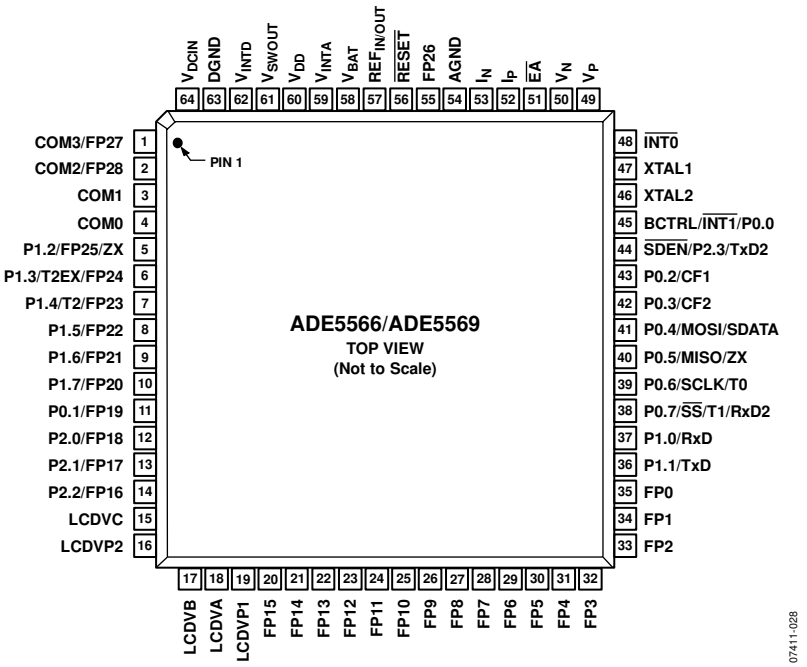


*Figure 10. ADE5566/ADE5569 Pin Configuration*

**Table 14. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | COM3/FP27 | Common Output 3/LCD Segment Output 27. COM3 is used for the LCD backplane. |
| 2 | COM2/FP28 | Common Output 2/LCD Segment Output 28. COM2 is used for the LCD backplane. |
| 3 | COM1 | Common Output 1. COM1 is used for the LCD backplane. |
| 4 | COM0 | Common Output 0. COM0 is used for the LCD backplane. |
| 5 | P1.2/FP25/ZX | General-Purpose Digital I/O Port 1.2/LCD Segment Output 25/ZX Output. |
| 6 | P1.3/T2EX/FP24 | General-Purpose Digital I/O Port 1.3/Timer 2 Control Input/LCD Segment Output 24. |
| 7 | P1.4/T2/FP23 | General-Purpose Digital I/O Port 1.4/Timer 2 Input/LCD Segment Output 23. |
| 8 | P1.5/FP22 | General-Purpose Digital I/O Port 1.5/LCD Segment Output 22. |
| 9 | P1.6/FP21 | General-Purpose Digital I/O Port 1.6/LCD Segment Output 21. |
| 10 | P1.7/FP20 | General-Purpose Digital I/O Port 1.7/LCD Segment Output 20. |
| 11 | P0.1/FP19 | General-Purpose Digital I/O Port 0.1/LCD Segment Output 19. |
| 12 | P2.0/FP18 | General-Purpose Digital I/O Port 2.0/LCD Segment Output 18. |
| 13 | P2.1/FP17 | General-Purpose Digital I/O Port 2.1/LCD Segment Output 17. |
| 14 | P2.2/FP16 | General-Purpose Digital I/O Port 2.2/LCD Segment Output 16. |
| 15 | LCDVC | Output Port for LCD Levels. This pin should be decoupled with a 470 nF capacitor. |
| 16 | LCDVP2 | Analog Output. A 100 nF capacitor should be connected between this pin and LCDVP1 for the internal LCD charge pump device. |
| 17, 18 | LCDVB, LCDVA | Output Ports for LCD Levels. These pins should be decoupled with a 470 nF capacitor. |
| 19 | LCDVP1 | Analog Output. A 100 nF capacitor should be connected between this pin and LCDVP2 for the internal LCD charge pump device. |
| 20 to 35 | FP15 to FP0 | LCD Segment Output 15 to LCD Segment Output 0. |
| 36 | P1.1/TxD | General-Purpose Digital I/O Port 1.1/Transmitter Data Output (Asynchronous). |
| 37 | P1.0/RxD | General-Purpose Digital I/O Port 1.0/Receive Data Input (Asynchronous). |
| 38 | P0.7/$\overline{SS}$/T1/RxD2 | General-Purpose Digital I/O Port 0.7/Slave Select When SPI Is in Slave Mode/Timer 1 Input/Receive Data Input 2 (Asynchronous). |
| 39 | P0.6/SCLK/T0 | General-Purpose Digital I/O Port 0.6/Clock Output for $I^2C$ or SPI Port/Timer 0 Input. |
| 40 | P0.5/MISO/ZX | General-Purpose Digital I/O Port 0.5/Data Input for SPI Port/ZX Output. |
| 41 | P0.4/MOSI/SDATA | General-Purpose Digital I/O Port 0.4/Data Output for SPI Port/$I^2C$-Compatible Data Line. |
| 42 | P0.3/CF2 | General-Purpose Digital I/O Port 0.3/Calibration Frequency Logic Output 2. The CF2 logic output gives instantaneous active, reactive, or apparent power or $I_{rms}$ information. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 43 | P0.2/CF1 | General-Purpose Digital I/O Port 0.2/Calibration Frequency Logic Output 1. The CF1 logic output gives instantaneous active, reactive, or apparent power or $I_{rms}$ information. |
| 44 | $\overline{SDEN}$/P2.3/TxD2 | Serial Download Mode Enable/General-Purpose Digital Output Port 2.3/Transmitter Data Output 2 (Asynchronous). This pin is used to enable serial download mode through a resistor when pulled low on power-up or reset. On reset, this pin momentarily becomes an input, and the status of the pin is sampled. If there is no pull-down resistor in place, the pin momentarily goes high, and then user code is executed. If the pin is pulled down on reset, the embedded serial download/debug kernel executes, and this pin remains low during the internal program execution. After reset, this pin can be used as a digital output port pin (P2.3) or as Transmitter Data Output 2 (asynchronous). |
| 45 | BCTRL/$\overline{INT1}$/P0.0 | Digital Input for Battery Control/External Interrupt Input 1/General-Purpose Digital I/O Port 0.0. This logic input connects $V_{DD}$ or $V_{BAT}$ to $V_{SWOUT}$ internally when set to logic high or logic low, respectively. When left open, the connection between $V_{DD}$ or $V_{BAT}$ and $V_{SWOUT}$ is selected internally. |
| 46 | XTAL2 | A crystal can be connected across this pin and XTAL1 (see the XTAL1 pin description) to provide a clock source. The XTAL2 pin can drive one CMOS load when an external clock is supplied at XTAL1 or by the gate oscillator circuit. An internal 6 pF capacitor is connected to this pin. |
| 47 | XTAL1 | An external clock can be provided at this logic input. Alternatively, a tuning fork crystal can be connected across XTAL1 and XTAL2 to provide a clock source. The clock frequency for specified operation is 32.768 kHz. An internal 6 pF capacitor is connected to this pin. |
| 48 | $\overline{INT0}$ | External Interrupt Input 0. |
| 49, 50 | $V_P$, $V_N$ | Analog Inputs for Voltage Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±500 mV for specified operation. This channel also has an internal PGA. |
| 51 | $\overline{EA}$ | Input for Emulation. When held high, this input enables the device to fetch code from internal program memory locations. The ADE5566/ADE5569 do not support external code memory. This pin should not be left floating. |
| 52, 53 | $I_P$, $I_N$ | Analog Inputs for Current Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±500 mV for specified operation. This channel also has an internal PGA. |
| 54 | AGND | Ground Reference for Analog Circuitry. |
| 55 | FP26 | LCD Segment Output 26. |
| 56 | $\overline{RESET}$ | Reset Input, Active Low. |
| 57 | $REF_{IN/OUT}$ | Access to On-Chip Voltage Reference. The on-chip reference has a nominal value of 1.2 V ± 0.1% and a typical temperature coefficient of 50 ppm/°C maximum. This pin should be decoupled with a 1 µF capacitor in parallel with a ceramic 100 nF capacitor. |
| 58 | $V_{BAT}$ | Power Supply Input from the Battery with a 2.4 V to 3.7 V Range. This pin is connected internally to $V_{DD}$ when the battery is selected as the power supply. |
| 59 | $V_{INTA}$ | Access to On-Chip 2.5 V Analog LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. |
| 60 | $V_{DD}$ | 3.3 V Power Supply Input from the Regulator. This pin is connected internally to $V_{SWOUT}$ when the regulator is selected as the power supply. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. |
| 61 | $V_{SWOUT}$ | 3.3 V Power Supply Output. This pin provides the supply voltage for the LDOs and the internal circuitry. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. |
| 62 | $V_{INTD}$ | Access to On-Chip 2.5 V Digital LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. |
| 63 | DGND | Ground Reference for Digital Circuitry. |
| 64 | $V_{DCIN}$ | Analog Input for DC Voltage Monitoring. The maximum input voltage on this pin is $V_{SWOUT}$ with respect to AGND. This pin is used to monitor the preregulated dc voltage. |

# TYPICAL PERFORMANCE CHARACTERISTICS

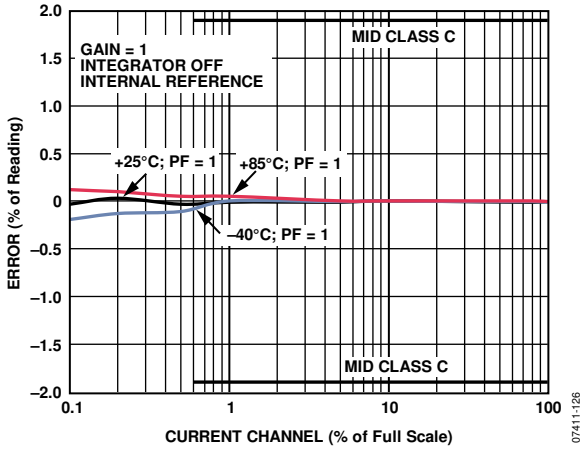


*Figure 11. Active Energy Error as a Percentage of Reading (Gain = 1) over Temperature with Internal Reference, Integrator Off*

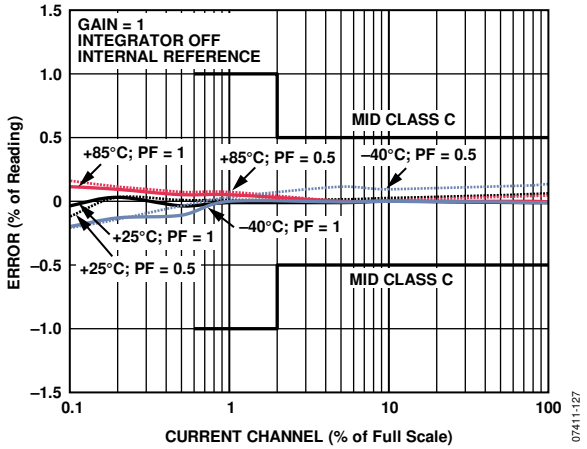


*Figure 12. Active Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference, Integrator Off*

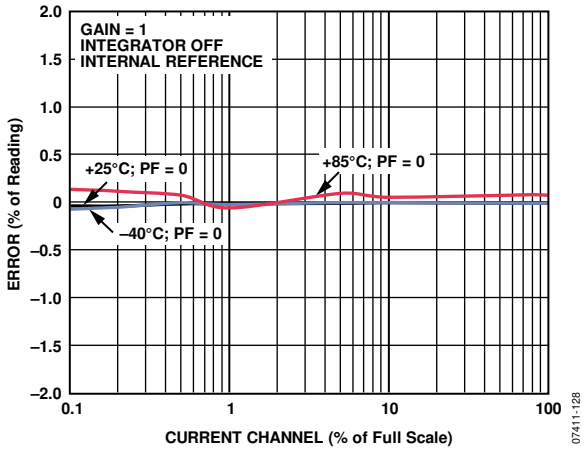


*Figure 13. Reactive Energy Error as a Percentage of Reading (Gain = 1) over Temperature with Internal Reference, Integrator Off*

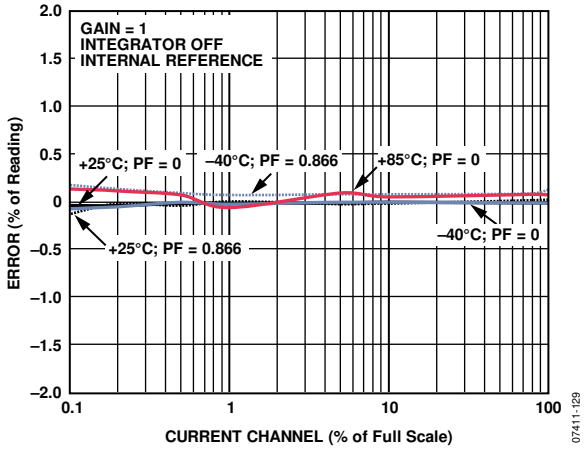


*Figure 14. Reactive Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference, Integrator Off*

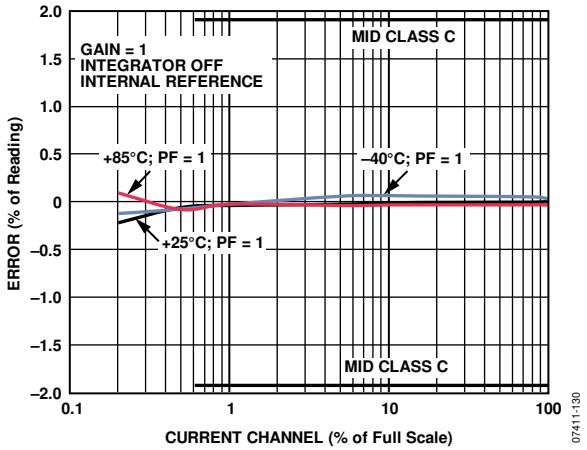


*Figure 15. Current RMS Error as a Percentage of Reading (Gain = 1) over Temperature with Internal Reference, Integrator Off*

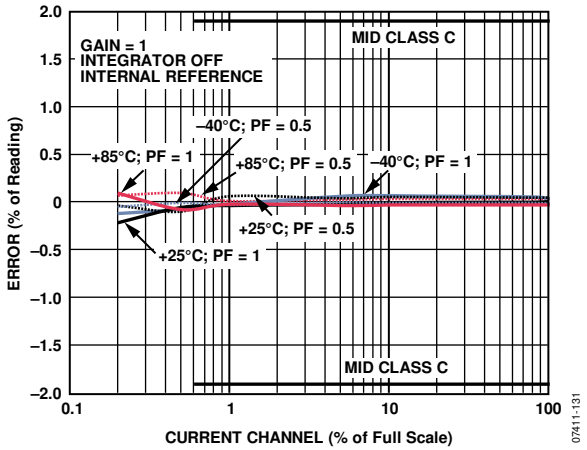


*Figure 16. Current RMS Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference, Integrator Off*

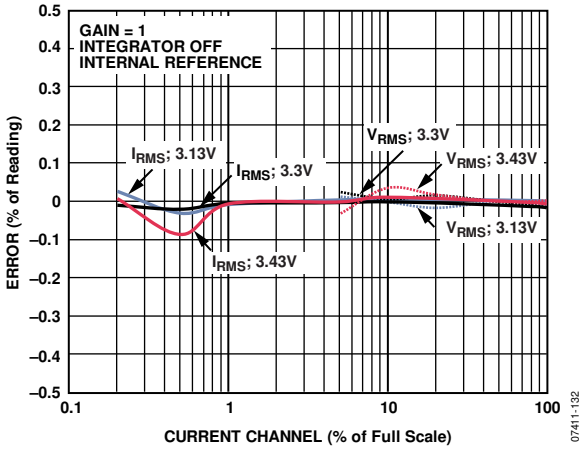


Figure 17. Voltage and Current RMS Error as a Percentage of Reading (Gain = 1) over Power Supply with Internal Reference

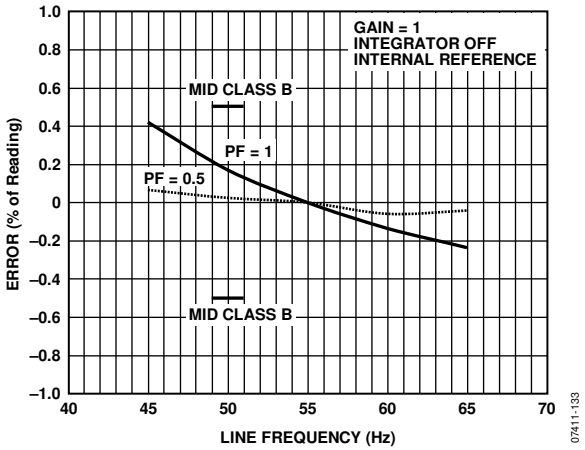


Figure 18. Active Energy Error as a Percentage of Reading (Gain = 1) over Frequency with Internal Reference, Integrator Off

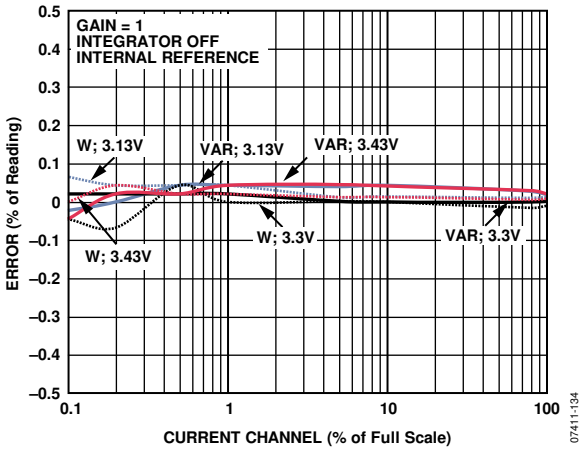


Figure 19. Active and Reactive Energy Error as a Percentage of Reading (Gain = 1) over Power Supply with Internal Reference, Integrator Off

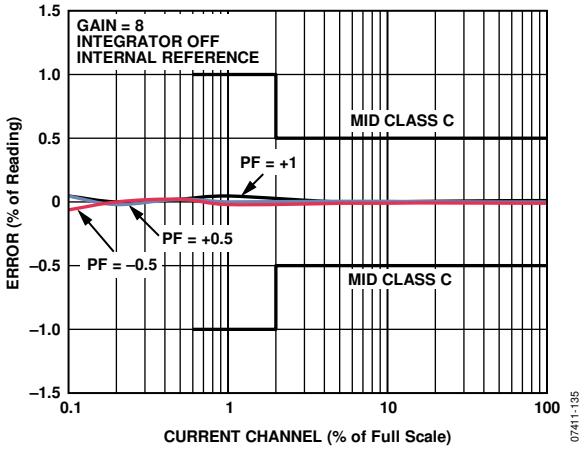


Figure 20. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference, Integrator Off

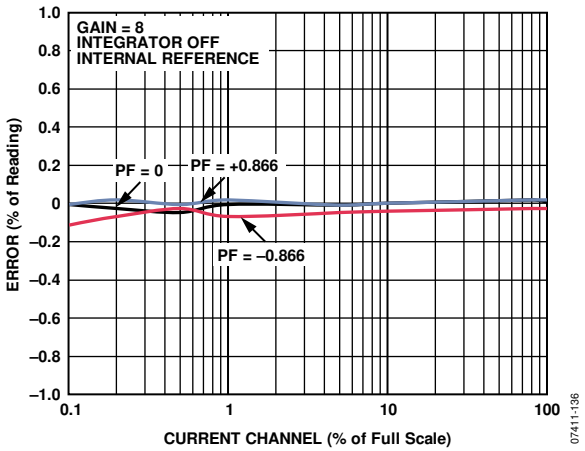


Figure 21. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference, Integrator Off

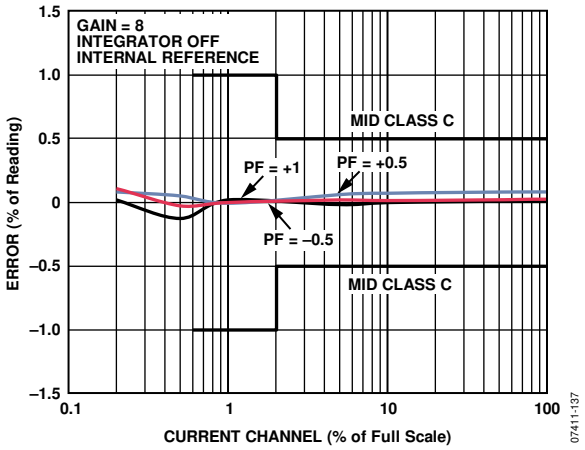


Figure 22. Current RMS Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference, Integrator Off

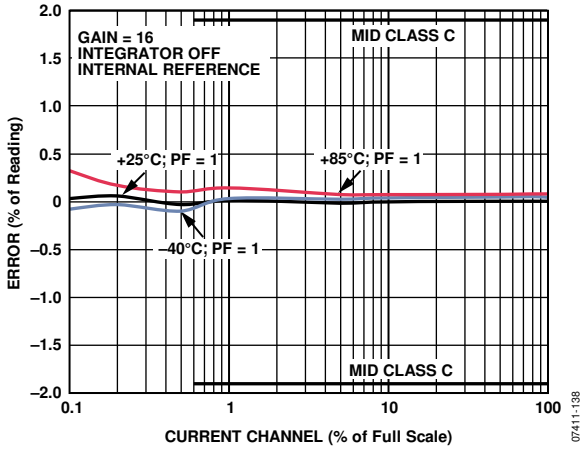


Figure 23. Active Energy Error as a Percentage of Reading (Gain = 16) over Temperature with Internal Reference, Integrator Off

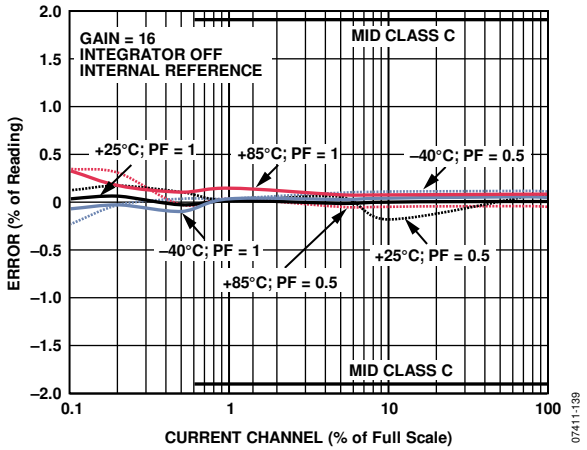


Figure 24. Active Energy Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference, Integrator Off

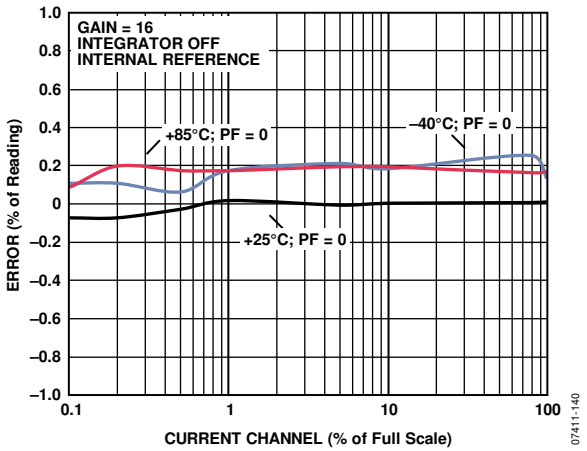


Figure 25. Reactive Energy Error as a Percentage of Reading (Gain = 16) over Temperature with Internal Reference, Integrator Off

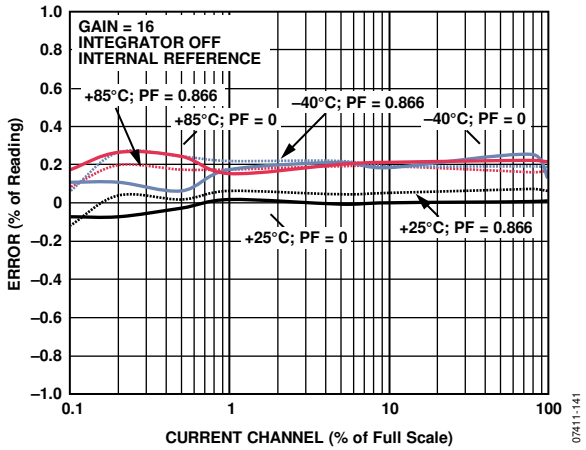


Figure 26. Reactive Energy Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference, Integrator Off

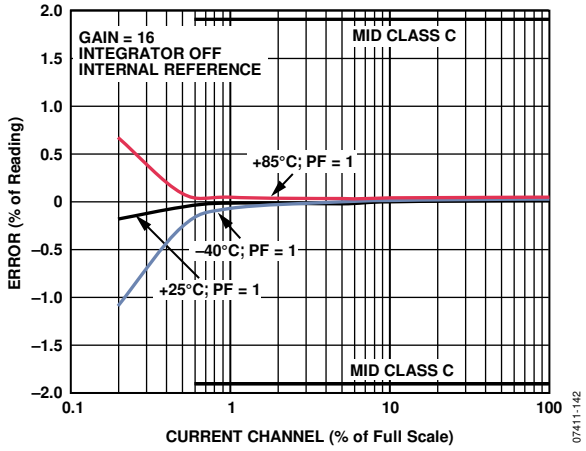


Figure 27. Current RMS Error as a Percentage of Reading (Gain = 16) over Temperature with Internal Reference, Integrator Off

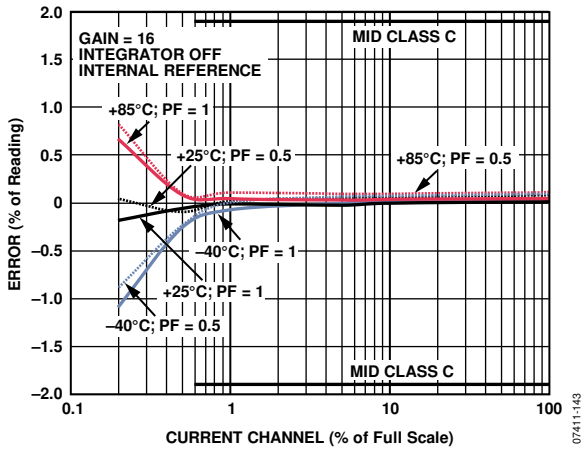


Figure 28. Current RMS Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference, Integrator Off

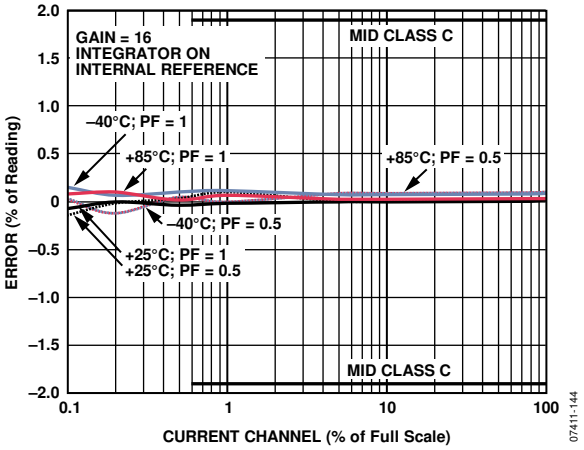


*Figure 29. Active Energy Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference, Integrator On*

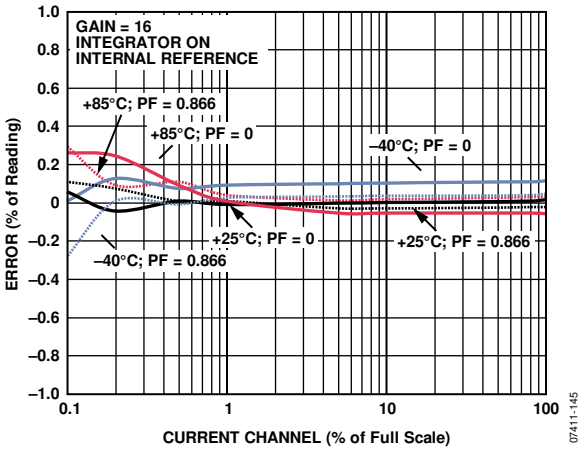


*Figure 30. Reactive Energy Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference, Integrator On*

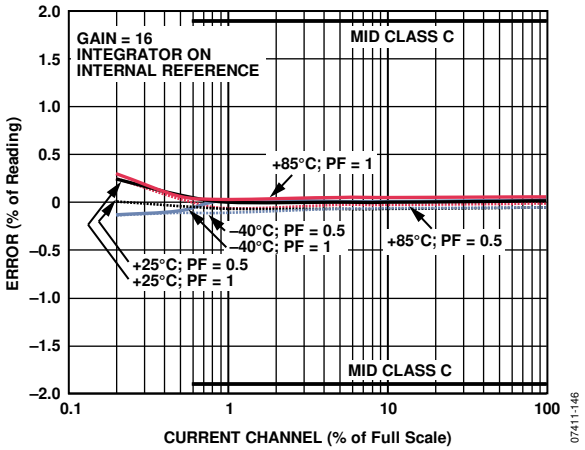


*Figure 31. Current RMS Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference, Integrator On*

# TERMINOLOGY

**Measurement Error**

The error associated with the energy measurement made by the ADE5166/ADE5169/ADE5566/ADE5569 is defined by the following formula:

$$Measurement\ Error = \left( \frac{Energy\ \ Register - True\ \ Energy}{True\ \ Energy} \right) \times 100\%$$

**Phase Error Between Channels**

The digital integrator and the high-pass filter (HPF) in the current channel have a nonideal phase response. To offset this phase response and equalize the phase response between channels, two phase correction networks are placed in the current channel: one for the digital integrator and the other for the HPF. The phase correction networks correct the phase response of the corresponding component and ensure a phase match between the current channel and the voltage channel to within ±0.1° over a range of 45 Hz to 65 Hz with the digital integrator off. With the digital integrator on, the phase is corrected to within ±0.4° over a range of 45 Hz to 65 Hz.

**Power Supply Rejection (PSR)**

PSR quantifies the ADE5166/ADE5169/ADE5566/ADE5569 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (100 mV rms/120 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of the reading (see the Measurement Error definition).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ±5%. Any error introduced is expressed as a percentage of the reading.

**ADC Offset Error**

ADC offset error is the dc offset associated with the analog inputs to the ADCs. It means that, with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection. However, when HPF1 is switched on, the offset is removed from the current channel, and the power calculation is not affected by this offset. The offsets can be removed by performing an offset calibration (see the Analog Inputs section).

**Gain Error**

Gain error is the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC section and the Voltage Channel ADC section). It is measured for each of the gain settings on the current channel (1, 2, 4, 8, and 16). The difference is expressed as a percentage of the ideal code.