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Single-Phase Energy Measurement IC with 8052 MCU, RTC, and LCD Driver

ADE7116/ADE7156/ADE7166/ADE7169/ADE7566/ADE7569

GENERAL FEATURES

- Wide supply voltage operation: 2.4 V to 3.7 V
- Internal bipolar switch between regulated and battery inputs
- Ultralow power operation with power saving modes (PSM)
  - Full operation: 4 mA to 1.6 mA (PLL clock dependent)
  - Battery mode: 3.2 mA to 400 µA (PLL clock dependent)
  - Sleep mode
    - Real-time clock (RTC) mode: 1.5 µA
    - RTC and LCD mode: 38 µA (LCD charge pump enabled)
- Reference: 1.2 V ± 0.1% (10 ppm/°C drift)
- 64-lead RoHS package options
  - Lead frame chip scale package (LFCSP)
  - Low profile quad flat package (LQFP)
- Operating temperature range: −40°C to +85°C

ENERGY MEASUREMENT FEATURES

- Proprietary analog-to-digital converters (ADCs) and digital signal processing (DSP) provide high accuracy active (watt), reactive (var), and apparent energy (volt-ampere (VA)) measurement
  - <0.1% error on active energy over a dynamic range of 1000 to 1 @ 25°C
  - <0.5% error on reactive energy over a dynamic range of 1000 to 1 @ 25°C (ADE7169 and ADE7569 only)
  - <0.5% error on root mean square (rms) measurements over a dynamic range of 500 to 1 for current (I_{rms}) and 100 to 1 for voltage (V_{rms}) @ 25°C
  - Supports IEC 62053-21, IEC 62053-22, and IEC 62053-23; EN 50470-3 Class A, Class B, and Class C; and ANSI C12-16
- Differential input with programmable gain amplifiers (PGAs) supports shunts, current transformers, and di/dt current sensors (ADE7169 and ADE7569 only)
- 2 current inputs for antitamper detection in the ADE7116/ADE7156/ADE7166/ADE7169
- High frequency outputs proportional to I_{rms}, active, reactive, or apparent power (AP)

Table 1. Features Available on Each Part

Feature	Part No.
Antitamper	ADE7116, ADE7156, ADE7166, ADE7169
Watt, VA, I_{rms}, V_{rms}	ADE7116, ADE7156, ADE7166, ADE7169, ADE7566, ADE7569
Var	ADE7169, ADE7569
di/dt Sensor	ADE7169, ADE7569

MICROPROCESSOR FEATURES

- 8052-based core
  - Single-cycle 4 MIPS 8052 core
  - 8052-compatible instruction set
  - 32.768 kHz external crystal with on-chip PLL
  - 2 external interrupt sources
  - External reset pin
- Low power battery mode
  - Wake-up from I/O, temperature change[1], alarm, and universal asynchronous receiver/transmitter (UART)
  - LCD driver operation
  - Temperature measurement
- Real-time clock (RTC)
  - Counter for seconds, minutes, and hours
  - Automatic battery switchover for RTC backup
  - Operation down to 2.4 V
  - Ultralow battery supply current: 1.5 µA
  - Selectable output frequency: 1 Hz to 16 kHz
  - Embedded digital crystal frequency compensation for calibration and temperature variation of 2 ppm resolution
- Integrated LCD driver
  - 108-segment driver for the ADE7566/ADE7569 and 104-segment driver for the ADE7116/ADE7156/ADE7166/ADE7169
  - 2×, 3×, or 4× multiplexing
  - LCD voltages generated internally[2] or with external resistors
  - Internal adjustable drive voltages up to 5 V independent of power supply level[2]
- On-chip peripherals
  - UART interface
  - SPI or I^2C
  - Watchdog timer
- Power supply management with user-selectable levels
- Memory: 16 kB flash memory, 512 bytes RAM
- Development tools
  - Single-pin emulation
  - IDE-based assembly and C-source debugging

[1] Not available in the ADE7116.
[2] Not available in the ADE7116 or ADE7156.

Rev. B

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REVISION HISTORY

11/08—Rev. A to Rev. B

Added ADE7116/ADE7156 ..... Throughout
Changes to Table 1 1
Added Figure 2 5
Changes to Table 13 16
Added Figure 10 and Table 14; Renumbered Sequentially 19
Added Exposed Pad Notation to Outline Dimensions 148
Changes to Ordering Guide 149

12/07—Rev. 0 to Rev. A

Added ADE7166/ADE7169 ..... Universal
Changes to Table 1 1
Changes to Ordering Guide 144

11/07—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADE7116/ADE7156/ADE7166/ADE7169/ADE7566/ADE7569[1] integrate the Analog Devices, Inc., energy (ADE) metering IC analog front end and fixed function DSP solution with an enhanced 8052 MCU core, an RTC, an LCD driver, and all the peripherals to make an electronic energy meter with an LCD display in a single part.

The ADE measurement core includes active, reactive, and apparent energy calculations, as well as voltage and current rms measurements. This information is accessible for energy billing by using the built-in energy scalars. Many power line supervisory features such as SAG, peak, and zero crossing are included in the energy measurement DSP to simplify energy meter design.

The microprocessor functionality includes a single-cycle 8052 core, a real-time clock with a power supply backup pin, an SPI or I²C® interface, and a UART interface. The ready-to-use information from the ADE core reduces the program memory size requirement, making it easy to integrate complicated design into 16 kB of flash memory.

The ADE7116/ADE7156/ADE7166/ADE7169/ADE7566/ADE7569 also include a 108-/104-segment LCD driver. In the ADE7166/ADE7169/ADE7566/ADE7569, this driver generates voltages capable of driving LCDs up to 5 V.

[1] Patents pending.

FUNCTIONAL BLOCK DIAGRAMS

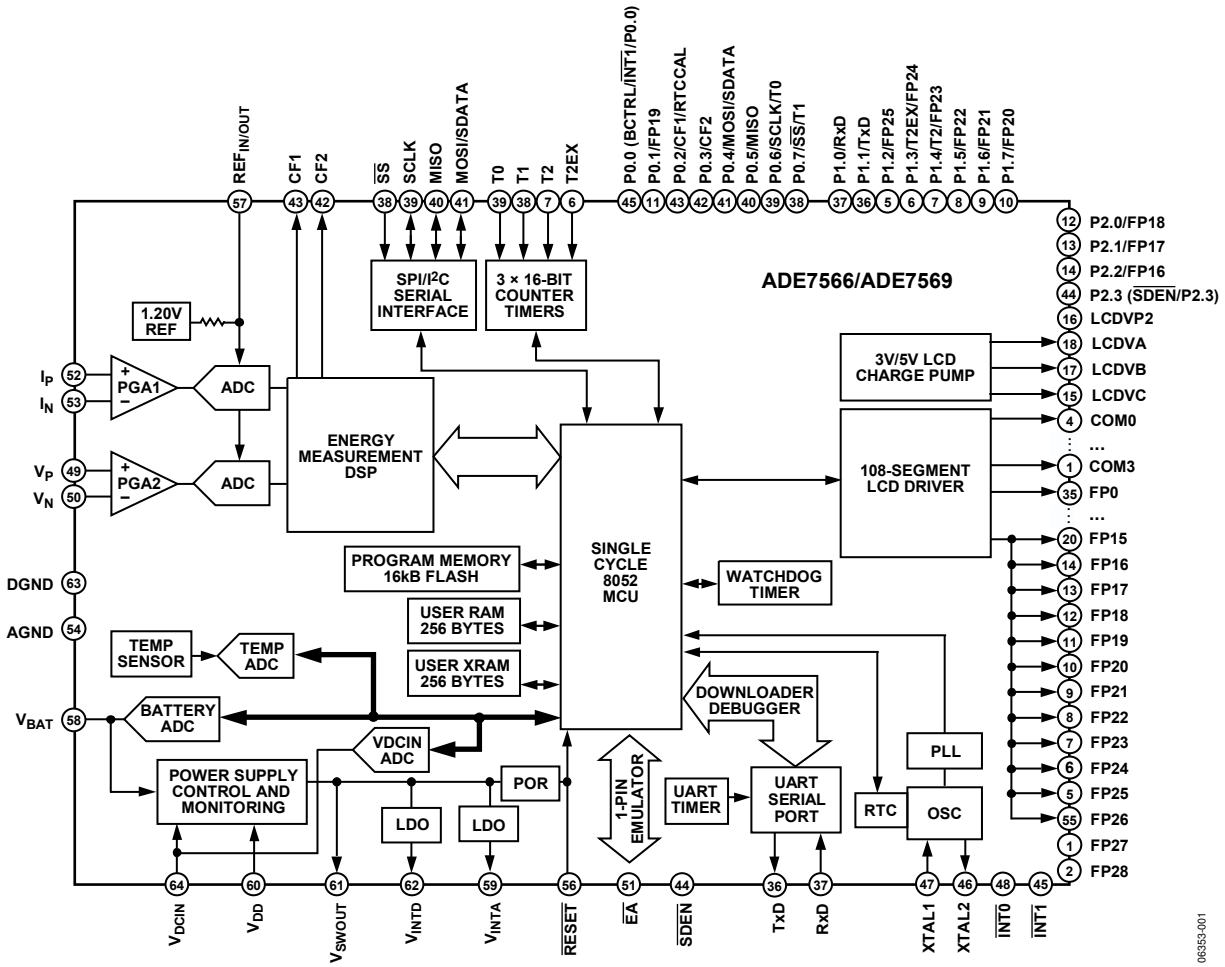

Figure 1. ADE7566/ADE7569 Functional Block Diagram

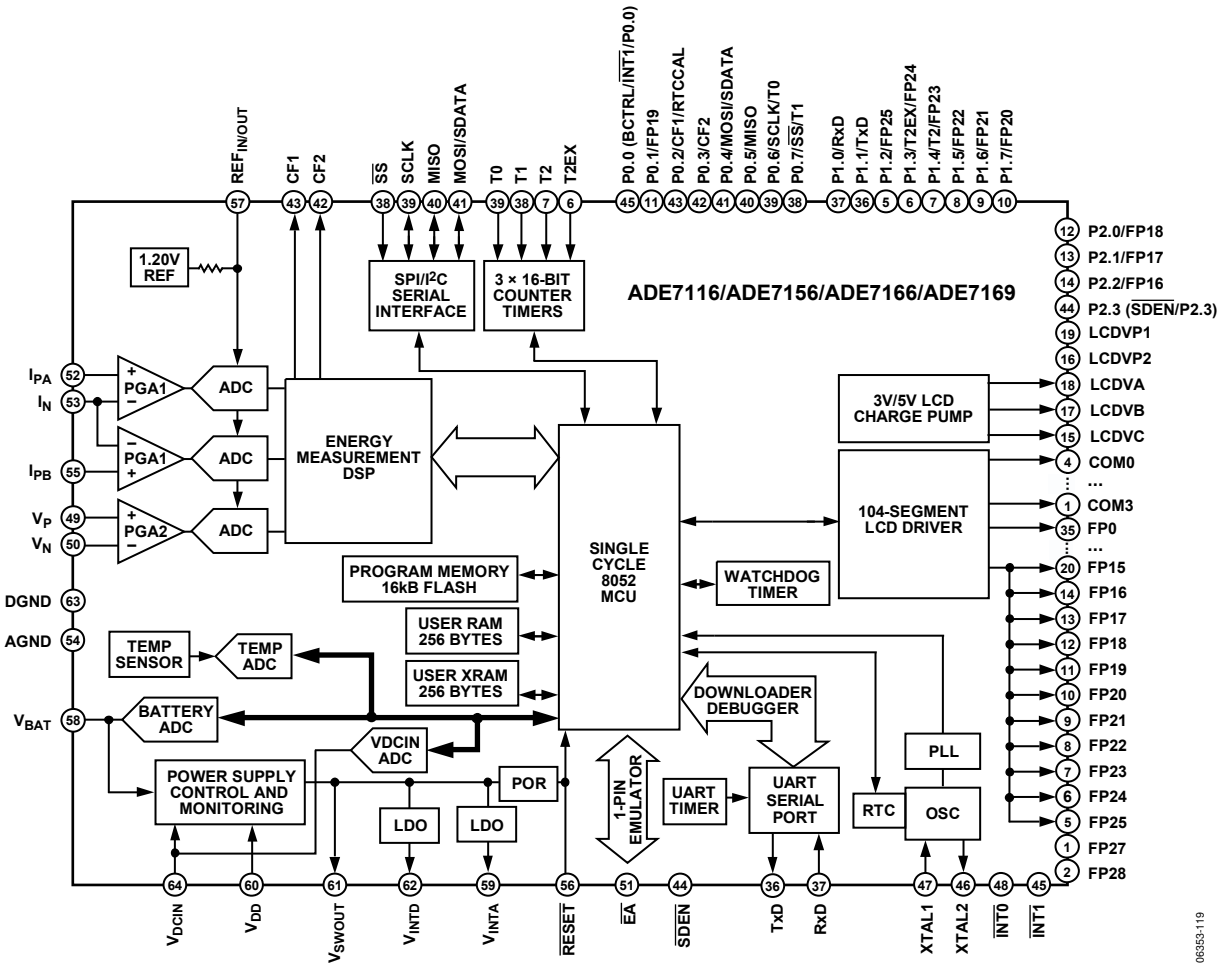

Figure 2. ADE7116/ADE7156/ADE7166/ADE7169 Functional Block Diagram

SPECIFICATIONS

V_{DD} = 3.3 V ± 5%, AGND = DGND = 0 V, on-chip reference XTALx = 32.768 kHz, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

ENERGY METERING

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MEASUREMENT ACCURACY[1]					
Phase Error Between Channels[2]					
PF = 0.8 Capacitive		±0.05		Degrees	Phase lead: 37°
PF = 0.5 Inductive		±0.05		Degrees	Phase lag: 60°
Active Energy Measurement Error[2]		0.1		% of reading	Over a dynamic range of 1000 to 1 at 25°C
AC Power Supply Rejection[2]					V_{DD} = 3.3 V + 100 mV rms/120 Hz
Output Frequency Variation		0.01		%	$I_{Px} = V_P$ = ±100 mV rms
DC Power Supply Rejection[2]					V_{DD} = 3.3 V ± 117 mV dc
Output Frequency Variation		0.01		%	
Active Energy Measurement Bandwidth[1]		8		kHz	
Reactive Energy Measurement Error[2, 3]		0.5		% of reading	Over a dynamic range of 1000 to 1 at 25°C
V_{rms} Measurement Error[2]		0.5		% of reading	Over a dynamic range of 100 to 1 at 25°C
V_{rms} Measurement Bandwidth[1]		3.9		kHz	
I_{rms} Measurement Error[2]		0.5		% of reading	Over a dynamic range of 500 to 1 at 25°C
I_{rms} Measurement Bandwidth[1]		3.9		kHz	
ANALOG INPUTS					
Maximum Signal Levels			±400	mV peak	$V_P - V_N$ differential input
ADE7566/ADE7569			±400	mV peak	$I_P - I_N$ differential input
ADE7116/ADE7156/ADE7166/ADE7169			±250	mV peak	$I_{PA} - I_N$ and $I_{PB} - I_N$ differential inputs
Input Impedance (DC)		770		kΩ	
ADC Offset Error[2]		±10		mV	PGA1 = PGA2 = 1
		±1		mV	PGA1 = 16
Gain Error[2]					
Current Channel		±3		%	$I_{PA} = I_{PB}$ = 0.4 V dc or I_P = 0.4 V dc
Voltage Channel		±3	+3	%	$V_P - V_N$ = 0.4 V dc
Gain Error Match		±0.2		%	
CF1 AND CF2 PULSE OUTPUT					
Maximum Output Frequency		13.5		kHz	$V_P - V_N$ = 400 mV peak, $I_{PA} - I_N$ = 250 mV, PGA1 = 2 sine wave
Duty Cycle		50		%	If CF1 or CF2 frequency, >5.55 Hz
Active High Pulse Width		90		ms	If CF1 or CF2 frequency, <5.55 Hz
FAULT DETECTION[4]					
Fault Detection Threshold					
Inactive Input ≠ Active Input		6.25		% of active	I_{PA} or I_{PB} active
Input Swap Threshold					
Inactive Input > Active Input		6.25		% of active	I_{PA} or I_{PB} active
Accuracy Fault Mode Operation					
I_{PA} Active, I_{PB} = AGND		0.1		% of reading	Over a dynamic range of 500 to 1
I_{PB} Active, I_{PA} = AGND		0.1		% of reading	Over a dynamic range of 500 to 1
Fault Detection Delay		3		Seconds	
Swap Delay		3		Seconds	

[1] These specifications are not production tested but are guaranteed by design and/or characterization data on production release.
[2] See the Terminology section for definition.
[3] This function is not available in the ADE7166 or ADE7566.
[4] This function is not available in the ADE7566 or ADE7569.

ANALOG PERIPHERALS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INTERNAL ADCs (BATTERY, TEMPERATURE, V_{DCIN})[1]					
Power Supply Operating Range	2.4		3.7	V	Measured on V_{SWOUT}
No Missing Codes[2]	8			Bits	
Conversion Delay[3]		38		µs	
ADC Gain					
V_{DCIN} Measurement		15.3		mV/LSB	
V_{BAT} Measurement		14.6		mV/LSB	
Temperature Measurement		0.78		°C/LSB	
ADC Offset					
V_{DCIN} Measurement at 3 V		206		LSB	
V_{BAT} Measurement at 3.7 V		205		LSB	
Temperature Measurement at 25°C		129		LSB	
V_{DCIN} Analog Input					
Maximum Signal Levels	0		3.3	V	
Input Impedance (DC)	1			MΩ	
Low V_{DCIN} Detection Threshold	1.09	1.2	1.27	V	
POWER-ON RESET (POR)					
V_{DD} POR					
Detection Threshold	2.5		2.95	V	
POR Active Timeout Period		33		ms	
V_{SWOUT} POR					
Detection Threshold	1.8		2.2	V	
POR Active Timeout Period		20		ms	
V_{INTD} POR					
Detection Threshold	2.0		2.25	V	
POR Active Timeout Period		16		ms	
V_{INTA} POR					
Detection Threshold	2.05		2.25	V	
POR Active Timeout Period		120		ms	
BATTERY SWITCHOVER					
Voltage Operating Range (V_{SWOUT})	2.4		3.7	V	
V_{DD} to V_{BAT} Switching					
Switching Threshold (V_{DD})	2.5		2.95	V	
Switching Delay		10		ns	When V_{DD} to V_{BAT} switch activated by V_{DD}
		30		ms	When V_{DD} to V_{BAT} switch activated by V_{DCIN}
V_{BAT} to V_{DD} Switching					
Switching Threshold (V_{DD})	2.5		2.95	V	
Switching Delay		30		ms	Based on V_{DD} > 2.75 V
V_{SWOUT} to V_{BAT} Leakage Current		10		nA	V_{BAT} = 0 V, V_{SWOUT} = 3.43 V, T_A = 25°C
LCD, CHARGE PUMP ACTIVE[4]					
Charge Pump Capacitance Between LCDVP1 and LCDVP2	100			nF	
LCDVA, LCDVB, LCDVC Decoupling Capacitance	470			nF	
LCDVA	0		1.75	V	
LCDVB	0		3.5	V	1/3 bias mode
LCDVC	0		5.3	V	1/3 bias mode
V1 Segment Line Voltage	LCDVA – 0.1		LCDVA	V	Current on segment line = −2 µA
V2 Segment Line Voltage	LCDVB – 0.1		LCDVB	V	Current on segment line = −2 µA
V3 Segment Line Voltage	LCDVC – 0.1		LCDVC	V	Current on segment line = −2 µA
DC Voltage Across Segment and COMx Pin			50	mV	LCDVC − LCDVB, LCDVC − LCDVA, or LCDVB − LCDVA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LCD, RESISTOR LADDER ACTIVE					
Leakage Current		±20		nA	1/2 and 1/3 bias modes, no load
V1 Segment Line Voltage	LCDVA – 0.1		LCDVA	V	Current on segment line = −2 µA
V2 Segment Line Voltage	LCDVB – 0.1		LCDVB	V	Current on segment line = −2 µA
V3 Segment Line Voltage	LCDVC – 0.1		LCDVC	V	Current on segment line = −2 µA
ON-CHIP REFERENCE					
Reference Error			±0.9	mV	T_A = 25°C
Power Supply Rejection		80		dB	
Temperature Coefficient[2]		10	50	ppm/°C	

[1] This function is not available in the ADE7116.
[2] These specifications are not production tested but are guaranteed by design and/or characterization data on production release.
[3] Delay between ADC conversion request and interrupt set.
[4] This function is not available in the ADE7116 or ADE7156.

DIGITAL INTERFACE

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS[1]					
All Inputs Except XTAL1, XTAL2, BCTRL, $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{RESET}}$					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.8	V	
BCTRL, $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{RESET}}$					
Input High Voltage, V_{INH}	1.3			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Currents					
$\overline{\text{RESET}}$			100	nA	$\overline{\text{RESET}}$ = V_{SWOUT} = 3.3 V
Port 0, Port 1, Port 2			±100	nA	Internal pull-up disabled, input = 0 V or V_{SWOUT}
	−3.75		−8.5	µA	Internal pull-up enabled, input = 0 V, V_{SWOUT} = 3.3 V
Input Capacitance		10		pF	All digital inputs
FLASH MEMORY					
Endurance[2]	20,000			Cycles	
Data Retention[3]	20			Years	T_J = 85°C
CRYSTAL OSCILLATOR[4]					
Crystal Equivalent Series Resistance	30		50	kΩ	
Crystal Frequency	32	32.768	33.5	kHz	
XTAL1 Input Capacitance		12		pF	
XTAL2 Output Capacitance		12		pF	
MCU CLOCK RATE (f_{CORE})		4.096		MHz	Crystal = 32.768 kHz and CD bits = 000
		32		kHz	Crystal = 32.768 kHz and CD bits = 111
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	V_{DD} = 3.3 V ± 5%
I_{SOURCE}			80	µA	
Output Low Voltage, V_{OL}[5]			0.4	V	V_{DD} = 3.3 V ± 5%
I_{SINK}			2	mA	
START-UP TIME[6]					
PSM0 Power-On Time		880		ms	V_{DD} at 2.75 V to PSM0 code execution
From Power Saving Mode 1 (PSM1)					
PSM1 to PSM0		130		ms	V_{DD} at 2.75 V to PSM0 code execution
From Power Saving Mode 2 (PSM2)					
PSM2 to PSM1		48		ms	Wake-up event to PSM1 code execution
PSM2 to PSM0		186		ms	V_{DD} at 2.75 V to PSM0 code execution

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY INPUTS					
V_{DD}	3.13	3.3	3.46	V	
V_{BAT}	2.4	3.3	3.7	V	
INTERNAL POWER SUPPLY SWITCH (V_{SWOUT})					
V_{BAT} to V_{SWOUT} On Resistance			22	Ω	V_{BAT} = 2.4 V
V_{DD} to V_{SWOUT} On Resistance			10.2	Ω	V_{DD} = 3.13 V
V_{BAT} to/from V_{DD} Switching Open Time		40		ns	
BCTRL State Change and Switch Delay		18		µs	
V_{SWOUT} Output Current Drive			6	mA	
POWER SUPPLY OUTPUTS					
V_{INTA}	2.3		2.70	V	
V_{INTD}	2.3		2.70	V	
V_{INTA} Power Supply Rejection		60		dB	
V_{INTD} Power Supply Rejection		50		dB	
POWER SUPPLY CURRENTS					
Current in Normal Mode (PSM0)		4	5.3	mA	f_{CORE} = 4.096 MHz, LCD and meter active
		2.1		mA	f_{CORE} = 1.024 MHz, LCD and meter active
		1.6		mA	f_{CORE} = 32.768 kHz, LCD and meter active
		3	3.9	mA	f_{CORE} = 4.096 MHz, metering ADC and DSP powered down
Current in PSM1		3.2	5.05	mA	f_{CORE} = 4.096 MHz, LCD active, V_{BAT} = 3.7 V
		880		µA	f_{CORE} = 1.024 MHz, LCD active
Current in PSM2		38		µA	LCD active with charge pump at 3.3 V + RTC, V_{BAT} = 3.3 V
		1.5		µA	RTC only, T_A = 25°C, V_{BAT} = 3.3 V

[1] Specifications guaranteed by design.
[2] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[3] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22 Method A117. Retention lifetime derates with junction temperature.
[4] Recommended crystal specifications.
[5] Test carried out with all the I/Os set to a low output level.
[6] Delay between power supply valid and execution of first instruction by 8052 core.

TIMING SPECIFICATIONS

AC inputs during testing were driven at V_{SWOUT} − 0.5 V for Logic 1 and at 0.45 V for Logic 0. Timing measurements were made at V_{IH} minimum for Logic 1 and at V_{IL} maximum for Logic 0, as shown in Figure 3.

For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs, as shown in Figure 3.

C_{LOAD} for all outputs is equal to 80 pF, unless otherwise noted. V_{DD} = 2.7 V to 3.6 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

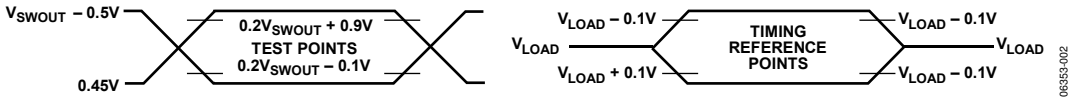

Figure 3. Timing Waveform Characteristics

Table 5. Clock Input (External Clock Driven XTAL1) Parameter

		32.768 kHz External Crystal			
Parameter	**Description**	**Min**	**Typ**	**Max**	**Unit**
t_{CK}	XTAL1 period		30.52		µs
t_{CKL}	XTAL1 width low		6.26		µs
t_{CKH}	XTAL1 width high		6.26		µs
t_{CKR}	XTAL1 rise time		9		ns
t_{CKF}	XTAL1 fall time		9		ns
$1/t_{CORE}$	Core clock frequency[1]		1.024		MHz

[1] The internal PLL locks onto a multiple (512×) of the 32.768 kHz external crystal frequency to provide a stable 4.096 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple defined by the CD bits of the POWCON SFR, Address 0xC5[2:0] (see Table 26).

Table 6. I²C-Compatible Interface Timing Parameters (400 kHz)

Parameter	**Description**	**Typ**	**Unit**
t_{BUF}	Bus-free time between stop condition and start condition	1.3	µs
t_L	SCLK low pulse width	1.36	µs
t_H	SCLK high pulse width	1.14	µs
t_{SHD}	Start condition hold time	251.35	µs
t_{DSU}	Data setup time	740	ns
t_{DHD}	Data hold time	400	ns
t_{RSU}	Setup time for repeated start	12.5	ns
t_{PSU}	Stop condition setup time	400	ns
t_R	Rise time of both SCLK and SDATA	200	ns
t_F	Fall time of both SCLK and SDATA	300	ns
t_{SUP}[1]	Pulse width of spike suppressed	50	ns

[1] Input filtering on both the SCLK and SDATA inputs suppresses noise spikes of <50 ns.

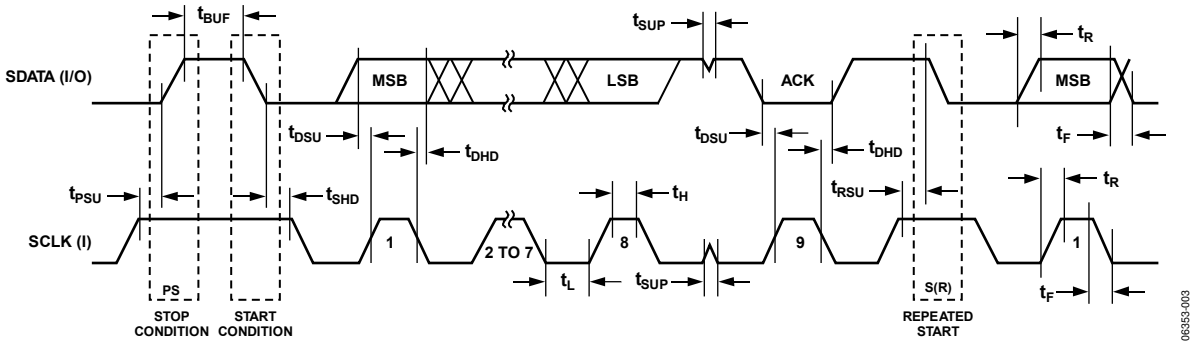

Figure 4. I²C-Compatible Interface Timing

Table 7. SPI Master Mode Timing (SPICPHA = 1) Parameters

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width	$2^{SPIR} \times t_{CORE}$[1]			ns
t_{SH}	SCLK high pulse width	$2^{SPIR} \times t_{CORE}$[1]			ns
t_{DAV}	Data output valid after SCLK edge			$3 \times t_{CORE}$[1]	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge	t_{CORE}[1]			ns
t_{DF}	Data output fall time		19		ns
t_{DR}	Data output rise time		19		ns
t_{SR}	SCLK rise time		19		ns
t_{SF}	SCLK fall time		19		ns

[1] t_{CORE} depends on the clock divider or CD[2:0] bits of the POWCON SFR, Address 0xC5 (see Table 26); $t_{CORE} = 2^{CD}/4.096$ MHz.

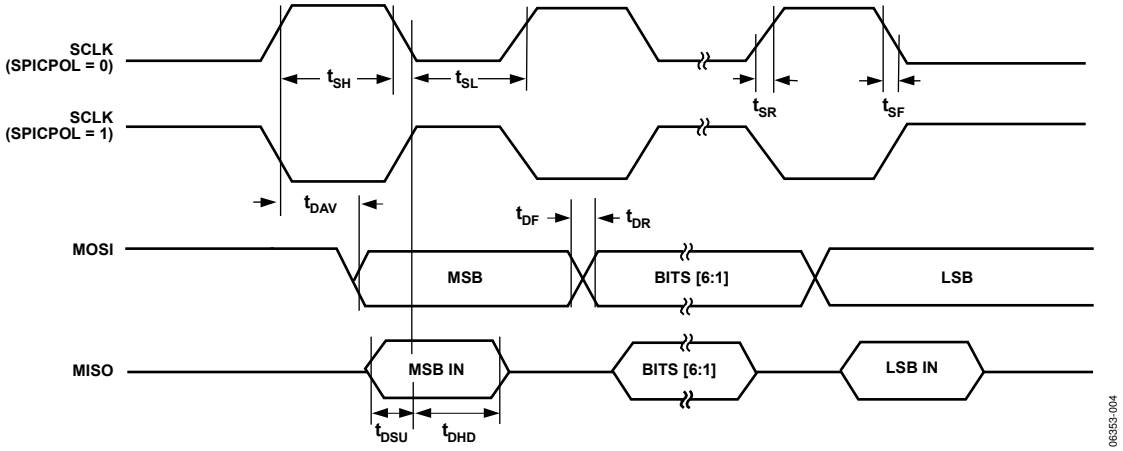

Figure 5. SPI Master Mode Timing (SPICPHA = 1)

Table 8. SPI Master Mode Timing (SPICPHA = 0) Parameters

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width	$2^{SPIR} \times t_{CORE}$[1]	(SPIR + 1) × t_{CORE}[1]		ns
t_{SH}	SCLK high pulse width	$2^{SPIR} \times t_{CORE}$[1]	(SPIR + 1) × t_{CORE}[1]		ns
t_{DAV}	Data output valid after SCLK edge			3 × t_{CORE}[1]	ns
t_{DOSU}	Data output setup before SCLK edge			75	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge	t_{CORE}[1]			ns
t_{DF}	Data output fall time		19		ns
t_{DR}	Data output rise time		19		ns
t_{SR}	SCLK rise time		19		ns
t_{SF}	SCLK fall time		19		ns

[1] t_{CORE} depends on the clock divider or CD[2:0] bits of the POWCON SFR, Address 0xC5 (see Table 26); $t_{CORE} = 2^{CD}/4.096$ MHz.

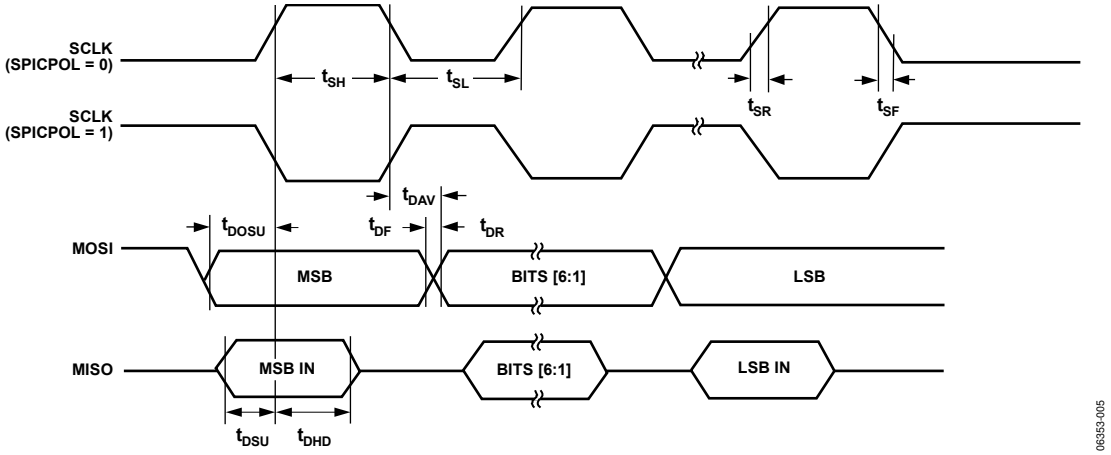

Figure 6. SPI Master Mode Timing (SPICPHA = 0)

Table 9. SPI Slave Mode Timing (SPICPHA = 1) Parameters

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{SS}}$	$\overline{SS}$ to SCLK edge	145			ns
t_{SL}	SCLK low pulse width	$6 \times t_{CORE}$[1]			ns
t_{SH}	SCLK high pulse width	$6 \times t_{CORE}$[1]			ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge	$2 \times t_{CORE}$[1] + 0.5 µs			µs
t_{DF}	Data output fall time		19		ns
t_{DR}	Data output rise time		19		ns
t_{SR}	SCLK rise time		19		ns
t_{SF}	SCLK fall time		19		ns
t_{SFS}	$\overline{SS}$ high after SCLK edge	0			ns

[1] t_{CORE} depends on the clock divider or CD[2:0] bits of the POWCON SFR, Address 0xC5 (see Table 26); $t_{CORE} = 2^{CD}/4.096$ MHz.

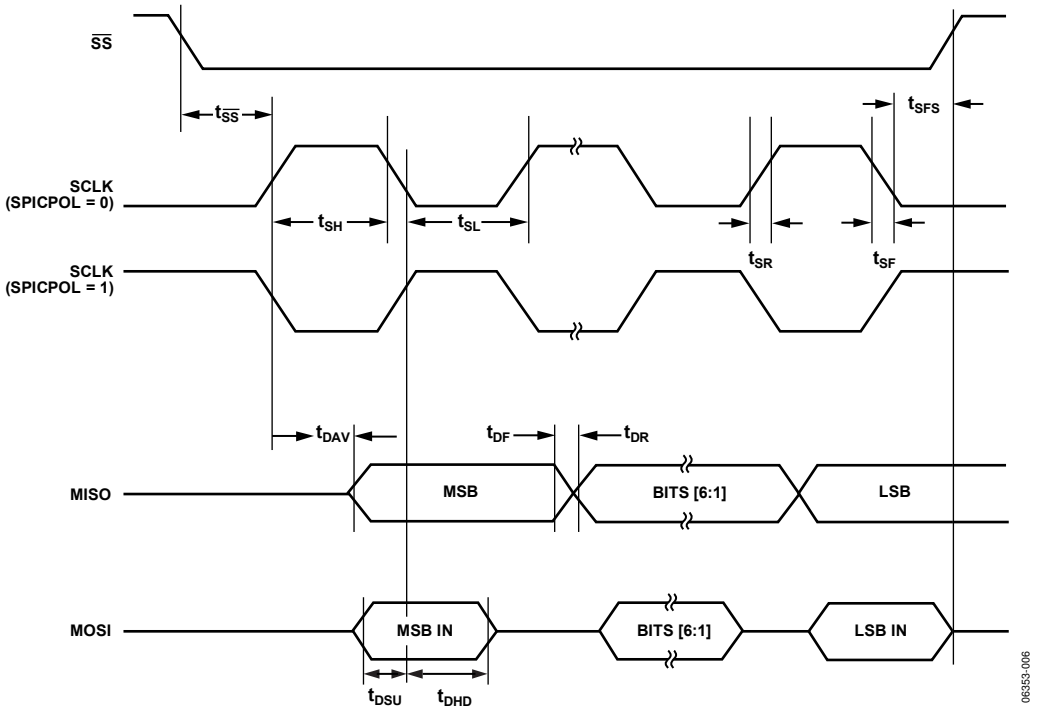

Figure 7. SPI Slave Mode Timing (SPICPHA = 1)

Table 10. SPI Slave Mode Timing (SPICPHA = 0) Parameters

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{SS}}$	$\overline{SS}$ to SCLK edge	145			ns
t_{SL}	SCLK low pulse width	$6 \times t_{CORE}$[1]			ns
t_{SH}	SCLK high pulse width	$6 \times t_{CORE}$[1]			ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge	$2 \times t_{CORE}$[1] + 0.5 µs			µs
t_{DF}	Data output fall time		19		ns
t_{DR}	Data output rise time		19		ns
t_{SR}	SCLK rise time		19		ns
t_{SF}	SCLK fall time		19		ns
t_{DOSS}	Data output valid after $\overline{SS}$ edge	0			ns
t_{SFS}	$\overline{SS}$ high after SCLK edge	0			ns

[1] t_{CORE} depends on the clock divider or CD[2:0] bits of the POWCON SFR, Address 0xC5 (see Table 26); $t_{CORE} = 2^{CD}/4.096$ MHz.

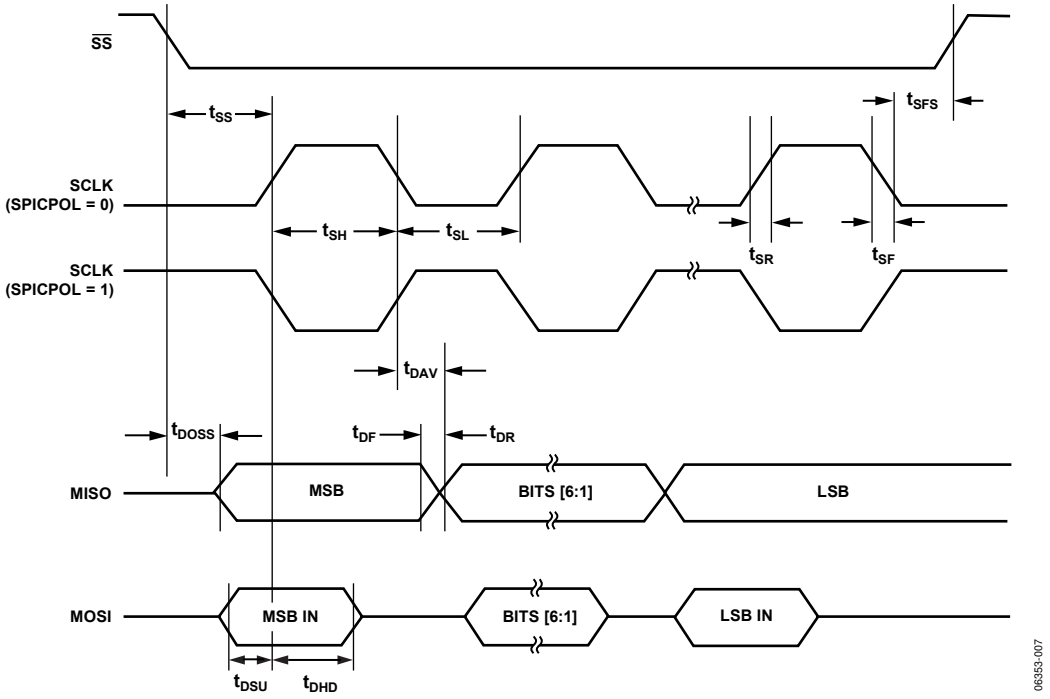

Figure 8. SPI Slave Mode Timing (SPICPHA = 0)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 11.

Parameter	Rating
V_{DD} to DGND	−0.3 V to +3.7 V
V_{BAT} to DGND	−0.3 V to +3.7 V
V_{DCIN} to DGND	−0.3 V to V_{SWOUT} + 0.3 V
Input LCD Voltage to AGND, LCDVA, LCDVB, LCDVC[1]	−0.3 V to V_{SWOUT} + 0.3 V
Analog Input Voltage to AGND, V_P, V_N, I_P, I_{PA}, I_{PB}, and I_N	−2 V to +2 V
Digital Input Voltage to DGND	−0.3 V to V_{SWOUT} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{SWOUT} + 0.3 V
Operating Temperature Range (Industrial)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
64-Lead LQFP, Power Dissipation	
Lead Temperature (Soldering, 30 sec)	300°C

[1] When used with external resistor divider.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 12. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
64-Lead LQFP	60	20.5	°C/W
64-Lead LFCSP	27.1	2.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

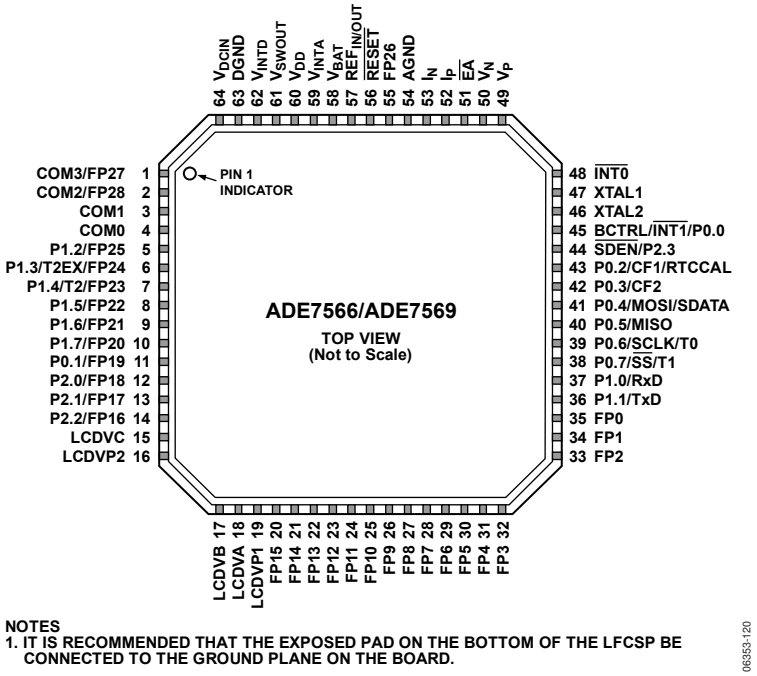

Figure 9. Pin Configuration for the ADE7566/ADE7569

Table 13. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COM3/FP27	Common Output 3/LCD Segment Output 27. COM3 is used for the LCD backplane.
2	COM2/FP28	Common Output 2/LCD Segment Output 28. COM2 is used for the LCD backplane.
3	COM1	Common Output 1. COM1 is used for the LCD backplane.
4	COM0	Common Output 0. COM0 is used for the LCD backplane.
5	P1.2/FP25	General-Purpose Digital I/O Port 1.2/LCD Segment Output 25.
6	P1.3/T2EX/FP24	General-Purpose Digital I/O Port 1.3/Timer 2 Control Input/LCD Segment Output 24.
7	P1.4/T2/FP23	General-Purpose Digital I/O Port 1.4/Timer 2 Input/LCD Segment Output 23.
8	P1.5/FP22	General-Purpose Digital I/O Port 1.5/LCD Segment Output 22.
9	P1.6/FP21	General-Purpose Digital I/O Port 1.6/LCD Segment Output 21.
10	P1.7/FP20	General-Purpose Digital I/O Port 1.7/LCD Segment Output 20.
11	P0.1/FP19	General-Purpose Digital I/O Port 0.1/LCD Segment Output 19.
12	P2.0/FP18	General-Purpose Digital I/O Port 2.0/LCD Segment Output 18.
13	P2.1/FP17	General-Purpose Digital I/O Port 2.1/LCD Segment Output 17.
14	P2.2/FP16	General-Purpose Digital I/O Port 2.2/LCD Segment Output 16.
15	LCDVC	This pin can be either an analog input when the LCD resistor driver is enabled or an analog output when the LCD charge pump is enabled. When this pin is an analog output, it should be decoupled with a 470 nF capacitor. When this pin is an analog input, it is internally connected to V_{DD}. A resistor should be connected between this pin and LCDVB to generate the two highest voltages for the LCD waveforms (see the LCD Driver section).
16	LCDVP2	This pin can be either an analog input when the LCD resistor driver is enabled or an analog output when the LCD charge pump is enabled. When this pin is an analog output, a 100 nF capacitor should be connected between this pin and LCDVP1. When this pin is an analog input, it is internally connected to LCDVP1 (see the LCD Driver section).
17	LCDVB	This pin can be either an analog input when the LCD resistor driver is enabled or an analog output when the LCD charge pump is enabled. When this pin is an analog output, it should be decoupled with a 470 nF capacitor. When this pin is an analog input, a resistor should be connected between this pin and LCDVC to generate an intermediate voltage for the LCD driver. In 1/3 bias LCD mode, another resistor must be connected between this pin and LCDVA to generate another intermediate voltage. In 1/2 bias LCD mode, LCDVB and LCDVA are internally connected (see the LCD Driver section).

Pin No.	Mnemonic	Description
18	LCDVA	This pin can be either an analog input when the LCD resistor driver is enabled or an analog output when the LCD charge pump is enabled. When this pin is an analog output, it should be decoupled with a 470 nF capacitor. When this pin is an analog input, a resistor should be connected between this pin and LCDVP1 to generate an intermediate voltage for the LCD driver. In 1/3 bias LCD mode, another resistor must be connected between this pin and LCDVB to generate another intermediate voltage. In 1/2 bias LCD mode, LCDVA and LCDVB are internally connected (see the LCD Driver section).
19	LCDVP1	This pin can be either an analog input when the LCD resistor driver is enabled or an analog output when the LCD charge pump is enabled. When this pin is an analog output, a 100 nF capacitor should be connected between this pin and LCDVP2. When this pin is an analog input, a resistor should be connected between this pin and LCDVA to generate an intermediate voltage for the LCD driver. Another resistor must be connected between LCDVP1 and DGND to generate another intermediate voltage (see the LCD Driver section).
20 to 35	FP15 to FP0	LCD Segment Output 15 to LCD Segment Output 0.
36	P1.1/TxD	General-Purpose Digital I/O Port 1.1/Transmitter Data Output (Asynchronous).
37	P1.0/RxD	General-Purpose Digital I/O Port 1.0/Receiver Data Input (Asynchronous).
38	P0.7/$\overline{SS}$/T1	General-Purpose Digital I/O Port 0.7/Slave Select When SPI Is in Slave Mode/Timer 1 Input.
39	P0.6/SCLK/T0	General-Purpose Digital I/O Port 0.6/Clock Output for I^2C or SPI Port/Timer 0 Input.
40	P0.5/MISO	General-Purpose Digital I/O Port 0.5/Data Input for SPI Port.
41	P0.4/MOSI/SDATA	General-Purpose Digital I/O Port 0.4/Data Output for SPI Port/I^2C-Compatible Data Line.
42	P0.3/CF2	General-Purpose Digital I/O Port 0.3/Calibration Frequency Logic Output 2. The CF2 logic output gives instantaneous active, reactive, I_{rms}, or apparent power information.
43	P0.2/CF1/RTCCAL	General-Purpose Digital I/O Port 0.2/Calibration Frequency Logic Output 1/RTC Calibration Frequency Logic Output. The CF1 logic output gives instantaneous active, reactive, I_{rms}, or apparent information. The RTCCAL logic output gives access to the calibrated RTC output.
44	$\overline{SDEN}$/P2.3	Serial Download Mode Enable/General-Purpose Digital I/O Port 2.3. This pin is used to enable serial download mode through a resistor when pulled low on power-up or reset. On reset, this pin momentarily becomes an input, and the status of the pin is sampled. If there is no pull-down resistor in place, the pin momentarily goes high and then user code is executed. If the pin is pulled down on reset, the embedded serial download/debug kernel executes, and this pin remains low during the internal program execution. After reset, this pin can be used as a digital output port pin (P2.3).
45	BCTRL/$\overline{INT1}$/P0.0	Digital Input for Battery Control/External Interrupt Input 1/General-Purpose Digital I/O Port 0.0. This logic input connects V_{DD} or V_{BAT} to V_{SWOUT} internally when set to logic high or logic low, respectively. When left open, the connection between V_{DD} or V_{BAT} and V_{SWOUT} is selected internally.
46	XTAL2	A crystal can be connected across this pin and XTAL1 to provide a clock source for the ADE7566/ADE7569. The XTAL2 pin can drive one CMOS load when an external clock is supplied at XTAL1 or by the gate oscillator circuit. An internal 6 pF capacitor is connected to this pin.
47	XTAL1	An external clock can be provided at this logic input. Alternatively, a tuning fork crystal can be connected across XTAL1 and XTAL2 to provide a clock source for the ADE7566/ADE7569. The clock frequency for specified operation is 32.768 kHz. An internal 6 pF capacitor is connected to this pin.
48	$\overline{INT0}$	External Interrupt Input 0.
49, 50	V_P, V_N	Analog Inputs for Voltage Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±400 mV for specified operation. This channel also has an internal PGA.
51	$\overline{EA}$	This pin is used as an input for emulation. When held high, this input enables the device to fetch code from internal program memory locations. The ADE7566/ADE7569 do not support external code memory. This pin should not be left floating.
52, 53	I_P, I_N	Analog Inputs for Current Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±400 mV for specified operation. This channel also has an internal PGA.
54	AGND	This pin provides the ground reference for the analog circuitry.
55	FP26	LCD Segment Output 26.
56	$\overline{RESET}$	Reset Input, Active Low.
57	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V ± 0.1% and a maximum temperature coefficient of 50 ppm/°C. This pin should be decoupled with a 1 µF capacitor in parallel with a ceramic 100 nF capacitor.
58	V_{BAT}	Power Supply Input from the Battery with a 2.4 V to 3.7 V Range. This pin is connected internally to V_{DD} when the battery is selected as the power supply for the ADE7566/ADE7569.
59	V_{INTA}	This pin provides access to the on-chip 2.5 V analog LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.

Pin No.	Mnemonic	Description
60	V_{DD}	3.3 V Power Supply Input from the Regulator. This pin is connected internally to V_{SWOUT} when the regulator is selected as the power supply for the ADE7566/ADE7569. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
61	V_{SWOUT}	3.3 V Power Supply Output. This pin provides the supply voltage for the LDOs and internal circuitry of the ADE7566/ADE7569. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
62	V_{INTD}	This pin provides access to the on-chip 2.5 V digital LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
63	DGND	Ground Reference for Digital Circuitry.
64	V_{DCIN}	Analog Input for DC Voltage Monitoring. The maximum input voltage on this pin is V_{SWOUT} with respect to AGND. This pin is used to monitor the preregulated dc voltage.
EP	Exposed Pad	The exposed pad on the bottom of the LFCSP enhances thermal performance and is electrically connected to ground inside the package. It is recommended that the exposed pad be connected to the ground plane on the board.

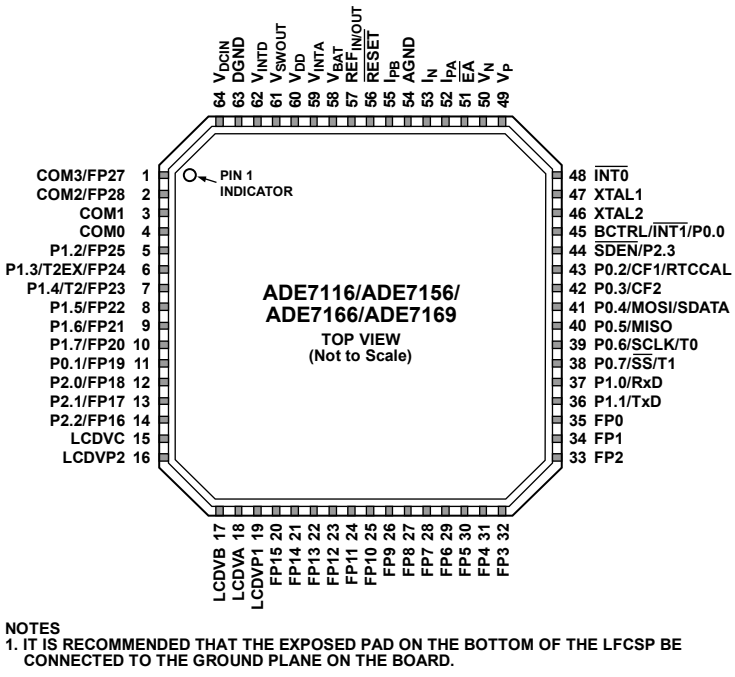

Figure 10. Pin Configuration for the ADE7116/ADE7156/ADE7166/ADE7169

Table 14. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COM3/FP27	Common Output 3/LCD Segment Output 27. COM3 is used for the LCD backplane.
2	COM2/FP28	Common Output 2/LCD Segment Output 28. COM2 is used for the LCD backplane.
3	COM1	Common Output 1. COM1 is used for the LCD backplane.
4	COM0	Common Output 0. COM0 is used for the LCD backplane.
5	P1.2/FP25	General-Purpose Digital I/O Port 1.2/LCD Segment Output 25.
6	P1.3/T2EX/FP24	General-Purpose Digital I/O Port 1.3/Timer 2 Control Input/LCD Segment Output 24.
7	P1.4/T2/FP23	General-Purpose Digital I/O Port 1.4/Timer 2 Input/LCD Segment Output 23.
8	P1.5/FP22	General-Purpose Digital I/O Port 1.5/LCD Segment Output 22.
9	P1.6/FP21	General-Purpose Digital I/O Port 1.6/LCD Segment Output 21.
10	P1.7/FP20	General-Purpose Digital I/O Port 1.7/LCD Segment Output 20.
11	P0.1/FP19	General-Purpose Digital I/O Port 0.1/LCD Segment Output 19.
12	P2.0/FP18	General-Purpose Digital I/O Port 2.0/LCD Segment Output 18.
13	P2.1/FP17	General-Purpose Digital I/O Port 2.1/LCD Segment Output 17.
14	P2.2/FP16	General-Purpose Digital I/O Port 2.2/LCD Segment Output 16.
15	LCDVC	In the ADE7166/ADE7169, this pin can be either an analog input when the LCD resistor driver is enabled or an analog output when the LCD charge pump is enabled. In the ADE7116/ADE7156, this pin is always an analog input. When this pin is an analog output, it should be decoupled with a 470 nF capacitor. When this pin is an analog input, it is internally connected to V_{DD}. A resistor should be connected between this pin and LCDVB to generate the two highest voltages for the LCD waveforms (see the LCD Driver section).
16	LCDVP2	In the ADE7166/ADE7169, this pin can be either an analog input when the LCD resistor driver is enabled or an analog output when the LCD charge pump is enabled. In the ADE7116 and ADE7156, this pin is always an analog input. When this pin is an analog output, a 100 nF capacitor should be connected between this pin and LCDVP1. When this pin is an analog input, it is internally connected to LCDVP1 (see the LCD Driver section).
17	LCDVB	In the ADE7166/ADE7169, this pin can be either an analog input when the LCD resistor driver is enabled or an analog output when the LCD charge pump is enabled. In the ADE7116/ADE7156, this pin is always an analog input. When this pin is an analog output, it should be decoupled with a 470 nF capacitor. When this pin is an analog input, a resistor should be connected between this pin and LCDVC to generate an intermediate voltage for the LCD driver. In 1/3 bias LCD mode, another resistor must be connected between this pin and LCDVA to generate another intermediate voltage. In 1/2 bias LCD mode, LCDVB and LCDVA are internally connected (see the LCD Driver section).

Pin No.	Mnemonic	Description
18	LCDVA	In the ADE7166/ADE7169, this pin can be either an analog input when the LCD resistor driver is enabled or an analog output when the LCD charge pump is enabled. In the ADE7116/ADE7156, this pin is always an analog input. When this pin is an analog output, it should be decoupled with a 470 nF capacitor. When this pin is an analog input, a resistor should be connected between this pin and LCDVP1 to generate an intermediate voltage for the LCD driver. In 1/3 bias LCD mode, another resistor must be connected between this pin and LCDVB to generate another intermediate voltage. In 1/2 bias LCD mode, LCDVA and LCDVB are internally connected (see the LCD Driver section).
19	LCDVP1	In the ADE7166/ADE7169, this pin can be either an analog input when the LCD resistor driver is enabled or an analog output when the LCD charge pump is enabled. In the ADE7116/ADE7156, this pin is always an analog input. When this pin is an analog output, a 100 nF capacitor should be connected between this pin and LCDVP2. When this pin is an analog input, a resistor should be connected between this pin and LCDVA to generate an intermediate voltage for the LCD driver. Another resistor must be connected between LCDVP1 and DGND to generate another intermediate voltage (see the LCD Driver section).
20 to 35	FP15 to FP0	LCD Segment Output 0 to LCD Segment Output 15.
36	P1.1/TxD	General-Purpose Digital I/O Port 1.1/Transmitter Data Output (Asynchronous).
37	P1.0/RxD	General-Purpose Digital I/O Port 1.0/Receiver Data Input (Asynchronous).
38	P0.7/$\overline{SS}$/T1	General-Purpose Digital I/O Port 0.7/Slave Select When SPI Is in Slave Mode/Timer 1 Input.
39	P0.6/SCLK/T0	General-Purpose Digital I/O Port 0.6/Clock Output for I^2C or SPI Port/Timer 0 Input.
40	P0.5/MISO	General-Purpose Digital I/O Port 0.5/Data Input for SPI Port.
41	P0.4/MOSI/SDATA	General-Purpose Digital I/O Port 0.4/Data Output for SPI Port/I^2C-Compatible Data Line.
42	P0.3/CF2	General-Purpose Digital I/O Port 0.3/Calibration Frequency Logic Output 2. The CF2 logic output gives instantaneous active, reactive, I_{rms}, or apparent power information.
43	P0.2/CF1/RTCCAL	General-Purpose Digital I/O Port 0.2/Calibration Frequency Logic Output 1/RTC Calibration Frequency Logic Output. The CF1 logic output gives instantaneous active, reactive, I_{rms}, or apparent power information. The RTCCAL logic output gives access to the calibrated RTC output.
44	$\overline{SDEN}$/P2.3	Serial Download Mode Enable/General-Purpose Digital I/O Port 2.3. This pin is used to enable serial download mode through a resistor when pulled low on power-up or reset. On reset, this pin momentarily becomes an input, and the status of the pin is sampled. If there is no pull-down resistor in place, the pin momentarily goes high and then user code is executed. If the pin is pulled down on reset, the embedded serial download/debug kernel executes, and this pin remains low during the internal program execution. After reset, this pin can be used as a digital output port pin (P2.3).
45	BCTRL/$\overline{INT1}$/P0.0	Digital Input for Battery Control/External Interrupt Input 1/General-Purpose Digital I/O Port 0.0. This logic input connects V_{DD} or V_{BAT} to V_{SWOUT} internally when set to logic high or logic low, respectively. When left open, the connection between V_{DD} or V_{BAT} and V_{SWOUT} is selected internally.
46	XTAL2	A crystal can be connected across this pin and XTAL1 to provide a clock source for the ADE7116/ADE7156/ADE7166/ADE7169. The XTAL2 pin can drive one CMOS load when an external clock is supplied at XTAL1 or by the gate oscillator circuit. An internal 6 pF capacitor is connected to this pin.
47	XTAL1	An external clock can be provided at this logic input. Alternatively, a tuning fork crystal can be connected across XTAL1 and XTAL2 to provide a clock source for the ADE7116/ADE7156/ADE7166/ADE7169. The clock frequency for specified operation is 32.768 kHz. An internal 6 pF capacitor is connected to this pin.
48	$\overline{INT0}$	External Interrupt Input 0.
49, 50	V_P, V_N	Analog Inputs for Voltage Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±400 mV for specified operation. This channel also has an internal PGA.
51	$\overline{EA}$	This pin is used as an input for emulation. When held high, this input enables the device to fetch code from internal program memory locations. The ADE7116/ADE7156/ADE7166/ADE7169 do not support external code memory. This pin should not be left floating.
52, 53	I_{PA}, I_N	Analog Inputs for Current Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±400 mV for specified operation. This channel also has an internal PGA.
54	AGND	This pin provides the ground reference for the analog circuitry.
55	I_{PB}	Analog Input for Second Current Channel (I_{PB}). This input is fully differential with a maximum differential level of ±400 mV, referred to I_N for specified operation. This channel also has an internal PGA.
56	$\overline{RESET}$	Reset Input, Active Low.
57	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V ± 0.1% and a maximum temperature coefficient of 50 ppm/°C. This pin should be decoupled with a 1 µF capacitor in parallel with a ceramic 100 nF capacitor.
58	V_{BAT}	Power Supply Input from the Battery with a 2.4 V to 3.7 V Range. This pin is connected internally to V_{DD} when the battery is selected as the power supply for the ADE7116/ADE7156/ADE7166/ADE7169.

Pin No.	Mnemonic	Description
59	V_{INTA}	This pin provides access to the on-chip 2.5 V analog LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
60	V_{DD}	3.3 V Power Supply Input from the Regulator. This pin is connected internally to V_{SWOUT} when the regulator is selected as the power supply for the ADE7116/ADE7156/ADE7166/ADE7169. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
61	V_{SWOUT}	3.3 V Power Supply Output. This pin provides the supply voltage for the LDOs and internal circuitry of the ADE7116/ADE7156/ADE7166/ADE7169. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
62	V_{INTD}	This pin provides access to the on-chip 2.5 V digital LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
63	DGND	Ground Reference for Digital Circuitry.
64	V_{DCIN}	Analog Input for DC Voltage Monitoring. The maximum input voltage on this pin is V_{SWOUT} with respect to AGND. This pin is used to monitor the preregulated dc voltage.
EP	Exposed Pad	The exposed pad on the bottom of the LFCSP enhances thermal performance and is electrically connected to ground inside the package. It is recommended that the exposed pad be connected to the ground plane on the board.

TYPICAL PERFORMANCE CHARACTERISTICS

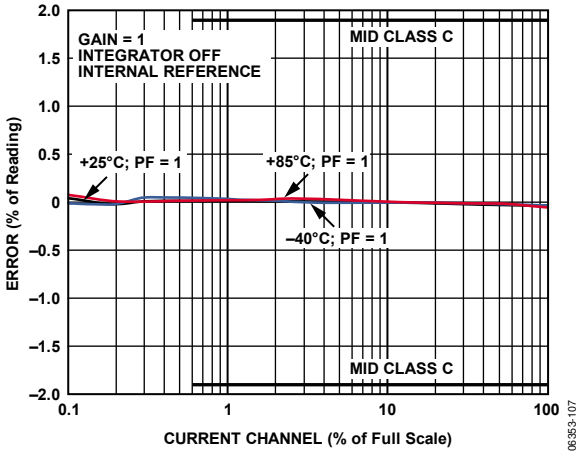

Figure 11. Active Energy Error as a Percentage of Reading (Gain = 1) over Temperature with Internal Reference, Integrator Off

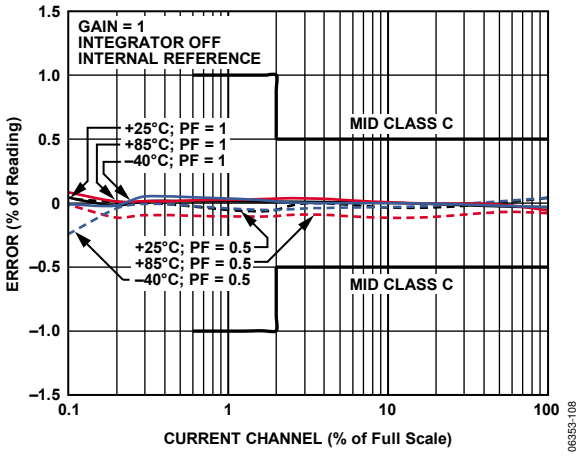

Figure 12. Active Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference, Integrator Off

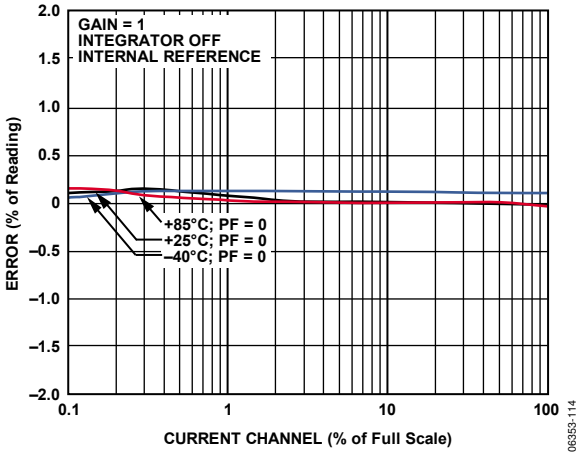

Figure 13. Reactive Energy Error as a Percentage of Reading (Gain = 1) over Temperature with Internal Reference, Integrator Off

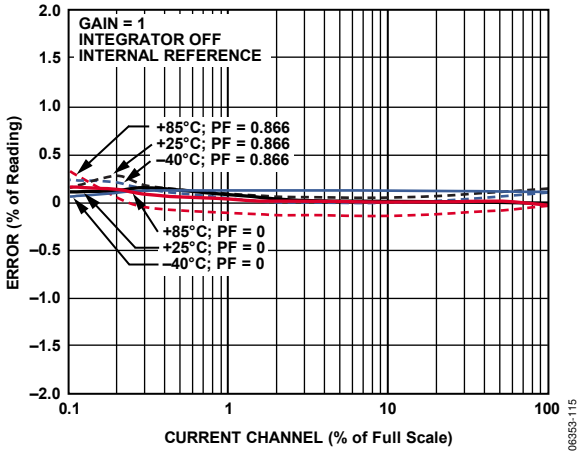

Figure 14. Reactive Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference, Integrator Off

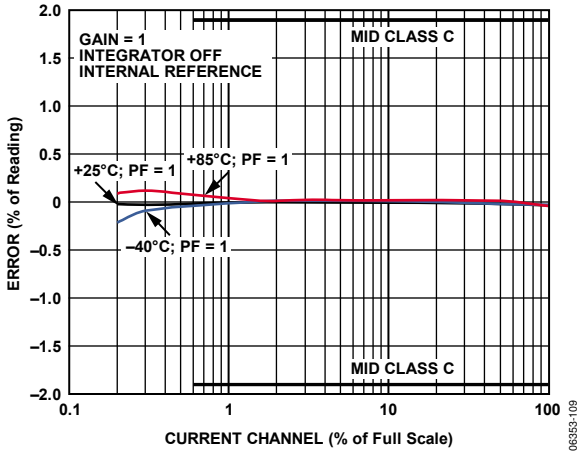

Figure 15. Current RMS Error as a Percentage of Reading (Gain = 1) over Temperature with Internal Reference, Integrator Off

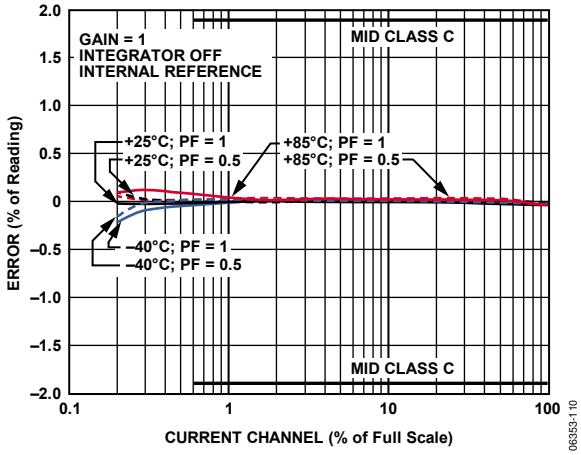

Figure 16. Current RMS Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference, Integrator Off

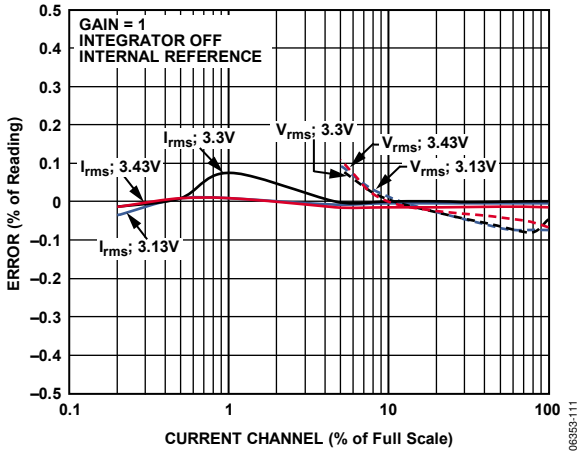

Figure 17. Voltage and Current RMS Error as a Percentage of Reading (Gain = 1) over Power Supply with Internal Reference, Integrator Off

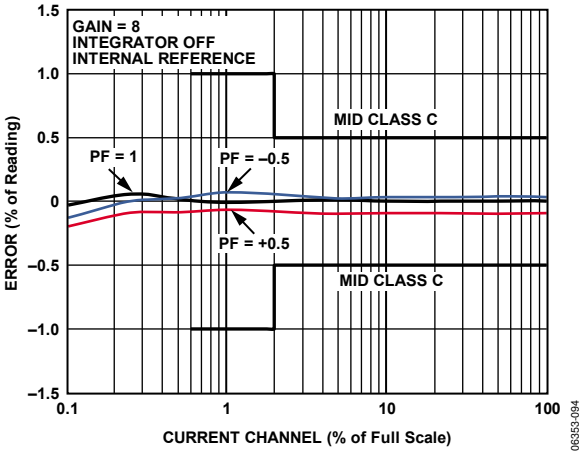

Figure 20. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference, Integrator Off

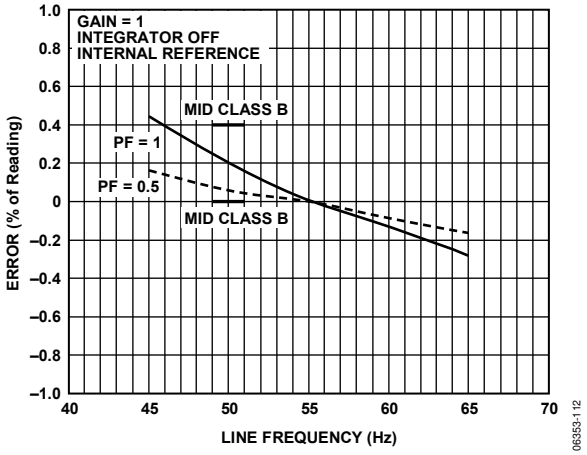

Figure 18. Active Energy Error as a Percentage of Reading (Gain = 1) over Frequency with Internal Reference, Integrator Off

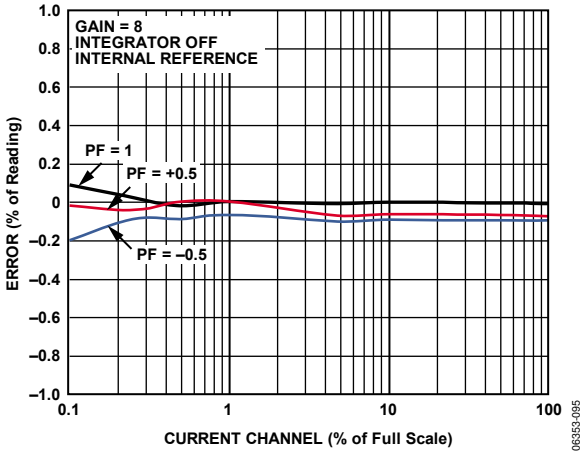

Figure 21. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference, Integrator Off

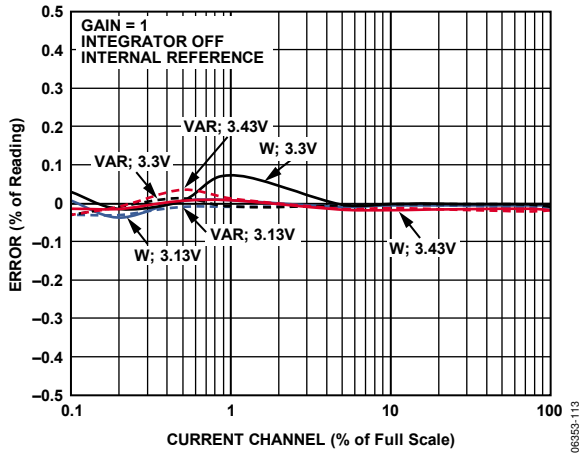

Figure 19. Active and Reactive Energy Error as a Percentage of Reading (Gain = 1) over Power Supply with Internal Reference, Integrator Off

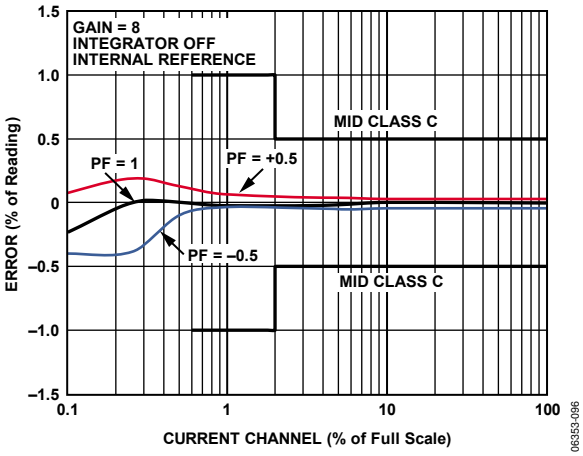

Figure 22. Current RMS Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference, Integrator Off

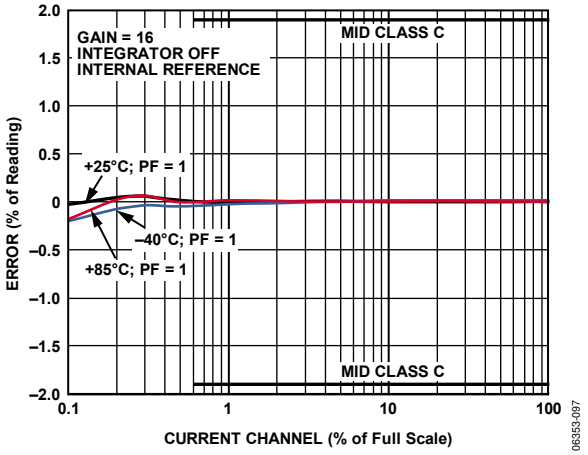

Figure 23. Active Energy Error as a Percentage of Reading (Gain = 16) over Temperature with Internal Reference, Integrator Off

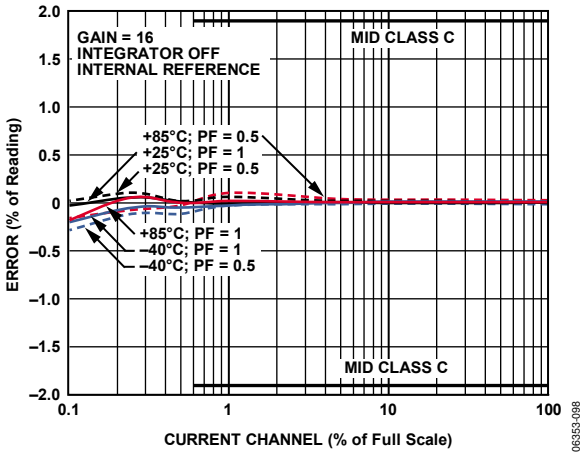

Figure 24. Active Energy Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference, Integrator Off

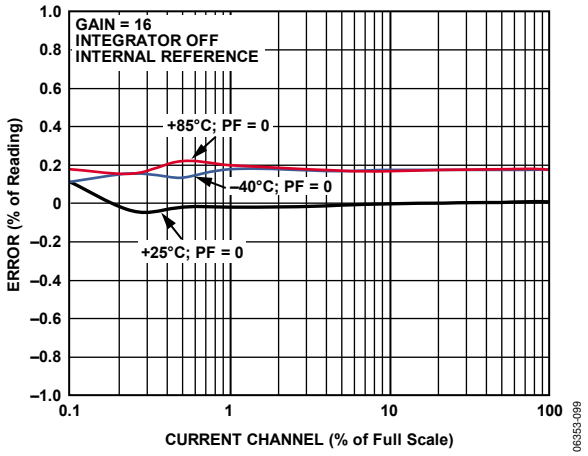

Figure 25. Reactive Energy Error as a Percentage of Reading (Gain = 16) over Temperature with Internal Reference, Integrator Off

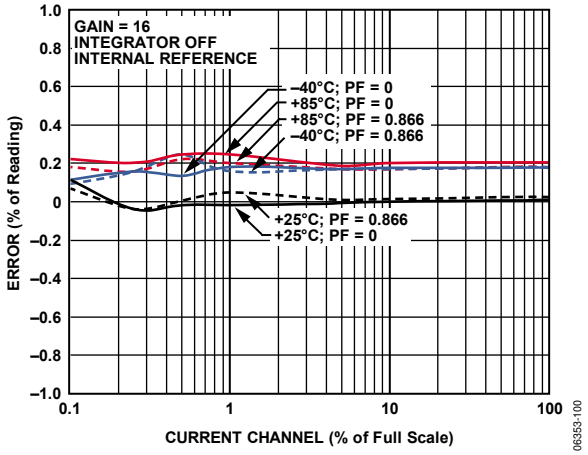

Figure 26. Reactive Energy Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference, Integrator Off

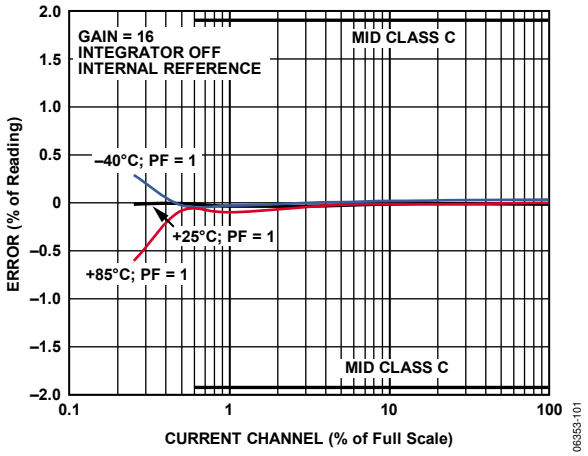

Figure 27. Current RMS Error as a Percentage of Reading (Gain = 16) over Temperature with Internal Reference, Integrator Off

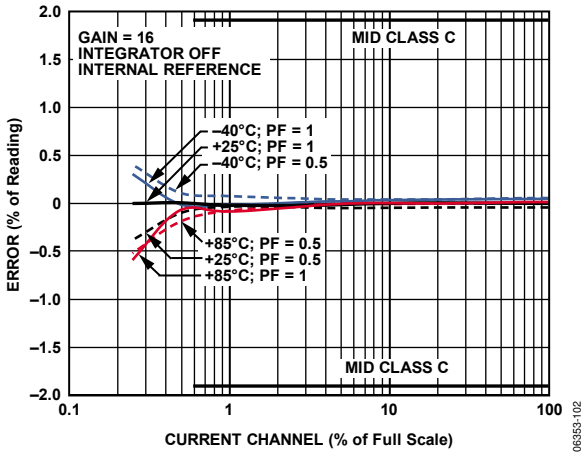

Figure 28. Current RMS Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference, Integrator Off

PERFORMANCE CURVES FOR THE ADE7169 AND ADE7569 ONLY

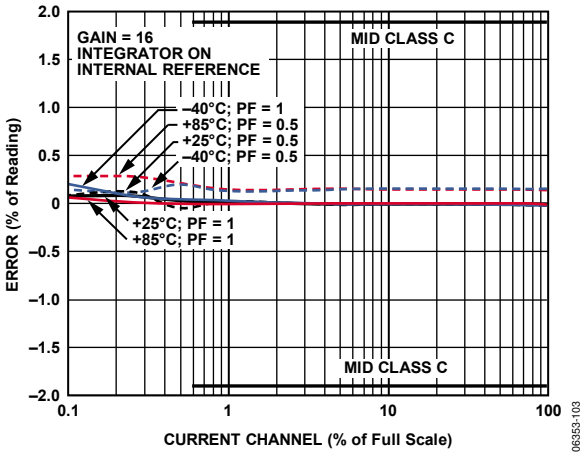

Figure 29. Active Energy Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference, Integrator On

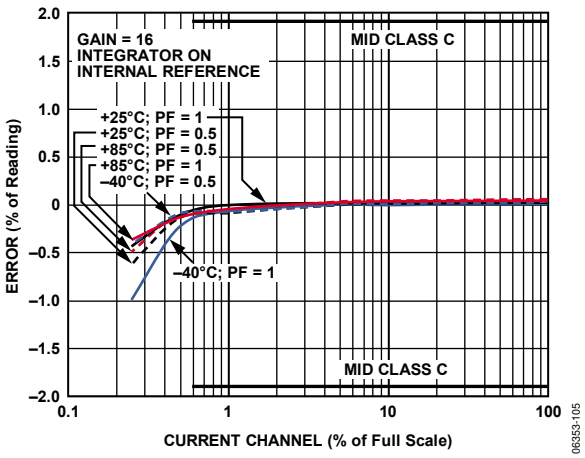

Figure 31. Current RMS Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference, Integrator On

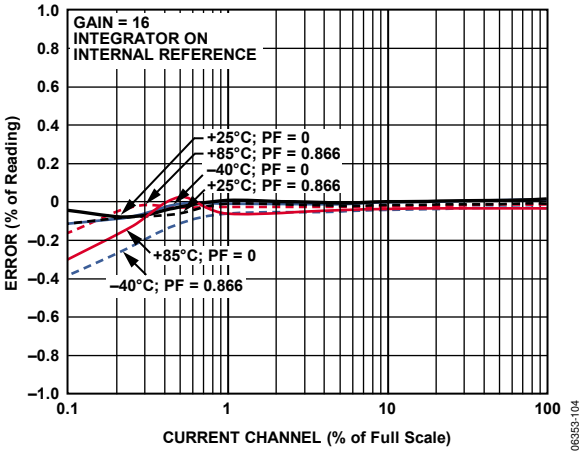

Figure 30. Reactive Energy Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference, Integrator On