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Single-Phase Energy Measurement IC with 8052 MCU, RTC, and LCD Driver

ADE7518

GENERAL FEATURES

- Wide supply voltage operation: 2.4 V to 3.7 V
- Internal bipolar switch between regulated and battery inputs
- Ultralow power operation with power saving modes
  - Full operation: 4 mA to 1.6 mA (PLL clock dependent)
  - Battery mode: 3.2 mA to 400 µA (PLL clock dependent)
  - Sleep mode
    - Real-time clock (RTC) mode: 1.5 µA
    - RTC and LCD mode: 27 µA
- Reference: 1.2 V ± 0.1% (10 ppm/°C drift)
- 64-lead RoHS package option
  - Low profile quad flat package (LQFP)
- Operating temperature range: −40°C to +85°C

ENERGY MEASUREMENT FEATURES

- Proprietary analog-to-digital converters (ADCs) and digital signal processing (DSP) provide high accuracy active (WATT), reactive (VAR), and apparent energy (VA) measurement
  - Less than 0.1% error on active energy over a dynamic range of 1000 to 1 @ 25°C
  - Less than 0.5% error on reactive energy over a dynamic range of 1000 to 1 @ 25°C
  - Less than 0.5% error on root mean square (rms) measurements over a dynamic range of 500 to 1 for current (I_{rms}) and 100 to 1 for voltage (V_{rms}) @ 25°C
  - Supports IEC 62053-21, IEC 62053-22, IEC 62053-23, EN 50470-3 Class A, Class B, and Class C, and ANSI C12-16
- Differential input with programmable gain amplifiers (PGAs) supports shunts and current transformers
- High frequency outputs proportional to I_{rms}, active, reactive, or apparent power (AP)

MICROPROCESSOR FEATURES

- 8052-based core
  - Single-cycle 4 MIPS 8052 core
  - 8052-compatible instruction set
  - 32.768 kHz external crystal with on-chip PLL
  - Two external interrupt sources
  - External reset pin
- Low power battery mode
  - Wake-up from I/O, alarm, and universal asynchronous receiver/transmitter (UART)
  - LCD driver operation
- Real-time clock
  - Counter for seconds, minutes, and hours
  - Automatic battery switchover for RTC backup
  - Operation down to 2.4 V
  - Ultralow battery supply current: 1.5 µA
  - Selectable output frequency: 1 Hz to 16.384 kHz
  - Embedded digital crystal frequency compensation for calibration and temperature variation: 2 ppm resolution
- Integrated LCD driver
  - 108-segment driver
  - 2×, 3×, or 4× multiplexing
  - LCD voltages generated with external resistors
- On-chip peripherals
  - UART, SPI or I^2C, and watchdog timer
- Power supply management with user-selectable levels
- Memory: 16 kB flash memory, 512 bytes RAM
- Development tools
  - Single-pin emulation
  - IDE-based assembly and C-source debugging

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

1/09—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADE7518[1] integrates the Analog Devices, Inc., energy (ADE) metering IC analog front end and fixed function DSP solution with an enhanced 8052 MCU core, an RTC, an LCD driver, and all the peripherals to make an electronic energy meter with an LCD display in a single part.

The ADE measurement core includes active, reactive, and apparent energy calculations, as well as voltage and current rms measurements. This information is ready to use for energy billing by using built-in energy scalars. Many power line supervisory features, such as SAG, peak, and zero crossing, are included in the energy measurement DSP to simplify energy meter design.

The microprocessor functionality includes a single-cycle 8052 core, a real-time clock with a power supply backup pin, a UART, and an SPI or I²C® interface. The ready-to-use information from the ADE core reduces the program memory size requirement, making it easy to integrate complicated design into 16 kB of flash memory.

The ADE7518 also includes a 108-segment LCD driver. This driver generates waveforms capable of driving LCDs up to 3.3 V.

FUNCTIONAL BLOCK DIAGRAM

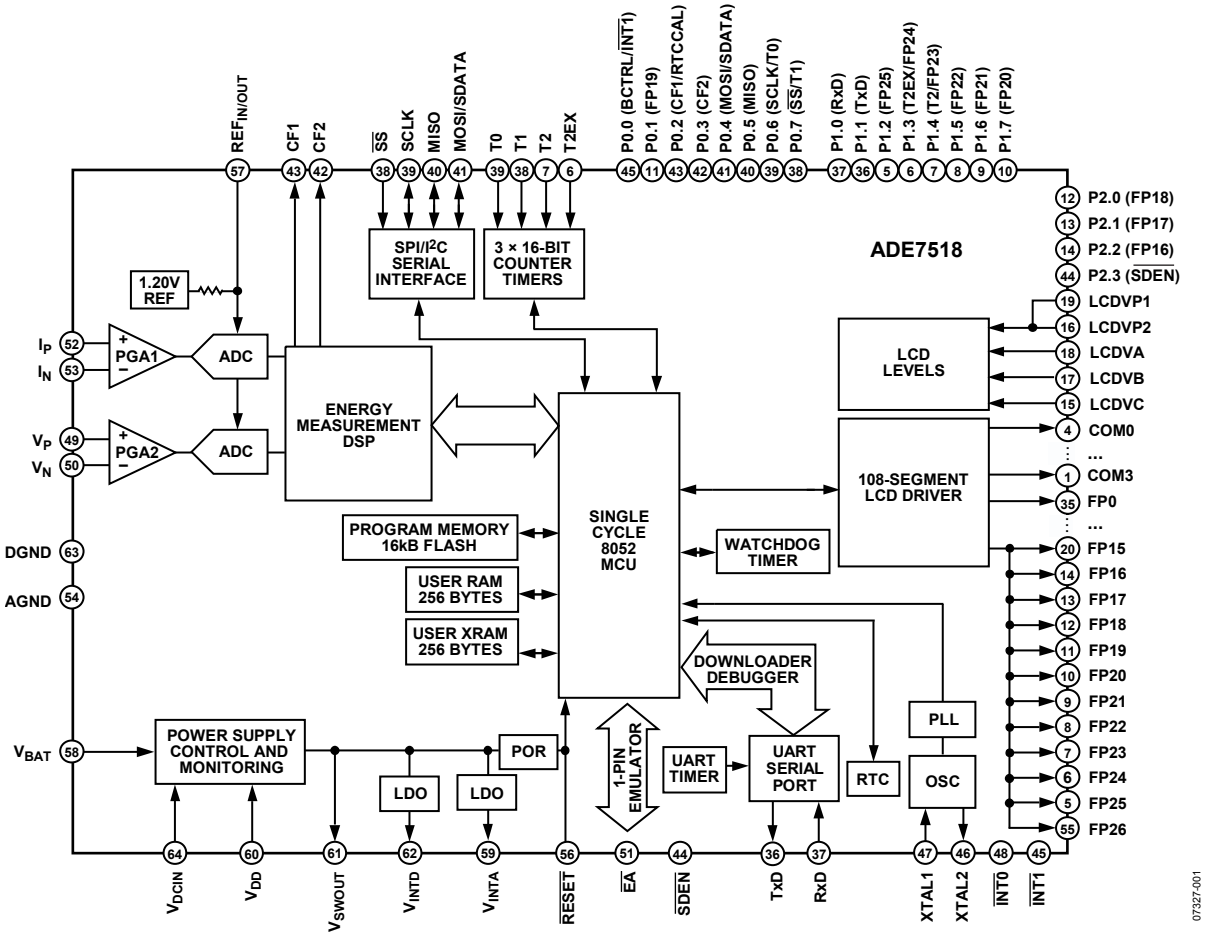

Figure 1.

[1] Patents pending.

SPECIFICATIONS

V_{DD} = 3.3 V ± 5%, AGND = DGND = 0 V, on-chip reference XTAL = 32.768 kHz, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

ENERGY METERING

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MEASUREMENT ACCURACY[1]					
Phase Error Between Channels					
PF = 0.8 Capacitive		±0.05		Degrees	37° phase lead
PF = 0.5 Inductive		±0.05		Degrees	60° phase lag
Active Energy Measurement Error[2]		0.1		% of reading	Over a dynamic range of 1000 to 1 @ 25°C
AC Power Supply Rejection[2]					V_{DD} = 3.3 V + 100 mV rms/120 Hz
Output Frequency Variation		0.01		%	$I_P = V_P$ = ±100 mV rms
DC Power Supply Rejection[2]					V_{DD} = 3.3 V ± 117 mV dc
Output Frequency Variation		0.01		%	
Active Energy Measurement Bandwidth[1]		8		kHz	
Reactive Energy Measurement Error[2]		0.5		% of reading	Over a dynamic range of 1000 to 1 @ 25°C
V_{rms} Measurement Error[2]		0.5		% of reading	Over a dynamic range of 100 to 1 @ 25°C
V_{rms} Measurement Bandwidth[1]		3.9		kHz	
I_{rms} Measurement Error[2]		0.5		% of reading	Over a dynamic range of 500 to 1 @ 25°C
I_{rms} Measurement Bandwidth[1]		3.9		kHz	
ANALOG INPUTS					
Maximum Signal Levels			±400	mV peak	$V_P - V_N$ differential input
			±400	mV peak	$I_P - I_N$ differential input
Input Impedance (DC)		770		kΩ	
ADC Offset Error[2]		±10		mV	PGA1 = PGA2 = 1
		±1		mV	PGA1 = 16
Gain Error[2]					
Current Channel	−3		+ 3	%	I_P = 0.4 V dc or I_P = 0.4 dc
Voltage Channel	−3		+ 3	%	Voltage channel = 0.4 V dc
Gain Error Match		±0.2		%	
CF1 AND CF2 PULSE OUTPUT					
Maximum Output Frequency		13.5		kHz	$V_P - V_N$ = 400 mV peak, $I_P - I_N$ = 250 mV, PGA1 = 2 sine wave
Duty Cycle		50		%	If CF1 or CF2 frequency, >5.55 Hz
Active High Pulse Width		90		ms	If CF1 or CF2 frequency, <5.55 Hz

[1] These specifications are not production tested but are guaranteed by design and/or characterization data on production release.
[2] See the Terminology section for definition.

ANALOG PERIPHERALS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER-ON RESET (POR)					
V_{DD} POR					
Detection Threshold	2.5		2.95	V	
POR Active Timeout Period		33		ms	
V_{SWOUT} POR					
Detection Threshold	1.8		2.2	V	
POR Active Timeout Period		20		ms	
V_{INTD} POR					
Detection Threshold	2.03		2.22	V	
POR Active Timeout Period		16		ms	
V_{INTA} POR					
Detection Threshold	2.05		2.15	V	
POR Active Timeout Period		120		ms	
BATTERY SWITCHOVER					
Voltage Operating Range (V_{SWOUT})	2.4		3.7	V	
V_{DD} to V_{BAT} Switching					
Switching Threshold (V_{DD})	2.5		2.95	V	
Switching Delay		10		ns	When V_{DD} to V_{BAT} switch activated by V_{DD}
		30		ms	When V_{DD} to V_{BAT} switch activated by V_{DCIN}
V_{BAT} to V_{DD} Switching					
Switching Threshold (V_{DD})	2.5		2.95	V	
Switching Delay		30		ms	Based on V_{DD} > 2.75 V
V_{SWOUT} To V_{BAT} Leakage Current		10		nA	V_{BAT} = 0 V, V_{SWOUT} = 3.43 V, T_A = 25°C
LCD, RESISTOR LADDER ACTIVE					
Leakage Current			±20	nA	1/2 and 1/3 bias modes, no load
V1 Segment Line Voltage	LCDVA – 0.1		LCDVA	V	Current on segment line = −2 µA
V2 Segment Line Voltage	LCDVB – 0.1		LCDVB	V	Current on segment line = −2 µA
V3 Segment Line Voltage	LCDVC – 0.1		LCDVC	V	Current on segment line = −2 µA
ON-CHIP REFERENCE					
Reference Error			±0.9	mV	T_A = 25°C
Power Supply Rejection		80		dB	
Temperature Coefficient		10	50	ppm/°C	

DIGITAL INTERFACE

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
All Inputs Except XTAL1, XTAL2, BCTRL, $\overline{INT0}$, $\overline{INT1}$, $\overline{RESET}$					
Input High Voltage, V_{INH}	2.0			V	
Input Low Voltage, V_{INL}			0.4	V	
BCTRL, $\overline{INT0}$, $\overline{INT1}$, $\overline{RESET}$					
Input High Voltage, V_{INH}	1.3			V	
Input Low Voltage, V_{INL}			0.4	V	
Input Currents					
$\overline{RESET}$			100	nA	$\overline{RESET}$ = V_{SWOUT} = 3.3 V
Port 0, Port 1, Port 2			±100	nA	Internal pull-up disabled, input = 0 V or V_{SWOUT}
		−3.75	−8.5	µA	Internal pull-up enabled, input = 0 V, V_{SWOUT} = 3.3 V
Input Capacitance		10		pF	All digital inputs
FLASH MEMORY					
Endurance[1]	10,000			Cycles	
Data Retention[2]	20			Years	T_J = 85°C
CRYSTAL OSCILLATOR					
Crystal Equivalent Series Resistance	30		50	kΩ	
Crystal Frequency	32	32.768	33.5	kHz	
XTAL1 Input Capacitance		12		pF	
XTAL2 Output Capacitance		12		pF	
MCU CLOCK RATE (f_{CORE})		4.096		MHz	Crystal = 32.768 kHz and CD[2:0] = 0b000
		32		kHz	Crystal = 32.768 kHz and CD[2:0] = 0b111
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	2.4			V	V_{DD} = 3.3 V ± 5%
I_{SOURCE}			80	µA	
Output Low Voltage, V_{OL}[3]			0.4	V	V_{DD} = 3.3 V ± 5%
I_{SINK}			2	mA	
START-UP TIME[4]					
PSM0 Power-On Time		448		ms	V_{DD} at 2.75 V to PSM0 code execution
From Power Saving Mode 1 (PSM1)					
PSM1 → PSM0		130		ms	V_{DD} at 2.75 V to PSM0 code execution
From Power Saving Mode 2 (PSM2)					
PSM2 → PSM1		48		ms	Wake-up event to PSM1 code execution
PSM2 → PSM0		186		ms	V_{DD} at 2.75 V to PSM0 code execution
POWER SUPPLY INPUTS					
V_{DD}	3.13	3.3	3.46	V	
V_{BAT}	2.4	3.3	3.7	V	
INTERNAL POWER SUPPLY SWITCH (V_{SWOUT})					
V_{BAT} to V_{SWOUT} On Resistance			22	Ω	V_{BAT} = 2.4 V
V_{DD} to V_{SWOUT} On Resistance			10.2	Ω	V_{DD} = 3.13 V
V_{BAT} ⟷ V_{DD} Switching Open Time		40		ns	
BCTRL State Change and Switch Delay		18		µs	
V_{SWOUT} Output Current Drive		1	6	mA	
POWER SUPPLY OUTPUTS					
V_{INTA}	2.25		2.75	V	
V_{INTD}	2.3		2.70	V	
V_{INTA} Power Supply Rejection		60		dB	
V_{INTD} Power Supply Rejection		50		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY CURRENTS					
Current in Normal Mode (PSM0)		4	5.3	mA	f_{CORE} = 4.096 MHz, LCD and meter active
		2.1		mA	f_{CORE} = 1.024 MHz, LCD and meter active
		1.6		mA	f_{CORE} = 32.768 kHz, LCD and meter active
		3.2	4.25	mA	f_{CORE} = 4.096 MHz, meter DSP active, metering ADC powered down
		3	3.9	mA	f_{CORE} = 4.096 MHz, metering ADC and DSP powered down
Current in PSM1		3.2	5.05	mA	f_{CORE} = 4.096 MHz, LCD active, V_{BAT} = 3.7 V
		880		µA	f_{CORE} = 1.024 MHz, LCD active
Current in PSM2		38		µA	LCD active at 3.3 V + RTC (real-time clock)
		1.5		µA	RTC only, T_A = 25°C, V_{BAT} = 3.3 V
POWER SUPPLY CURRENTS					
Current in Normal Mode (PSM0)		4	5.3	mA	f_{CORE} = 4.096 MHz, LCD and meter active

[1] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[2] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22 Method A117. Retention lifetime derates with junction temperature.
[3] Test performed with all the I/Os set to a low output level.
[4] Delay between power supply valid and execution of first instruction by 8052 core.

TIMING SPECIFICATIONS

AC inputs during testing were driven at V_{SWOUT} − 0.5 V for Logic 1 and 0.45 V for Logic 0. Timing measurements were made at V_{IH} minimum for Logic 1 and V_{IL} maximum for Logic 0, as shown in Figure 2.

For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs, as shown in Figure 2.

For Table 4 to Table 9, C_{LOAD} = 80 pF for all outputs, V_{DD} = 2.7 V to 3.6 V, and all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

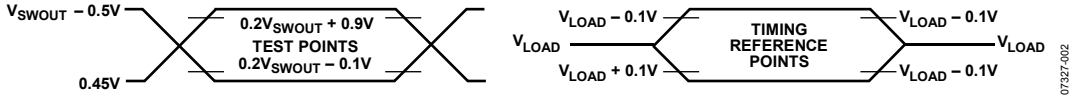

Figure 2. Timing Waveform Characteristics

Table 4. Clock Input (External Clock Driven XTAL1) Parameters

		32.768 kHz External Crystal			
Parameter	**Description**	**Min**	**Typ**	**Max**	**Unit**
t_{CK}	XTAL1 period		30.52		µs
t_{CKL}	XTAL1 width low		6.26		µs
t_{CKH}	XTAL1 width high		6.26		µs
t_{CKR}	XTAL1 rise time		9		ns
t_{CKF}	XTAL1 fall time		9		ns
$1/t_{CORE}$	Core clock frequency[1]	0.032768	1.024	4.096	MHz

[1] The ADE7518 internal PLL locks onto a multiple (512 times) of the 32.768 kHz external crystal frequency to provide a stable 4.096 MHz internal clock for the system. The core can operate at this frequency or at a binary submultiple defined by the CD[2:0] bits, selected via the POWCON SFR (see Table 24).

Table 5. I²C-Compatible Interface Timing Parameters (400 kHz)

Parameter	**Description**	**Typ**	**Unit**
t_{BUF}	Bus-free time between stop condition and start condition	1.3	µs
t_L	SCLK low pulse width	1.36	µs
t_H	SCLK high pulse width	1.14	µs
t_{SHD}	Start condition hold time	251.35	µs
t_{DSU}	Data setup time	740	ns
t_{DHD}	Data hold time	400	ns
t_{RSU}	Setup time for repeated start	12.5	ns
t_{PSU}	Stop condition setup time	400	ns
t_R	Rise time of both SCLK and SDATA	200	ns
t_F	Fall time of both SCLK and SDATA	300	ns
t_{SUP}[1]	Pulse width of spike suppressed	50	ns

[1] Input filtering on both the SCLK and SDATA inputs suppresses noise spikes of less than 50 ns.

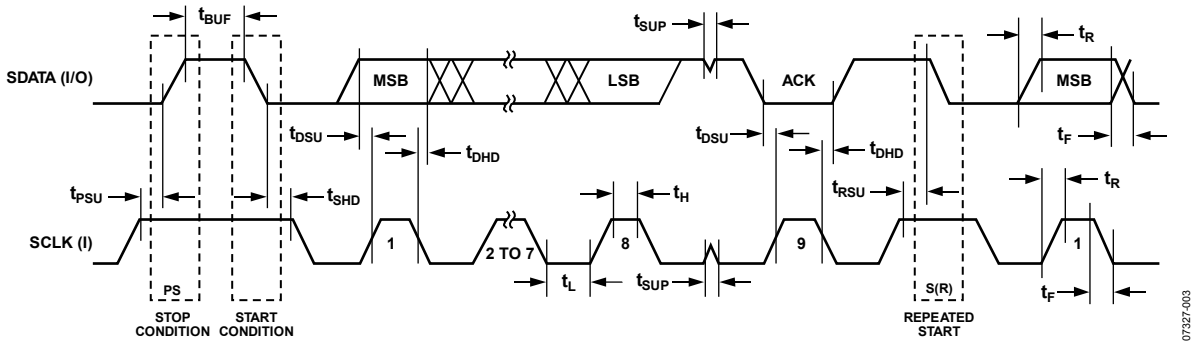

Figure 3. I²C-Compatible Interface Timing

Table 6. SPI Master Mode Timing (SPICPHA = 1) Parameters

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width	$2^{SPIR} \times t_{CORE}$[1]			ns
t_{SH}	SCLK high pulse width	$2^{SPIR} \times t_{CORE}$[1]			ns
t_{DAV}	Data output valid after SCLK edge			$3 \times t_{CORE}$[1]	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge	t_{CORE}[1]			ns
t_{DF}	Data output fall time		19		ns
t_{DR}	Data output rise time		19		ns
t_{SR}	SCLK rise time		19		ns
t_{SF}	SCLK fall time		19		ns

[1] t_{CORE} depends on the clock divider or CD[2:0] bits of the POWCON SFR (see Table 24); $t_{CORE} = 2^{CD}/4.096$ MHz.

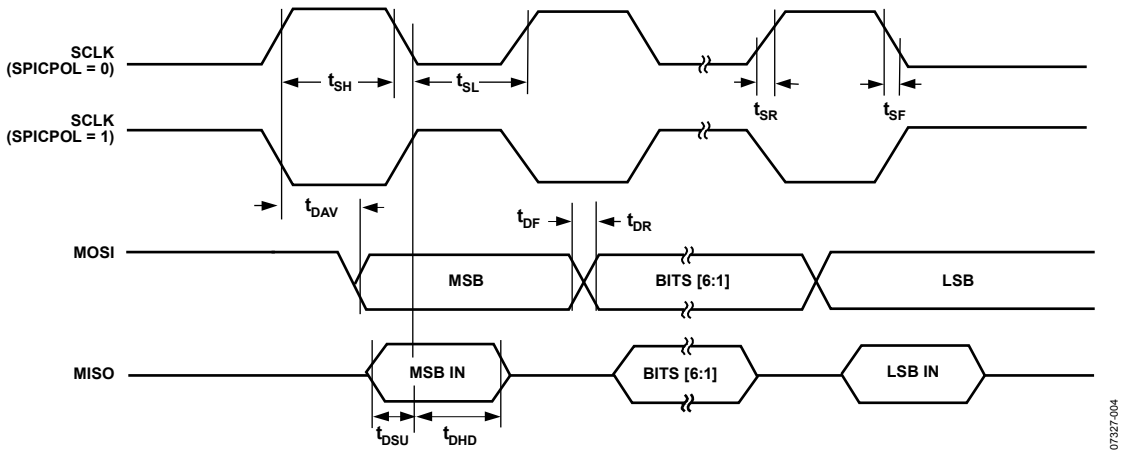

Figure 4. SPI Master Mode Timing (SPICPHA = 1)

Table 7. SPI Master Mode Timing (SPICPHA = 0) Parameters

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width	$2^{SPIR} \times t_{CORE}$[1]	(SPIR + 1) × t_{CORE}[1]		ns
t_{SH}	SCLK high pulse width	$2^{SPIR} \times t_{CORE}$[1]	(SPIR + 1) × t_{CORE}[1]		ns
t_{DAV}	Data output valid after SCLK edge			3 × t_{CORE}[1]	ns
t_{DOSU}	Data output setup before SCLK edge			75	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge	t_{CORE}[1]			ns
t_{DF}	Data output fall time		19		ns
t_{DR}	Data output rise time		19		ns
t_{SR}	SCLK rise time		19		ns
t_{SF}	SCLK fall time		19		ns

[1] t_{CORE} depends on the clock divider or CD[2:0] bits of the POWCON SFR (see Table 24); $t_{CORE} = 2^{CD}/4.096$ MHz.

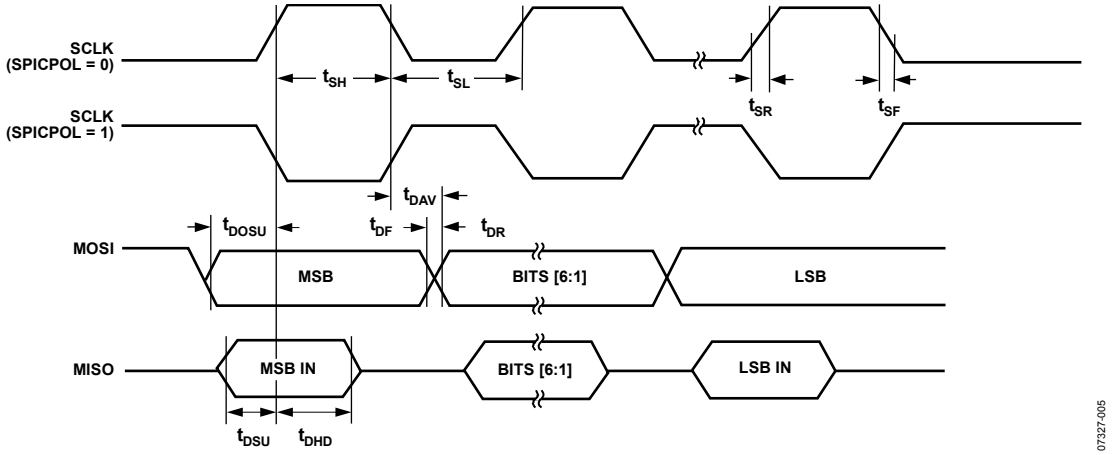

Figure 5. SPI Master Mode Timing (SPICPHA = 0)

Table 8. SPI Slave Mode Timing (SPICPHA = 1) Parameters

Parameter	Description	Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLK edge	145			ns
t_{SL}	SCLK low pulse width	$6 \times t_{CORE}$[1]			ns
t_{SH}	SCLK high pulse width	$6 \times t_{CORE}$[1]			ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge	$2 \times t_{CORE}$[1] + 0.5			µs
t_{DF}	Data output fall time		19		ns
t_{DR}	Data output rise time		19		ns
t_{SR}	SCLK rise time		19		ns
t_{SF}	SCLK fall time		19		ns
t_{SFS}	$\overline{SS}$ high after SCLK edge	0			ns

[1] t_{CORE} depends on the clock divider or CD[2:0] bits of the POWCON SFR (see Table 24); $t_{CORE} = 2^{CD}/4.096$ MHz.

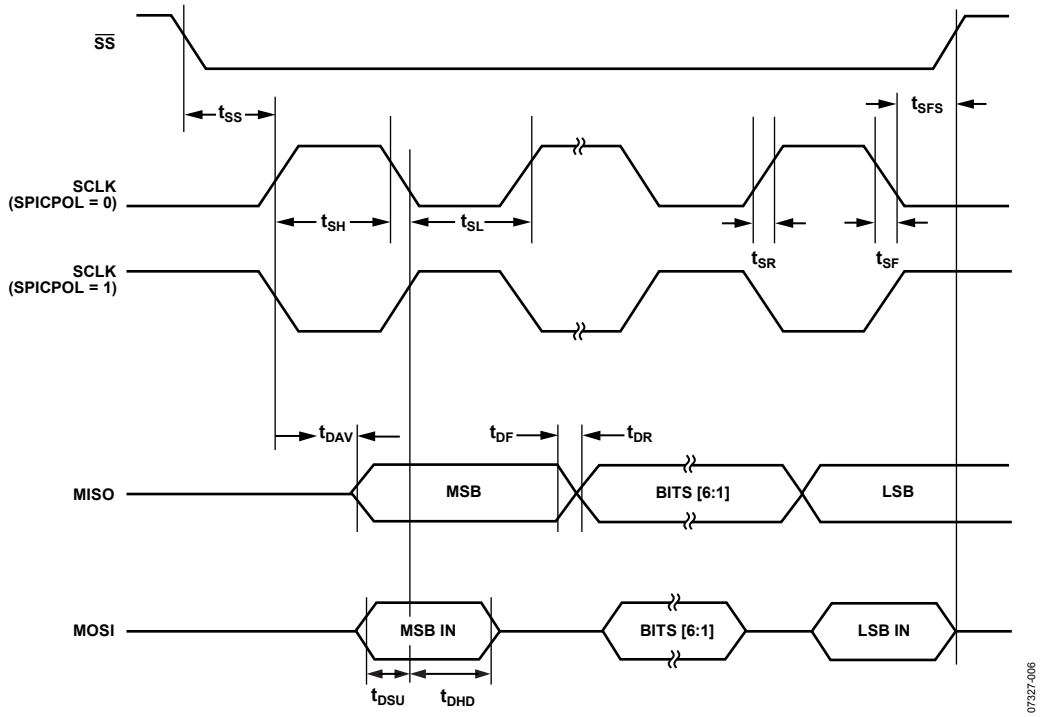

Figure 6. SPI Slave Mode Timing (SPICPHA = 1)

Table 9. SPI Slave Mode Timing (SPICPHA = 0) Parameters

Parameter	Description	Min	Typ	Max	Unit
t_{SS}	$\overline{SS}$ to SCLK edge	145			ns
t_{SL}	SCLK low pulse width	$6 \times t_{CORE}$[1]			ns
t_{SH}	SCLK high pulse width	$6 \times t_{CORE}$[1]			ns
t_{DAV}	Data output valid after SCLK edge			25	ns
t_{DSU}	Data input setup time before SCLK edge	0			ns
t_{DHD}	Data input hold time after SCLK edge	$2 \times t_{CORE}$[1] + 0.5			µs
t_{DF}	Data output fall time		19		ns
t_{DR}	Data output rise time		19		ns
t_{SR}	SCLK rise time		19		ns
t_{SF}	SCLK fall time		19		ns
t_{DOSS}	Data output valid after $\overline{SS}$ edge	0			ns
t_{SFS}	$\overline{SS}$ high after SCLK edge	0			ns

[1] t_{CORE} depends on the clock divider or CD[2:0] bits of the POWCON SFR (see Table 24); $t_{CORE} = 2^{CD}/4.096$ MHz.

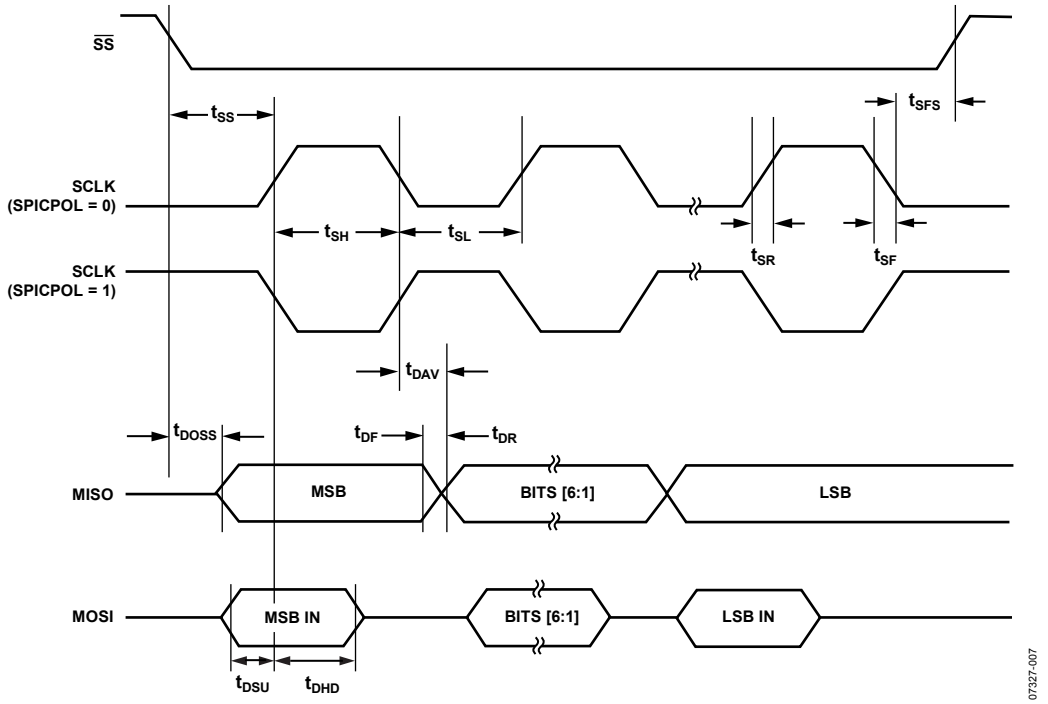

Figure 7. SPI Slave Mode Timing (SPICPHA = 0)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 10.

Parameter	Rating
V_{DD} to DGND	−0.3 V to +3.7 V
V_{BAT} to DGND	−0.3 V to +3.7 V
V_{DCIN} to DGND	−0.3 V to V_{SWOUT} + 0.3 V
Input LCD Voltage to AGND, LCDVA, LCDVB, LCDVC[1]	−0.3 V to V_{SWOUT} + 0.3 V
Analog Input Voltage to AGND, V_P, V_N, I_P, and I_N	−2 V to +2 V
Digital Input Voltage to DGND	−0.3 V to V_{SWOUT} + 0.3 V
Digital Output Voltage to DGND	−0.3 V to V_{SWOUT} + 0.3 V
Operating Temperature Range (Industrial)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
64-Lead LQFP, Power Dissipation	1 W
Lead Temperature	
Soldering	300°C
Time	30 sec

[1] When used with external resistor divider.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 11. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
64-Lead LQFP	60	20.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

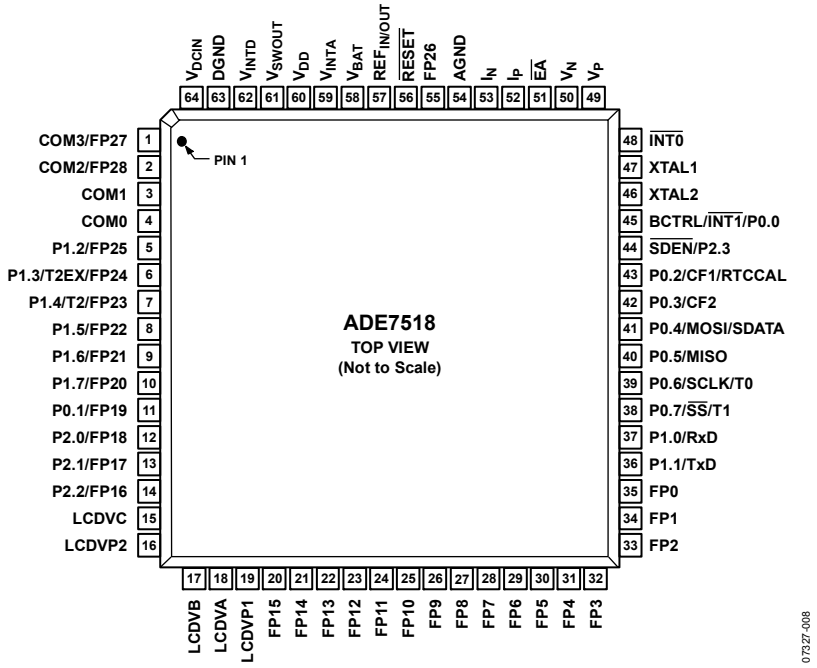

Figure 8. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COM3/FP27	Common Output 3 or LCD Segment Output 27. COM3 is used for LCD backplane.
2	COM2/FP28	Common Output 2 or LCD Segment Output 28. COM2 is used for LCD backplane.
3	COM1	Common Output 1. COM1 is used for LCD backplane.
4	COM0	Common Output 0. COM0 is used for LCD backplane.
5	P1.2/FP25	General-Purpose Digital I/O Port 1.2 or LCD Segment Output 25.
6	P1.3/T2EX/FP24	General-Purpose Digital I/O Port 1.3, Timer 2 Control Input, or LCD Segment Output 24.
7	P1.4/T2/FP23	General-Purpose Digital I/O Port 1.4, Timer 2 Input, or LCD Segment Output 23.
8	P1.5/FP22	General-Purpose Digital I/O Port 1.5 or LCD Segment Output 22.
9	P1.6/FP21	General-Purpose Digital I/O Port 1.6 or LCD Segment Output 21.
10	P1.7/FP20	General-Purpose Digital I/O Port 1.7 or LCD Segment Output 20.
11	P0.1/FP19	General-Purpose Digital I/O Port 0.1 or LCD Segment Output 19.
12	P2.0/FP18	General-Purpose Digital I/O Port 2.0 or LCD Segment Output 18.
13	P2.1/FP17	General-Purpose Digital I/O Port 2.1 or LCD Segment Output 17.
14	P2.2/FP16	General-Purpose Digital I/O Port 2.2 or LCD Segment Output 16.
15	LCDVC	This pin is internally connected to V_{DD}. A resistor should be connected between LCDVC and LCDVB to generate the top two voltages for the LCD waveforms (see the LCD Driver section).
16	LCDVP2	This pin is internally connected to LCDVP1 (see the LCD Driver section).
17	LCDVB	This pin is an input voltage for the LCD driver. A resistor should be connected between LCDVB and LCDVC to generate an intermediate voltage for the LCD driver. In 1/3 bias LCD mode, another resistor must be connected between LCDVB and LCDVA to generate another intermediate voltage. In 1/2 bias LCD mode, LCDVB and LCDVA are internally connected (see the LCD Driver section).
18	LCDVA	This pin is an input voltage for the LCD driver. A resistor should be connected between LCDVA and LCDVP1 to generate an intermediate voltage for the LCD driver. In 1/3 bias LCD mode, another resistor must be connected between LCDVB and LCDVA to generate another intermediate voltage. In 1/2 bias LCD mode, LCDVB and LCDVA are internally connected (see the LCD Driver section).
19	LCDVP1	This pin is an input voltage for the LCD driver. A resistor should be connected between LCDVA and LCDVP1 to generate an intermediate voltage for the LCD driver. Another resistor must be connected between LCDVP1 and DGND to generate another intermediate voltage (see the LCD Driver section).
35 to 20	FP0 to F15	LCD Segment Output 0 to LCD Segment Output 15.
36	P1.1/TxD	General-Purpose Digital I/O Port 1.1 or Transmitter Data Output (Asynchronous).

Pin No.	Mnemonic	Description
37	P1.0/RxD	General-Purpose Digital I/O Port 1.0 or Receiver Data Input (Asynchronous).
38	P0.7/$\overline{SS}$/T1	General-Purpose Digital I/O Port 0.7, Slave Select When SPI is in Slave Mode, or Timer 1 Input.
39	P0.6/SCLK/T0	General-Purpose Digital I/O Port 0.6, Clock Output for I^2C or SPI Port, or Timer 0 Input.
40	P0.5/MISO	General-Purpose Digital I/O Port 0.5 or Data Input for SPI Port.
41	P0.4/MOSI/SDATA	General-Purpose Digital I/O Port 0.4, Data Output for SPI Port, or I^2C-Compatible Data Line.
42	P0.3/CF2	General-Purpose Digital I/O Port 0.3 or Calibration Frequency Logic Output 2. The CF2 logic output gives instantaneous active, reactive, I_{rms}, or apparent power information.
43	P0.2/CF1/RTCCAL	General-Purpose Digital I/O Port 0.2, Calibration Frequency Logic Output 1, or RTC Calibration Frequency Logic Output. The CF1 logic output gives instantaneous active, reactive, I_{rms}, or apparent power information. The RTCCAL logic output gives access to the calibrated RTC output.
44	$\overline{SDEN}$/P2.3	Serial Download Mode Enable or Digital Output Port P2.3. This pin is used to enable serial download mode through a resistor when pulled low on power-up or reset. On reset, this pin momentarily becomes an input and the status of the pin is sampled. If there is no pull-down resistor in place, the pin momentarily goes high and then user code is executed. If the pin is pulled down on reset, the embedded serial download/debug kernel executes, and this pin remains low during the internal program execution. After reset, this pin can be used as a digital output port pin (P2.3).
45	BCTRL/$\overline{INT1}$/P0.0	Digital Input for Battery Control, External Interrupt Input 1, or General-Purpose Digital I/O Port 0.0. This logic input connects V_{DD} or V_{BAT} to V_{SWOUT} internally when set to logic high or logic low, respectively. When left open, the connection between V_{DD} and V_{SWOUT} or between V_{BAT} and V_{SWOUT} is selected internally.
46	XTAL2	A crystal can be connected across this pin and XTAL1 (see the XTAL1 pin description) to provide a clock source for the ADE7518. The XTAL2 pin can drive one CMOS load when an external clock is supplied at XTAL1 or by the gate oscillator circuit. An internal 6 pF capacitor is connected to this pin.
47	XTAL1	An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across XTAL1 and XTAL2 to provide a clock source for the ADE7518. The clock frequency for specified operation is 32.768 kHz. An internal 6 pF capacitor is connected to this pin.
48	$\overline{INT0}$	External Interrupt Input 0.
49, 50	V_P, V_N	Analog Inputs for Voltage Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±400 mV for specified operation. This channel also has an internal PGA.
51	$\overline{EA}$	This pin is used as an input for emulation. When held high, this input enables the device to fetch code from internal program memory locations. The ADE7518 does not support external code memory. This pin should not be left floating.
52, 53	I_P, I_N	Analog Inputs for Current Channel. These inputs are fully differential voltage inputs with a maximum differential level of ±400 mV for specified operation. This channel also has an internal PGA.
54	AGND	This pin provides the ground reference for the analog circuitry.
55	FP26	LCD Segment Output 26.
56	$\overline{RESET}$	Reset Input, Active Low.
57	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V ± 0.1% and a typical temperature coefficient of 50 ppm/°C maximum. This pin should be decoupled with a 1 µF capacitor in parallel with a ceramic 100 nF capacitor.
58	V_{BAT}	Power Supply Input from the Battery with a 2.4 V to 2.7 V Range. This pin is connected internally to V_{DD} when the battery is selected as the power supply for the ADE7518.
59	V_{INTA}	This pin provides access to the on-chip 2.5 V analog LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
60	V_{DD}	3.3 V Power Supply Input from the Regulator. This pin is connected internally to V_{DD} when the regulator is selected as the power supply for the ADE7518. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
61	V_{SWOUT}	3.3 V Power Supply Output. This pin provides the supply voltage for the LDOs and internal circuitry of the ADE7518. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
62	V_{INTD}	This pin provides access to the on-chip 2.5 V digital LDO. No external active circuitry should be connected to this pin. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
63	DGND	This pin provides the ground reference for the digital circuitry.
64	V_{DCIN}	Analog Input for DC Voltage Monitoring. The maximum input voltage on this pin is V_{SWOUT} with respect to AGND. This pin is used to monitor the preregulated dc voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

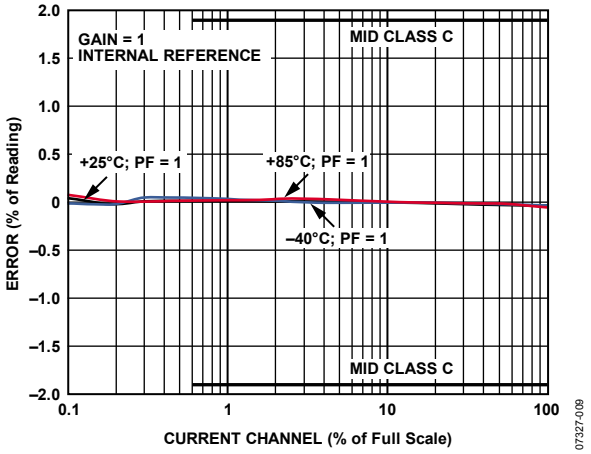

Figure 9. Active Energy Error as a Percentage of Reading (Gain = 1) over Temperature with Internal Reference

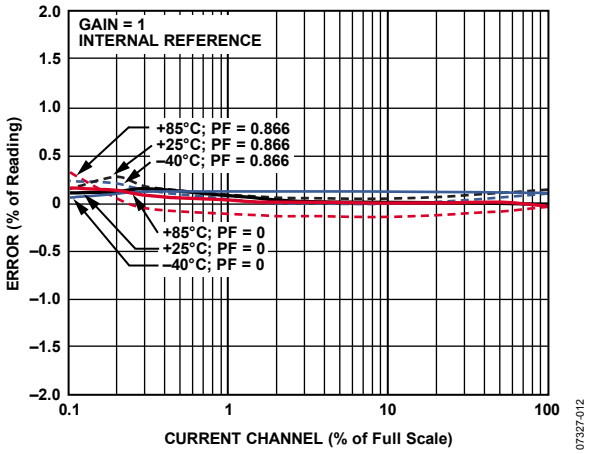

Figure 12. Reactive Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference

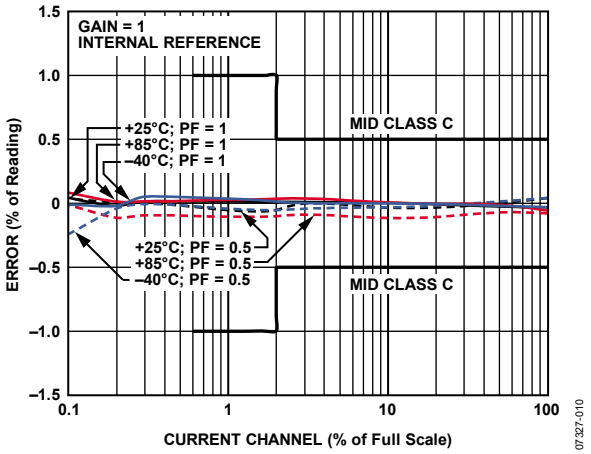

Figure 10. Active Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference

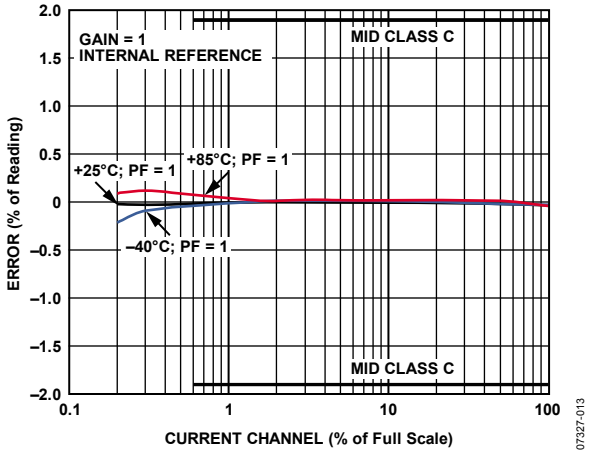

Figure 13. Current RMS Error as a Percentage of Reading (Gain = 1) over Temperature with Internal Reference

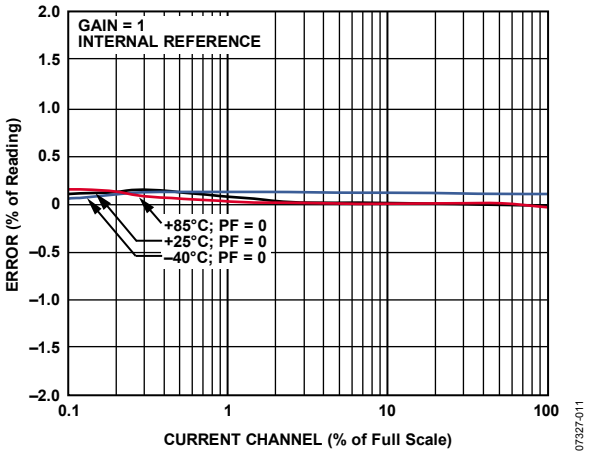

Figure 11. Reactive Energy Error as a Percentage of Reading (Gain = 1) over Temperature with Internal Reference

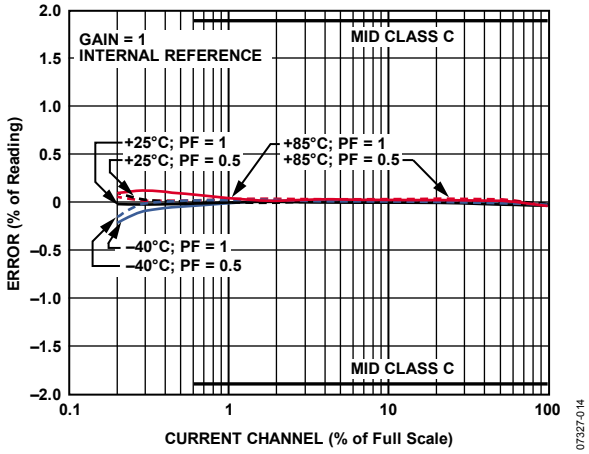

Figure 14. Current RMS Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference

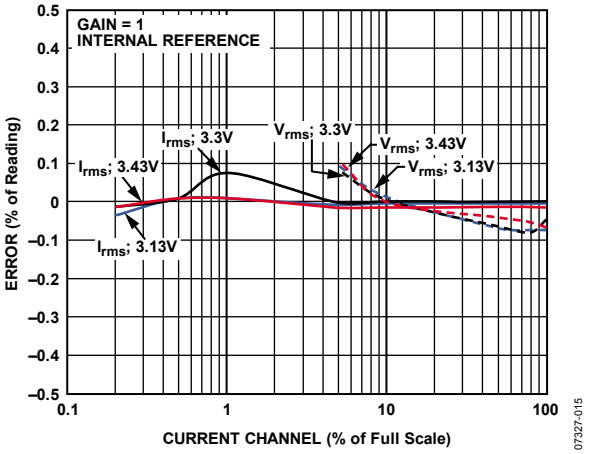

Figure 15. Voltage and Current RMS Error as a Percentage of Reading (Gain = 1) over Power Supply with Internal Reference

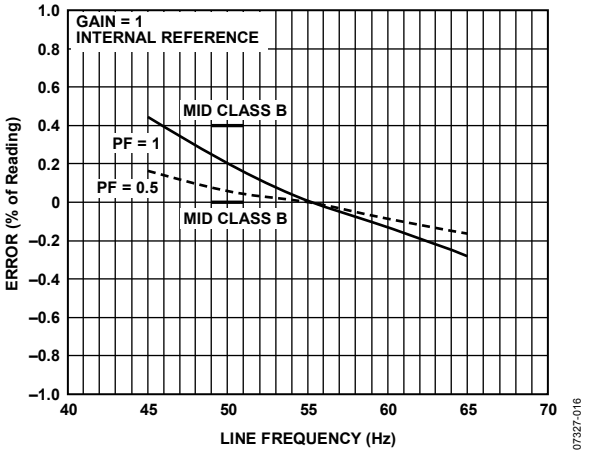

Figure 16. Active Energy Error as a Percentage of Reading (Gain = 1) over Frequency with Internal Reference

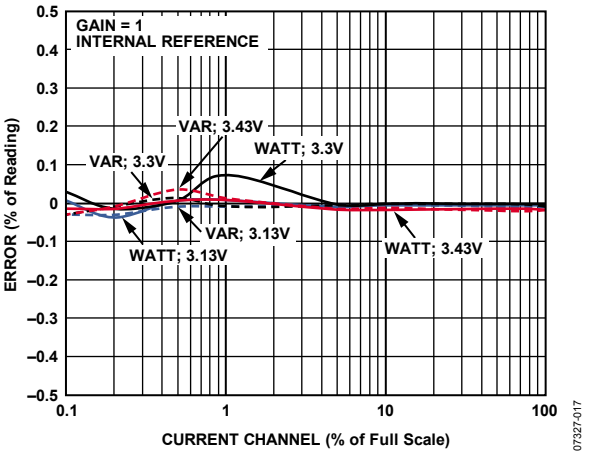

Figure 17. Active and Reactive Energy Error as a Percentage of Reading (Gain = 1) over Power Supply with Internal Reference

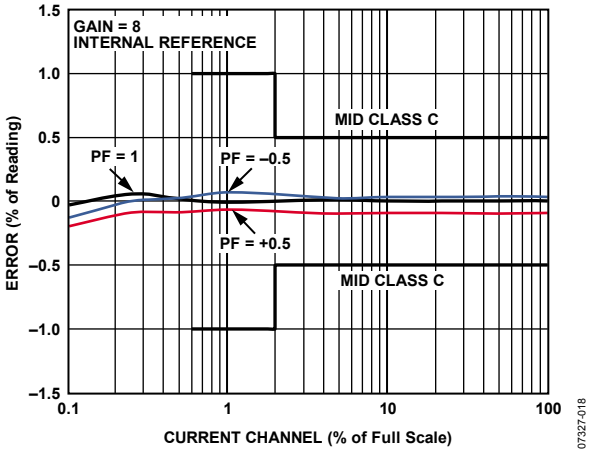

Figure 18. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference

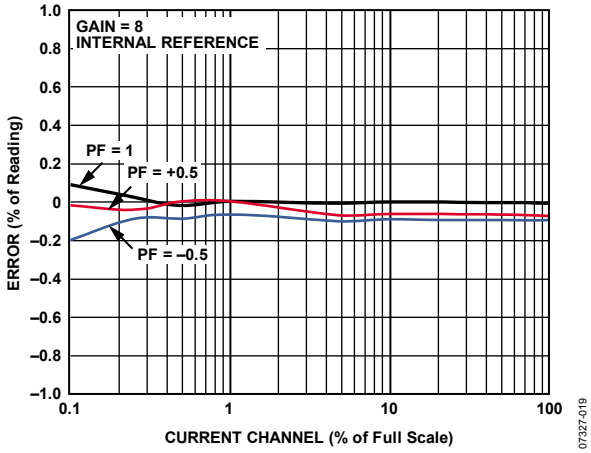

Figure 19. Reactive Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference

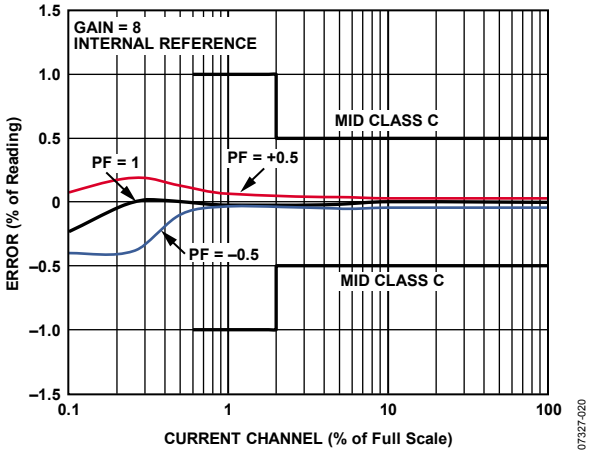

Figure 20. Current RMS Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference

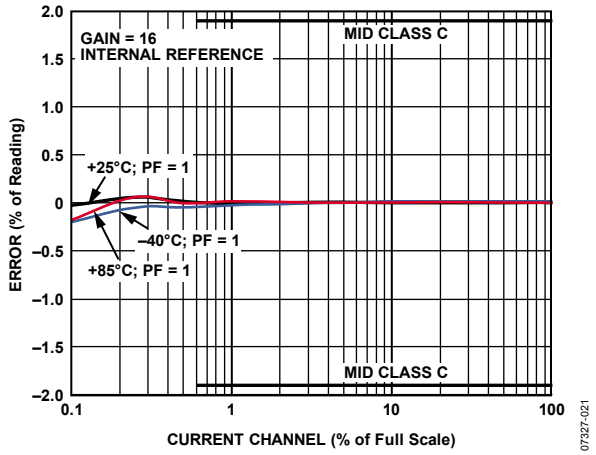

Figure 21. Active Energy Error as a Percentage of Reading (Gain = 16) over Temperature with Internal Reference

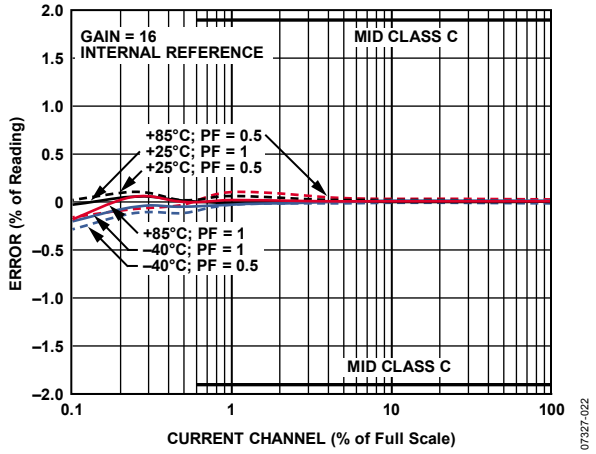

Figure 22. Active Energy Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference

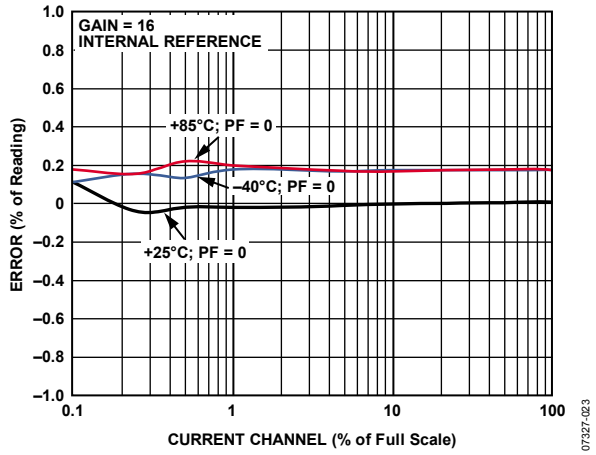

Figure 23. Reactive Energy Error as a Percentage of Reading (Gain = 16) over Temperature with Internal Reference

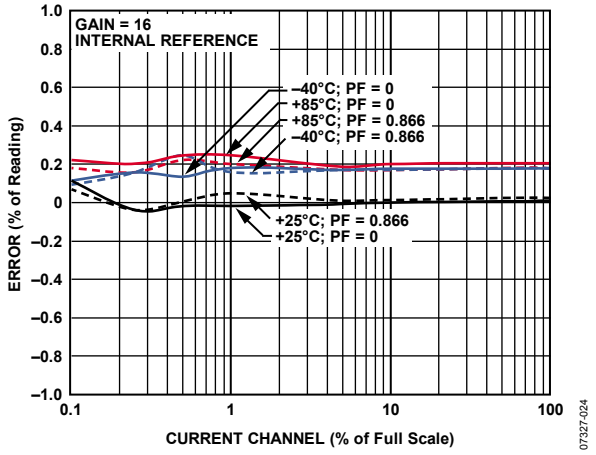

Figure 24. Reactive Energy Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference

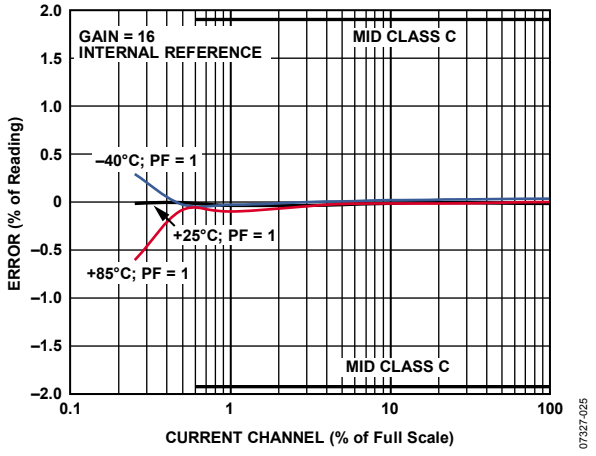

Figure 25. Current RMS Error as a Percentage of Reading (Gain = 16) over Temperature with Internal Reference

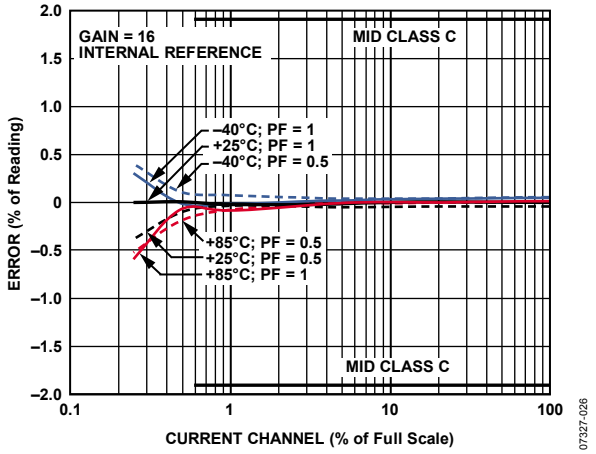

Figure 26. Current RMS Error as a Percentage of Reading (Gain = 16) over Power Factor with Internal Reference

TERMINOLOGY

Measurement Error
The error associated with the energy measurement made by the ADE7518 is defined by the following formula:

$$Percentage\ Error = \left(\frac{Energy\ Register - True\ Energy}{True\ Energy} \right) \times 100\%$$

Phase Error Between Channels
The digital integrator and the high-pass filter (HPF) in the current channel have a nonideal phase response. To offset this phase response and equalize the phase response between channels, two phase correction networks are placed in the current channel: one for the digital integrator and the other for the HPF. The phase correction networks correct the phase response of the corresponding component and ensure a phase match between current channel and voltage channel to within ±0.1° over a range of 45 Hz to 65 Hz with the digital integrator off. With the digital integrator on, the phase is corrected to within ±0.4° over a range of 45 Hz to 65 Hz.

Power Supply Rejection (PSR)
PSR quantifies the ADE7518 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac (100 mV rms/120 Hz) signal is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading (see the Measurement Error definition).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ±5%. Any error introduced is again expressed as a percentage of the reading.

ADC Offset Error
ADC offset error is the dc offset associated with the analog inputs to the ADCs. It means that, with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection (see the Typical Performance Characteristics section). However, when HPF1 is switched on, the offset is removed from the current channel, and the power calculation is not affected by this offset. The offsets can be removed by performing an offset calibration (see the Analog Inputs section).

Gain Error
Gain error is the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC section and the Voltage Channel ADC section). It is measured for each of the gain settings on the current channel (1, 2, 4, 8, and 16). The difference is expressed as a percentage of the ideal code.

SFR MAPPING

Table 13.

Mnemonic	Address	Details
INTPR	0xFF	Table 15
SCRATCH4	0xFE	Table 23
SCRATCH3	0xFD	Table 22
SCRATCH2	0xFC	Table 21
SCRATCH1	0xFB	Table 20
IPSMF	0xF8	Table 16
TEMPCAL	0xF7	Table 116
RTCCOMP	0xF6	Table 115
BATPR	0xF5	Table 17
PERIPH	0xF4	Table 18
B	0xF0	Table 45
LCDSEGE2	0xED	Table 77
IPSME	0xEC	Table 19
SPISTAT	0xEA	Table 131
SPI2CSTAT	0xEA	Table 135
SPIMOD2	0xE9	Table 130
I2CADR	0xE9	Table 134
SPIMOD1	0xE8	Table 129
I2CMOD	0xE8	Table 133
WAV2H	0xE7	Table 29
WAV2M	0xE6	Table 29
WAV2L	0xE5	Table 29
WAV1H	0xE4	Table 29
WAV1M	0xE3	Table 29
WAV1L	0xE2	Table 29
ACC	0xE0	Table 45
MIRQSTH	0xDE	Table 39
MIRQSTM	0xDD	Table 38
MIRQSTL	0xDC	Table 37
MIRQENH	0xDB	Table 42
MIRQENM	0xDA	Table 41
MIRQENL	0xD9	Table 40
IRMSH	0xD6	Table 29
IRMSM	0xD5	Table 29
IRMSL	0xD4	Table 29
VRMSH	0xD3	Table 29
VRMSM	0xD2	Table 29
VRMSL	0xD1	Table 29
PSW	0xD0	Table 46
TH2	0xCD	Table 99
TL2	0xCC	Table 100
RCAP2H	0xCB	Table 101
RCAP2L	0xCA	Table 102
T2CON	0xC8	Table 94
EADRH	0xC7	Table 89
EADRL	0xC6	Table 88
POWCON	0xC5	Table 24
KYREG	0xC1	Table 105
WDCON	0xC0	Table 65
PROTR	0xBF	Table 87
PROTB1	0xBE	Table 86
PROTB0	0xBD	Table 85
EDATA	0xBC	Table 84
PROTKY	0xBB	Table 83
FLSHKY	0xBA	Table 82
ECON	0xB9	Table 81
IP	0xB8	Table 59
PINMAP2	0xB4	Table 140
PINMAP1	0xB3	Table 139
PINMAP0	0xB2	Table 138
LCDCONY	0xB1	Table 70
CFG	0xAF	Table 52
LCDDAT	0xAE	Table 76
LCDPTR	0xAC	Table 75
IEIP2	0xA9	Table 60
IE	0xA8	Table 58
DPCON	0xA7	Table 56
INTVAL	0xA6	Table 114
HOUR	0xA5	Table 113
MIN	0xA4	Table 112
SEC	0xA3	Table 111
HTHSEC	0xA2	Table 110
TIMECON	0xA1	Table 109
P2	0xA0	Table 143
EPCFG	0x9F	Table 137
SBAUDT	0x9E	Table 123
SBAUDF	0x9D	Table 124
LCDCONX	0x9C	Table 69
SPI2CRx	0x9B	Table 128
SPI2CTx	0x9A	Table 127
SBUF	0x99	Table 122
SCON	0x98	Table 121
LCDSEGE	0x97	Table 74
LCDCLK	0x96	Table 71
LCDCON	0x95	Table 68
MDATH	0x94	Table 29
MDATM	0x93	Table 29
MDATL	0x92	Table 29
MADDPT	0x91	Table 29
P1	0x90	Table 142
TH1	0x8D	Table 97
TH0	0x8C	Table 95
TL1	0x8B	Table 98
TL0	0x8A	Table 96
TMOD	0x89	Table 92
TCON	0x88	Table 93
PCON	0x87	Table 47
DPH	0x83	Table 49
DPL	0x82	Table 48
SP	0x81	Table 51
P0	0x80	Table 141

POWER MANAGEMENT

The ADE7518 has elaborate power management circuitry that manages the regular power supply to battery switchover and power supply failures. The power management functionalities can be accessed directly through the 8052 SFRs (see Table 14).

Table 14. Power Management SFRs

SFR Address	R/W	Mnemonic	Description
0xEC	R/W	IPSME	Power Management Interrupt Enable. See Table 19.
0xF5	R/W	BATPR	Battery Switchover Configuration. See Table 17.
0xF8	R/W	IPSMF	Power Management Interrupt Flag. See Table 16.
0xFF	R/W	INTPR	Interrupt Pins Configuration. See Table 15.
0xF4	R/W	PERIPH	Peripheral Configuration SFR. See Table 18.
0xC5	R/W	POWCON	Power Control. See Table 24.
0xFB	R/W	SCRATCH1	Scratch Pad 1. See Table 20.
0xFC	R/W	SCRATCH2	Scratch Pad 2. See Table 21.
0xFD	R/W	SCRATCH3	Scratch Pad 3. See Table 22.
0xFE	R/W	SCRATCH4	Scratch Pad 4. See Table 23.

POWER MANAGEMENT REGISTER DETAILS

Table 15. Interrupt Pins Configuration SFR (INTPR, 0xFF)

Bit	Mnemonic	Default	Description	
7	RTCCAL	0	Controls the RTC calibration output. When this bit is set, the RTC calibration frequency selected by FSEL[1:0] is output on the P0.2/CF1/RTCCAL pin.	
6 to 5	FSEL[1:0]	00	Sets the RTC calibration output frequency and calibration window.	
			FSEL[1:0]	**Result (Calibration Window, Frequency)**
			00	30.5 sec, 1 Hz
			01	30.5 sec, 512 Hz
			10	0.244 sec, 500 Hz
			11	0.244 sec, 16.384 kHz
4	Reserved	N/A		
3 to 1	INT1PRG[2:0]	000	Controls the function of $\overline{\text{INT1}}$.	
			INT1PRG[2:0]	**Result**
			x00	GPIO enabled
			x01	BCTRL enabled
			01x	$\overline{\text{INT1}}$ input disabled
			11x	$\overline{\text{INT1}}$ input enabled
0	INT0PRG	0	Controls the function of $\overline{\text{INT0}}$.	
			INT0PRG	**Result**
			0	$\overline{\text{INT0}}$ input disabled
			1	$\overline{\text{INT0}}$ input enabled

Writing to the Interrupt Pins Configuration SFR (INTPR, 0xFF)

To protect the RTC from runaway code, a key must be written to the Key SFR (KYREG, 0xC1) to obtain write access to INTPR. KYREG (see Table 105) should be set to 0xEA to unlock this SFR and then reset to zero after a timekeeping register is written to. The RTC registers can be written using the following 8052 assembly code:

```
MOV    KYREG, #0EAh
MOV    INTPR, #080h
```

Table 16. Power Management Interrupt Flag SFR (IPSMF, 0xF8)

Bit	Address	Mnemonic	Default	Description
7	0xFF	FPSR	0	Power Supply Restored Interrupt Flag. Set when the V_{DD} power supply has been restored. This occurs when the source of V_{SWOUT} changes from V_{BAT} to V_{DD}.
6	0xFE	FPSM	0	PSM Interrupt Flag. Set when an enabled PSM interrupt condition occurs.
5	0xFD	FSAG	0	Voltage SAG Interrupt Flag. Set when an ADE energy measurement SAG condition occurs.
4	0xFC	Reserved	0	This bit must be kept cleared for proper operation.
3	0xFB	Reserved	0	This bit must be kept cleared for proper operation.
2	0xFA	Reserved	0	This bit must be kept cleared for proper operation.
1	0xF9	FBSO	0	Battery Switchover Interrupt Flag. Set when V_{SWOUT} switches from V_{DD} to $V_{BAT.}$
0	0xF8	FVDCIN	0	V_{DCIN} Monitor Interrupt Flag. Set when V_{DCIN} falls below 1.2 V.

Table 17. Battery Switchover Configuration SFR (BATPR, 0xF5)

Bit	Mnemonic	Default	Description	
7 to 2	Reserved	0	These bits must be kept to 0 for proper operation.	
1 to 0	BATPRG[1:0]	00	Control Bits for Battery Switchover.	
			BATPRG[1:0]	**Result**
			00	Battery switchover enabled on low V_{DD}
			01	Battery switchover enabled on low V_{DD} and low V_{DCIN}
			1x	Battery switchover disabled

Table 18. Peripheral Configuration SFR (PERIPH, 0xF4)

Bit	Mnemonic	Default	Description	
7	RXFLAG	0	If set, indicates that an Rx edge event triggered wake-up from PSM2.	
6	VSWSOURCE	1	Indicates the power supply that is internally connected to V_{SWOUT} (0 $V_{SWOUT} = V_{BAT}$, 1 $V_{SWOUT} = V_{DD}$).	
5	VDD_OK	1	If set, indicates that the V_{DD} power supply is ready for operation.	
4	PLL_FLT	0	If set, indicates that a PLL fault occurred where the PLL lost lock. Set the PLL_FTL_ACK bit (see Table 107) in the Start ADC Measurement SFR (ADCGO, 0xD8) to acknowledge the fault and clear the PLL_FLT bit.	
3	Reserved	0	This bit should be kept to 0.	
2	Reserved	0	This bit should be kept to 0.	
1 to 0	RXPROG[1:0]	00	Controls the function of the P1.0/RxD pin.	
			RXPROG[1:0]	**Result**
			00	GPIO
			01	RxD with wake-up disabled
			11	RxD with wake-up enabled

Table 19. Power Management Interrupt Enable SFR (IPSME, 0xEC)

Bit	Mnemonic	Default	Description
7	EPSR	0	Enables a PSM interrupt when the power supply restored flag (FPSR) is set.
6	Reserved	0	Reserved.
5	ESAG	0	Enables a PSM interrupt when the voltage SAG flag (FSAG) is set.
4 to 2	Reserved	0	These bits must be kept cleared for proper operation.
1	EBSO	0	Enables a PSM interrupt when the battery switchover flag (FBSO) is set.
0	EVDCIN	0	Enables a PSM interrupt when the V_{DCIN} monitor flag (FVDCIN) is set.

Table 20. Scratch Pad 1 SFR (SCRATCH1, 0xFB)

Bit	Mnemonic	Default	Description
7 to 0	SCRATCH1	0	Value can be written/read in this register. This value is maintained in all the power saving modes.

Table 21. Scratch Pad 2 SFR (SCRATCH2, 0xFC)

Bit	Mnemonic	Default	Description
7 to 0	SCRATCH2	0	Value can be written/read in this register. This value is maintained in all the power saving modes.

Table 22. Scratch Pad 3 SFR (SCRATCH3, 0xFD)

Bit	Mnemonic	Default	Description
7 to 0	SCRATCH3	0	Value can be written/read in this register. This value is maintained in all the power saving modes.

Table 23. Scratch Pad 4 SFR (SCRATCH4, 0xFE)

Bit	Mnemonic	Default	Description
7 to 0	SCRATCH4	0	Value can be written/read in this register. This value is maintained in all the power saving modes.

Clearing the Scratch Pad Registers (SCRATCH1, 0xFB to SCRATCH4, 0xFE)

Note that these scratch pad registers are only cleared when the part loses V_{DD} and V_{BAT}. They are not cleared by software, watchdog, or PLL reset and, therefore, need to be set correctly in these situations.

Table 24. Power Control SFR (POWCON, 0xC5)

Bit	Mnemonic	Default	Description	
7	Reserved	1	Reserved.	
6	METER_OFF	0	Set this bit to turn off the modulators and energy metering DSP circuitry to reduce power if metering functions are not needed in PSM0.	
5	Reserved	0	This bit should be kept at 0 for proper operation.	
4	COREOFF	0	Set this bit to shut down the core and enter PSM2 if in PSM1 operating mode.	
3	Reserved	0	Reserved.	
2 to 0	CD[2:0]	010	Controls the core clock frequency, f_{CORE}. f_{CORE} = 4.096 MHz/2^{CD}.	
			CD[2:0]	**Result (f_{CORE} in MHz)**
			000	4.096
			001	2.048
			010	1.024
			011	0.512
			100	0.256
			101	0.128
			110	0.064
			111	0.032

Writing to the Power Control SFR (POWCON, 0xC5)

Writing data to the POWCON SFR involves writing 0xA7 into the Key SFR (KYREG, 0xC1), which is described in Table 105, followed by a write to the POWCON SFR. For example,

```
MOV KYREG,#0A7h     ;Write KYREG to 0xA7 to get write access to the POWCON SFR
MOV POWCON,#10h     ;Shutdown the core
```

POWER SUPPLY ARCHITECTURE

The ADE7518 has two power supply inputs, V_{DD} and V_{BAT}, and requires only a single 3.3 V power supply at V_{DD} for full operation. A battery backup, or secondary power supply, with a maximum of 3.7 V, can be connected to the V_{BAT} input. Internally, the ADE7518 connects V_{DD} or V_{BAT} to V_{SWOUT}, which is used to derive power for the ADE7518 circuitry. The V_{SWOUT} output pin reflects the voltage at the internal power supply (V_{SWOUT}) and has a maximum output current of 6 mA. This pin can also be used to power a limited number of peripheral components. The 2.5 V analog supply (V_{INTA}) and the 2.5 V supply for the core logic (V_{INTD}) are derived by on-chip linear regulators from V_{SWOUT}. Figure 27 shows the power supply architecture of ADE7518.

The ADE7518 provides automatic battery switchover between V_{DD} and V_{BAT} based on the voltage level detected at V_{DD} or V_{DCIN}. Additionally, the BCTRL input can be used to trigger a battery switchover. The conditions for switching V_{SWOUT} from V_{DD} to V_{BAT} and back to V_{DD} are described in the Battery Switchover section. V_{DCIN} is an input pin that can be connected to a 0 V to 3.3 V dc signal. This input is intended for power supply supervisory purposes and does not provide power to the ADE7518 circuitry (see the Battery Switchover section).

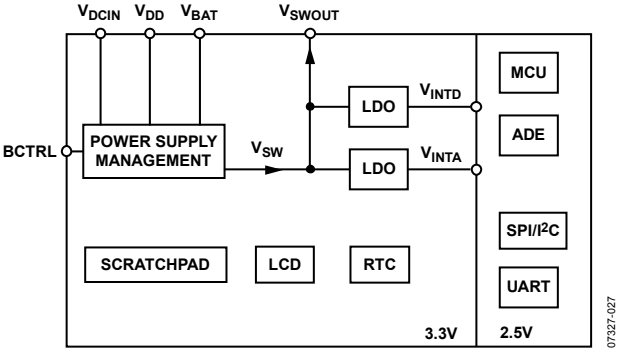

Figure 27. Power Supply Architecture

BATTERY SWITCHOVER

The ADE7518 monitors V_{DD}, V_{BAT}, and V_{DCIN}. Automatic battery switchover from V_{DD} to V_{BAT} can be configured based on the status of the V_{DD}, V_{DCIN}, or BCTRL pin. Battery switchover is enabled by default. Setting Bit 1 in the Battery Switchover Configuration SFR (BATPR, 0xF5) disables battery switchover so that V_{DD} is always connected to V_{SWOUT} (see Table 17). The source of V_{SWOUT} is indicated by Bit 6 in the Peripheral Configuration SFR (PERIPH, 0xF4), which is described in Table 18. Bit 6 is set when V_{SWOUT} is connected to V_{DD} and cleared when V_{SWOUT} is connected to V_{BAT}.

The battery switchover functionality provided by the ADE7518 allows a seamless transition from V_{DD} to V_{BAT}. An automatic battery switchover option ensures a stable power supply to the ADE7518, as long as the external battery voltage is above 2.75 V. It allows continuous code execution even while the internal power supply is switching from V_{DD} to V_{BAT} and back. Note that the energy metering ADCs are not available when V_{BAT} is being used for V_{SWOUT}.

Power supply management (PSM) interrupts can be enabled to indicate when battery switchover occurs and when the V_{DD} power supply is restored (see the Power Supply Management (PSM) Interrupt section).

V_{DD} to V_{BAT}

The following three events switch the internal power supply (V_{SWOUT}) from V_{DD} to V_{BAT}:

- V_{DCIN} < 1.2 V. When V_{DCIN} falls below 1.2 V, V_{SWOUT} switches from V_{DD} to V_{BAT}. This event is enabled when the BATPRG[1:0] bits in the Battery Switchover Configuration SFR (BATPR, 0xF5) = 0b01. Setting these bits disables switchover based on V_{DCIN}. Battery switchover on low V_{DCIN} is disabled by default.
- V_{DD} < 2.75 V. When V_{DD} falls below 2.75 V, V_{SWOUT} switches from V_{DD} to V_{BAT}. This event is enabled when BATPRG[1:0] in the BATPR SRF are cleared.
- Falling edge on BCTRL. When the battery control pin, BCTRL, goes low, V_{SWOUT} switches from V_{DD} to V_{BAT}. This external switchover signal can trigger a switchover to V_{BAT} at any time. Setting the bits INT1PRG[2:0] to 0bx01 in the Interrupt Pins Configuration SFR (INTPR, 0xFF) enables the battery control pin (see Table 15).

Switching from V_{BAT} to V_{DD}

To switch V_{SWOUT} from V_{BAT} to V_{DD}, all of the following events that are enabled to force battery switchover must be false:

- V_{DCIN} < 1.2 V and V_{DD} < 2.75 V enabled. If the low V_{DCIN} condition is enabled, V_{SWOUT} switches to V_{DD} after V_{DCIN} remains above 1.2 V and V_{DD} remains above 2.75 V.
- V_{DD} < 2.75 V enabled. V_{SWOUT} switches back to V_{DD} after V_{DD} remains above 2.75 V.
- BCTRL enabled. V_{SWOUT} switches back to V_{DD} after BCTRL is high, and the first or second bullet point is satisfied.