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Poly Phase Multifunction Energy Metering IC with Per Phase Information

Data Sheet

ADE7758

FEATURES

- **Highly accurate; supports IEC 60687, IEC 61036, IEC 61268, IEC 62053-21, IEC 62053-22, and IEC 62053-23**
- **Compatible with 3-phase/3-wire, 3-phase/4-wire, and other 3-phase services**
- **Less than 0.1% active energy error over a dynamic range of 1000 to 1 at 25°C**
- **Supplies active/reactive/apparent energy, voltage rms, current rms, and sampled waveform data**
- **Two pulse outputs, one for active power and the other selectable between reactive and apparent power with programmable frequency**
- **Digital power, phase, and rms offset calibration**
- **On-chip, user-programmable thresholds for line voltage SAG and overvoltage detections**
- **An on-chip, digital integrator enables direct interface-to-current sensors with di/dt output**
- **A PGA in the current channel allows direct interface to current transformers**
- **An SPI®-compatible serial interface with $\overline{IRQ}$**
- **Proprietary ADCs and DSP provide high accuracy over large variations in environmental conditions and time**
- **Reference 2.4 V (drift 30 ppm/°C typical) with external overdrive capability**
- **Single 5 V supply, low power (70 mW typical)**

GENERAL DESCRIPTION

The ADE7758 is a high accuracy, 3-phase electrical energy measurement IC with a serial interface and two pulse outputs. The ADE7758 incorporates second-order Σ-Δ ADCs, a digital integrator, reference circuitry, a temperature sensor, and all the signal processing required to perform active, reactive, and apparent energy measurement and rms calculations.

The ADE7758 is suitable to measure active, reactive, and apparent energy in various 3-phase configurations, such as WYE or DELTA services, with both three and four wires. The ADE7758 provides system calibration features for each phase, that is, rms offset correction, phase calibration, and power calibration. The APCF logic output gives active power information, and the VARCF logic output provides instantaneous reactive or apparent power information.

FUNCTIONAL BLOCK DIAGRAM

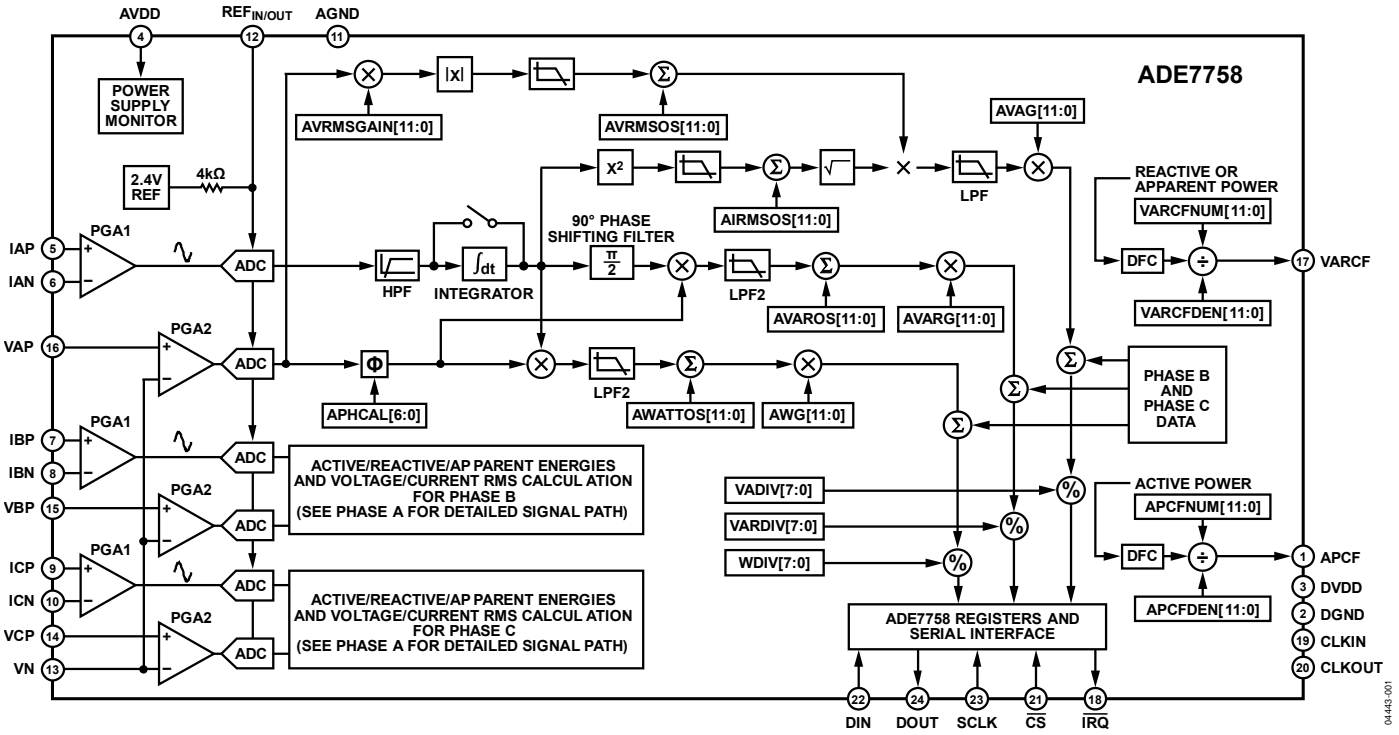

Figure 1.

Rev. E

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADE7758 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1334: Impact of Adding a Neutral Attenuation Network in a 3P4W Wye System
- AN-750: ADE7758 Phase Dropout Detection for VAR Calculation

Data Sheet

- ADE7758: Poly Phase Multifunction Energy Metering IC with Per Phase Information Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADE7758 Evaluation Board Software

REFERENCE MATERIALS

Technical Articles

- IC Technology and Failure Mechanisms - Understanding Reliability Standards Can Raise Quality of Meters
- Measuring Harmonic Energy with a Solid State Energy Meter
- Reactive Energy Measurement Made Simple
- RF Meets Power Lines: Designing Intelligent Smart Grid Systems that Promote Energy Efficiency

DESIGN RESOURCES

- ADE7758 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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1/04—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADE7758 has a waveform sample register that allows access to the ADC outputs. The part also incorporates a detection circuit for short duration low or high voltage variations. The voltage threshold levels and the duration (number of half-line cycles) of the variation are user programmable. A zero-crossing detection is synchronized with the zero-crossing point of the line voltage of any of the three phases. This information can be used to measure the period of any one of the three voltage inputs. The zero-crossing detection is used inside the chip for the line cycle energy accumulation mode. This mode permits faster and more accurate calibration by synchronizing the energy accumulation with an integer number of line cycles.

Data is read from the ADE7758 via the SPI serial interface. The interrupt request output ($\overline{\text{IRQ}}$) is an open-drain, active low logic output. The $\overline{\text{IRQ}}$ output goes active low when one or more interrupt events have occurred in the ADE7758. A status register indicates the nature of the interrupt. The ADE7758 is available in a 24-lead SOIC package.

SPECIFICATIONS

AVDD = DVDD = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 10 MHz XTAL, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 1.

Parameter[1, 2]	Specification	Unit	Test Conditions/Comments
ACCURACY			
Active Energy Measurement Error (per Phase)	0.1	% typ	Over a dynamic range of 1000 to 1
Phase Error Between Channels			Line frequency = 45 Hz to 65 Hz, HPF on
PF = 0.8 Capacitive	±0.05	°max	Phase lead 37°
PF = 0.5 Inductive	±0.05	°max	Phase lag 60°
AC Power Supply Rejection			AVDD = DVDD = 5 V + 175 mV rms/120 Hz
Output Frequency Variation	0.01	% typ	V1P = V2P = V3P = 100 mV rms
DC Power Supply Rejection			AVDD = DVDD = 5 V ± 250 mV dc
Output Frequency Variation	0.01	% typ	V1P = V2P = V3P = 100 mV rms
Active Energy Measurement Bandwidth	14	kHz	
IRMS Measurement Error	0.5	% typ	Over a dynamic range of 500:1
IRMS Measurement Bandwidth	14	kHz	
VRMS Measurement Error	0.5	% typ	Over a dynamic range of 20:1
VRMS Measurement Bandwidth	260	Hz	
ANALOG INPUTS			See the Analog Inputs section
Maximum Signal Levels	±500	mV max	Differential input
Input Impedance (DC)	380	kΩ min	
ADC Offset Error[3]	±30	mV max	Uncalibrated error, see the Terminology section
Gain Error[3]	±6	% typ	External 2.5 V reference
WAVEFORM SAMPLING			Sampling CLKIN/128, 10 MHz/128 = 78.1 kSPS
Current Channels			See the Current Channel ADC section
Signal-to-Noise Plus Distortion	62	dB typ	
Bandwidth (−3 dB)	14	kHz	
Voltage Channels			See the Voltage Channel ADC section
Signal-to-Noise Plus Distortion	62	dB typ	
Bandwidth (−3 dB)	260	Hz	
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	2.6	V max	2.4 V + 8%
	2.2	V min	2.4 V − 8%
Input Capacitance	10	pF max	
ON-CHIP REFERENCE			Nominal 2.4 V at $REF_{IN/OUT}$ pin
Reference Error	±200	mV max	
Current Source	6	µA max	
Output Impedance	4	kΩ min	
Temperature Coefficient	30	ppm/°C typ	
CLKIN			All specifications CLKIN of 10 MHz
Input Clock Frequency	15	MHz max	
	5	MHz min	
LOGIC INPUTS			
DIN, SCLK, CLKIN, and $\overline{CS}$			
Input High Voltage, V_{INH}	2.4	V min	DVDD = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	V max	DVDD = 5 V ± 5%
Input Current, I_{IN}	±3	µA max	Typical 10 nA, V_{IN} = 0 V to DVDD
Input Capacitance, C_{IN}	10	pF max	

Parameter[1, 2]	Specification	Unit	Test Conditions/Comments
LOGIC OUTPUTS			DVDD = 5 V ± 5%
$\overline{IRQ}$, DOUT, and CLKOUT			$\overline{IRQ}$ is open-drain, 10 kΩ pull-up resistor
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5 mA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 1 mA
APCF and VARCF			
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 8 mA
Output Low Voltage, V_{OL}	1	V max	I_{SINK} = 5 mA
POWER SUPPLY			For specified performance
AVDD	4.75	V min	5 V − 5%
	5.25	V max	5 V + 5%
DVDD	4.75	V min	5 V − 5%
	5.25	V max	5 V + 5%
AI_{DD}	8	mA max	Typically 5 mA
DI_{DD}	13	mA max	Typically 9 mA

[1] See the Typical Performance Characteristics.
[2] See the Terminology section for a definition of the parameters.
[3] See the Analog Inputs section.

TIMING CHARACTERISTICS

AVDD = DVDD = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 10 MHz XTAL, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 2.

Parameter[1, 2]	Specification	Unit	Test Conditions/Comments
WRITE TIMING			
t_1	50	ns (min)	$\overline{CS}$ falling edge to first SCLK falling edge
t_2	50	ns (min)	SCLK logic high pulse width
t_3	50	ns (min)	SCLK logic low pulse width
t_4	10	ns (min)	Valid data setup time before falling edge of SCLK
t_5	5	ns (min)	Data hold time after SCLK falling edge
t_6	1200	ns (min)	Minimum time between the end of data byte transfers
t_7	400	ns (min)	Minimum time between byte transfers during a serial write
t_8	100	ns (min)	$\overline{CS}$ hold time after SCLK falling edge
READ TIMING			
t_9[3]	4	µs (min)	Minimum time between read command (that is, a write to communication register) and data read
t_{10}	50	ns (min)	Minimum time between data byte transfers during a multibyte read
t_{11}[4]	30	ns (min)	Data access time after SCLK rising edge following a write to the communications register
t_{12}[5]	100	ns (max)	Bus relinquish time after falling edge of SCLK
	10	ns (min)	
t_{13}[5]	100	ns (max)	Bus relinquish time after rising edge of $\overline{CS}$
	10	ns (min)	

[1] Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are specified with tr = tf = 5 ns (10% to 90%) and timed from a voltage level of 1.6 V.
[2] See the timing diagrams in Figure 3 and Figure 4 and the Serial Interface section.
[3] Minimum time between read command and data read for all registers except waveform register, which is t_9 = 500 ns min.
[4] Measured with the load circuit in Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V.
[5] Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time quoted here is the true bus relinquish time of the part and is independent of the bus loading.

TIMING DIAGRAMS

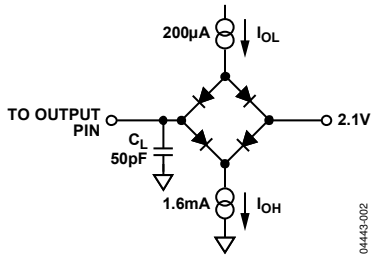

Figure 2. Load Circuit for Timing Specifications

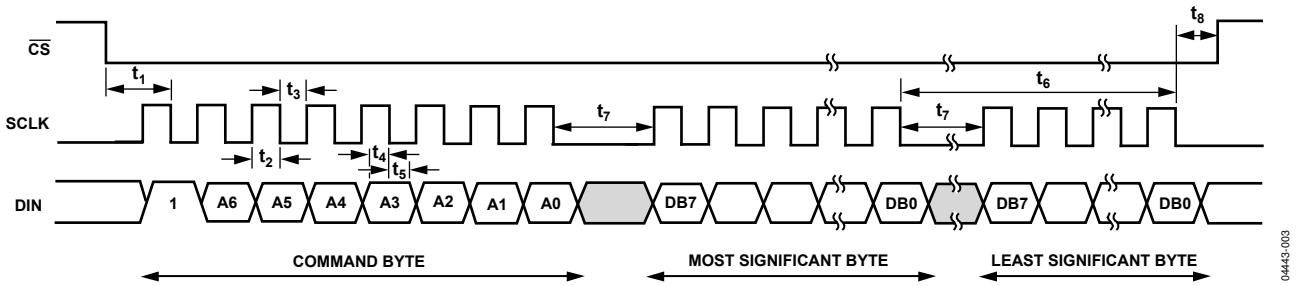

Figure 3. Serial Write Timing

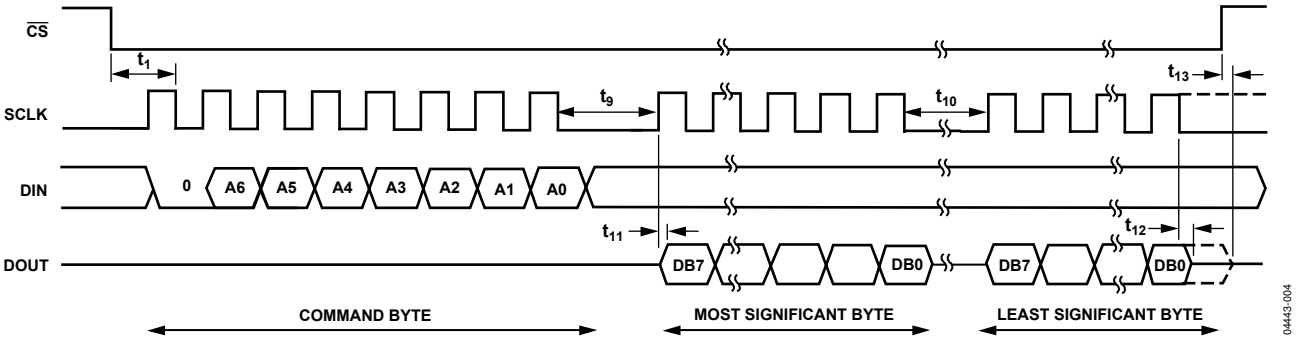

Figure 4. Serial Read Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AVDD to AGND	–0.3 V to +7 V
DVDD to DGND	–0.3 V to +7 V
DVDD to AVDD	–0.3 V to +0.3 V
Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, VCP, VN	–6 V to +6 V
Reference Input Voltage to AGND	–0.3 V to AVDD + 0.3 V
Digital Input Voltage to DGND	–0.3 V to DVDD + 0.3 V
Digital Output Voltage to DGND	–0.3 V to DVDD + 0.3 V
Operating Temperature	
Industrial Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
24-Lead SOIC, Power Dissipation	88 mW
θ_{JA} Thermal Impedance	53°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

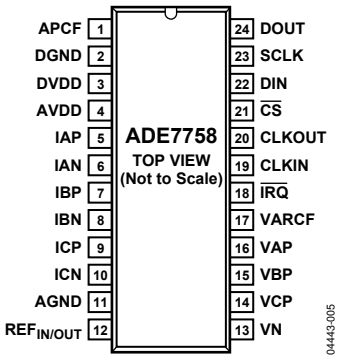

Figure 5. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	APCF	Active Power Calibration Frequency (APCF) Logic Output. It provides active power information. This output is used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the APCFNUM and APCFDEN registers (see the Active Power Frequency Output section).
2	DGND	This provides the ground reference for the digital circuitry in the ADE7758, that is, the multiplier, filters, and digital-to-frequency converter. Because the digital return currents in the ADE7758 are small, it is acceptable to connect this pin to the analog ground plane of the whole system. However, high bus capacitance on the DOUT pin can result in noisy digital current that could affect performance.
3	DVDD	Digital Power Supply. This pin provides the supply voltage for the digital circuitry in the ADE7758. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled to DGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
4	AVDD	Analog Power Supply. This pin provides the supply voltage for the analog circuitry in the ADE7758. The supply should be maintained at 5 V ± 5% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. The Typical Performance Characteristics show the power supply rejection performance. This pin should be decoupled to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
5, 6, 7, 8, 9, 10	IAP, IAN, IBP, IBN, ICP, ICN	Analog Inputs for Current Channel. This channel is used with the current transducer and is referenced in this document as the current channel. These inputs are fully differential voltage inputs with maximum differential input signal levels of ±0.5 V, ±0.25 V, and ±0.125 V, depending on the gain selections of the internal PGA (see the Analog Inputs section). All inputs have internal ESD protection circuitry. In addition, an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
11	AGND	This pin provides the ground reference for the analog circuitry in the ADE7758, that is, ADCs, temperature sensor, and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, for example, antialiasing filters, current, and voltage transducers. To keep ground noise around the ADE7758 to a minimum, the quiet ground plane should be connected to the digital ground plane at only one point. It is acceptable to place the entire device on the analog ground plane.
12	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.4 V ± 8% and a typical temperature coefficient of 30 ppm/°C. An external reference source can also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 µF ceramic capacitor.
13, 14, 15, 16	VN, VCP, VBP, VAP	Analog Inputs for the Voltage Channel. This channel is used with the voltage transducer and is referenced as the voltage channels in this document. These inputs are single-ended voltage inputs with the maximum signal level of ±0.5 V with respect to VN for specified operation. These inputs are voltage inputs with maximum input signal levels of ±0.5 V, ±0.25 V, and ±0.125 V, depending on the gain selections of the internal PGA (see the Analog Inputs section). All inputs have internal ESD protection circuitry, and in addition, an overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.

Pin No.	Mnemonic	Description
17	VARCF	Reactive Power Calibration Frequency Logic Output. It gives reactive power or apparent power information depending on the setting of the VACF bit of the WAVMODE register. This output is used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the VARCFNUM and VARCFDEN registers (see the Reactive Power Frequency Output section).
18	$\overline{IRQ}$	Interrupt Request Output. This is an active low open-drain logic output. Maskable interrupts include: an active energy register at half level, an apparent energy register at half level, and waveform sampling up to 26 kSPS (see the Interrupts section).
19	CLKIN	Master Clock for ADCs and Digital Signal Processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7758. The clock frequency for specified operation is 10 MHz. Ceramic load capacitors of a few tens of picofarad should be used with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for the load capacitance requirements
20	CLKOUT	A crystal can be connected across this pin and CLKIN as previously described to provide a clock source for the ADE7758. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
21	$\overline{CS}$	Chip Select. Part of the 4-wire serial interface. This active low logic input allows the ADE7758 to share the serial bus with several other devices (see the Serial Interface section).
22	DIN	Data Input for the Serial Interface. Data is shifted in at this pin on the falling edge of SCLK (see the Serial Interface section).
23	SCLK	Serial Clock Input for the Synchronous Serial Interface. All serial data transfers are synchronized to this clock (see the Serial Interface section). The SCLK has a Schmidt-trigger input for use with a clock source that has a slow edge transition time, for example, opto-isolator outputs.
24	DOUT	Data Output for the Serial Interface. Data is shifted out at this pin on the rising edge of SCLK. This logic output is normally in a high impedance state, unless it is driving data onto the serial data bus (see the Serial Interface section).

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7758 is defined by

$$Measurement\ Error = \frac{Energy\ Registered\ by\ ADE7758 - True\ Energy}{True\ Energy} \times 100\% \quad (1)$$

Phase Error Between Channels

The high-pass filter (HPF) and digital integrator introduce a slight phase mismatch between the current and the voltage channel. The all-digital design ensures that the phase matching between the current channels and voltage channels in all three phases is within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range of 40 Hz to 1 kHz. This internal phase mismatch can be combined with the external phase error (from current sensor or component tolerance) and calibrated with the phase calibration registers.

Power Supply Rejection (PSR)

This quantifies the ADE7758 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (175 mV rms/100 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see the Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±5%. Any error introduced is again expressed as a percentage of the reading.

ADC Offset Error

This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND that the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection (see the Typical Performance Characteristics section). However, when HPFs are switched on, the offset is removed from the current channels and the power calculation is not affected by this offset.

Gain Error

The gain error in the ADCs of the ADE7758 is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC section and the Voltage Channel ADC section). The difference is expressed as a percentage of the ideal code.

Gain Error Match

The gain error match is defined as the gain error (minus the offset) obtained when switching between a gain of 1, 2, or 4. It is expressed as a percentage of the output ADC code obtained under a gain of 1.

TYPICAL PERFORMANCE CHARACTERISTICS

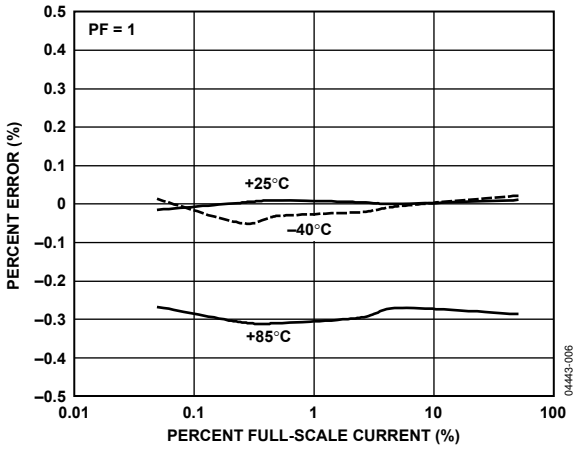

Figure 6. Active Energy Error as a Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator Off

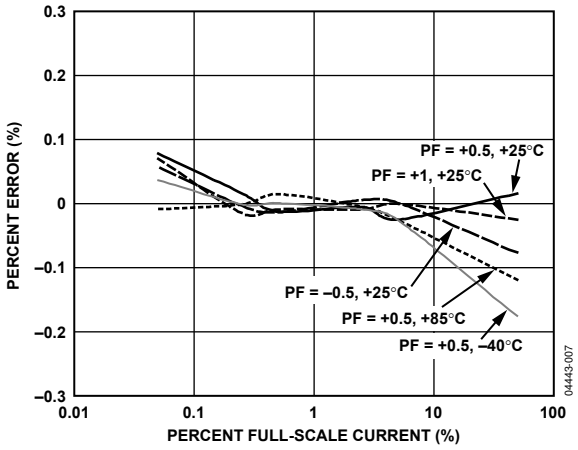

Figure 7. Active Energy Error as a Percentage of Reading (Gain = +1) over Power Factor with Internal Reference and Integrator Off

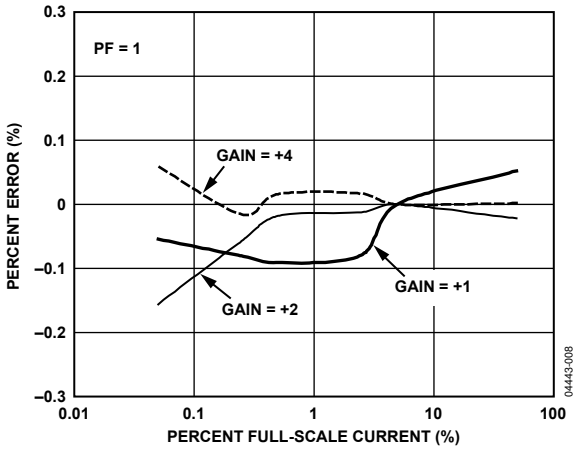

Figure 8. Active Energy Error as a Percentage of Reading over Gain with Internal Reference and Integrator Off

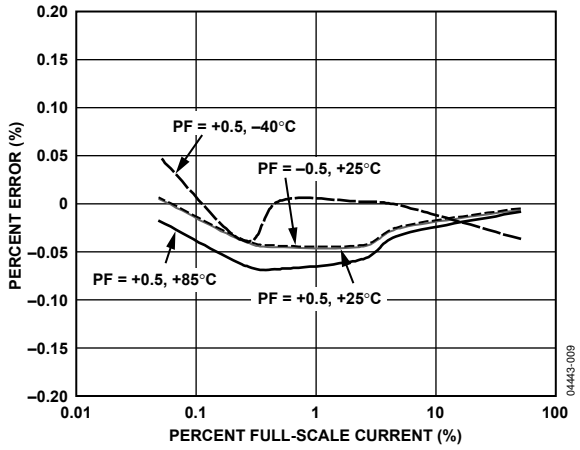

Figure 9. Active Energy Error as a Percentage of Reading (Gain = +1) over Temperature with External Reference and Integrator Off

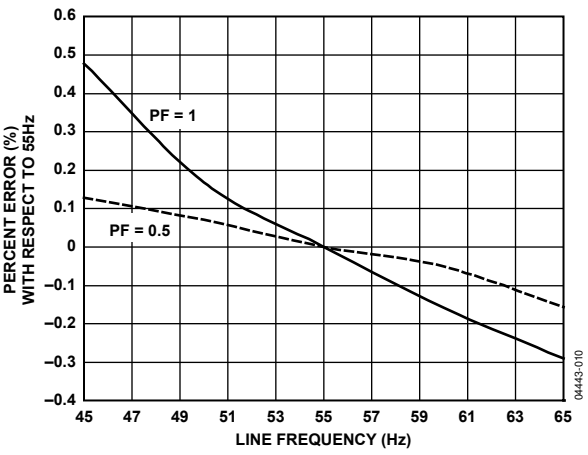

Figure 10. Active Energy Error as a Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

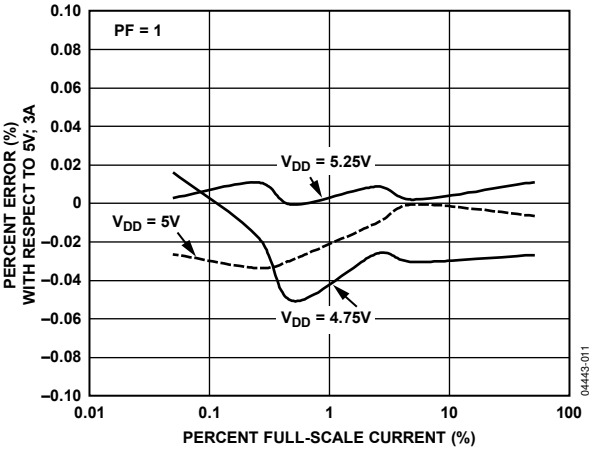

Figure 11. Active Energy Error as a Percentage of Reading (Gain = +1) over Power Supply with Internal Reference and Integrator Off

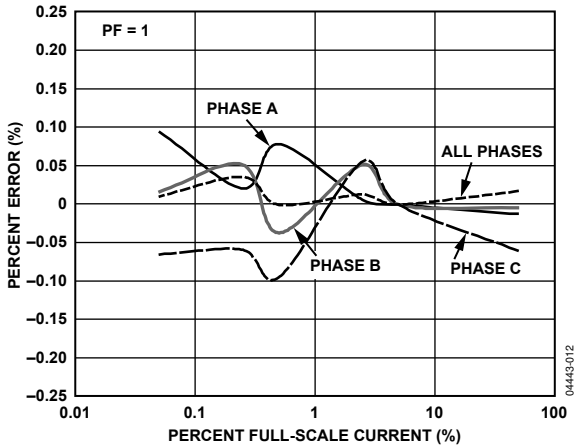

Figure 12. APCF Error as a Percentage of Reading (Gain = +1) with Internal Reference and Integrator Off

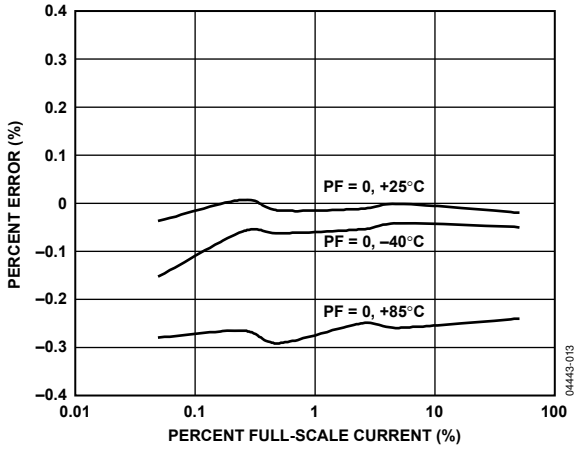

Figure 13. Reactive Energy Error as a Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator Off

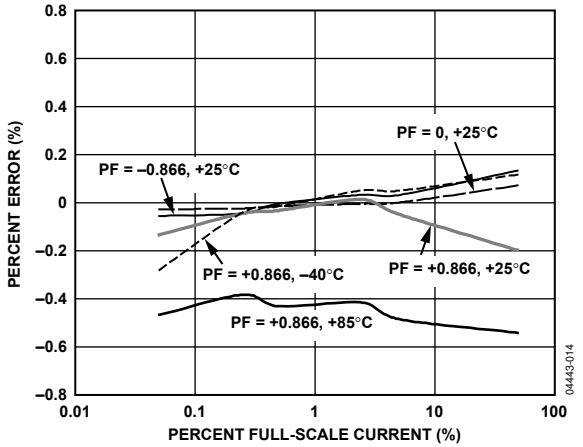

Figure 14. Reactive Energy Error as a Percentage of Reading (Gain = +1) over Power Factor with Internal Reference and Integrator Off

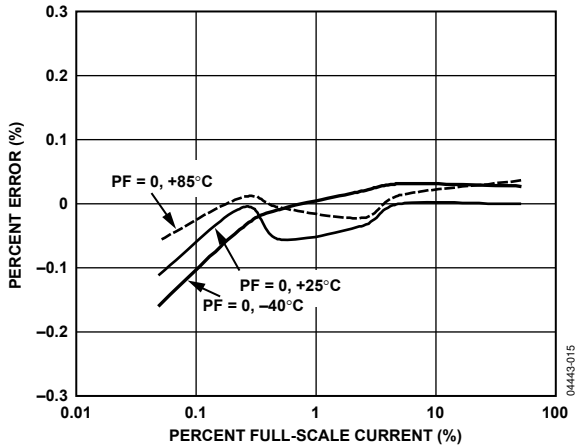

Figure 15. Reactive Energy Error as a Percentage of Reading (Gain = +1) over Temperature with External Reference and Integrator Off

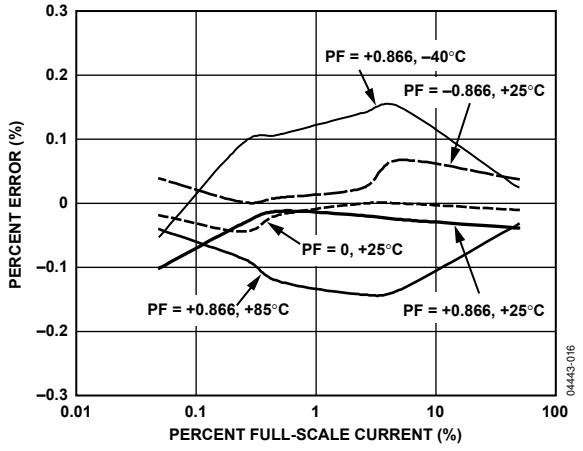

Figure 16. Reactive Energy Error as a Percentage of Reading (Gain = +1) over Power Factor with External Reference and Integrator Off

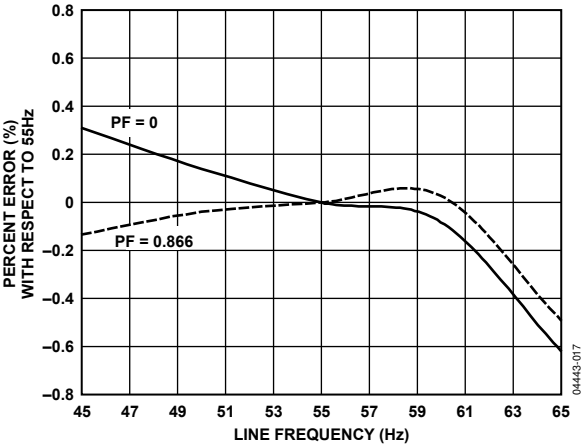

Figure 17. Reactive Energy Error as a Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

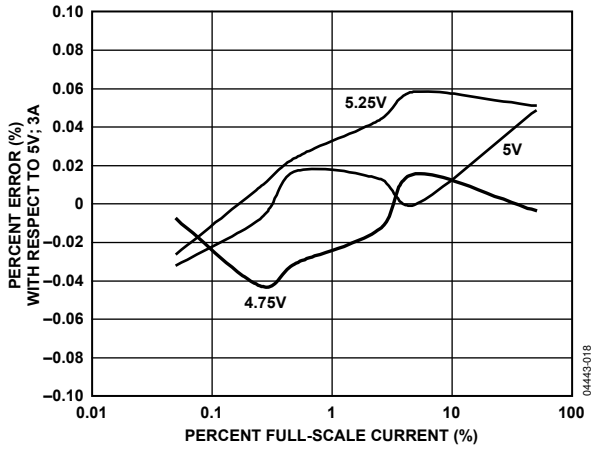

Figure 18. Reactive Energy Error as a Percentage of Reading (Gain = +1) over Supply with Internal Reference and Integrator Off

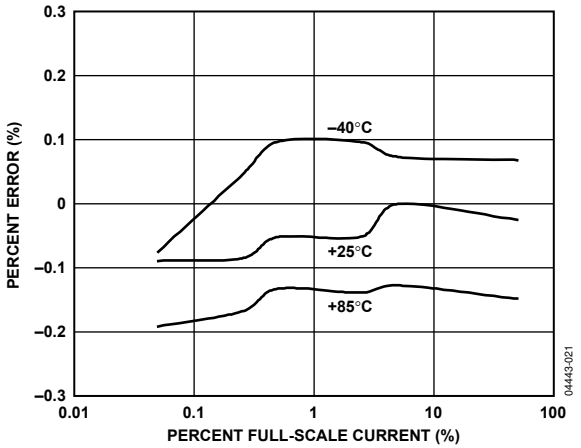

Figure 21. Active Energy Error as a Percentage of Reading (Gain = +4) over Temperature with Internal Reference and Integrator On

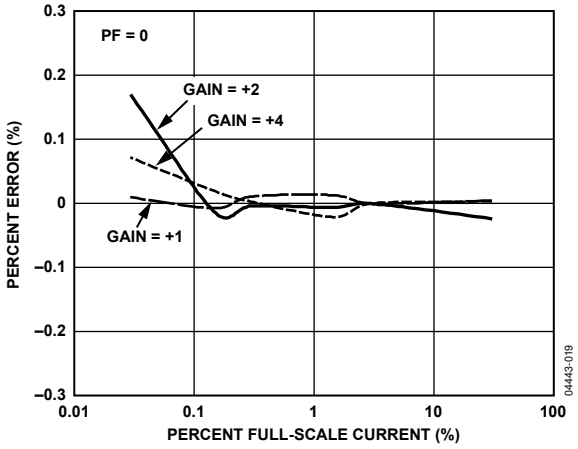

Figure 19. Reactive Energy Error as a Percentage of Reading over Gain with Internal Reference and Integrator Off

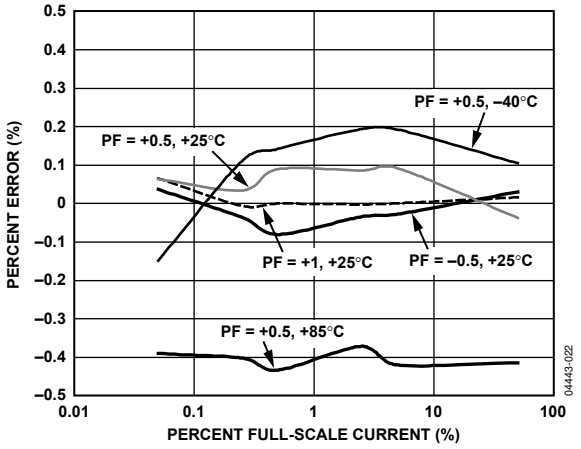

Figure 22. Active Energy Error as a Percentage of Reading (Gain = +4) over Power Factor with Internal Reference and Integrator On

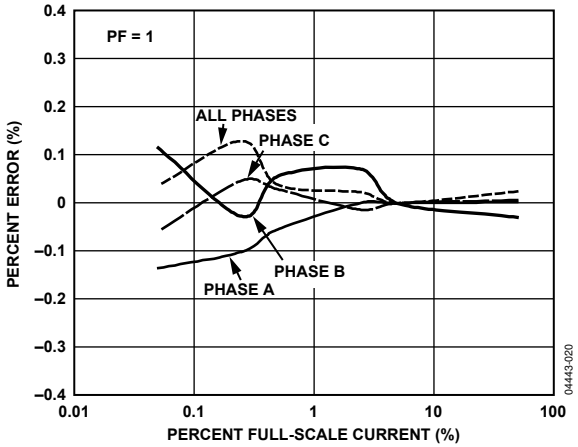

Figure 20. VARCF Error as a Percentage of Reading (Gain = +1) with Internal Reference and Integrator Off

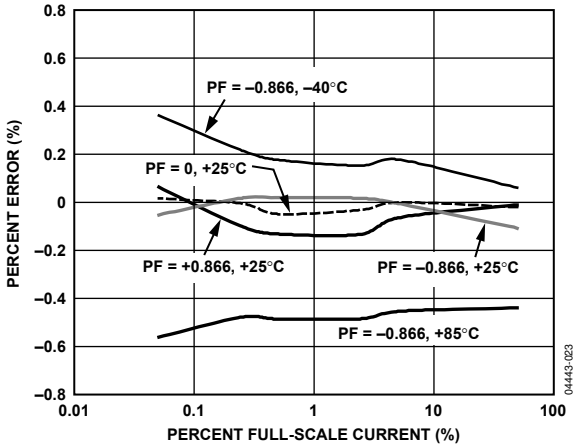

Figure 23. Reactive Energy Error as a Percentage of Reading (Gain = +4) over Power Factor with Internal Reference and Integrator On

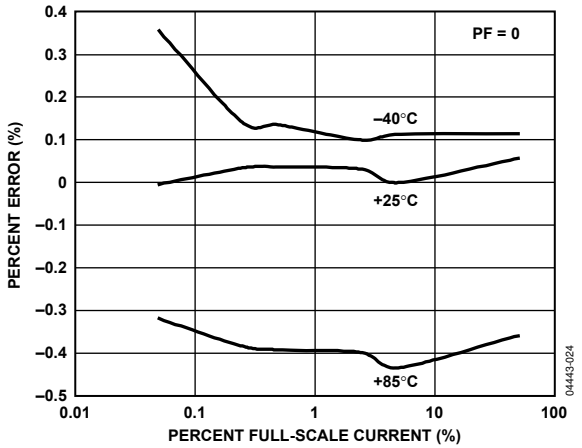

Figure 24. Reactive Energy Error as a Percentage of Reading (Gain = +4) over Temperature with Internal Reference and Integrator On

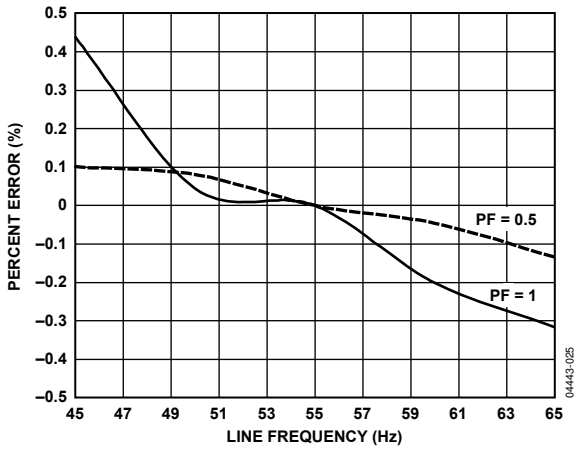

Figure 25. Active Energy Error as a Percentage of Reading (Gain = +4) over Frequency with Internal Reference and Integrator On

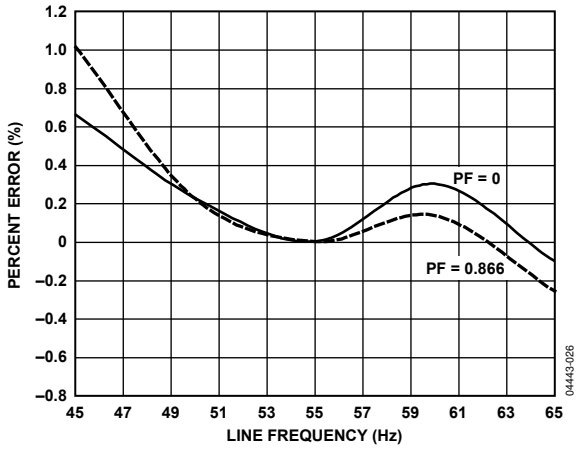

Figure 26. Reactive Energy Error as a Percentage of Reading (Gain = +4) over Frequency with Internal Reference and Integrator On

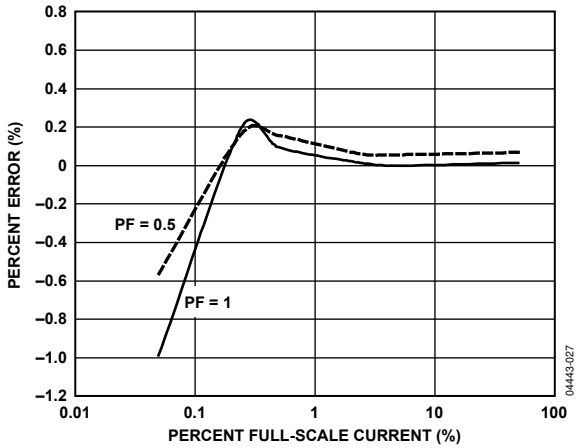

Figure 27. IRMS Error as a Percentage of Reading (Gain = +1) with Internal Reference and Integrator Off

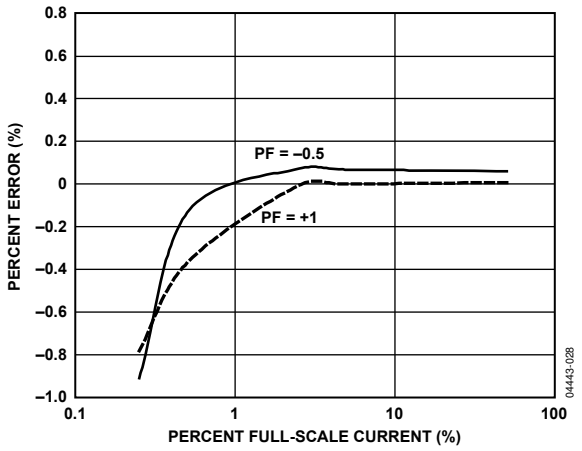

Figure 28. IRMS Error as a Percentage of Reading (Gain = +4) with Internal Reference and Integrator On

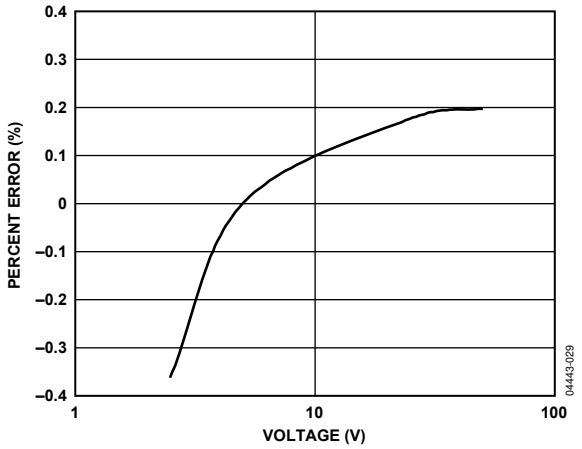

Figure 29. VRMS Error as a Percentage of Reading (Gain = +1) with Internal Reference

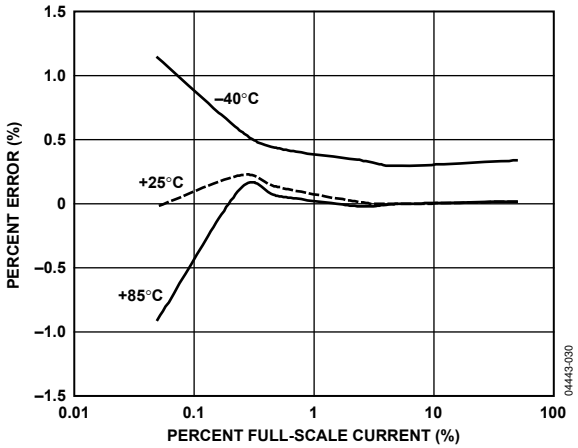

Figure 30. Apparent Energy Error as a Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator Off

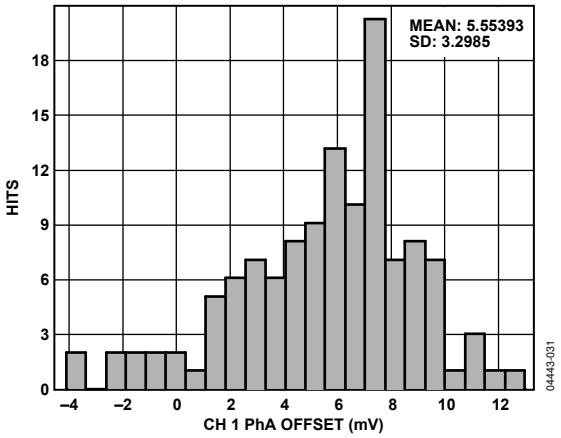

Figure 31. Phase A Channel 1 Offset Distribution

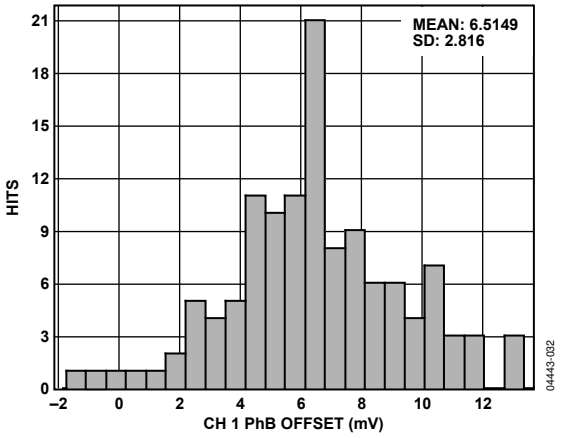

Figure 32. Phase B Channel 1 Offset Distribution

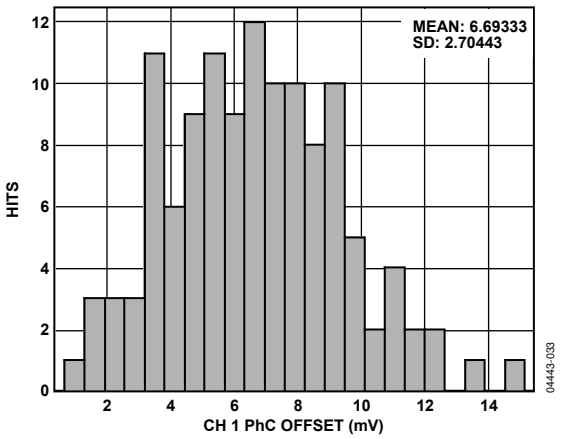

Figure 33. Phase C Channel 1 Offset Distribution

TEST CIRCUITS

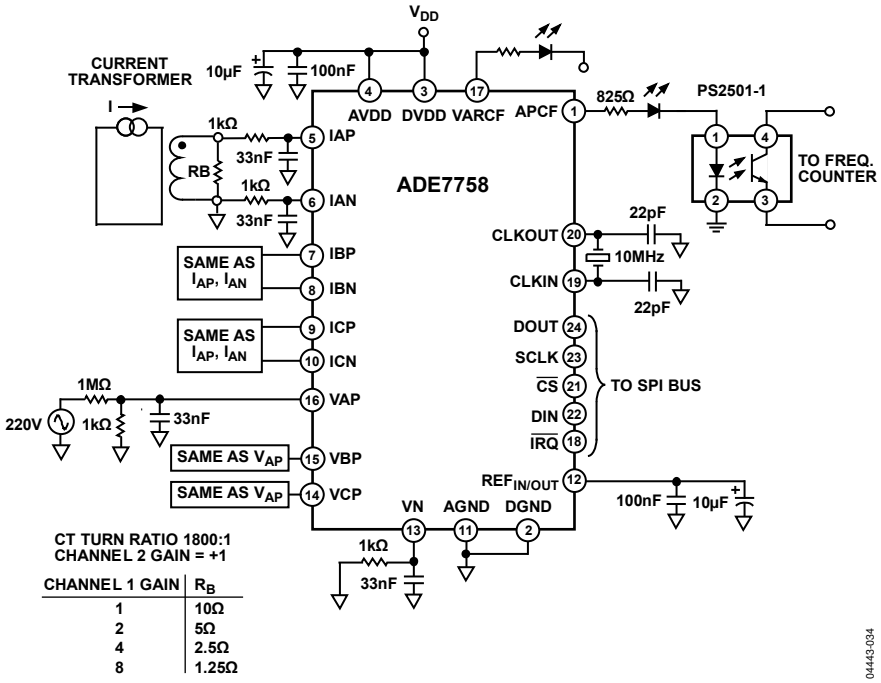

Figure 34. Test Circuit for Integrator Off

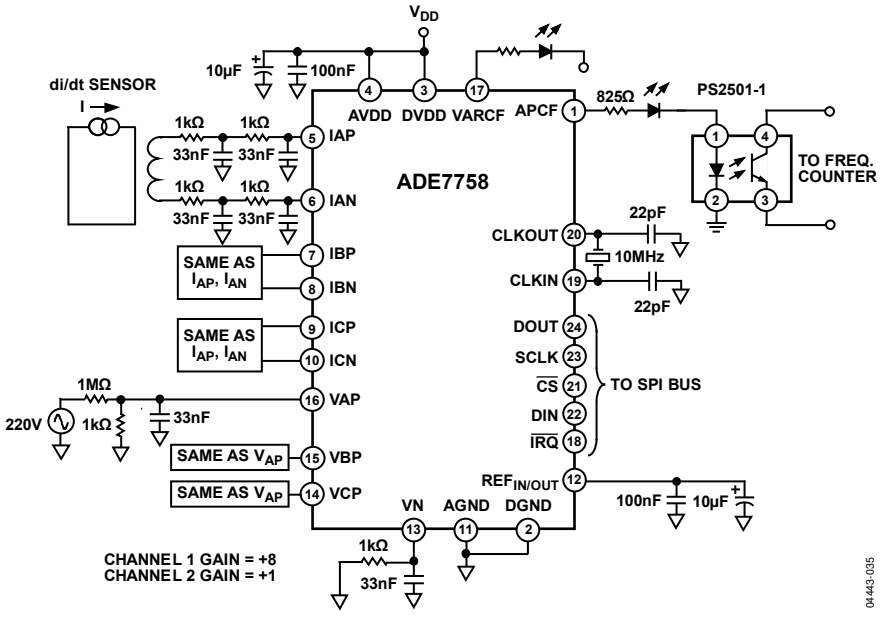

Figure 35. Test Circuit for Integrator On

THEORY OF OPERATION

ANTIALIASING FILTER

This filter prevents aliasing, which is an artifact of all sampled systems. Input signals with frequency components higher than half the ADC sampling rate distort the sampled signal at a frequency below half the sampling rate. This happens with all ADCs, regardless of the architecture. The combination of the high sampling rate Σ-Δ ADC used in the ADE7758 with the relatively low bandwidth of the energy meter allows a very simple low-pass filter (LPF) to be used as an antialiasing filter. A simple RC filter (single pole) with a corner frequency of 10 kHz produces an attenuation of approximately 40 dB at 833 kHz. This is usually sufficient to eliminate the effects of aliasing.

ANALOG INPUTS

The ADE7758 has six analog inputs divided into two channels: current and voltage. The current channel consists of three pairs of fully differential voltage inputs: IAP and IAN, IBP and IBN, and ICP and ICN. These fully differential voltage input pairs have a maximum differential signal of ±0.5 V. The current channel has a programmable gain amplifier (PGA) with possible gain selection of 1, 2, or 4. In addition to the PGA, the current channels also have a full-scale input range selection for the ADC. The ADC analog input range selection is also made using the gain register (see Figure 38). As mentioned previously, the maximum differential input voltage is ±0.5 V. However, by using Bit 3 and Bit 4 in the gain register, the maximum ADC input voltage can be set to ±0.5 V, ±0.25 V, or ±0.125 V on the current channels. This is achieved by adjusting the ADC reference (see the Reference Circuit section).

Figure 36 shows the maximum signal levels on the current channel inputs. The maximum common-mode signal is ±25 mV, as shown in Figure 37.

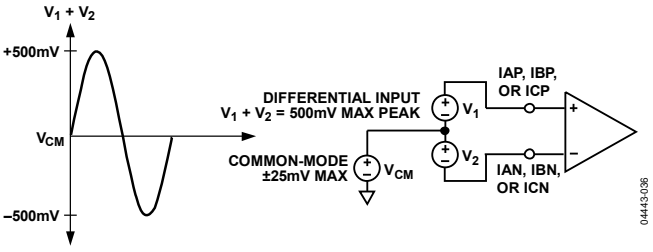

Figure 36. Maximum Signal Levels, Current Channels, Gain = 1

The voltage channel has three single-ended voltage inputs: VAP, VBP, and VCP. These single-ended voltage inputs have a maximum input voltage of ±0.5 V with respect to VN. Both the current and voltage channel have a PGA with possible gain selections of 1, 2, or 4. The same gain is applied to all the inputs of each channel.

Figure 37 shows the maximum signal levels on the voltage channel inputs. The maximum common-mode signal is ±25 mV, as shown in Figure 36.

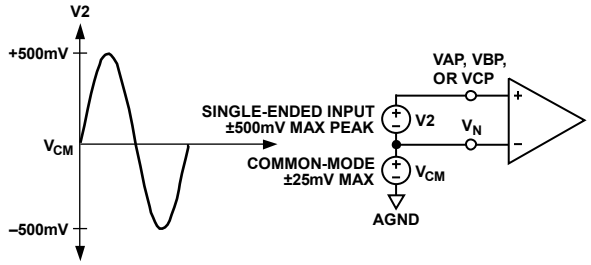

Figure 37. Maximum Signal Levels, Voltage Channels, Gain = 1

The gain selections are made by writing to the gain register. Bit 0 to Bit 1 select the gain for the PGA in the fully differential current channel. The gain selection for the PGA in the single-ended voltage channel is made via Bit 5 to Bit 6. Figure 38 shows how a gain selection for the current channel is made using the gain register.

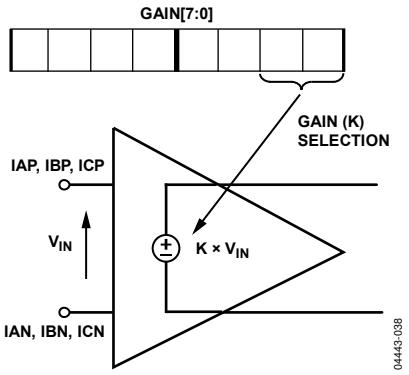

Figure 38. PGA in Current Channel

Figure 39 shows how the gain settings in PGA 1 (current channel) and PGA 2 (voltage channel) are selected by various bits in the gain register.

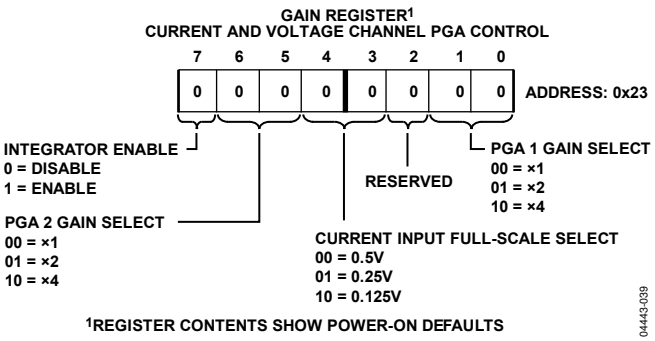

Figure 39. Analog Gain Register

Bit 7 of the gain register is used to enable the digital integrator in the current signal path. Setting this bit activates the digital integrator (see the DI/DT Current Sensor and Digital Integrator section).

CURRENT CHANNEL ADC

Figure 41 shows the ADC and signal processing path for the input IA of the current channels (same for IB and IC). In waveform sampling mode, the ADC outputs are signed twos complement 24-bit data-words at a maximum of 26.0 kSPS (thousand samples per second). With the specified full-scale analog input signal of ±0.5 V, the ADC produces its maximum output code value (see Figure 41). This diagram shows a full-scale voltage signal being applied to the differential inputs IAP and IAN. The ADC output swings between 0xD7AE14 (−2,642,412) and 0x2851EC (+2,642,412).

Current Channel Sampling

The waveform samples of the current channel can be routed to the WFORM register at fixed sampling rates by setting the WAVSEL[2:0] bit in the WAVMODE register to 000 (binary) (see Table 20). The phase in which the samples are routed is set by setting the PHSEL[1:0] bits in the WAVMODE register. Energy calculation remains uninterrupted during waveform sampling.

When in waveform sample mode, one of four output sample rates can be chosen by using Bit 5 and Bit 6 of the WAVMODE register (DTRT[1:0]). The output sample rate can be 26.04 kSPS, 13.02 kSPS, 6.51 kSPS, or 3.25 kSPS. By setting the WFSM bit in the interrupt mask register to Logic 1, the interrupt request output $\overline{\text{IRQ}}$ goes active low when a sample is available. The timing is shown in Figure 40. The 24-bit waveform samples are transferred from the ADE7758 one byte (8-bits) at a time, with the most significant byte shifted out first.

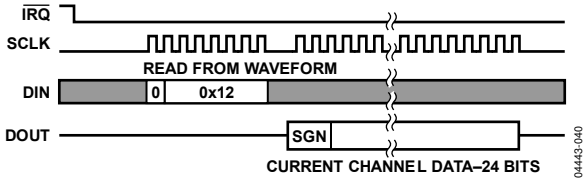

Figure 40. Current Channel Waveform Sampling

The interrupt request output $\overline{\text{IRQ}}$ stays low until the interrupt routine reads the reset status register (see the Interrupts section).

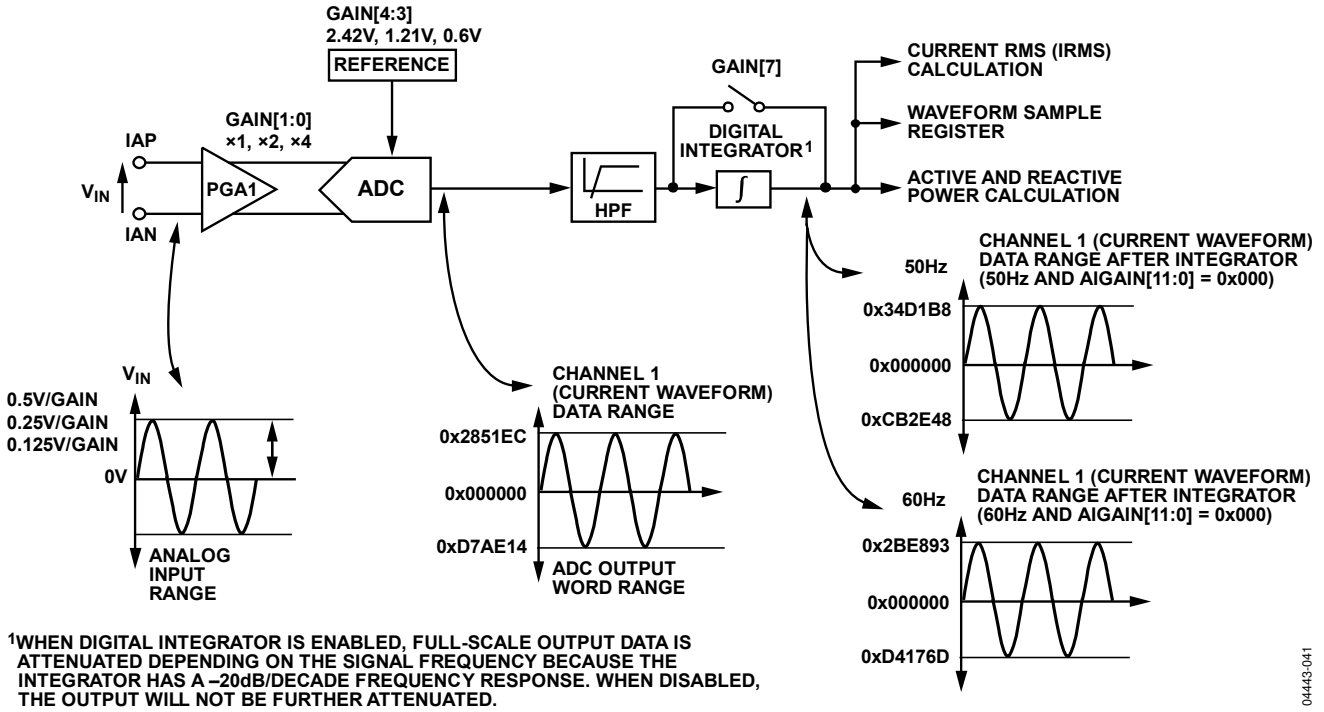

Figure 41. Current Channel Signal Path

DI/DT CURRENT SENSOR AND DIGITAL INTEGRATOR

The di/dt sensor detects changes in the magnetic field caused by the ac current. Figure 42 shows the principle of a di/dt current sensor.

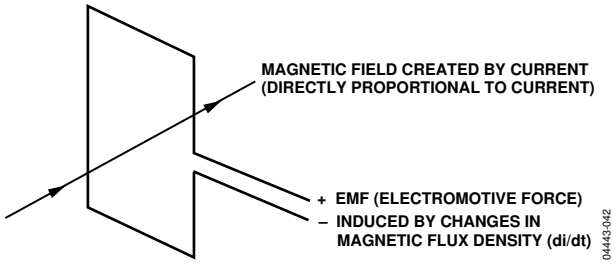

Figure 42. Principle of a di/dt Current Sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. The changes in the magnetic flux density passing through a conductor loop generate an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal that is proportional to the di/dt of the current. The voltage output from the di/dt current sensor is determined by the mutual inductance between the current carrying conductor and the di/dt sensor.

The current signal needs to be recovered from the di/dt signal before it can be used. An integrator is therefore necessary to restore the signal to its original form. The ADE7758 has a built-in digital integrator to recover the current signal from the di/dt sensor. The digital integrator on Channel 1 is disabled by default when the ADE7758 is powered up. Setting the MSB of the GAIN[7:0] register turns on the integrator. Figure 43 to Figure 46 show the magnitude and phase response of the digital integrator.

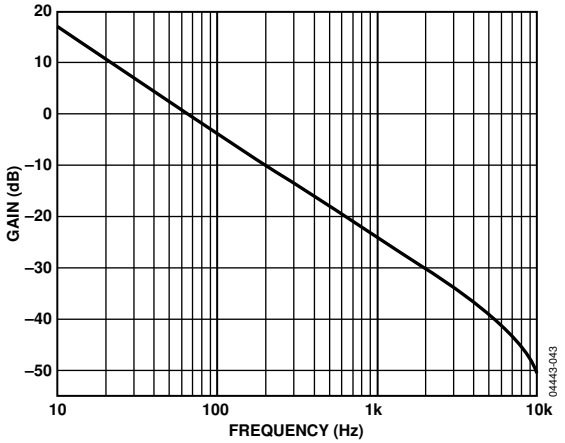

Figure 43. Combined Gain Response of the Digital Integrator and Phase Compensator

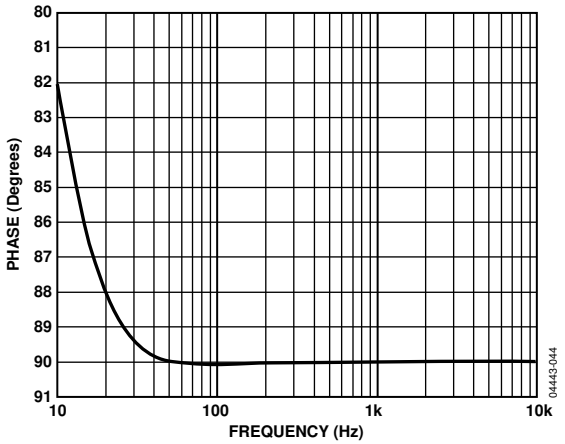

Figure 44. Combined Phase Response of the Digital Integrator and Phase Compensator

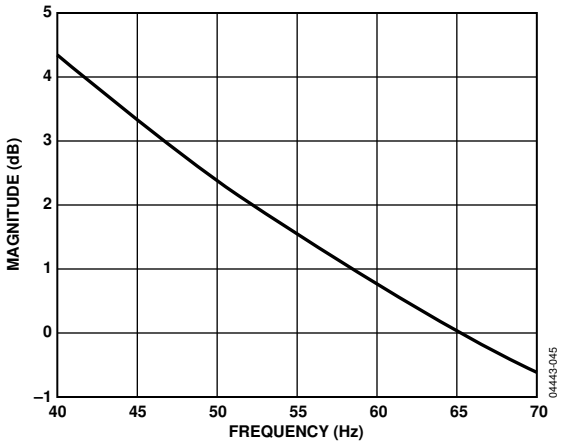

Figure 45. Combined Gain Response of the Digital Integrator and Phase Compensator (40 Hz to 70 Hz)

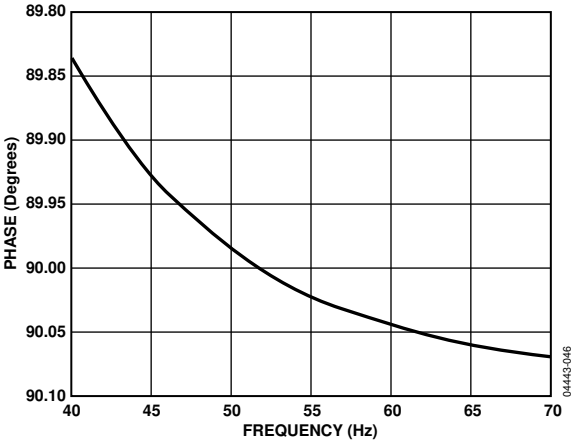

Figure 46. Combined Phase Response of the Digital Integrator and Phase Compensator (40 Hz to 70 Hz)

Note that the integrator has a −20 dB/dec attenuation and approximately −90° phase shift. When combined with a di/dt sensor, the resulting magnitude and phase response should be a flat gain over the frequency band of interest. However, the di/dt sensor has a 20 dB/dec gain associated with it and generates significant high frequency noise. A more effective antialiasing filter is needed to avoid noise due to aliasing (see the Theory of Operation section).

When the digital integrator is switched off, the ADE7758 can be used directly with a conventional current sensor, such as a current transformer (CT) or a low resistance current shunt.

PEAK CURRENT DETECTION

The ADE7758 can be programmed to record the peak of the current waveform and produce an interrupt if the current exceeds a preset limit.

Peak Current Detection Using the PEAK Register

The peak absolute value of the current waveform within a fixed number of half-line cycles is stored in the IPEAK register. Figure 47 illustrates the timing behavior of the peak current detection.

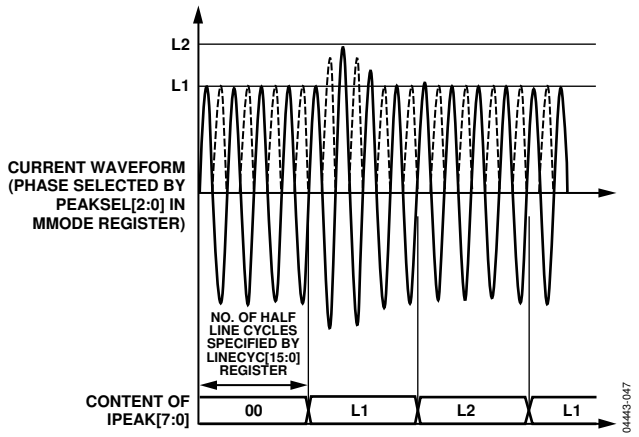

Figure 47. Peak Current Detection Using the IPEAK Register

Note that the content of the IPEAK register is equivalent to Bit 14 to Bit 21 of the current waveform sample. At full-scale analog input, the current waveform sample is 0x2851EC. The IPEAK at full-scale input is therefore expected to be 0xA1.

In addition, multiple phases can be activated for the peak detection simultaneously by setting more than one of the PEAKSEL[2:4] bits in the MMODE register to logic high. These bits select the phase for both voltage and current peak measurements. Note that if more than one bit is set, the VPEAK and IPEAK registers can hold values from two different phases, that is, the voltage and current peak are independently processed (see the Peak Current Detection section).

Note that the number of half-line cycles is based on counting the zero crossing of the voltage channel. The ZXSEL[2:0] bits in the LCYCMODE register determine which voltage channels are used for the zero-crossing detection. The same signal is also used for line cycle energy accumulation mode if activated (see the Line Cycle Accumulation Mode Register (0X17) section).

OVERCURRENT DETECTION INTERRUPT

Figure 48 illustrates the behavior of the overcurrent detection.

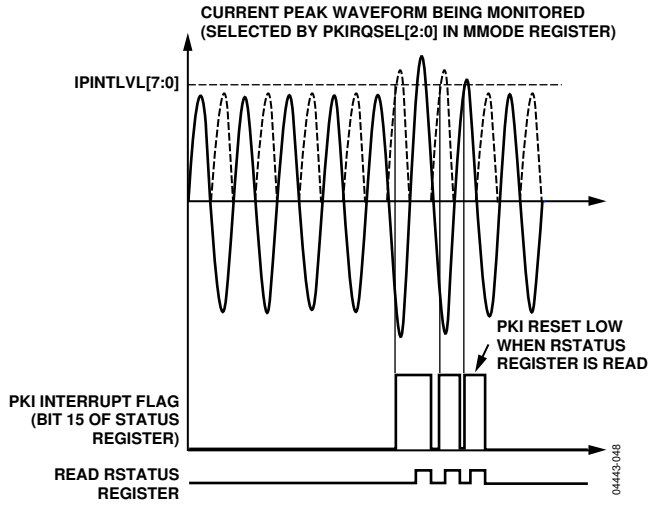

Figure 48. ADE7758 Overcurrent Detection

Note that the content of the IPINTLVL[7:0] register is equivalent to Bit 14 to Bit 21 of the current waveform sample. Therefore, setting this register to 0xA1 represents putting peak detection at full-scale analog input. Figure 48 shows a current exceeding a threshold. The overcurrent event is recorded by setting the PKI flag (Bit 15) in the interrupt status register. If the PKI enable bit is set to Logic 1 in the interrupt mask register, the $\overline{\text{IRQ}}$ logic output goes active low (see the Interrupts section).

Similar to peak level detection, multiple phases can be activated for peak detection. If any of the active phases produce waveform samples above the threshold, the PKI flag in the interrupt status register is set. The phase of which overcurrent is monitored is set by the PKIRQSEL[2:0] bits in the MMODE register (see Table 19).

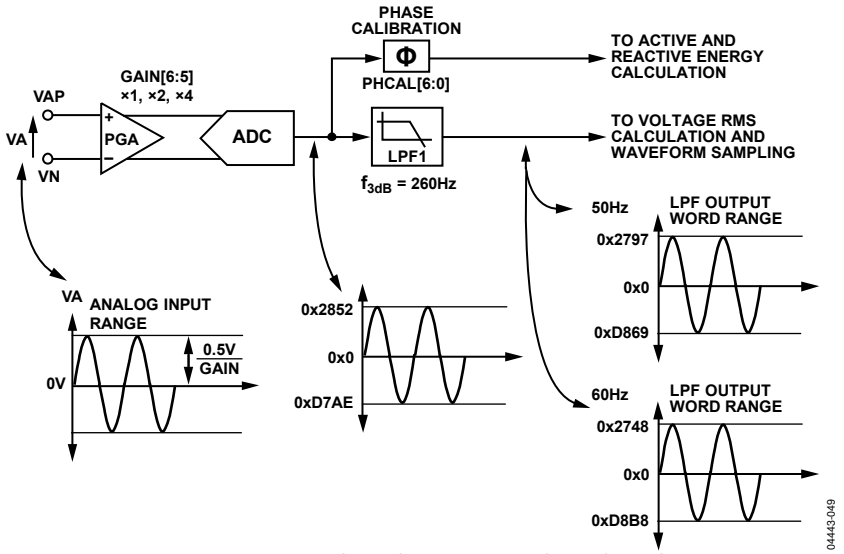

Figure 49. ADC and Signal Processing in Voltage Channel

VOLTAGE CHANNEL ADC

Figure 49 shows the ADC and signal processing chain for the input VA in the voltage channel. The VB and VC channels have similar processing chains.

For active and reactive energy measurements, the output of the ADC passes to the multipliers directly and is not filtered. This solution avoids the much larger multibit multiplier and does not affect the accuracy of the measurement. An HPF is not implemented on the voltage channel to remove the dc offset because the HPF on the current channel alone should be sufficient to eliminate error due to ADC offsets in the power calculation. However, ADC offset in the voltage channels produces large errors in the voltage rms calculation and affects the accuracy of the apparent energy calculation.

Voltage Channel Sampling

The waveform samples on the voltage channels can also be routed to the WFORM register. However, before passing to the WFORM register, the ADC outputs pass through a single-pole, low-pass filter (LPF1) with a cutoff frequency at 260 Hz. Figure 50 shows the magnitude and phase response of LPF1. This filter attenuates the signal slightly. For example, if the line frequency is 60 Hz, the signal at the output of LPF1 is attenuated by 3.575%. The waveform samples are 16-bit, twos complement data ranging between 0x2748 (+10,056d) and 0xD8B8 (−10,056d). The data is sign extended to 24-bit in the WFORM register.

$$H(f) = \frac{1}{\sqrt{1+\left(\frac{60\text{ Hz}}{260\text{ Hz}}\right)^2}} = 0.974 = -0.225\text{ dB} \quad (3)$$

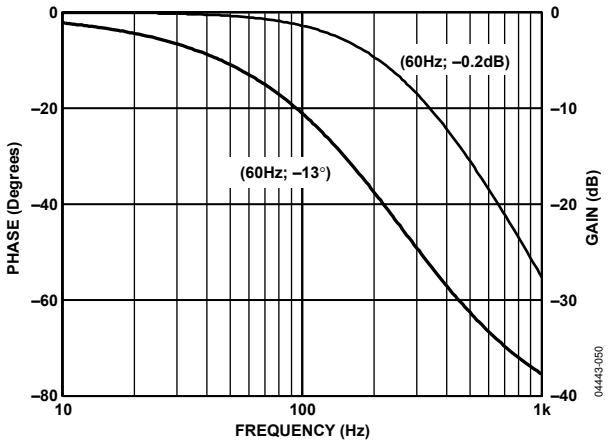

Figure 50. Magnitude and Phase Response of LPF1

Note that LPF1 does not affect the active and reactive energy calculation because it is only used in the waveform sampling signal path. However, waveform samples are used for the voltage rms calculation and the subsequent apparent energy accumulation.

The WAVSEL[2:0] bits in the WAVMODE register should be set to 001 (binary) to start the voltage waveform sampling. The PHSEL[1:0] bits control the phase from which the samples are routed. In waveform sampling mode, one of four output sample rates can be chosen by changing Bit 5 and Bit 6 of the WAVMODE register (see Table 20). The available output sample rates are 26.0 kSPS, 13.5 kSPS, 6.5 kSPS, or 3.3 kSPS. By setting the WFSM bit in the interrupt mask register to Logic 1, the interrupt request output $\overline{\text{IRQ}}$ goes active low when a sample is available. The 24-bit waveform samples are transferred from the ADE7758 one byte (8 bits) at a time, with the most significant byte shifted out first.

The sign of the register is extended in the upper 8 bits. The timing is the same as for the current channels, as seen in Figure 40.

ZERO-CROSSING DETECTION

The ADE7758 has zero-crossing detection circuits for each of the voltage channels (VAN, VBN, and VCN). Figure 51 shows how the zero-cross signal is generated from the output of the ADC of the voltage channel.

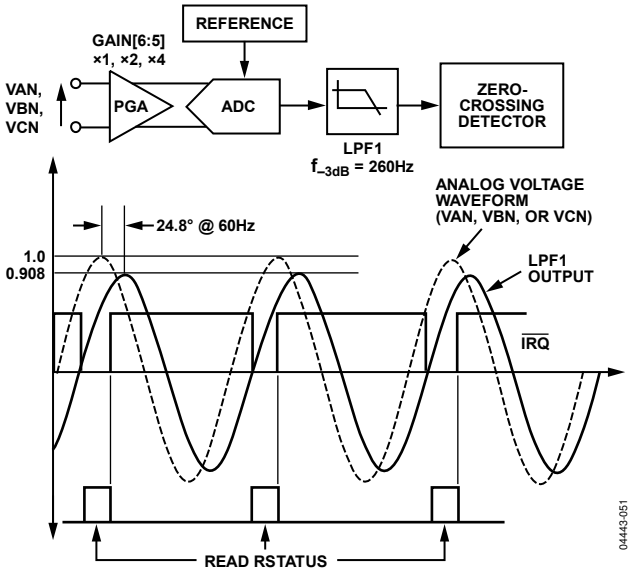

Figure 51. Zero-Crossing Detection on Voltage Channels

The zero-crossing interrupt is generated from the output of LPF1. LPF1 has a single pole at 260 Hz (CLKIN = 10 MHz). As a result, there is a phase lag between the analog input signal of the voltage channel and the output of LPF1. The phase response of this filter is shown in the Voltage Channel Sampling section. The phase lag response of LPF1 results in a time delay of approximately 1.1 ms (at 60 Hz) between the zero crossing on the voltage inputs and the resulting zero-crossing signal. Note that the zero-crossing signal is used for the line cycle accumulation mode, zero-crossing interrupt, and line period/frequency measurement.

When one phase crosses from negative to positive, the corresponding flag in the interrupt status register (Bit 9 to Bit 11) is set to Logic 1. An active low in the $\overline{\text{IRQ}}$ output also appears if the corresponding ZX bit in the interrupt mask register is set to Logic 1. Note that only zero crossing from negative to positive generates an interrupt.

The flag in the interrupt status register is reset to 0 when the interrupt status register with reset (RSTATUS) is read. Each phase has its own interrupt flag and mask bit in the interrupt register.

Zero-Crossing Timeout

Each zero-crossing detection has an associated internal timeout register (not accessible to the user). This unsigned, 16-bit register is decreased by 1 every 384/CLKIN seconds. The registers are reset to a common user-programmed value, that is, the zero-crossing timeout register (ZXTOUT[15:0], Address 0x1B), every time a zero crossing is detected on its associated input. The default value of ZXTOUT is 0xFFFF. If the internal register decrements to 0 before a zero crossing at the corresponding input is detected, it indicates an absence of a zero crossing in the time determined by the ZXTOUT[15:0]. The ZXTOx detection bit of the corresponding phase in the interrupt status register is then switched on (Bit 6 to Bit 8). An active low on the $\overline{\text{IRQ}}$ output also appears if the ZXTOx mask bit for the corresponding phase in the interrupt mask register is set to Logic 1. Figure 52 shows the mechanism of the zero-crossing timeout detection when the Line Voltage A stays at a fixed dc level for more than 384/CLKIN × ZXTOUT[15:0] seconds.

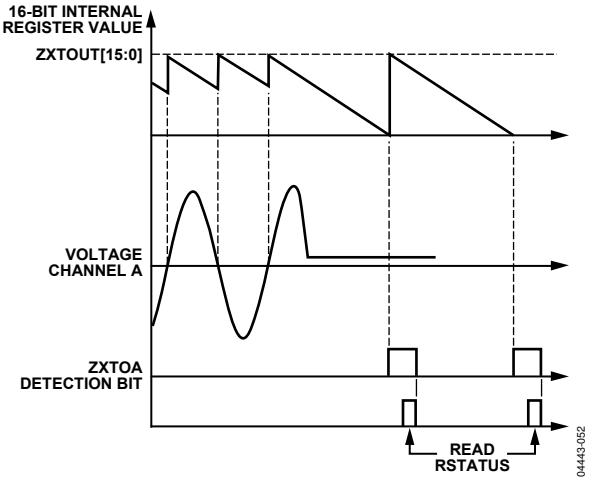

Figure 52. Zero-Crossing Timeout Detection

PHASE COMPENSATION

When the HPF in the current channel is disabled, the phase error between the current channel (IA, IB, or IC) and the corresponding voltage channel (VA, VB, or VC) is negligible. When the HPF is enabled, the current channels have phase response (see Figure 53 through Figure 55). The phase response is almost 0 from 45 Hz to 1 kHz. The frequency band is sufficient for the requirements of typical energy measurement applications.

However, despite being internally phase compensated, the ADE7758 must work with transducers that may have inherent phase errors. For example, a current transformer (CT) with a phase error of 0.1° to 0.3° is not uncommon. These phase errors can vary from part to part, and they must be corrected to perform accurate power calculations.

The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE7758 provides a means of digitally calibrating these small phase errors. The ADE7758 allows a small time delay or time advance to be introduced into the signal processing chain to compensate for the small phase errors.

The phase calibration registers (APHCAL, BPHCAL, and CPHCAL) are twos complement, 7-bit sign-extended registers that can vary the time advance in the voltage channel signal path from +153.6 µs to −75.6 µs (CLKIN = 10 MHz),

respectively. Negative values written to the PHCAL registers represent a time advance, and positive values represent a time delay. One LSB is equivalent to 1.2 μs of time delay or 2.4 μs of time advance with a CLKIN of 10 MHz. With a line frequency of 60 Hz, this gives a phase resolution of 0.026° (360° × 1.2 μs × 60 Hz) at the fundamental in the positive direction (delay) and 0.052° in the negative direction (advance). This corresponds to a total correction range of −3.32° to +1.63° at 60 Hz.

Figure 56 illustrates how the phase compensation is used to remove a 0.1° phase lead in IA of the current channel from the external current transducer. To cancel the lead (0.1°) in the current channel of Phase A, a phase lead must be introduced into the corresponding voltage channel. The resolution of the phase adjustment allows the introduction of a phase lead of 0.104°. The phase lead is achieved by introducing a time advance into VA. A time advance of 4.8 μs is made by writing −2 (0x7E) to the time delay block (APHCAL[6:0]), thus reducing the amount of time delay by 4.8 μs or equivalently, 360° × 4.8 μs × 60 Hz = 0.104° at 60 Hz.

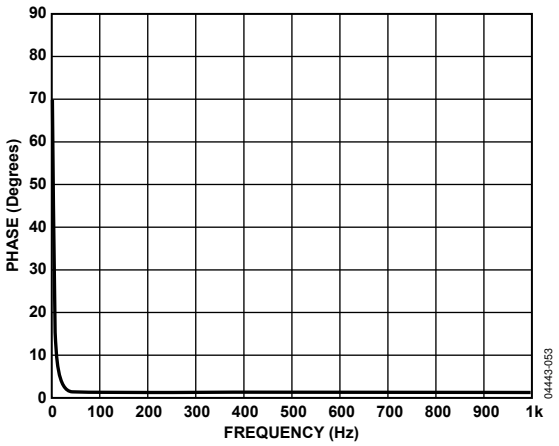

Figure 53. Phase Response of the HPF and Phase Compensation (10 Hz to 1 kHz)

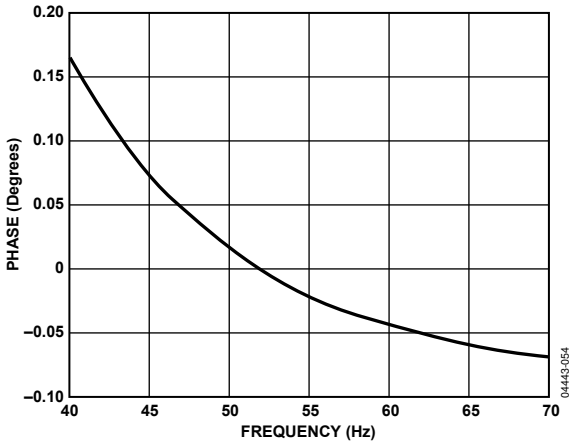

Figure 54. Phase Response of the HPF and Phase Compensation (40 Hz to 70 Hz)

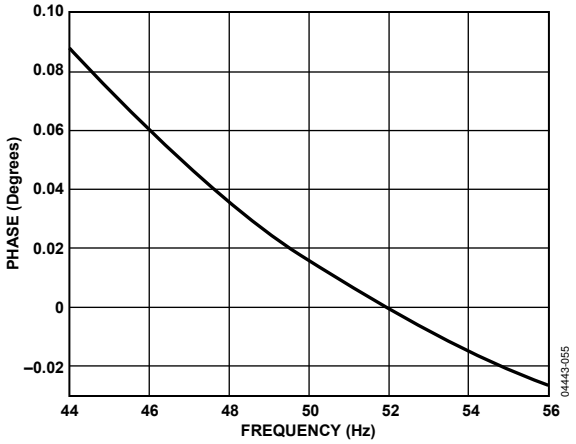

Figure 55. Phase Response of HPF and Phase Compensation (44 Hz to 56 Hz)