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Single-Phase Active and Apparent Energy Metering IC

Data Sheet

ADE7763

FEATURES

High accuracy; supports IEC 61036/60687, IEC62053-21, and IEC62053-22
On-chip digital integrator enables direct interface-to-current sensors with di/dt output
A PGA in the current channel allows direct interface to shunts and current transformers
Active and apparent energy, sampled waveform, and current and voltage rms
Less than 0.1% error in active energy measurement over a dynamic range of 1000 to 1 at 25°C
Positive-only energy accumulation mode available
On-chip user programmable threshold for line voltage surge and SAG and PSU supervisory
Digital calibration for power, phase, and input offset
On-chip temperature sensor (±3°C typical)
SPI®-compatible serial interface
Pulse output with programmable frequency
Interrupt request pin ($\overline{\text{IRQ}}$) and status register
Reference 2.4 V with external overdrive capability
Single 5 V supply, low power (25 mW typical)

GENERAL DESCRIPTION

The ADE7763[1] features proprietary ADCs and fixed function DSP for high accuracy over large variations in environmental conditions and time. The ADE7763 incorporates two second-order, 16-bit Σ-Δ ADCs, a digital integrator (on Ch1), reference circuitry, a temperature sensor, and all the signal processing required to perform active and apparent energy measurements, line-voltage period measurements, and rms calculation on the voltage and current channels. The selectable on-chip digital integrator provides direct interface to di/dt current sensors such as Rogowski coils, eliminating the need for an external analog integrator and resulting in excellent long-term stability and precise phase matching between the current and the voltage channels.

The ADE7763 provides a serial interface to read data and a pulse output frequency (CF) that is proportional to the active power. Various system calibration features such as channel offset correction, phase calibration, and power calibration ensure high accuracy. The part also detects short duration, low or high voltage variations.

The positive-only accumulation mode gives the option to accumulate energy only when positive power is detected. An internal no-load threshold ensures that the part does not exhibit any creep when there is no load. The zero-crossing output (ZX) produces a pulse that is synchronized to the zero-crossing point of the line voltage. This signal is used internally in the line cycle active and apparent energy accumulation modes, which enables faster calibration.

The interrupt status register indicates the nature of the interrupt, and the interrupt enable register controls which event produces an output on the $\overline{\text{IRQ}}$ pin, an open-drain, active low logic output.

The ADE7763 is available in a 20-lead SSOP package.

FUNCTIONAL BLOCK DIAGRAM

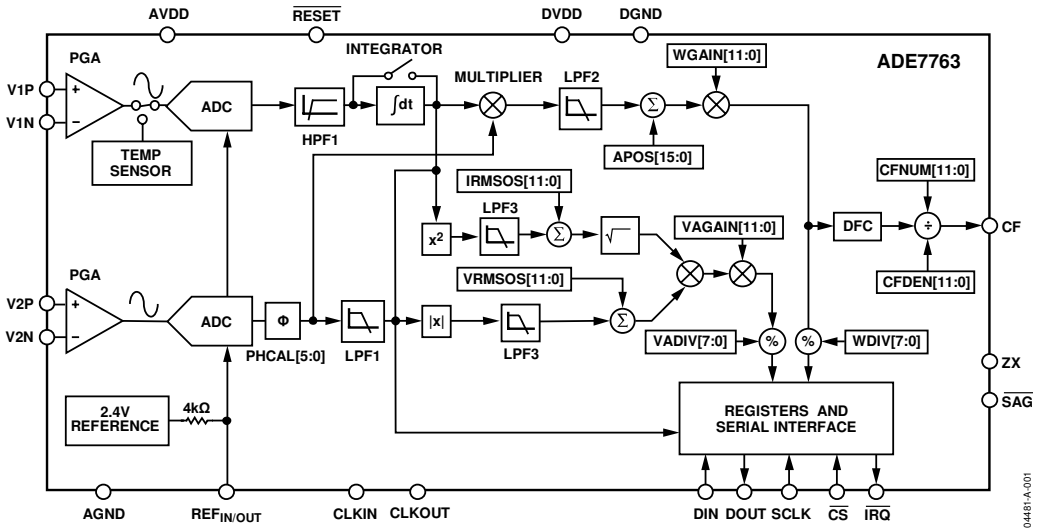

Figure 1.

[1] U.S. Patents 5,745,323; 5,760,617; 5,862,069; 5,872,469.

Rev. C Document Feedback

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Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADE7763 Evaluation Board

DOCUMENTATION

Application Notes

- AN-564: A Power Meter Reference Design Based on the ADE7756
- AN-639: Frequently Asked Questions (FAQs) Analog Devices Energy (ADE) Products

Data Sheet

- ADE7763: Single-Phase Active and Apparent Energy Metering IC Data Sheet

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Emerging Energy Applications Solutions Bulletin, Volume 10, Issue 4

Technical Articles

- Current Sensing for Energy Metering
- Digital Energy Meters by the Millions
- Energy measurement ICs Simplify Meter Design
- How Solid Is Your Solid-State Energy Meter? Not All Ics Are Created Equal.
- IC Technology and Failure Mechanisms - Understanding Reliability Standards Can Raise Quality of Meters
- Measuring Harmonic Energy with a Solid State Energy Meter
- Measuring Reactive Power in Energy Meters
- Reactive Energy Measurement Made Simple
- RF Meets Power Lines: Designing Intelligent Smart Grid Systems that Promote Energy Efficiency
- Solid State Solutions For Electricity Metrology
- Tapping The Potential Of Electronic Energy Metering
- Trusting Integrated Circuits in Metering Applications

DESIGN RESOURCES

- ADE7763 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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TABLE OF CONTENTS

REVISION HISTORY

1/13—Rev. B to Rev. C

Changes to Figure 1 1
Moved Revision History Section 3
Changes to Table 2 6
Changes to Table 4 9
Changes to Figure 24 14
Changes to Zero-Crossing Detection Section 16
Changes to Period Measurement Section 17
Changes to Peak Level Record Section 18
Change to Figure 37 19
Changes to Figure 43, Channel 1 Sampling Section, and Channel 1 RMS Calculation Section 22
Changes to Channel 1 RMS Offset Compensation Section and Channel 2 Sampling Section 23
Changes to Channel 2 RMS Calculation Section and Channel 2 RMS Offset Compensation Section 24
Changes to Energy Calculation Section 27
Changes to Power Offset Calibration Section 29
Changes to Positive-Only Accumulation Mode Section 31
Changes to Serial Interface Section 45
Changes to Table 9 48
Change to Table 12, Bit 1 Description 53
Changes to Ordering Guide 55

7/09—Rev. A to Rev. B

Changes to Zero Crossing Detection Section 15
Changes to Period Measurement Section 16
Changes to Channel 1 RMS Offset Calculation Section 22
Changes to Channel 1 RMS Offset Compensation Section 22
Changes to Figure 48 23
Changes to Channel 2 RMS Calculation Section 23
Changes to Table 11, Bit 15 Description 51
Changes to Table 12, Bit 4 Description 52

10/04—Data Sheet Changed from Rev. 0 to Rev. A

Changes to Period Measurement Section 16
Changes to Temperature Measurement Section 19
Change to Energy-to-Frequency Conversion Section 28
Update to Figure 61 29
Change to Apparent Energy Calculation Section 32
Change to Description of AEHF and VAEHF Bits 52
Changes to Ordering Guide 54

4/04—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 3.579545 MHz XTAL, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 1. Specifications[1, 2]

Parameter	Spec	Unit	Test Conditions/Comments
ENERGY MEASUREMENT ACCURACY			
Active Power Measurement Error			CLKIN = 3.579545 MHz
Channel 1 Range = 0.5 V Full Scale			Channel 2 = 300 mV rms/60 Hz, gain = 2
Gain = 1	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 2	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 4	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 8	0.1	% typ	Over a dynamic range 1000 to 1
Channel 1 Range = 0.25 V Full Scale			
Gain = 1	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 2	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 4	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 8	0.2	% typ	Over a dynamic range 1000 to 1
Channel 1 Range = 0.125 V Full Scale			
Gain = 1	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 2	0.1	% typ	Over a dynamic range 1000 to 1
Gain = 4	0.2	% typ	Over a dynamic range 1000 to 1
Gain = 8	0.2	% typ	Over a dynamic range 1000 to 1
Active Power Measurement Bandwidth	14	kHz	
Phase Error 1 between Channels	±0.05	max	Line frequency = 45 Hz to 65 Hz, HPF on
AC Power Supply Rejection[1]			AVDD = DVDD = 5 V + 175 mV rms/120 Hz
Output Frequency Variation (CF)	0.2	% typ	Channel 1 = 20 mV rms, gain = 16, range = 0.5 V
			Channel 2 = 300 mV rms/60 Hz, gain = 1
DC Power Supply Rejection[1]			AVDD = DVDD = 5 V ± 250 mV dc
Output Frequency Variation (CF)	±0.3	% typ	Channel 1 = 20 mV rms/60 Hz, gain = 16, range = 0.5 V
			Channel 2 = 300 mV rms/60 Hz, gain = 1
IRMS Measurement Error	0.5	% typ	Over a dynamic range 100 to 1
IRMS Measurement Bandwidth	14	kHz	
VRMS Measurement Error	0.5	% typ	Over a dynamic range 20 to 1
VRMS Measurement Bandwidth	140	Hz	
ANALOG INPUTS[3]			See the Analog Inputs section
Maximum Signal Levels	±0.5	V max	V1P, V1N, V2N, and V2P to AGND
Input Impedance (dc)	390	k min	
Bandwidth	14	kHz	CLKIN/256, CLKIN = 3.579545 MHz
Gain Error[1, 3]			External 2.5 V reference, gain = 1 on Channels 1 and 2
Channel 1			
Range = 0.5 V Full Scale	±4	% typ	V1 = 0.5 V dc
Range = 0.25 V Full Scale	±4	% typ	V1 = 0.25 V dc
Range = 0.125 V Full Scale	±4	% typ	V1 = 0.125 V dc
Channel 2	±4	% typ	V2 = 0.5 V dc
Offset Error 1	±32	mV max	Gain 1
Channel 1	±13	mV max	Gain 16
	±32	mV max	Gain 1
Channel 2	±13	mV max	Gain 16
WAVEFORM SAMPLING			Sampling CLKIN/128, 3.579545 MHz/128 = 27.9 kSPS
Channel 1			See the Channel 1 Sampling section
Signal-to-Noise Plus Distortion	62	dB typ	150 mV rms/60 Hz, range = 0.5 V, gain = 2
Bandwidth (−3 dB)	14	kHz	CLKIN = 3.579545 MHz
Channel 2			See the Channel 2 Sampling section
Signal-to-Noise Plus Distortion	60	dB typ	150 mV rms/60 Hz, gain = 2
Bandwidth (−3 dB)	140	Hz	CLKIN = 3.579545 MHz

Parameter	Spec	Unit	Test Conditions/Comments
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	2.6	V max	2.4 V + 8%
	2.2	V min	2.4 V – 8%
Input Capacitance	10	pF max	
ON-CHIP REFERENCE			Nominal 2.4 V at $REF_{IN/OUT}$ pin
Reference Error	±200	mV max	
Current Source	10	µA max	
Output Impedance	3.4	kΩ min	
Temperature Coefficient	30	ppm/°C typ	
CLKIN			All specifications CLKIN of 3.579545 MHz
Input Clock Frequency	4	MHz max	
	1	MHz min	
LOGIC INPUTS			
$\overline{RESET}$, DIN, SCLK, CLKIN, and $\overline{CS}$			
Input High Voltage, V_{INH}	2.4	V min	DVDD = 5 V ± 10%
Input Low Voltage, V_{INL}	0.8	V max	DVDD = 5 V ± 10%
Input Current, I_{IN}	±3	µA max	Typically 10 nA, V_{IN} = 0 V to DVDD
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS			
$\overline{SAG}$ and $\overline{IRQ}$			Open-drain outputs, 10 kΩ pull-up resistor
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5 mA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 0.8 mA
ZX and DOUT			
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5 mA
Output Low Voltage, V_{OL}	0.4	V max	I_{SINK} = 0.8 mA
CF			
Output High Voltage, V_{OH}	4	V min	I_{SOURCE} = 5 mA
Output Low Voltage, V_{OL}	1	V max	I_{SINK} = 7 mA
POWER SUPPLY			For specified performance
AVDD	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
DVDD	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
AIDD	3	mA max	Typically 2.0 mA
DIDD	4	mA max	Typically 3.0 mA

[1] See the Terminology section for explanation of specifications.
[2] See the plots in the Typical Performance Characteristics section.
[3] See the Analog Inputs section.

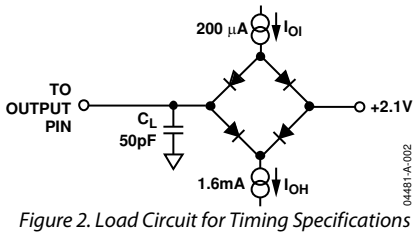

Figure 2. Load Circuit for Timing Specifications

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = 5 V ± 5%, AGND = DGND = 0 V, on-chip reference, CLKIN = 3.579545 MHz XTAL, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 2. Timing Characteristics[1, 2]

Parameter	Spec	Unit	Test Conditions/Comments
Write Timing			
t_1	50	ns min	$\overline{CS}$ falling edge to first SCLK falling edge.
t_2	50	ns min	SCLK logic high pulse width.
t_3	50	ns min	SCLK logic low pulse width.
t_4	10	ns min	Valid data setup time before falling edge of SCLK.
t_5	5	ns min	Data hold time after SCLK falling edge.
t_6	4	µs min	Minimum time between the end of data byte transfers.
t_7	3200	ns min	Minimum time between byte transfers during a serial write.
t_8	100	ns min)	$\overline{CS}$ hold time after SCLK falling edge.
Read Timing			
t_9[3]	4	µs min	Minimum time between read command (i.e., a write to communication register) and data read.
t_{10}	50	ns min	Minimum time between data byte transfers during a multibyte read.
t_{11}	30	ns min	Data access time after SCLK rising edge following a write to the communication register.
t_{12}[4]	100	ns max	Bus relinquish time after falling edge of SCLK.
	10	ns min	
t_{13}[5]	100	ns max	Bus relinquish time after rising edge of $\overline{CS}$.
	10	ns min	

[1] Sample tested during initial release and after any redesign or process change that could affect this parameter. All input signals are specified with tr = tf = 5 ns (10% to 90%) and timed from a voltage level of 1.6 V.
[2] See Figure 3, Figure 4, and the Serial Interface section.
[3] Minimum time between read command and data read for all registers except waveform register, which is t_9 = 500 ns min.
[4] Measured with the load circuit in Figure 2 and defined as the time required for the output to cross 0.8 V or 2.4 V.
[5] Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 2. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

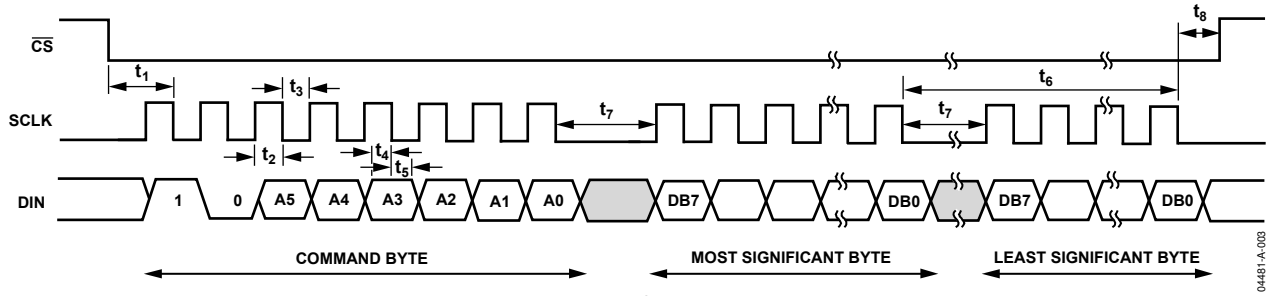

Figure 3. Serial Write Timing

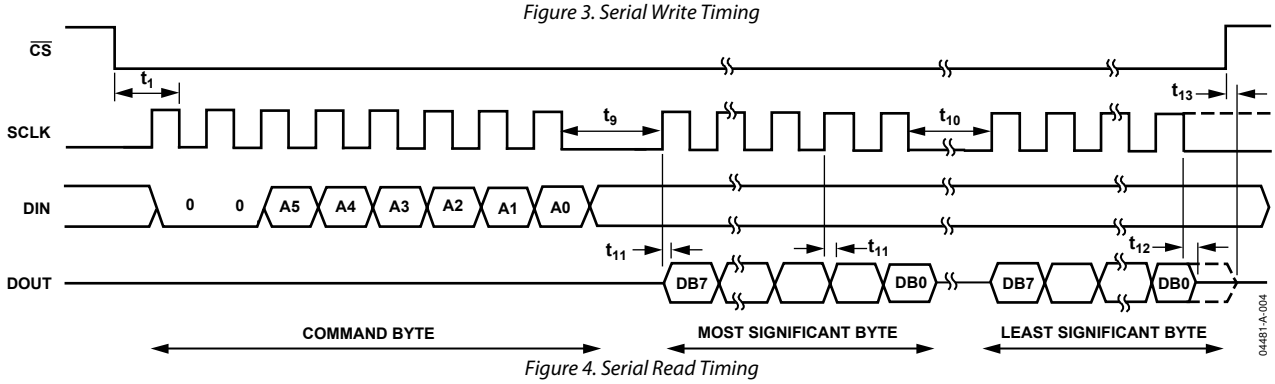

Figure 4. Serial Read Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AVDD to AGND	–0.3 V to +7 V
DVDD to DGND	–0.3 V to +7 V
DVDD to AVDD	–0.3 V to +0.3 V
Analog Input Voltage to AGND V1P, V1N, V2P, and V2N	–6 V to +6 V
Reference Input Voltage to AGND	–0.3 V to AVDD + 0.3 V
Digital Input Voltage to DGND	–0.3 V to DVDD + 0.3 V
Digital Output Voltage to DGND	–0.3 V to DVDD + 0.3 V
Operating Temperature Range	
Industrial	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
20-Lead SSOP, Power Dissipation	450 mW
θ_{JA} Thermal Impedance	112°C/W
Lead Temperature, Soldering	
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7763 is defined by the following formula:

$$Percent\ Error = \left(\frac{Energy\ Register\ ADE7763 - True\ Energy}{True\ Energy} \right) \times 100\%$$

Phase Error between Channels

The digital integrator and the high-pass filter (HPF) in Channel 1 have a nonideal phase response. To offset this phase response and equalize the phase response between channels, two phase-correction networks are placed in Channel 1: one for the digital integrator and the other for the HPF. The phase correction networks correct the phase response of the corresponding component and ensure a phase match between Channel 1 (current) and Channel 2 (voltage) to within ±0.1° over a range of 45 Hz to 65 Hz with the digital integrator off. With the digital integrator on, the phase is corrected to within ±0.4° over a range of 45 Hz to 65 Hz.

Power Supply Rejection

This quantifies the ADE7763 measurement error as a percentage of the reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when an ac (175 mV rms/120 Hz) signal is introduced to the supplies. Any error introduced by this ac signal is expressed as a percentage of the reading—see the Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained with the same input signal levels when the supplies are varied ±5%. Any error introduced is again expressed as a percentage of the reading.

ADC Offset Error

The dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection—see the Typical Performance Characteristics section. However, when HPF1 is switched on, the offset is removed from Channel 1 (current) and the power calculation is not affected by this offset. The offsets can be removed by performing an offset calibration—see the Analog Inputs section.

Gain Error

The difference between the measured ADC output code (minus the offset) and the ideal output code—see the Channel 1 ADC and Channel 2 ADC sections. It is measured for each of the input ranges on Channel 1 (0.5 V, 0.25 V, and 0.125 V). The difference is expressed as a percentage of the ideal code.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

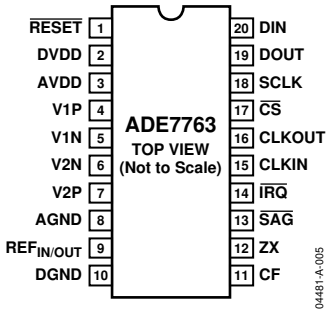

Figure 5. Pin Configuration (SSOP Package)

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Reset Pin[1]. A logic low on this pin holds the ADCs and digital circuitry (including the serial interface) in a reset condition.
2	DVDD	Digital Power Supply. This pin provides the supply voltage for the digital circuitry. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled to DGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
3	AVDD	Analog Power Supply. This pin provides the supply voltage for the analog circuitry. The supply should be maintained at 5 V ± 5% for specified operation. Minimize power supply ripple and noise at this pin by using proper decoupling. The typical performance graphs show the power supply rejection performance. This pin should be decoupled to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
4, 5	V1P, V1N	Analog Inputs for Channel 1. This channel is intended for use with a di/dt current transducer, i.e., a Rogowski coil or another current sensor such as a shunt or current transformer (CT). These inputs are fully differential voltage inputs with maximum differential input signal levels of ±0.5 V, ±0.25 V, and ±0.125 V, depending on the full-scale selection—see the Analog Inputs section. Channel 1 also has a PGA with gain selections of 1, 2, 4, 8, or 16. The maximum signal level at these pins with respect to AGND is ±0.5 V. Both inputs have internal ESD protection circuitry and can sustain an overvoltage of ±6 V without risk of permanent damage.
6, 7	V2N, V2P	Analog Inputs for Channel 2. This channel is intended for use with the voltage transducer. These inputs are fully differential voltage inputs with a maximum differential signal level of ±0.5 V. Channel 2 also has a PGA with gain selections of 1, 2, 4, 8, or 16. The maximum signal level at these pins with respect to AGND is ±0.5 V. Both inputs have internal ESD protection circuitry and can sustain an overvoltage of ±6 V without risk of permanent damage.
8	AGND	Analog Ground Reference. This pin provides the ground reference for the analog circuitry, i.e., ADCs and reference. This pin should be tied to the analog ground plane or to the quietest ground reference in the system. Use this quiet ground reference for all analog circuitry, such as antialiasing filters and current and voltage transducers. To minimize ground noise around the ADE7763, connect the quiet ground plane to the digital ground plane at only one point. It is acceptable to place the entire device on the analog ground plane.
9	$\text{REF}_{\text{IN/OUT}}$	Access to the On-Chip Voltage Reference. The on-chip reference has a nominal value of 2.4 V ± 8% and a typical temperature coefficient of 30 ppm/°C. An external reference source can also be connected at this pin. In either case, this pin should be decoupled to AGND with a 10 µF capacitor in parallel with a 100nF ceramic capacitor.
10	DGND	Digital Ground Reference. This pin provides the ground reference for the digital circuitry, i.e., multiplier, filters, and digital-to-frequency converter. Because the digital return currents in the ADE7763 are small, it is acceptable to connect this pin to the analog ground plane of the system. However, high bus capacitance on the DOUT pin could result in noisy digital current, which could affect performance.
11	CF	Calibration Frequency Logic Output. The CF logic output gives active power information. This output is intended to be used for operational and calibration purposes. The full-scale output frequency can be adjusted by writing to the CFDEN and CFNUM registers—see the Energy-to-Frequency Conversion section.
12	ZX	Voltage Waveform (Channel 2) Zero-Crossing Output. This output toggles logic high and logic low at the zero crossing of the differential signal on Channel 2—see the Zero-Crossing Detection section.
13	$\overline{\text{SAG}}$	This open-drain logic output goes active low when either no zero crossings are detected or a low voltage threshold (Channel 2) is crossed for a specified duration—see the Line Voltage Sag Detection section.

Pin No.	Mnemonic	Description
14	$\overline{\text{IRQ}}$	Interrupt Request Output. This is an active low, open-drain logic output. Maskable interrupts include active energy register rollover, active energy register at half level, and arrivals of new waveform samples—see the Interrupts section.
15	CLKIN	Master Clock for ADCs and Digital Signal Processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7763. The clock frequency for specified operation is 3.579545 MHz. Ceramic load capacitors between 22 pF and 33 pF should be used with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for load capacitance requirements.
16	CLKOUT	A crystal can be connected across this pin and CLKIN, as described for Pin 15, to provide a clock source for the ADE7763. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
17	$\overline{\text{CS}}$	Chip Select[1]. Part of the 4-wire SPI serial interface. This active low logic input allows the ADE7763 to share the serial bus with several other devices—see the Serial Interface section.
18	SCLK	Serial Clock Input for the Synchronous Serial Interface[1]. All serial data transfers are synchronized to this clock—see the Serial Interface section. The SCLK has a Schmitt-trigger input for use with a clock source that has a slow edge transition time, such as an opto-isolator output.
19	DOUT	Data Output for the Serial Interface. Data is shifted out at this pin upon the rising edge of SCLK. This logic output is normally in a high impedance state, unless it is driving data onto the serial data bus—see the Serial Interface section.
20	DIN	Data Input for the Serial Interface. Data is shifted in at this pin upon the falling edge of SCLK—see the Serial Interface section.

[1] It is recommended to drive the $\overline{\text{RESET}}$, SCLK, and $\overline{\text{CS}}$ pins with either a push-pull without an external series resistor or with an open-collector with a 10 kΩ pull-up Pull-down resistors are not recommended because under some conditions, they may interact with internal circuitry.

TYPICAL PERFORMANCE CHARACTERISTICS

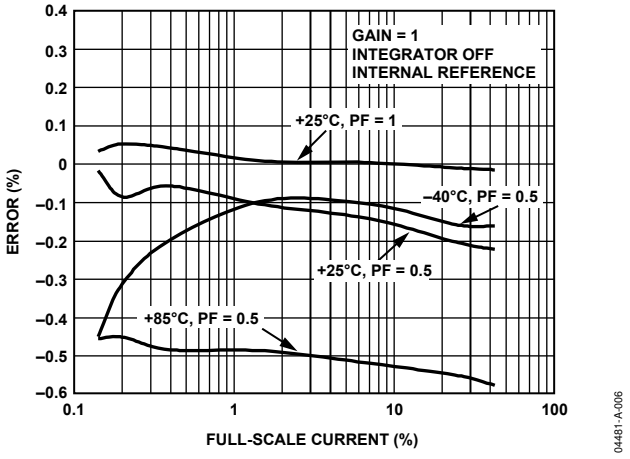

Figure 6. Active Energy Error as a Percentage of Reading (Gain = 1) over Power Factor with Internal Reference and Integrator Off

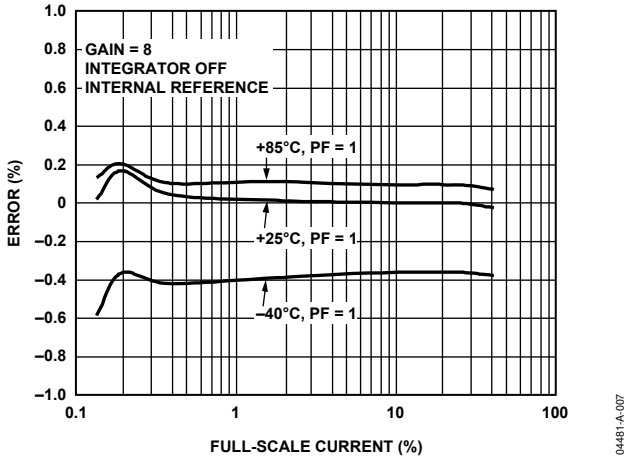

Figure 7. Active Energy as a Percentage of Reading (Gain = 8) over Temperature with Internal Reference and Integrator Off

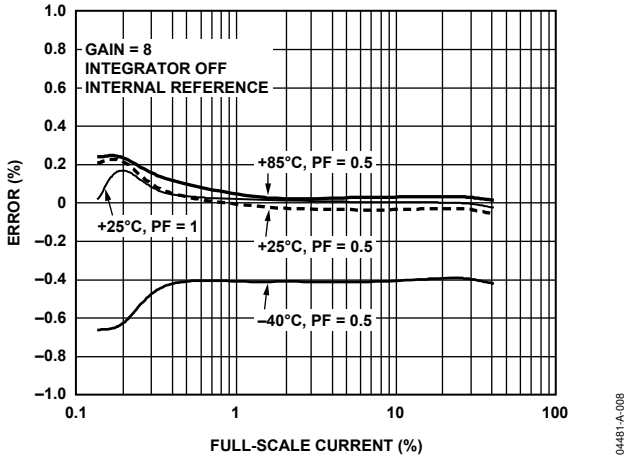

Figure 8. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator Off

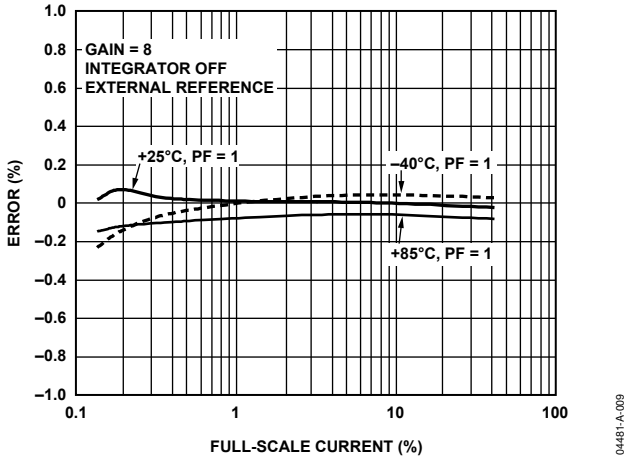

Figure 9. Active Energy Error as a Percentage of Reading (Gain = 8) over Temperature with External Reference and Integrator Off

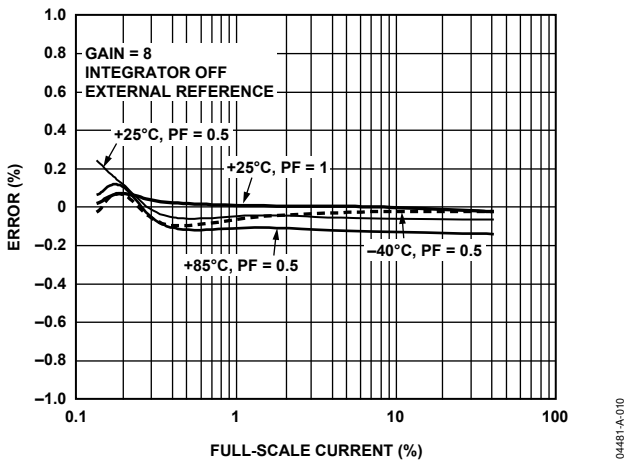

Figure 10. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with External Reference and Integrator Off

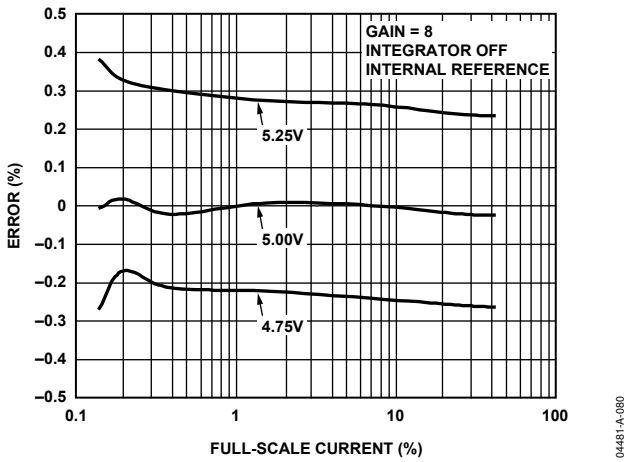

Figure 11. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Supply with Internal Reference and Integrator Off

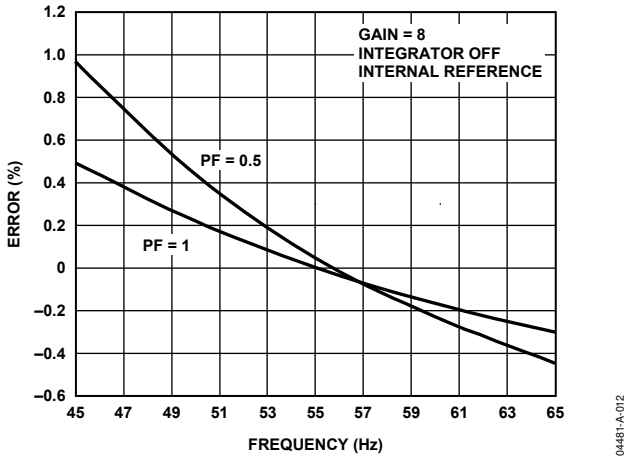

Figure 12. Active Energy Error as a Percentage of Reading (Gain = 8) over Frequency with Internal Reference and Integrator Off

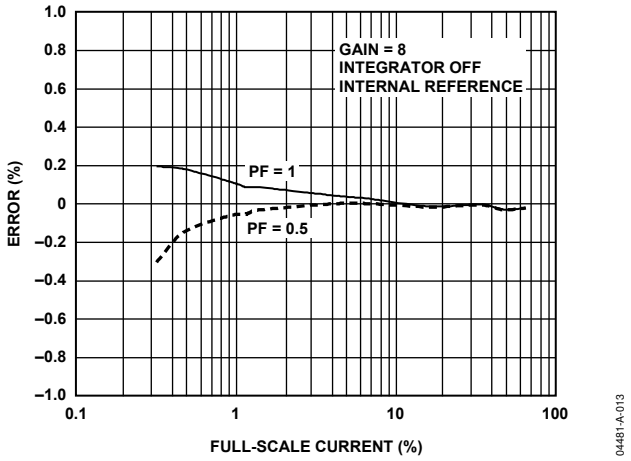

Figure 13. IRMS Error as a Percentage of Reading (Gain = 8) with Internal Reference and Integrator Off

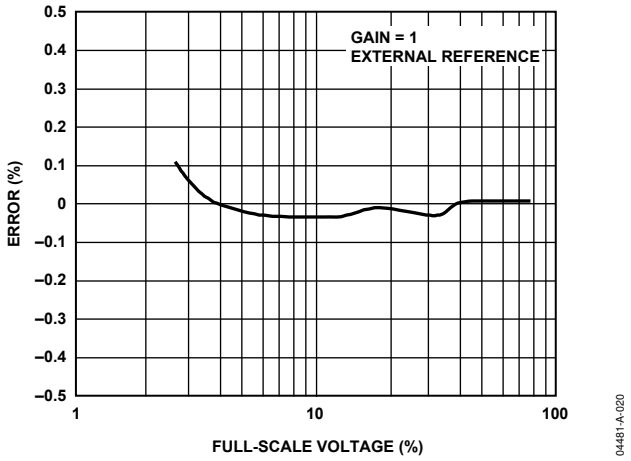

Figure 14. VRMS Error as a Percentage of Reading (Gain = 1) with External Reference

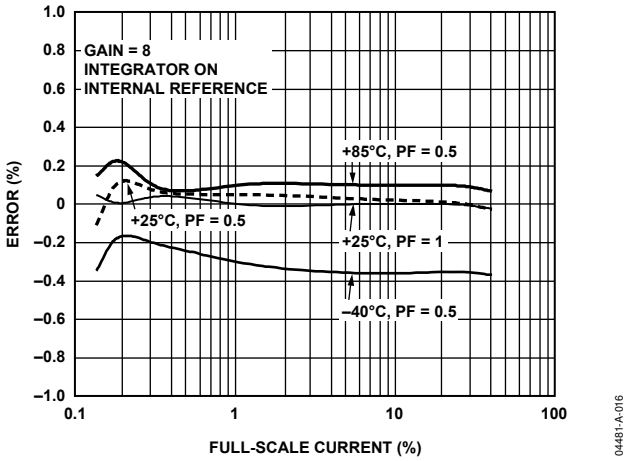

Figure 15. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Factor with Internal Reference and Integrator On

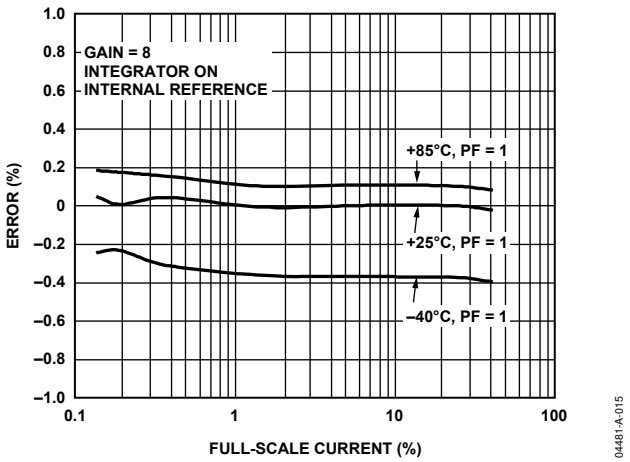

Figure 16. Active Energy Error as a Percentage of Reading (Gain = 8) over Temperature with External Reference and Integrator On

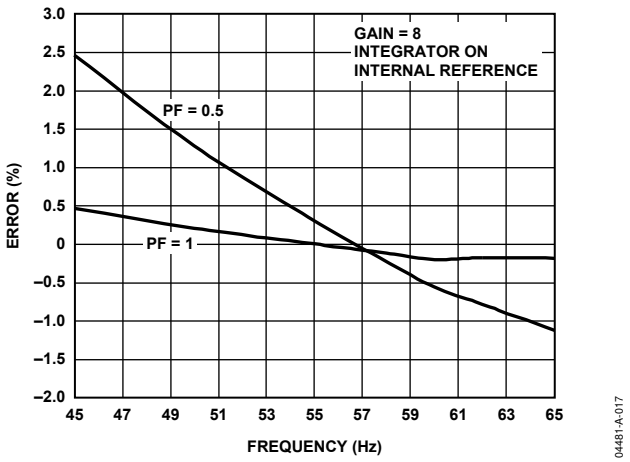

Figure 17. Active Energy Error as a Percentage of Reading (Gain = 8) over Frequency with Internal Reference and Integrator On

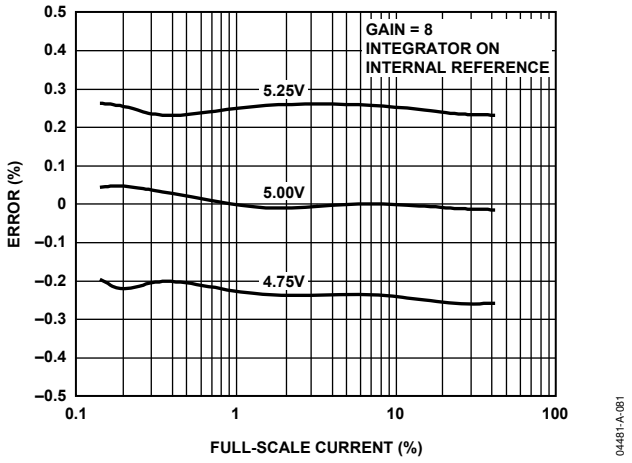

Figure 18. Active Energy Error as a Percentage of Reading (Gain = 8) over Power Supply with Internal Reference and Integrator On

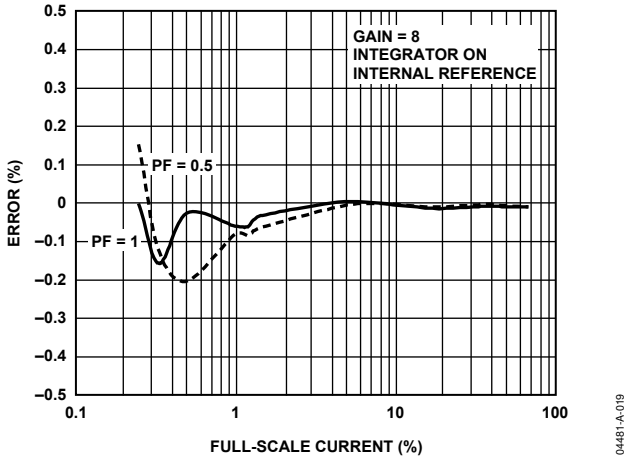

Figure 19. IRMS Error as a Percentage of Reading (Gain = 8) with Internal Reference and Integrator On

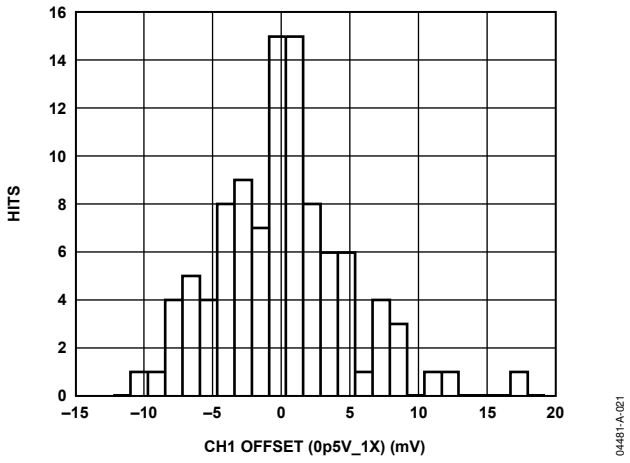

Figure 20. Channel 1 Offset (Gain = 1)

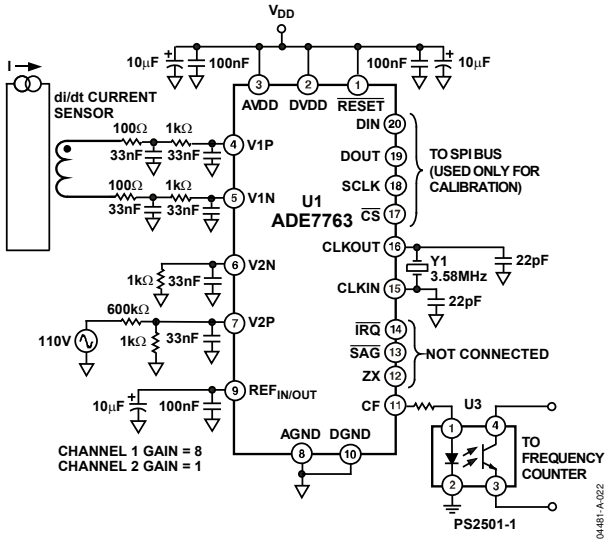

Figure 21. Test Circuit for Performance Curves with Integrator On

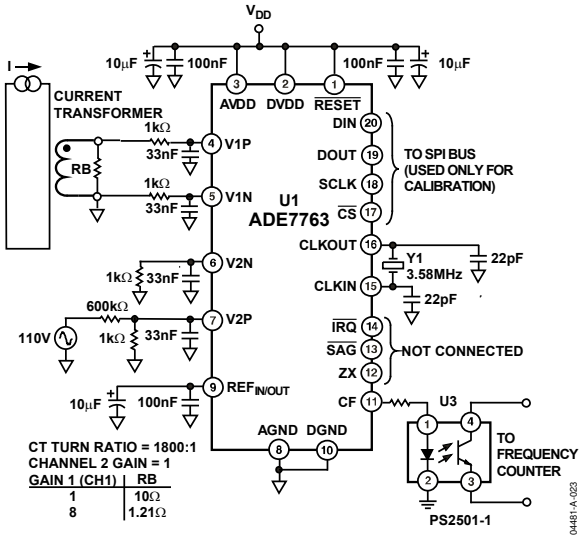

Figure 22. Test Circuit for Performance Curves with Integrator Off

THEORY OF OPERATION

ANALOG INPUTS

The ADE7763 has two fully differential voltage input channels. The maximum differential input voltage for input pairs V1P/V1N and V2P/V2N is ±0.5 V. In addition, the maximum signal level on analog inputs for V1P/V1N and V2P/V2N is ±0.5 V with respect to AGND.

Each analog input channel has a programmable gain amplifier (PGA) with possible gain selections of 1, 2, 4, 8, and 16. The gain selections are made by writing to the gain register—see Figure 24. Bits 0 to 2 select the gain for the PGA in Channel 1; the gain selection for the PGA in Channel 2 is made via Bits 5 to 7. Figure 23 shows how a gain selection for Channel 1 is made using the gain register.

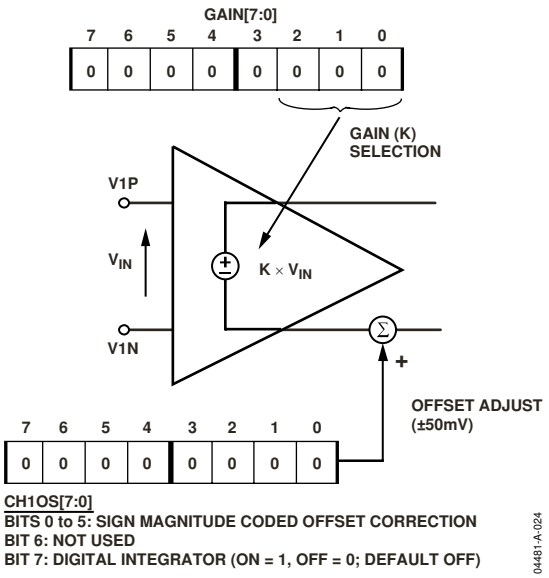

Figure 23. PGA in Channel 1

In addition to the PGA, Channel 1 also has a full-scale input range selection for the ADC. The ADC analog input range selection is also made using the gain register—see Figure 24. As previously mentioned, the maximum differential input voltage is 0.5 V. However, by using Bits 3 and 4 in the gain register, the maximum ADC input voltage can be set to 0.5 V, 0.25 V, or 0.125 V. This is achieved by adjusting the ADC reference—see the Reference Circuit section. Table 5 summarizes the maximum differential input signal level on Channel 1 for the various ADC range and gain selections.

Table 5. Maximum Input Signal Levels for Channel 1

Max Signal Channel 1	ADC Input Range Selection		
	0.5 V	0.25 V	0.125 V
0.5 V	Gain = 1	–	–
0.25 V	Gain = 2	Gain = 1	–
0.125 V	Gain = 4	Gain = 2	Gain = 1
0.0625 V	Gain = 8	Gain = 4	Gain = 2
0.0313 V	Gain = 16	Gain = 8	Gain = 4
0.0156 V	–	Gain = 16	Gain = 8
0.00781 V	–	–	Gain = 16

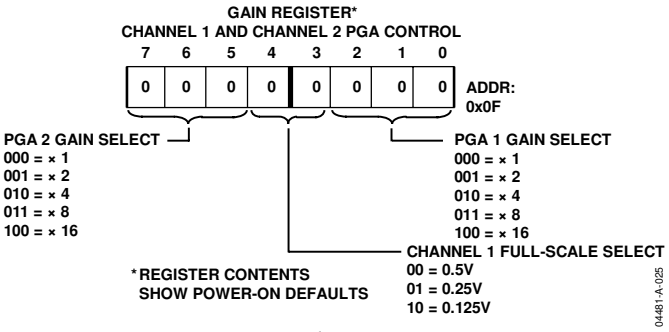

Figure 24. Analog Gain Register

It is also possible to adjust offset errors on Channel 1 and Channel 2 by writing to the offset correction registers (CH1OS and CH2OS, respectively). These registers allow channel offsets in the range ±20 mV to ±50 mV (depending on the gain setting) to be removed. Note that it is not necessary to perform an offset correction in an energy measurement application if HPF in Channel 1 is switched on. Figure 25 shows the effect of offsets on the real power calculation. As seen from Figure 25, an offset on Channel 1 and Channel 2 contributes a dc component after multiplication. Because this dc component is extracted by LPF2 to generate the active (real) power information, the offsets contribute an error to the active power calculation. This problem is easily avoided by enabling HPF in Channel 1. By removing the offset from at least one channel, no error component is generated at dc by the multiplication. Error terms at cos(ωt) are removed by LPF2 and by integration of the active power signal in the active energy register (AENERGY[23:0])—see the Energy Calculation section.

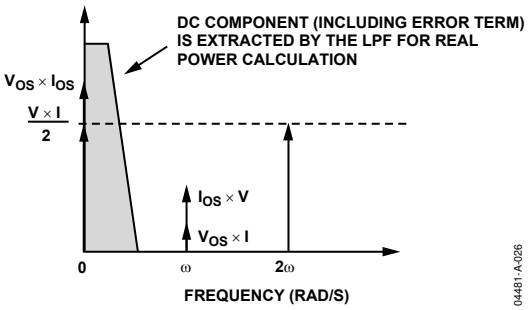

Figure 25. Effect of Channel Offsets on the Real Power Calculation

The contents of the offset correction registers are 6-bit, sign and magnitude coded. The weight of the LSB depends on the gain setting, i.e., 1, 2, 4, 8, or 16. Table 6 shows the correctable offset span for each of the gain settings and the LSB weight (mV) for the offset correction registers. The maximum value that can be written to the offset correction registers is ±31d—see Figure 26. Figure 26 shows the relationship between the offset correction register contents and the offset (mV) on the analog inputs for a gain of 1. To perform an offset adjustment, connect the analog inputs to AGND; there should be no signal on either Channel 1 or Channel 2. A read from Channel 1 or Channel 2 using the waveform register indicates the offset in the channel. This offset can be canceled by writing an equal and opposite offset value to the Channel 1 offset register, or an equal value to the Channel 2 offset register. The offset correction can be confirmed by performing another read. Note that when adjusting the offset of Channel 1, the digital integrator and the HPF should be disabled.

Table 6. Offset Correction Range—Channels 1 and 2

Gain	Correctable Span	LSB Size
1	±50 mV	1.61 mV/LSB
2	±37 mV	1.19 mV/LSB
4	±30 mV	0.97 mV/LSB
8	±26 mV	0.84 mV/LSB
16	±24 mV	0.77 mV/LSB

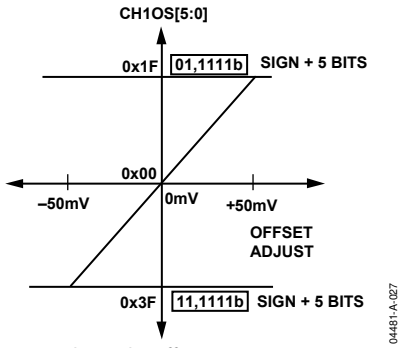

Figure 26. Channel 1 Offset Correction Range (Gain = 1)

The current and voltage rms offsets can be adjusted with the IRMSOS and VRMSOS registers—see the Channel 1 RMS Offset Compensation and Channel 2 RMS Offset Compensation sections.

di/dt CURRENT SENSOR AND DIGITAL INTEGRATOR

A di/dt sensor detects changes in magnetic field caused by ac current. Figure 27 shows the principle of a di/dt current sensor.

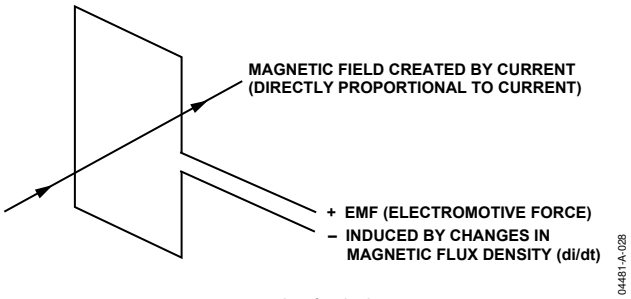

Figure 27. Principle of a di/dt Current Sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. Changes in the magnetic flux density passing through a conductor loop generate an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal that is proportional to the di/dt of the current. The voltage output from the di/dt current sensor is determined by the mutual inductance between the current-carrying conductor and the di/dt sensor. The current signal must be recovered from the di/dt signal before it can be used. An integrator is therefore necessary to restore the signal to its original form. The ADE7763 has a built-in digital integrator to recover the current signal from the di/dt sensor. The digital integrator on Channel 1 is switched off by default when the ADE7763 is powered up. Setting the MSB of CH1OS register turns on the integrator. Figure 28, Figure 29, Figure 30, and Figure 31 show the magnitude and phase response of the digital integrator.

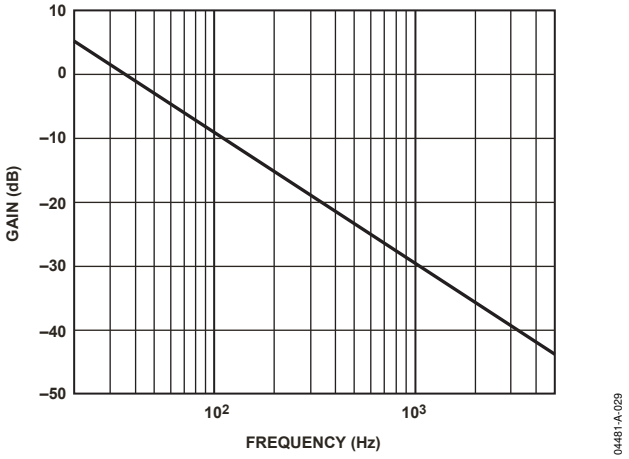

Figure 28. Combined Gain Response of the Digital Integrator and Phase Compensator

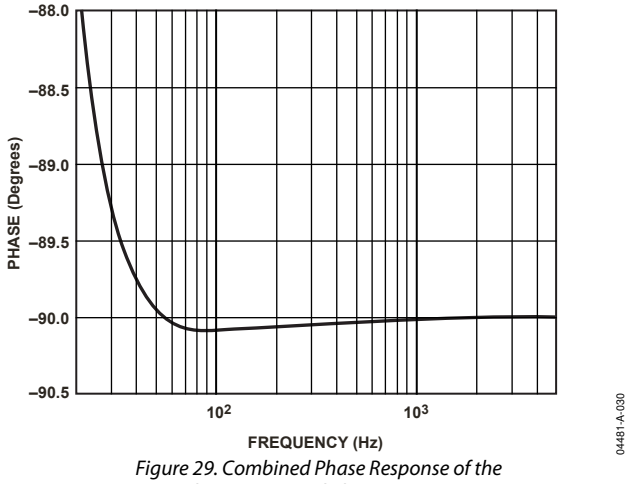

Figure 29. Combined Phase Response of the Digital Integrator and Phase Compensator

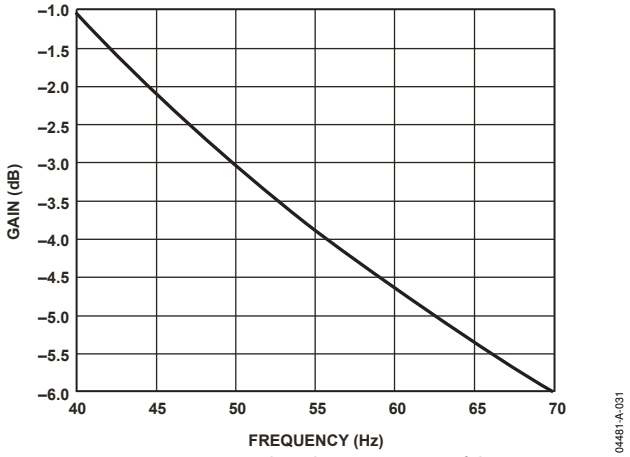

Figure 30. Combined Gain Response of the Digital Integrator and Phase Compensator (40 Hz to 70 Hz)

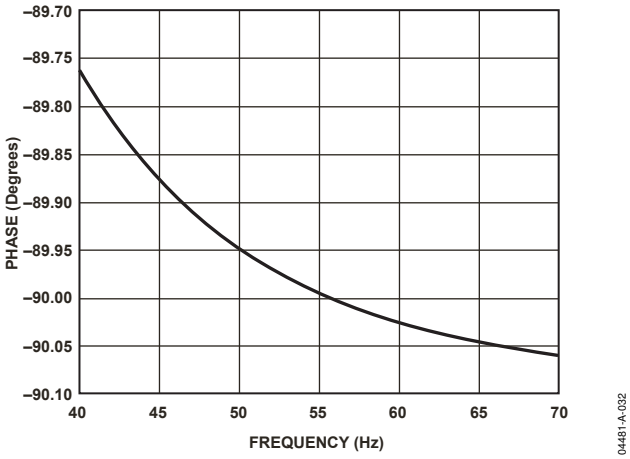

Figure 31. Combined Phase Response of the Digital Integrator and Phase Compensator (40 Hz to 70 Hz)

Note that the integrator has a –20 dB/dec attenuation and approximately a –90° phase shift. When combined with a di/dt sensor, the resulting magnitude and phase response should be a flat gain over the frequency band of interest. The di/dt sensor has a 20 dB/dec gain. It also generates significant high frequency noise, necessitating a more effective antialiasing filter to avoid noise due to aliasing—see the Antialias Filter section.

When the digital integrator is switched off, the ADE7763 can be used directly with a conventional current sensor such as a current transformer (CT) or with a low resistance current shunt.

ZERO-CROSSING DETECTION

The ADE7763 has a zero-crossing detection circuit on Channel 2. This zero crossing is used to produce an external zero-crossing signal (ZX), which is used in the calibration mode (see the Calibrating an Energy Meter section). This signal is also used to initiate a temperature measurement (see the Temperature Measurement section).

Figure 32 shows how the zero-crossing signal is generated from the output of LPF1.

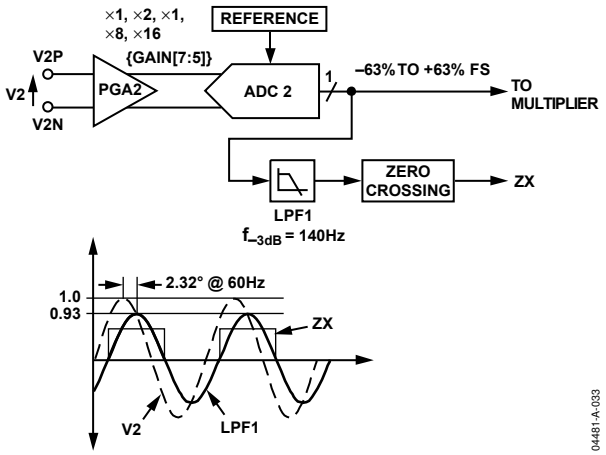

Figure 32. Zero-Crossing Detection on Channel 2

The ZX signal goes logic high upon a positive-going zero crossing and logic low upon a negative-going zero crossing on Channel 2. The ZX signal is generated from the output of LPF1. LPF1 has a single pole at 140 Hz (@ CLKIN = 3.579545 MHz). As a result, there is a phase lag between the analog input signal V2 and the output of LPF1. The phase response of this filter is shown in the Channel 2 Sampling section. The phase lag response of LPF1 results in a time delay of approximately 1.14 ms (@ 60 Hz) between the zero crossing on the analog inputs of Channel 2 and the rising or falling edge of ZX.

Zero-crossing detection also drives the ZX flag in the interrupt status register. The ZX flag is set to Logic 1 on the rising and falling edge of the voltage waveform. It remains high until the status register is read with reset. An active low in the $\overline{\text{IRQ}}$ output appears if the corresponding bit in the interrupt enable register is set to Logic 1.

The flag in the interrupt status register and the $\overline{\text{IRQ}}$ output are set to their default values when reset (RSTSTATUS) is read in the interrupt status register.

Zero-Crossing Timeout

Zero-crossing detection has an associated timeout register, ZXTOUT. This unsigned, 12-bit register is decremented (1 LSB)

every 128/CLKIN seconds. The register is reset to its user-programmed, full-scale value when a zero crossing on Channel 2 is detected. The default power-on value in this register is 0xFFF. If the internal register decrements to 0 before a zero crossing is detected and the DISSAG bit in the mode register is Logic 0, the $\overline{\text{SAG}}$ pin goes active low. The absence of a zero crossing is also indicated on the $\overline{\text{IRQ}}$ pin if the ZXTO enable bit in the interrupt enable register is set to Logic 1. Irrespective of the enable bit setting, the ZXTO flag in the interrupt status register is always set when the internal ZXTOUT register is decremented to 0—see the Interrupts section.

The ZXOUT register, Address 0x1D, can be written to and read from by the user—see the Serial Interface section. The resolution of the register is 128/CLKIN seconds per LSB; therefore, the maximum delay for an interrupt is 0.15 seconds ($128/CLKIN \times 2^{12}$).

Figure 33 shows the zero-crossing timeout detection when the line voltage stays at a fixed dc level for more than CLKIN/128 × ZXTOUT seconds.

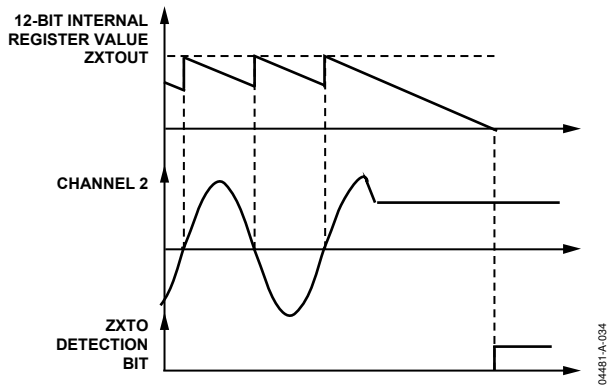

Figure 33. Zero-Crossing Timeout Detection

PERIOD MEASUREMENT

The ADE7763 provides the period measurement of the line. The PERIOD register is an unsigned, 16-bit register that is updated every period and always has an MSB of zero.

The formula for the period register is shown below:

$$PERIOD = \frac{CLKIN \times 16}{4 \times 32 \times f}$$

Where CLKIN is the crystal frequency (3.579545 MHz recommended), and f is the line frequency.

When CLKIN = 3.579545 MHz, the resolution of this register is 2.2 µs/LSB, which represents 0.013% when the line frequency is 60 Hz. When the line frequency is 60 Hz, the value of the period register is approximately 7457d. The length of the register enables the measurement of line frequencies as low as 13.9 Hz.

The period register is stable at ±1 LSB when the line is established and the measurement does not change. This filter is associated with a settling time of 1.8 seconds before the measurement is stable. See the Calibrating an Energy Meter section for more on the period register.

POWER SUPPLY MONITOR

The ADE7763 contains an on-chip power supply monitor. The analog supply (AVDD) is continuously monitored. If the supply is less than 4 V ± 5%, the ADE7763 will go into an inactive state and no energy will accumulate. This is useful to ensure correct device operation during power-up and power-down stages. In addition, built-in hysteresis and filtering help prevent false triggering due to noisy supplies.

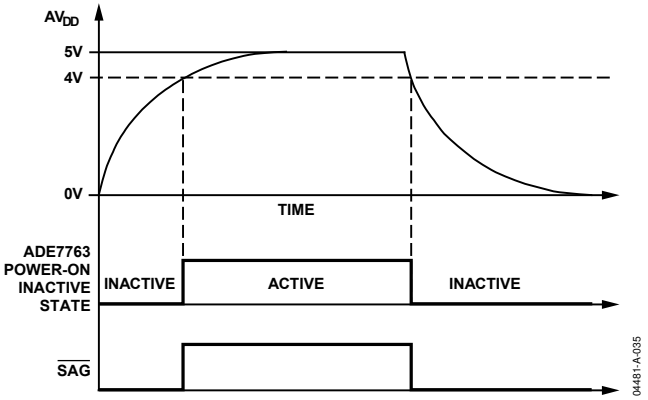

Figure 34. On-Chip Power Supply Monitor

As seen in Figure 34, the trigger level is nominally set at 4 V. The tolerance on this trigger level is about ±5%. The $\overline{\text{SAG}}$ pin can also be used as a power supply monitor input to the MCU. The $\overline{\text{SAG}}$ pin goes logic low when the ADE7763 is in its inactive state. The power supply and decoupling for the part should be such that the ripple at AVDD does not exceed 5 V ± 5%, as specified for normal operation.

LINE VOLTAGE SAG DETECTION

In addition to detecting the loss of the line voltage when there are no zero crossings on the voltage channel, the ADE7763 can also be programmed to detect when the absolute value of the line voltage drops below a peak value for a specified number of line cycles. This condition is illustrated in Figure 35.

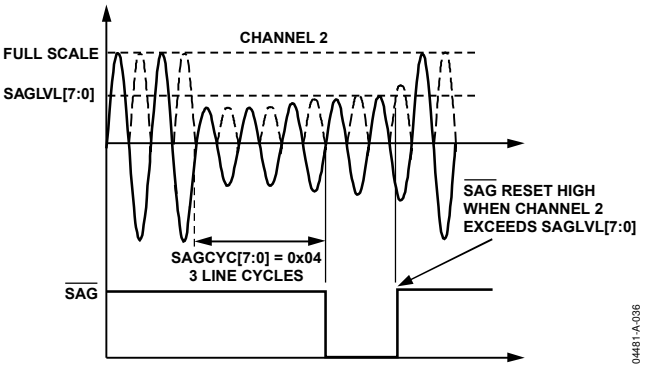

Figure 35. Sag Detection

In Figure 35 the line voltage falls below a threshold that has been set in the sag level register (SAGLVL[7:0]) for three line cycles. The quantities 0 and 1 are not valid for the SAGCYC register, and the contents represent one more than the desired number of full line cycles. For example, if the DISSAG bit in the mode register is Logic 0 and the sag cycle register (SAGCYC[7:0]) contains 0x04, the $\overline{\text{SAG}}$ pin goes active low at the end of the third line cycle for which the line voltage (Channel 2 signal) falls below the threshold. As is the case when zero crossings are no longer detected, the sag event is also recorded by setting the SAG flag in the interrupt status register. If the SAG enable bit is set to Logic 1, the $\overline{\text{IRQ}}$ logic output will go active low—see the Interrupts section. The $\overline{\text{SAG}}$ pin goes logic high again when the absolute value of the signal on Channel 2 exceeds the level set in the sag level register. This is shown in Figure 35 when the $\overline{\text{SAG}}$ pin goes high again during the fifth line cycle from the time when the signal on Channel 2 first dropped below the threshold level.

Sag Level Set

The contents of the sag level register (1 byte) are compared to the absolute value of the most significant byte output from LPF1 after it is shifted left by one bit. For example, the nominal maximum code from LPF1 with a full-scale signal on Channel 2 is 0x2518—see the Channel 2 Sampling section. Shifting one bit left gives 0x4A30. Therefore, writing 0x4A to the SAG level register puts the sag detection level at full scale. Writing 0x00 or 0x01 puts the sag detection level at 0. The SAG level register is compared to the most significant byte of a waveform sample after the shift left, and detection occurs when the contents of the sag level register are greater.

PEAK DETECTION

The ADE7763 can also be programmed to detect when the absolute value of the voltage or current channel exceeds a specified peak value. Figure 36 illustrates the behavior of the peak detection for the voltage channel.

Both Channel 1 and Channel 2 are monitored at the same time.

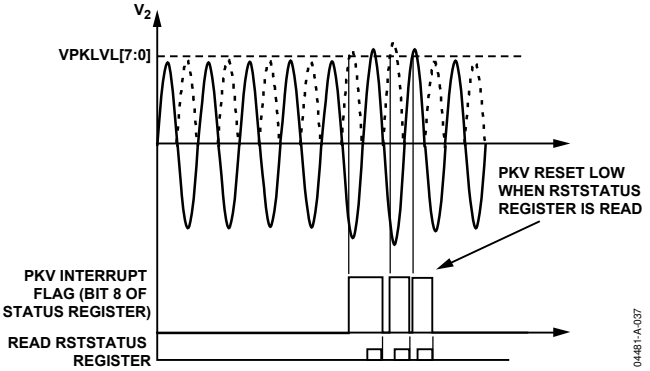

Figure 36. Peak Level Detection

Figure 36 shows a line voltage exceeding a threshold that has been set in the voltage peak register (VPKLVL[7:0]). The voltage peak event is recorded by setting the PKV flag in the interrupt status register. If the PKV enable bit is set to Logic 1 in the interrupt mask register, the $\overline{\text{IRQ}}$ logic output will go active low. Similarly, the current peak event is recorded by setting the PKI flag in the interrupt status register—see the Interrupts section.

Peak Level Set

The contents of the VPKLVL and IPKLVL registers are compared to the absolute value of Channel 1 and Channel 2, respectively, after they are multiplied by 2. For example, the nominal maximum code from the Channel 1 ADC with a full-scale signal is 0x2851EC—see the Channel 1 Sampling section. Multiplying by 2 gives 0x50A3D8. Therefore, writing 0x50 to the IPKLVL register, for example, puts the Channel 1 peak detection level at full scale and sets the current peak detection to its least sensitive value. Writing 0x00 puts the Channel 1 detection level at 0. Peak level detection is done by comparing the contents of the IPKLVL register to the incoming Channel 1 sample. The $\overline{\text{IRQ}}$ pin indicates that the peak level is exceeded if the PKI or PKV bits are set in the interrupt enable register (IRQEN [15:0]) at Address 0x0A.

Peak Level Record

The ADE7763 records the maximum absolute value reached by Channel 1 and Channel 2 in two different registers—IPEAK and VPEAK, respectively. VPEAK and IPEAK are 24-bit, unsigned registers. These registers are updated at a rate of CLKIN/4 regardless of the waveform sampling rate. The contents of the VPEAK register correspond to two times the maximum absolute value observed on the Channel 2 input. The contents of IPEAK represent the maximum absolute value observed on the Channel 1

input. Reading the RSTVPEAK and RSTIPEAK registers clears their respective contents after the read operation.

INTERRUPTS

Interrupts are managed through the interrupt status register (STATUS[15:0]) and the interrupt enable register (IRQEN[15:0]). When an interrupt event occurs, the corresponding flag in the status register is set to Logic 1—see the Interrupt Status Register section. If the enable bit for this interrupt in the interrupt enable register is Logic 1, the $\overline{\text{IRQ}}$ logic output will go active low. The flag bits in the status register are set irrespective of the state of the enable bits.

To determine the source of the interrupt, the system master (MCU) should perform a read from the status register with reset (RSTSTATUS[15:0]). This is achieved by carrying out a read from Address 0Ch. The $\overline{\text{IRQ}}$ output goes logic high after the completion of the interrupt status register read command—see the Interrupt Timing section. When carrying out a read with reset, the ADE7763 is designed to ensure that no interrupt events are missed. If an interrupt event occurs as the status register is being read, the event will not be lost and the $\overline{\text{IRQ}}$ logic output will be guaranteed to go high for the duration of the interrupt status register data transfer before going logic low again to indicate the pending interrupt. See the next section for a more detailed description.

Using Interrupts with an MCU

Figure 38 shows a timing diagram with a suggested implementation of ADE7763 interrupt management using an MCU. At time t_1, the $\overline{\text{IRQ}}$ line goes active low, indicating that one or more interrupt events have occurred. Tie the $\overline{\text{IRQ}}$ logic output to a negative edge-triggered external interrupt on the MCU. Configure the MCU to start executing its interrupt service routine (ISR) when a negative edge is detected on the $\overline{\text{IRQ}}$ line. After entering the ISR, disable all interrupts by using the global interrupt enable bit. At this point, the MCU $\overline{\text{IRQ}}$ external interrupt flag can be cleared to capture interrupt events that occur during the current ISR. When the MCU interrupt flag is cleared, a read from the status register with reset is carried out. This causes the $\overline{\text{IRQ}}$ line to reset to logic high (t_2)—see the Interrupt Timing section. The status register contents are used to determine the source of the interrupt(s) and, therefore, the appropriate action to be taken. If a subsequent interrupt event occurs during the ISR, that event will be recorded by the MCU external interrupt flag being set again (t_3). Upon the completion of the ISR, the global interrupt mask is cleared (same instruction cycle) and the external interrupt flag causes the MCU to jump to its ISR again. This ensures that the MCU does not miss any external interrupts.

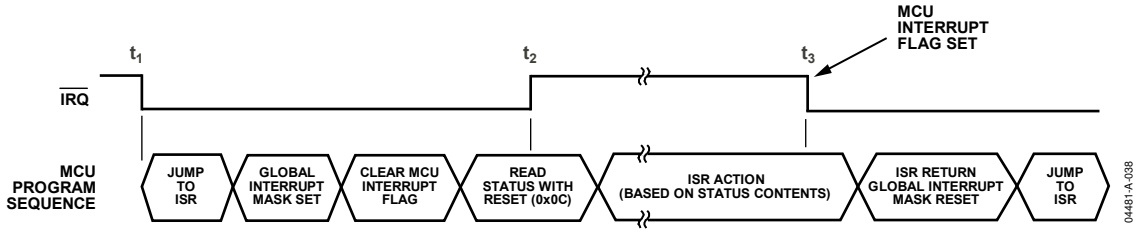

Figure 37. Interrupt Management

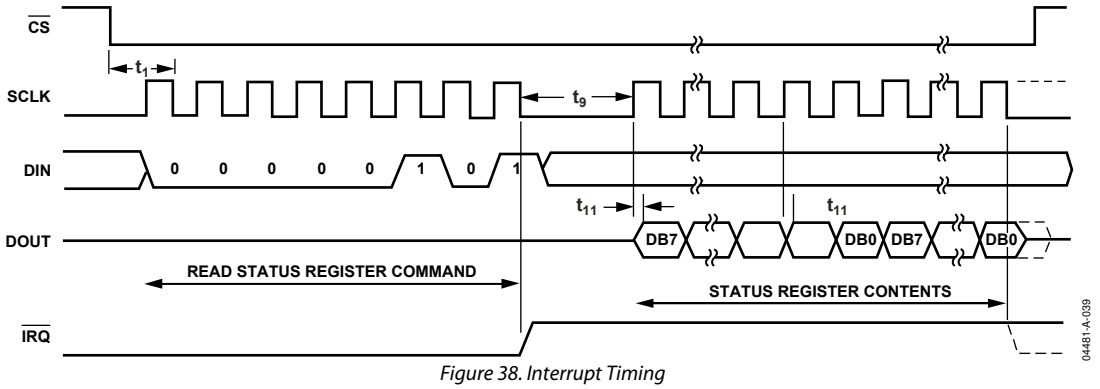

Figure 38. Interrupt Timing

Interrupt Timing

Review the Serial Interface section before reading this section. As previously described, when the $\overline{\text{IRQ}}$ output goes low, the MCU ISR will read the interrupt status register to determine the source of the interrupt. When reading the status register contents, the $\overline{\text{IRQ}}$ output is set high upon the last falling edge of SCLK of the first byte transfer (read interrupt status register command). The $\overline{\text{IRQ}}$ output is held high until the last bit of the next 15-bit transfer is shifted out (interrupt status register contents)—see Figure 37. If an interrupt is pending at this time, the $\overline{\text{IRQ}}$ output will go low again. If no interrupt is pending, the $\overline{\text{IRQ}}$ output will stay high.

TEMPERATURE MEASUREMENT

There is an on-chip temperature sensor. A temperature measurement can be made by setting Bit 5 in the mode register. When Bit 5 is set logic high in the mode register, the ADE7763 initiates a temperature measurement of the next zero crossing. When the zero crossing on Channel 2 is detected, the voltage output from the temperature sensing circuit is connected to ADC1 (Channel 1) for digitizing. The resulting code is processed and placed in the temperature register (TEMP[7:0]) approximately 26 μs later (24 CLKIN/4 cycles). If enabled in the interrupt enable register (Bit 5), the $\overline{\text{IRQ}}$ output will go active low when the temperature conversion is finished.

The contents of the temperature register are signed (twos complement) with a resolution of approximately 1.5 LSB/°C. The temperature register produces a code of 0x00 when the ambient temperature is approximately −25°C. The temperature measurement is uncalibrated in the ADE7763 and might have an offset tolerance as high as ±25°C.

ANALOG-TO-DIGITAL CONVERSION

The analog-to-digital conversion is carried out using two second-order Σ-Δ ADCs. For simplicity, the block diagram in Figure 39 shows a first-order Σ-Δ ADC. The converter comprises two parts: the Σ-Δ modulator and the digital low-pass filter.

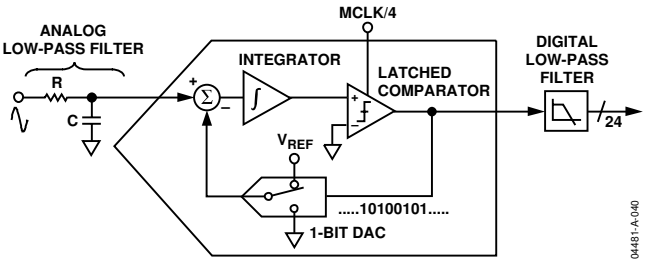

Figure 39. First-Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7763, the sampling clock is equal to CLKIN/4. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and therefore the bit stream) will approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged can a meaningful result be obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling. Oversampling means that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, the sampling rate in the ADE7763 is CLKIN/4 (894 kHz) and the band of interest is 40 Hz to 2 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest decreases—see Figure 40. However, oversampling alone is not efficient enough to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling ratio of 4 is required just to increase the SNR by 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at higher frequencies. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass-type response for the quantization noise. The result is that most of the noise is at higher frequencies, where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 40.

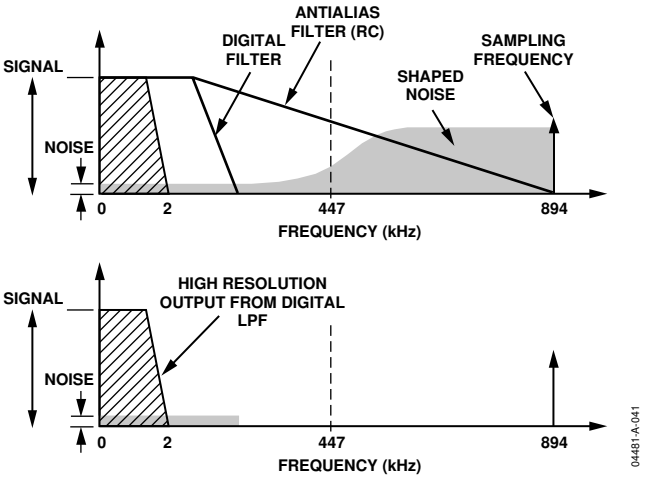

Figure 40. Noise Reduction due to Oversampling and Noise Shaping in the Analog Modulator

Antialias Filter

Figure 39 also shows an analog low-pass filter (RC) on the input to the modulator. This filter prevents aliasing, which is an artifact of all sampled systems. Aliasing means that frequency components in the input signal to the ADC that are higher than half the sampling rate of the ADC appear in the sampled signal at a frequency below half the sampling rate. Figure 41 illustrates the effect. Frequency components (shown as arrows) above half the sampling frequency (also known as the Nyquist frequency, i.e., 447 kHz) are imaged or folded back down below 447 kHz. This happens with all ADCs, regardless of the architecture. In the example shown, only frequencies near the sampling frequency, i.e., 894 kHz, move into the band of interest for metering, i.e., 40 Hz to 2 kHz. This allows the use of a very simple LPF (low-pass filter) to attenuate high frequency (near 900 kHz) noise, and it prevents distortion in the band of interest. For conventional current sensors, a simple RC filter (single-pole LPF) with a corner frequency of 10 kHz produces an attenuation of approximately 40 dB at 894 kHz—see Figure 41. The 20 dB per decade attenuation is usually sufficient to eliminate the effects of aliasing for conventional current sensors; however, for a di/dt sensor such as a Rogowski coil, the sensor has a 20 dB per decade gain. This neutralizes the –20 dB per decade attenuation produced by one simple LPF. Therefore, when using a di/dt sensor, care should be taken to offset the 20 dB per decade gain. One simple approach is to cascade two RC filters to produce the –40 dB per decade attenuation.

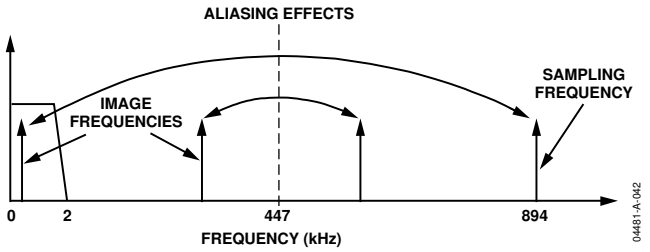

Figure 41. ADC and Signal Processing in Channel 1 Outline Dimensions

ADC Transfer Function

The following expression relates the output of the LPF in the Σ-Δ ADC to the analog input signal level. Both ADCs in the ADE7763 are designed to produce the same output code for the same input signal level.

$$Code\ (ADC) = 3.0492 \times \frac{V_{IN}}{V_{OUT}} \times 262{,}144 \quad (1)$$

Therefore, with a full-scale signal on the input of 0.5 V and an internal reference of 2.42 V, the ADC output code is nominally 165,151, or 0x2851F. The maximum code from the ADC is ±262,144; this is equivalent to an input signal level of ±0.794 V. However, for specified performance, do not exceed the 0.5 V full-scale input signal level.

Reference Circuit

Figure 42 shows a simplified version of the reference output circuitry. The nominal reference voltage at the $REF_{IN/OUT}$ pin is 2.42 V. This is the reference voltage used for the ADCs. However, Channel 1 has three input range options that are selected by dividing down the reference value used for the ADC in Channel 1. The reference value used for Channel 1 is divided down to ½ and ¼ of the nominal value by using an internal resistor divider, as shown in Figure 42.

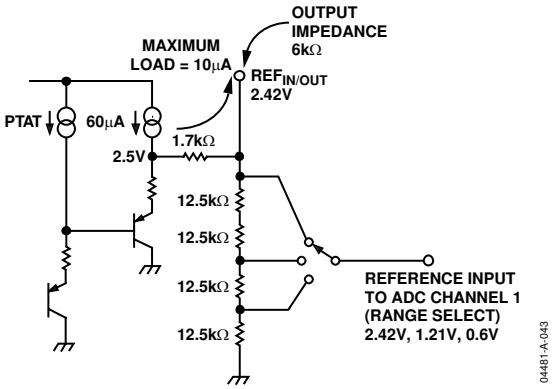

Figure 42. Reference Circuit Output

The $REF_{IN/OUT}$ pin can be overdriven by an external source such as a 2.5 V reference. Note that the nominal reference value supplied to the ADCs is now 2.5 V, not 2.42 V, which increases the nominal analog input signal range by 2.5/2.42 × 100% = 3% or from 0.5 V to 0.5165 V.

The voltage of the ADE7763 reference drifts slightly with changes in temperature—see Table 1 for the temperature coefficient specification (in ppm/°C). The value of the temperature drift varies from part to part. Because the reference is used for the ADCs in both Channels 1 and 2, any x% drift in the reference results in 2x% deviation in the meter accuracy. The reference drift that results from a temperature change is usually very small, typically much smaller than the drift of other components on a meter. However, if guaranteed temperature performance is needed, use an external voltage reference. Alternatively, the meter can be calibrated at multiple temperatures. Real-time compensation can be achieved easily by using the on-chip temperature sensor.

CHANNEL 1 ADC

Figure 43 shows the ADC and signal processing chain for Channel 1. In waveform sampling mode, the ADC outputs a signed, twos complement, 24-bit data-word at a maximum of 27.9 kSPS (CLKIN/128). With the specified full-scale analog input signal of 0.5 V (or 0.25 V or 0.125 V—see the Analog Inputs section), the ADC produces an output code that is approximately between 0x28 51EC (+2,642,412d) and 0xD7 AE14 (–2,642,412d)—see Figure 43.

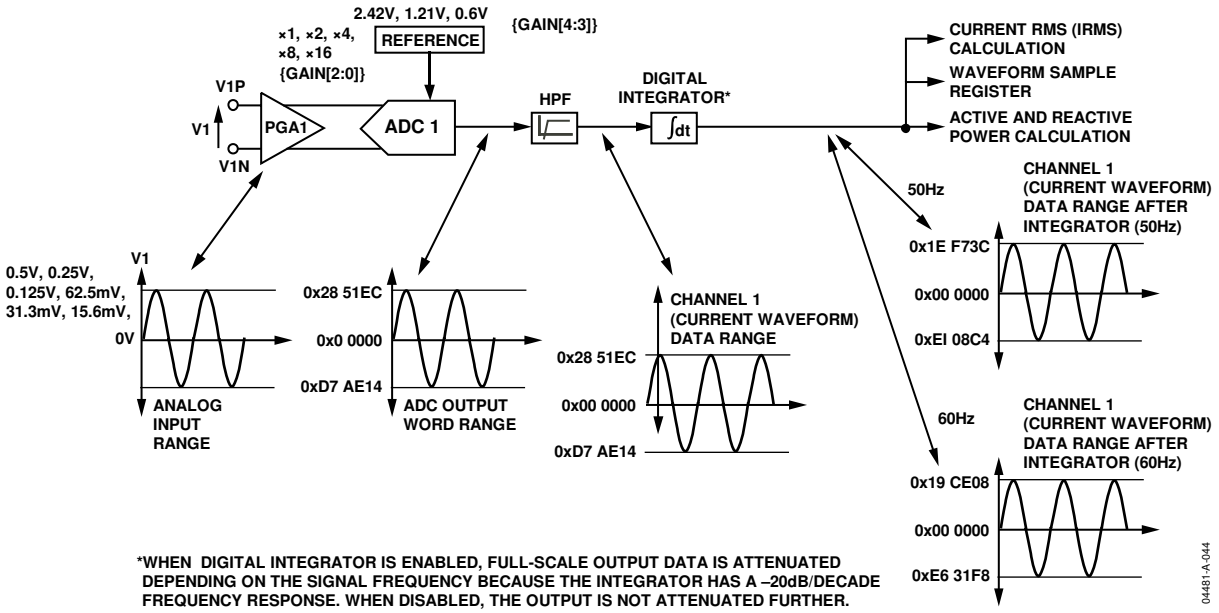

Figure 43. ADC and Signal Processing in Channel 1

Channel 1 Sampling

The waveform samples may be routed to the waveform register (MODE[14:13] = 1, 0) for the system master (MCU) to read. To enable waveform sampling mode, set the WSMP bit (Bit 3) in the interrupt enable register to Logic 1. The active and apparent power as well as the energy calculation remain uninterrupted during waveform sampling.

In waveform sampling mode, choose one of four output sample rates using Bits 11 and 12 of the mode register (WAVSEL 1, 0). The output sample rate can be 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS—see the Mode Register (0X09) section. The interrupt request output, $\overline{\text{IRQ}}$, signals a new sample availability by going active low. The timing is shown in Figure 44. The 24-bit waveform samples are transferred from the ADE7763 one byte (eight bits) at a time, with the most significant byte shifted out first. The 24-bit data-word is right justified—see the Serial Interface section. The Channel 1 waveform samples have a settling time of approximately 150 μs. The interrupt request output $\overline{\text{IRQ}}$ stays low until the interrupt routine reads the reset status register—see the Interrupts section.

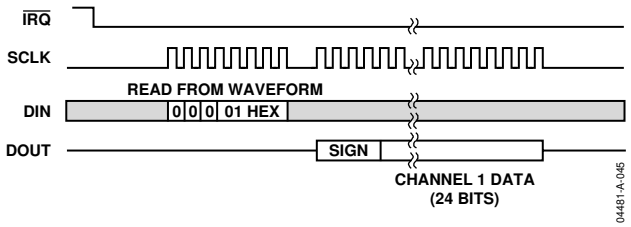

Figure 44. Waveform Sampling Channel 1

Channel 1 RMS Calculation

The root mean square (rms) value of a continuous signal I(t) is defined as

$$IRMS = \sqrt{\frac{1}{T} \times \int_0^T I^2(t)\,dt} \quad (2)$$

For time sampling signals, the rms calculation involves squaring the signal, taking the average, and obtaining the square root:

$$IRMS = \sqrt{\frac{1}{N} \times \sum_{i=1}^{N} I^2(i)} \quad (3)$$

Figure 45 shows the detail of the signal processing chain for the rms calculation on Channel 1. The Channel 1 rms value is processed from the samples used in the Channel 1 waveform sampling mode. The Channel 1 rms value is stored in an unsigned, 24-bit register (IRMS). One LSB of the Channel 1 rms register is equivalent to 1 LSB of a Channel 1 waveform sample. The update rate of the Channel 1 rms measurement is CLKIN/4. The channel 1 rms measurement has a settling time of approximately 876 ms with the integrator off and 1340 ms with the integrator on.

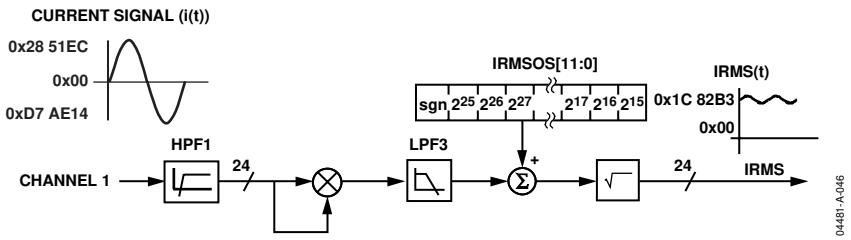

Figure 45. Channel 1 RMS Signal Processing

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately ±2,642,412d—see the Channel 1 ADC section. The equivalent rms value of a full-scale ac signal is 1,868,467d (0x1C82B3). The current rms measurement provided in the ADE7763 is accurate to within 0.5% for signal input between full scale and full scale/100. Converting the register value to its equivalent in amps must be done externally in the microprocessor using an amps/LSB constant. To minimize noise, synchronize the reading of the rms register with the zero crossing of the voltage input and take the average of a number of readings.

Channel 1 RMS Offset Compensation

The ADE7763 incorporates a Channel 1 rms offset compensation register (IRMSOS). This is a 12-bit, signed register that can be used to remove offset in the Channel 1 rms calculation. An offset might exist in the rms calculation due to input noises that are integrated in the dc component of $V^2(t)$. The offset calibration eliminates the influence of input noises from the rms measurement.

One LSB of the Channel 1 rms offset is equivalent to 32,768 LSB of the square of the Channel 1 rms register. Assuming that the maximum value from the Channel 1 rms calculation is 1,868,467d with full-scale ac inputs, then 1 LSB of the Channel 1 rms offset represents 0.46% of the measurement error at –60 dB down of full scale.

$$IRMS = \sqrt{IRMS_0^2 + IRMSOS \times 32768} \quad (4)$$

where $IRMS_0$ is the rms measurement without offset correction.

To measure the offset of the rms measurement, two data points are needed from nonzero input values, for example, the base current, I_b, and $I_{max}/100$. The offset can be calculated from these measurements. Note that for correct operation, only positive values should be written to the IRMSOS register.

CHANNEL 2 ADC

Channel 2 Sampling

To enable waveform sampling mode, set the WSMP bit (Bit 3) in the interrupt enable register to Logic 1. In Channel 2 waveform sampling mode (MODE[14:13] = 1, 1 and WSMP = 1), the ADC output code scaling for Channel 2 is not the same as it is for Channel 1. The Channel 2 waveform sample is a 16-bit word and sign extended to 24 bits. The Channel 2 waveform samples have a settling time of approximately 1.23 ms.For normal operation, the differential voltage signal between V2P and V2N should not exceed 0.5 V. With maximum voltage input (±0.5 V at PGA gain of 1), the output from the ADC swings between 0x2852 and 0xD7AE (±10,322d). However, before being passed to the waveform register, the ADC output is passed through a single-pole, low-pass filter with a cutoff frequency of 140 Hz. The plots in Figure 46 show the magnitude and phase response of this filter.

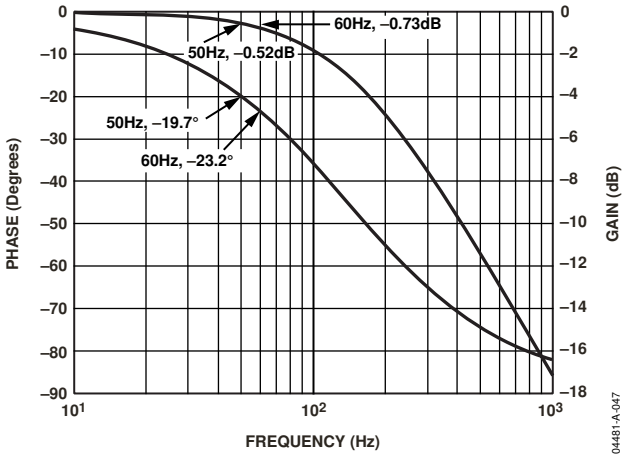

Figure 46. Magnitude and Phase Response of LPF1

The LPF1 has the effect of attenuating the signal. For example, if the line frequency is 60 Hz, the signal at the output of LPF1 will be attenuated by about 8%.

$$|H(f)| = \frac{1}{\sqrt{1+\left(\frac{60\text{ Hz}}{140\text{ Hz}}\right)^2}} = 0.919 = -0.73\text{ db} \quad (5)$$

Note LPF1 does not affect the active power calculation. The signal processing chain in Channel 2 is illustrated in Figure 47.

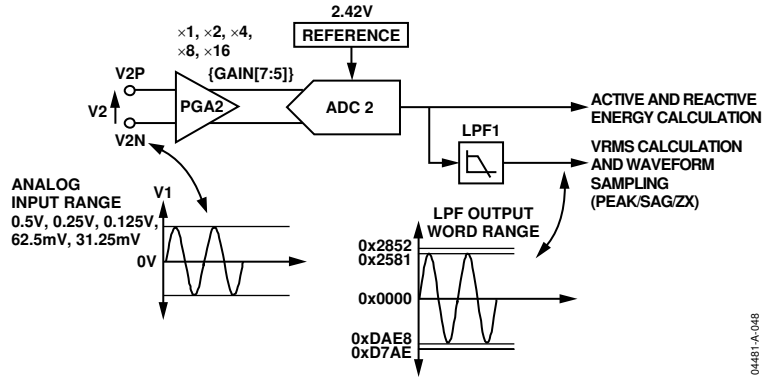

Figure 47. ADC and Signal Processing in Channel 2

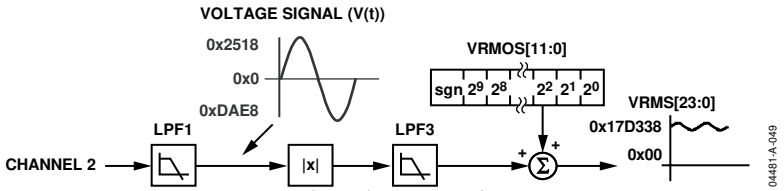

Figure 48. Channel 2 RMS Signal Processing

Channel 2 has only one analog input range (0.5 V differential). Like Channel 1, Channel 2 has a PGA with gain selections of 1, 2, 4, 8, and 16. For energy measurement, the output of the ADC is passed directly to the multiplier and is not filtered. An HPF is not required to remove any dc offset; it is only required that the offset is removed from one channel to eliminate errors caused by offsets in the power calculation. In waveform sampling mode, one of four output sample rates can be chosen by using Bits 11 and 12 of the mode register. The available output sample rates are 27.9 kSPS, 14 kSPS, 7 kSPS, or 3.5 kSPS—see the Mode Register (0X09) section. The interrupt request output $\overline{\text{IRQ}}$ indicates that a sample is available by going active low. The timing is the same as that for Channel 1, as shown in Figure 44.

Channel 2 RMS Calculation

Figure 48 shows the details of the signal processing chain for the rms estimation on Channel 2. This Channel 2 rms estimation is done in the ADE7763 using the mean absolute value calculation, as shown in Figure 48.The Channel 2 rms value is processed from the samples used in the Channel 2 waveform sampling mode. The rms value is slightly attenuated due to LPF1. The Channel 2 rms value is stored in the unsigned, 24-bit VRMS register. The update rate of the Channel 2 rms measurement is CLKIN/4. The Channel 2 rms measurement has a settling time of approximately 670 ms.

With the specified full-scale ac analog input signal of 0.5 V, the output from LPF1 swings between 0x2518 and 0xDAE8 at 60 Hz—see the Channel 2 ADC section. The equivalent rms value of this full-scale ac signal is approximately 1,561,400 (0x17 D338) in the VRMS register. The voltage rms measurement provided in the ADE7763 is accurate to within ±0.5% for signal input between full scale and full scale/20. The conversion from the register value to volts must be done externally in the microprocessor using a volts/LSB constant. Because the low-pass filter used for calculating the rms value is imperfect, there is some ripple noise from 2ω term present in the rms measurement. To minimize the effect of noise in the reading, synchronize the rms reading with the zero crossings of the voltage input.

Channel 2 RMS Offset Compensation

The ADE7763 incorporates a Channel 2 rms offset compensation register (VRMSOS). This is a 12-bit, signed register that can be used to remove offset in the Channel 2 rms calculation. An offset could exist in the rms calculation due to input noises and dc offset in the input samples. One LSB of the Channel 2 rms offset is equivalent to 1 LSB of the rms register. Assuming that the maximum value of the Channel 2 rms calculation is 1,561,400d with full-scale ac inputs, then 1 LSB of the Channel 2 rms offset represents 0.064% of measurement error at −60 dB down of full scale.

$$VRMS = VRMS_0 + VRMSOS \quad (6)$$

where $VRMS_0$ is the rms measurement without offset correction.

The voltage rms offset compensation should be done by testing the rms results at two nonzero input levels. One measurement can be done close to full scale and the other at approximately full scale/10. The voltage offset compensation can be derived from these measurements. If the voltage rms offset register does not have enough range, the CH2OS register can also be used.

PHASE COMPENSATION

When the HPF is disabled, the phase error between Channel 1 and Channel 2 is 0 from dc to 3.5 kHz. When HPF is enabled, Channel 1 has the phase response illustrated in Figure 50 and