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Six Current Channels, One Voltage Channel Energy Metering IC

Data Sheet

ADE7816

FEATURES

Measures active and reactive energy, sampled waveforms, and current and voltage rms
6 current input channels and 1 voltage channel
<0.1% error in active and reactive energy over a dynamic range of 1000:1
Supports current transformer and Rogowski coil sensors
Provides instantaneous current and voltage readings
Angle measurements on all 6 channels
2 kHz bandwidth operation
Reference: 1.2 V (drift 10 ppm/°C typical) with external overdrive capability
Flexible I²C, SPI, and HSDC serial interfaces

GENERAL DESCRIPTION

The ADE7816 is a highly accurate, multichannel metering device that is capable of measuring one voltage channel and up to six current channels. It measures line voltage and current and calculates active and reactive energy, as well as instantaneous rms voltage and current. The device incorporates seven sigma-delta (Σ-Δ) ADCs with a high accuracy energy measurement core. The six current input channels allow multiple loads to be measured simultaneously. The voltage channel and the six current channels each have a complete signal path allowing for a full range of measurements. Each input channel supports a flexible gain stage and is suitable for use with current transformers (CTs). Six on-chip digital integrators facilitate the use of the Rogowski coil sensors.

The ADE7816 provides access to on-chip meter registers via either the SPI or I²C interface. A dedicated high speed interface, the high speed data capture (HSDC) port, can be used in conjunction with I²C to provide access to real-time ADC output information. A full range of power quality information, such as overcurrent, overvoltage, peak, and sag detection, is accessible via the two external interrupt pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$.

The ADE7816 energy metering IC operates from a 3.3 V supply voltage and is available in a 40-lead LFCSP that is Pb free and RoHS compliant.

FUNCTIONAL BLOCK DIAGRAM

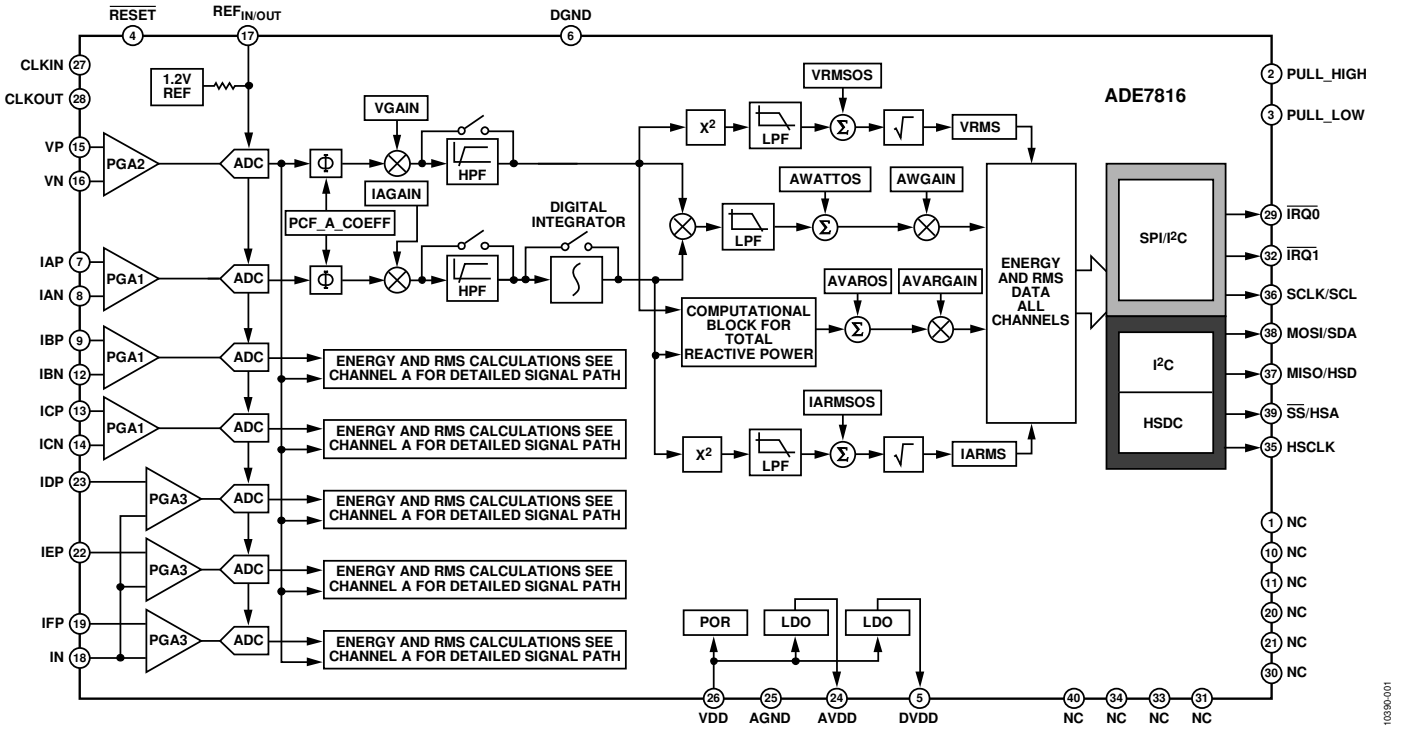

Figure 1.

Rev. A Document Feedback

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Technical Support www.analog.com

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- ADE7816 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1137: ADE7816 Theory of Operation
- AN-1152: Calibrating a Single-Phase Energy Meter Based on the ADE7816
- AN-639: Frequently Asked Questions (FAQs) Analog Devices Energy (ADE) Products

Data Sheet

- ADE7816: Six Current Channels, One Voltage Channel Energy Metering IC Data Sheet

Product Highlight

- ADE7816 Multichannel Energy Measurement

User Guides

- UG-370: Evaluation Board for the ADE7816 Six Current Channels, One Voltage Channel Energy Metering IC

TOOLS AND SIMULATIONS

- ADE7816 Phase Calibration Calculator

DESIGN RESOURCES

- ADE7816 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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TABLE OF CONTENTS

REVISION HISTORY

12/13—Rev. 0 to Rev. A

Changes to EPAD Notation and Changed Pin 33 and Pin 34 Descriptions ... 9
Changes to Energy Phase Calibration Section ... 25
Changes to Zero-Crossing Detection Section and Figure 33 ... 26
Changes to Indication of Power Direction Section ... 28
Changes to Table 12 ... 38
Changes to Bits[7:6] Description; Table 26 ... 43

2/12—Revision 0: Initial Version

SPECIFICATIONS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 1.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					
Active Energy Measurement					
Active Energy Measurement Error (per Channel)		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8,16; integrator on
Phase Error Between Channels					Line frequency = 45 Hz to 65 Hz, HPF on
Power Factor (PF) = 0.8 Capacitive			±0.05	Degrees	Phase lead = 37°
PF = 0.5 Inductive			±0.05	Degrees	Phase lag = 60°
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz, IxP = VP = ±100 mV rms
Energy Register Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Energy Register Variation		0.01		%	
Total Active Energy Measurement Bandwidth		2		kHz	
REACTIVE ENERGY MEASUREMENT					
Reactive Energy Measurement Error (per Channel)		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8,16; integrator on
Phase Error Between Channels					Line frequency = 45 Hz to 65 Hz, HPF on
PF = 0.8 Capacitive			±0.05	Degrees	Phase lead = 37°
PF = 0.5 Inductive			±0.05	Degrees	Phase lag = 60°
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz, IxP = VP = ±100 mV rms
Energy Register Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Energy Register Variation		0.01		%	
Total Reactive Energy Measurement Bandwidth		2		kHz	
RMS MEASUREMENTS					
I_{RMS} and V_{RMS} Measurement Bandwidth		2		kHz	
I_{RMS} and V_{RMS} Measurement Error		0.1		%	Over a dynamic range of 500 to 1; one second of averaging (100 samples)
ANALOG INPUTS					
Maximum Signal Levels			±500	mV peak	Single-ended inputs between the following pins: IAP and IAN, IBP and IBN, ICP and ICN, IDP and IN, IEP and IN, IFP and IN.
Input Impedance (DC)					
IAP, IAN, IBP, IBN, ICP, ICN, IDP, IEP, and IFP Pins	400			kΩ	
IN Pin	130			kΩ	
ADC Offset Error		±2		mV	PGA = 1, uncalibrated error, see the Terminology section
Gain Error		±4		%	External 1.2 V reference

Parameter [1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
WAVEFORM SAMPLING					Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS
Current and Voltage Channels					See the Instantaneous Waveforms section
Signal-to-Noise Ratio, SNR		70		dB	PGA = 1
Signal-to-Noise-and-Distortion Ratio, SINAD		60		dB	PGA = 1
Bandwidth (−3 dB)		2		kHz	
TIME INTERVAL BETWEEN CHANNELS					
Measurement Error		0.3		Degrees	Line frequency = 45 Hz to 65 Hz, HPF on
REFERENCE INPUT					
$REF_{IN/OUT}$ Input Voltage Range	1.1		1.3	V	Minimum = 1.2 V − 8%; maximum = 1.2 V + 8%
Input Capacitance			10	pF	
ON-CHIP REFERENCE					Nominal 1.207 V at the $REF_{IN/OUT}$ pin at T_A = 25°C
Reference Error		±2		mV	
Output Impedance	1.2			kΩ	
Temperature Coefficient		10	50	ppm/°C	Maximum value across full temperature range of −40°C to +85°C
CLKIN, CLKOUT					All specifications are for CLKIN, CLKOUT of 16.384 MHz
Input Clock Frequency	16.22	16.384	16.55	MHz	
Crystal Equivalent Series Resistance	30		200	Ω	
CLKIN Input Capacitance		20		pF	
CLKOUT Output Capacitance		20		pF	
LOGIC INPUTS—MOSI/SDA, SCLK/SCL, $\overline{SS}$/HSA, $\overline{RESET}$, PULL_HIGH, PULL_LOW					
Input High Voltage, V_{INH}	2.0			V	VDD = 3.3 V ± 10%
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V ± 10%
Input Current, I_{IN}			−8.7	µA	Input = 0 V, VDD = 3.3 V
			3	µA	Input = VDD = 3.3 V
		100		nA	Input = VDD = 3.3 V
Input Capacitance, C_{IN}		10		pF	
LOGIC OUTPUTS—$\overline{IRQ0}$, $\overline{IRQ1}$, MISO/HSD					VDD = 3.3 V ± 10%
Output High Voltage, V_{OH}	2.4			V	VDD = 3.3 V ± 10%
I_{SOURCE}			800	µA	
Output Low Voltage, V_{OL}			0.4	V	VDD = 3.3 V ± 10%
I_{SINK}			2	mA	
POWER SUPPLY					For specified performance
VDD Pin	3.0		3.6	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
I_{DD}		25	27.8	mA	

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for a definition of the parameters.

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C. Note that, within the timing tables and diagrams, the dual function pin names are referenced by the relevant function only; see the Pin Configuration and Function Descriptions section for full pin mnemonics and function descriptions.

I²C-Compatible Interface Timing

Table 2. I²C-Compatible Interface Timing Parameters

		Standard Mode		Fast Mode		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) Start Condition	$t_{HD;STA}$	4.0		0.6		µs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		µs
High Period of SCL Clock	t_{HIGH}	4.0		0.6		µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$	4.7		0.6		µs
Data Hold Time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data Setup Time	$t_{SU;DAT}$	250		100		ns
Rise Time of Both SDA and SCL Signals	t_R		1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_F		300	20	300	ns
Setup Time for Stop Condition	$t_{SU;STO}$	4.0		0.6		µs
Bus Free Time Between a Stop and Start Condition	t_{BUF}	4.7		1.3		µs
Pulse Width of Suppressed Spikes	t_{SP}	N/A[1]			50	ns

[1] N/A means not applicable.

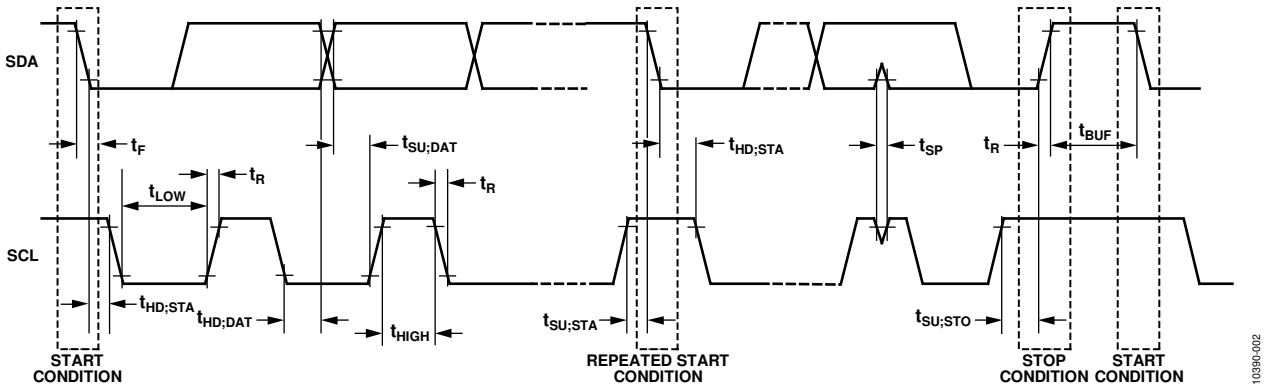


Figure 2. I²C-Compatible Interface Timing

SPI Interface Timing

Table 3. SPI Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	50		ns
SCLK Period		0.4	4000[1]	µs
SCLK Low Pulse Width	t_{SL}	175		ns
SCLK High Pulse Width	t_{SH}	175		ns
Data Output Valid After SCLK Edge	t_{DAV}		100	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	100		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	5		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}		200	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0		ns

[1] Guaranteed by design.

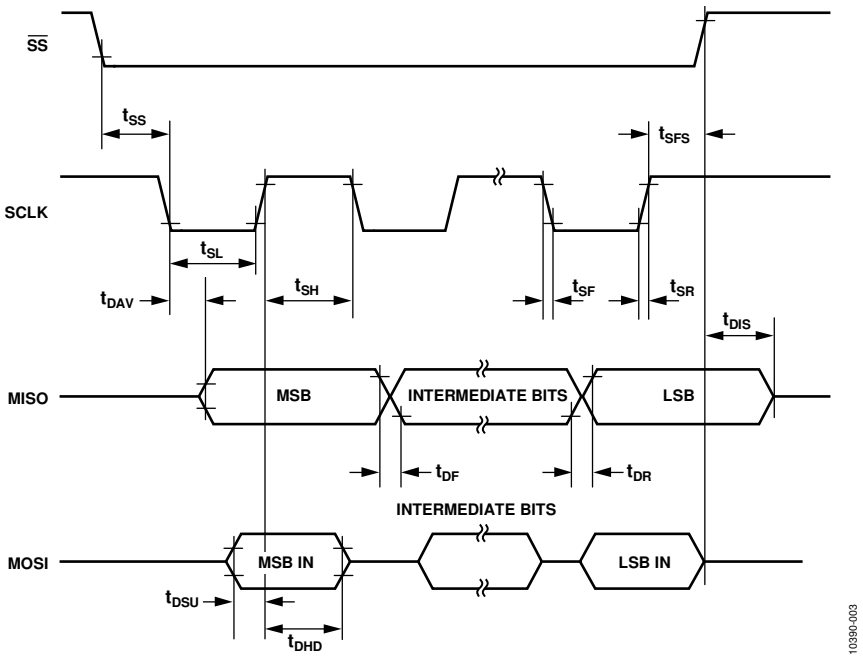


Figure 3. SPI Interface Timing

HSDC Interface Timing

Table 4. HSDC Interface Timing Parameter

Parameter	Symbol	Min	Max	Unit
HSA to HSCLK Edge	t_{SS}	0		ns
HSCLK Period		125		ns
HSCLK Low Pulse Width	t_{SL}	50		ns
HSCLK High Pulse Width	t_{SH}	50		ns
Data Output Valid After HSCLK Edge	t_{DAV}		40	ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
HSCLK Rise Time	t_{SR}		10	ns
HSCLK Fall Time	t_{SF}		10	ns
HSD Disable After HSA Rising Edge	t_{DIS}	5		ns
HSA High After HSCLK Edge	t_{SFS}	0		ns

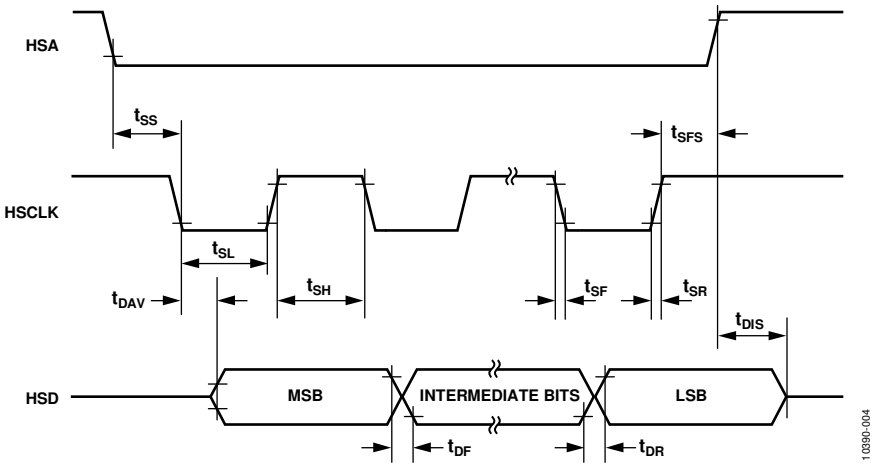


Figure 4. HSDC Interface Timing

Load Circuit for All Timing Specifications

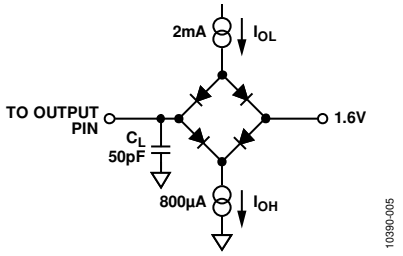


Figure 5. Load Circuit for All Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
VDD to AGND	−0.3 V to +3.7 V
VDD to DGND	−0.3 V to +3.7 V
Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, ICP, ICN, IDP, IEP, IFP, IN	−2 V to +2 V
Analog Input Voltage to VP and VN	−2 V to +2 V
Reference Input Voltage to AGND	−0.3 V to VDD + 0.3 V
Digital Input Voltage to DGND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Regarding the temperature profile used in soldering RoHS-compliant parts, Analog Devices, Inc., advises that reflow profiles should conform to J-STD-20 from JEDEC. Refer to the JEDEC website for the latest revision.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

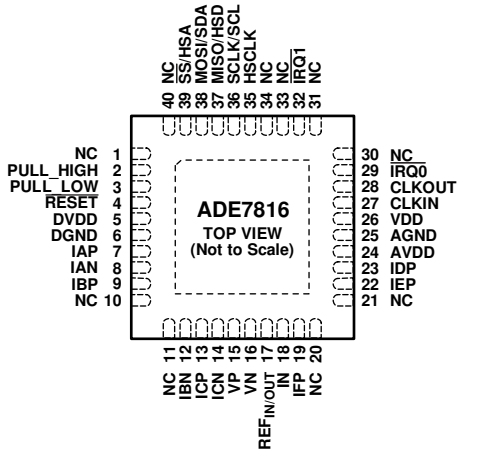
Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	29.3	1.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. THESE PINS ARE NOT CONNECTED INTERNALLY AND SHOULD BE LEFT FLOATING.
2. CREATE A SIMILAR PAD ON THE PCB UNDER THE EXPOSED PAD. SOLDER THE EXPOSED PAD TO THE PAD ON THE PCB TO CONFER MECHANICAL STRENGTH TO THE PACKAGE. CONNECT THE PADS TO AGND AND DGND.

10390-006

Figure 6. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10, 11, 20, 21, 30, 31, 40	NC	No Connect. These pins are not connected internally and should be left floating.
33, 34	NC	No Connect. These pins should be left floating. Do not connect to GND.
2	PULL_HIGH	Connect this pin to VDD for proper operation.
3	PULL_LOW	Connect this pin to AGND for proper operation.
4	$\overline{\text{RESET}}$	Active Low Reset Input. Hold this pin low for at least 10 µs to trigger a hardware reset.
5	DVDD	On-Chip 2.5 V Digital LDO Access. Do not connect any external active circuitry to this pin. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor.
6	DGND	Ground Reference. This pin provides the ground reference for the digital circuitry.
7, 8	IAP, IAN	Analog Inputs for Current Channel A. This channel is used with the current transducers and is referenced in this data sheet as Current Channel A. Connect these inputs in a single-ended configuration with a maximum signal level of ±0.5 V with respect to IAN.
9, 12	IBP, IBN	Analog Inputs for Current Channel B. This channel is used with the current transducers and is referenced in this data sheet as Current Channel B. Connect these inputs in a single-ended configuration with a maximum signal level of ±0.5 V with respect to IBN.
13, 14	ICP, ICN	Analog Inputs for Current Channel C. This channel is used with the current transducers and is referenced in this data sheet as Current Channel C. Connect these inputs in a single-ended configuration with a maximum signal level of ±0.5 V with respect to ICN.
15, 16	VP, VN	Analog Inputs for the Voltage Channel. This channel is used with the voltage transducer and is referenced as the voltage channel in this data sheet. Connect these inputs in a single-ended configuration with a maximum signal level of ±0.5 V with respect to VN. This channel also has an internal PGA.
17	$\text{REF}_{\text{IN/OUT}}$	On-Chip Voltage Reference Access. The on-chip reference has a nominal value of 1.2 V. An external reference source with 1.2 V ± 8% can also be connected at this pin. In either case, decouple this pin to AGND with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor.
18	IN	Analog Input Common Pin for Current Channel D, Current Channel E, and Current Channel F. See the pin descriptions for Pin 19, Pin 22, and Pin 23 for more details.
19	IFP	Analog Input for Current Channel F. This channel is used with the current transducers and is referenced in this data sheet as Current Channel F. Connect this input in a single-ended configuration with a maximum signal level of ±0.5 V with respect to IN.
22	IEP	Analog Input for Current Channel E. This channel is used with the current transducers and is referenced in this data sheet as Current Channel E. Connect this input in a single-ended configuration with a maximum signal level of ±0.5 V with respect to IN.
23	IDP	Analog Input for Current Channel D. This channel is used with the current transducers and is referenced in

Pin No.	Mnemonic	Description
		this data sheet as Current Channel D. Connect this input in a single-ended configuration with a maximum signal level of ±0.5 V with respect to IN.
24	AVDD	On-Chip 2.5 V Analog Low Dropout (LDO) Regulator Access. Do not connect external active circuitry to this pin. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor.
25	AGND	Ground Reference. This pin provides the ground reference for the analog circuitry. Tie this pin to the analog ground plane or to the quietest ground reference in the system. Use this quiet ground reference for all analog circuitry, such as antialiasing filters and current and voltage transducers.
26	VDD	Supply Voltage. This pin provides the supply voltage and should be set at 3.3 V ± 10% for specified operation. Decouple this pin to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
27	CLKIN	Master Clock. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT-cut crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7816. The clock frequency for specified operation is 16.384 MHz. Use ceramic load capacitors of a few tens of picofarads (pF) with the gate oscillator circuit. Refer to the crystal manufacturer data sheet for load capacitance requirements.
28	CLKOUT	A crystal can be connected across this pin and CLKIN (as stated in the description for Pin 27) to provide a clock source for the ADE7816. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used.
29, 32	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$	Interrupt Request Outputs. These are active low logic outputs. See the Interrupts section for a detailed presentation of the events that can trigger interrupts.
35	HSCLK	Serial Clock Output for the HSDC Port.
36	SCLK/SCL	Serial Clock Input for the SPI Port/Serial Clock Input for the I²C Port. All serial data transfers are synchronized to this clock (see the Communication section). This pin has a Schmidt trigger input for use with a clock source that has a slow edge transition time (for example, opto-isolator outputs).
37	MISO/HSD	Data Output for SPI Port/Data Output for HSDC Port.
38	MOSI/SDA	Data Input for SPI Port/Data Output for I²C Port.
39	$\overline{\text{SS}}$/HSA	Slave Select for SPI Port/HSDC Port Active.
EP	Exposed Pad	Exposed Pad. Create a similar pad on the PCB under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package. Connect the pads to AGND and DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

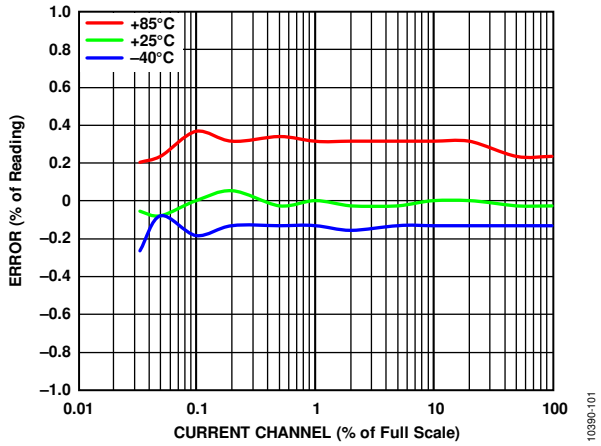


Figure 7. Active Energy Error as a Percentage of Reading (Gain = 1, Power Factor = 1) over Temperature with Internal Reference, Integrator Off

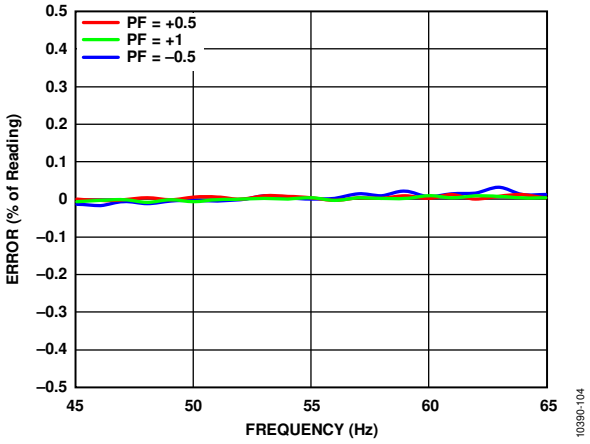


Figure 10. Active Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Frequency and Power Factor with Internal Reference, Integrator Off

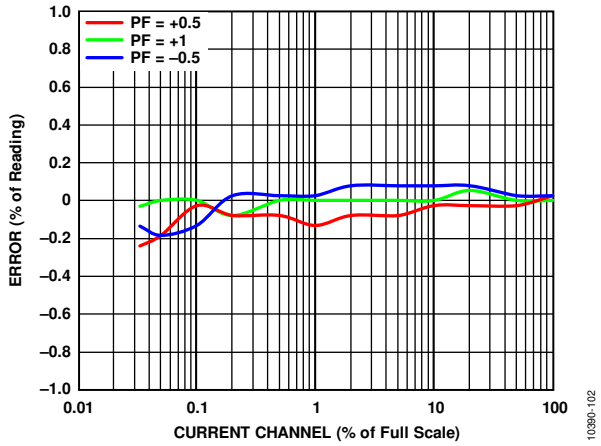


Figure 8. Active Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Power Factor with Internal Reference, Integrator Off

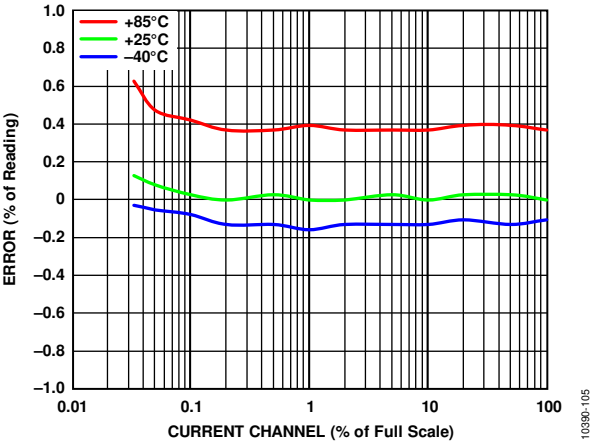


Figure 11. Reactive Energy Error as a Percentage of Reading (Gain = 1, Power Factor = 0) over Temperature with Internal Reference, Integrator Off

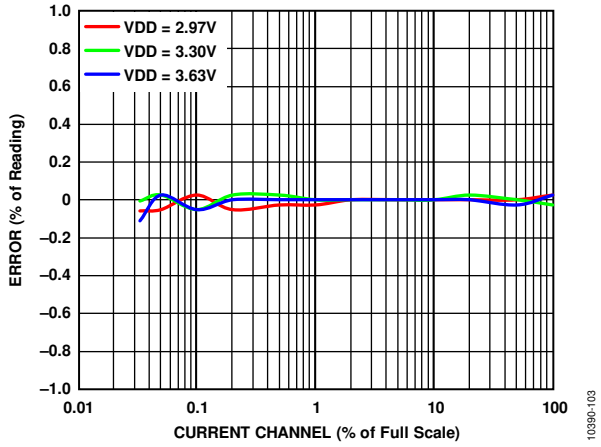


Figure 9. Active Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C, Power Factor = 1) over Supply Voltage with Internal Reference, Integrator Off

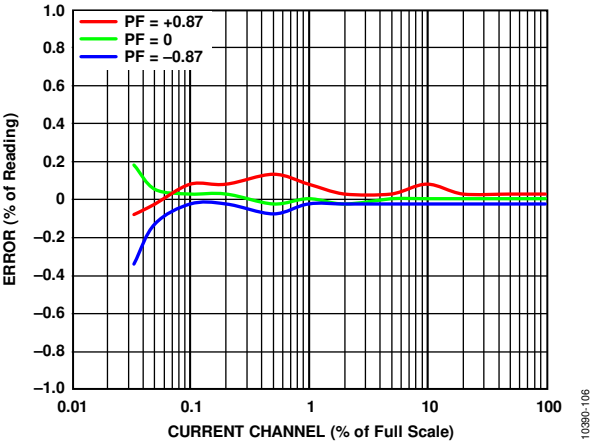


Figure 12. Reactive Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Power Factor with Internal Reference, Integrator Off

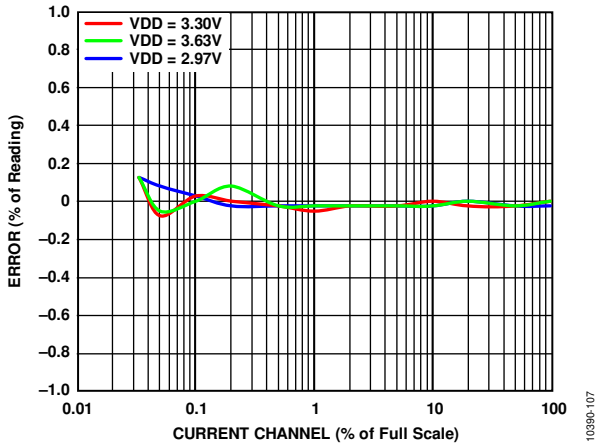


Figure 13. Reactive Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C, Power Factor = 0) over Supply Voltage with Internal Reference, Integrator Off

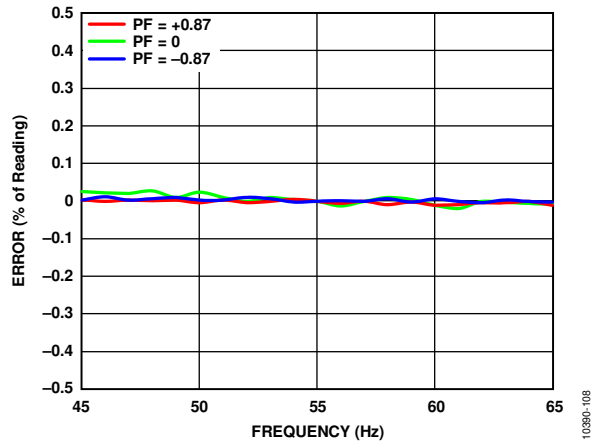


Figure 14. Reactive Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Frequency and Power Factor with Internal Reference

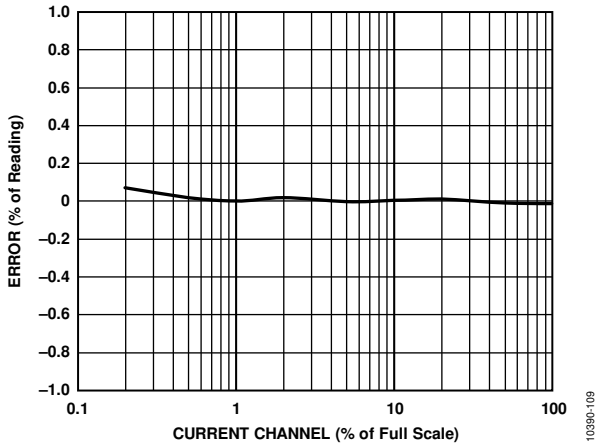


Figure 15. I_{RMS} Error as a Percentage of Reading (Gain = 1, Temperature = 25°C, Power Factor = 1) with Internal Reference, Integrator Off

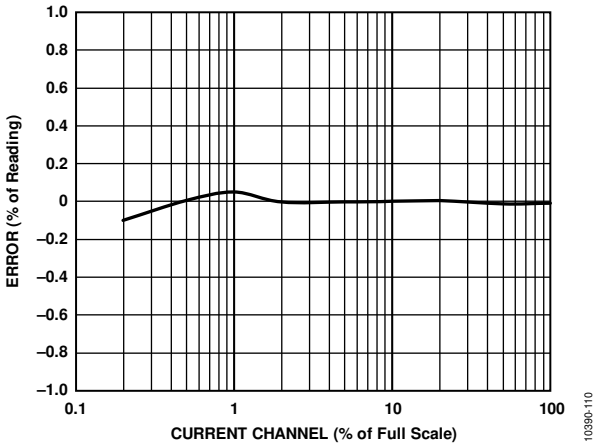


Figure 16. V_{RMS} Error as a Percentage of Reading (Gain = 1, Temperature = 25°C, Power Factor = 1) with Internal Reference, Integrator Off

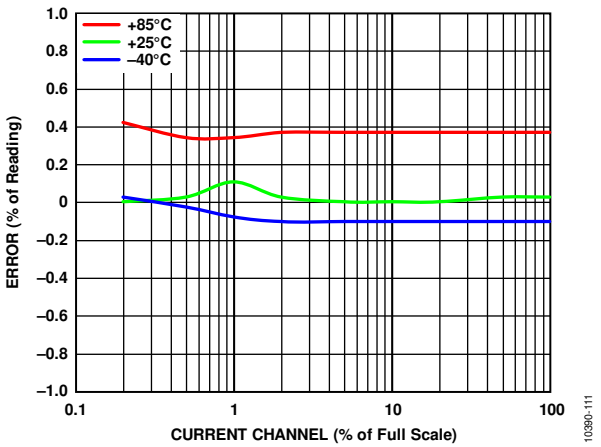


Figure 17. Active Energy Error as a Percentage of Reading (Gain = 16, Power Factor = 1) over Temperature with Internal Reference, Integrator On

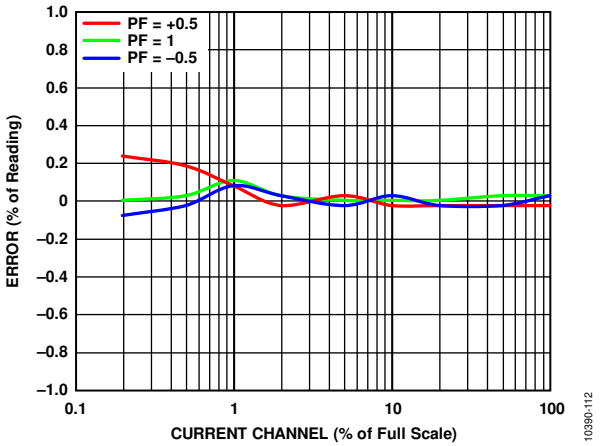


Figure 18. Active Energy Error as a Percentage of Reading (Gain = 16, Temperature = 25°C) over Power Factor with Internal Reference, Integrator On

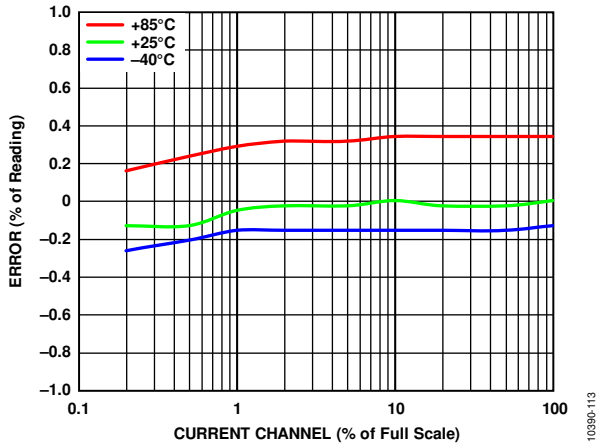


Figure 19. Reactive Energy Error as a Percentage of Reading (Gain = 16, Power Factor = 0) over Temperature with Internal Reference, Integrator On

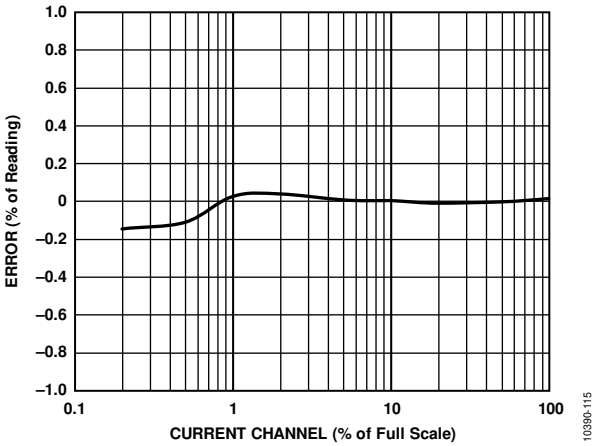


Figure 21. I_{RMS} Error as a Percentage of Reading (Gain = 16, Temperature = 25°C, Power Factor = 1) with Internal Reference, Integrator On

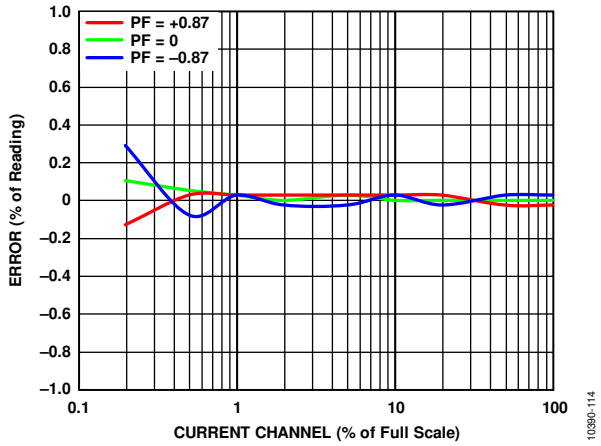


Figure 20. Reactive Energy Error as a Percentage of Reading (Gain = 16, Temperature = 25°C) over Power Factor with Internal Reference, Integrator On

TEST CIRCUIT

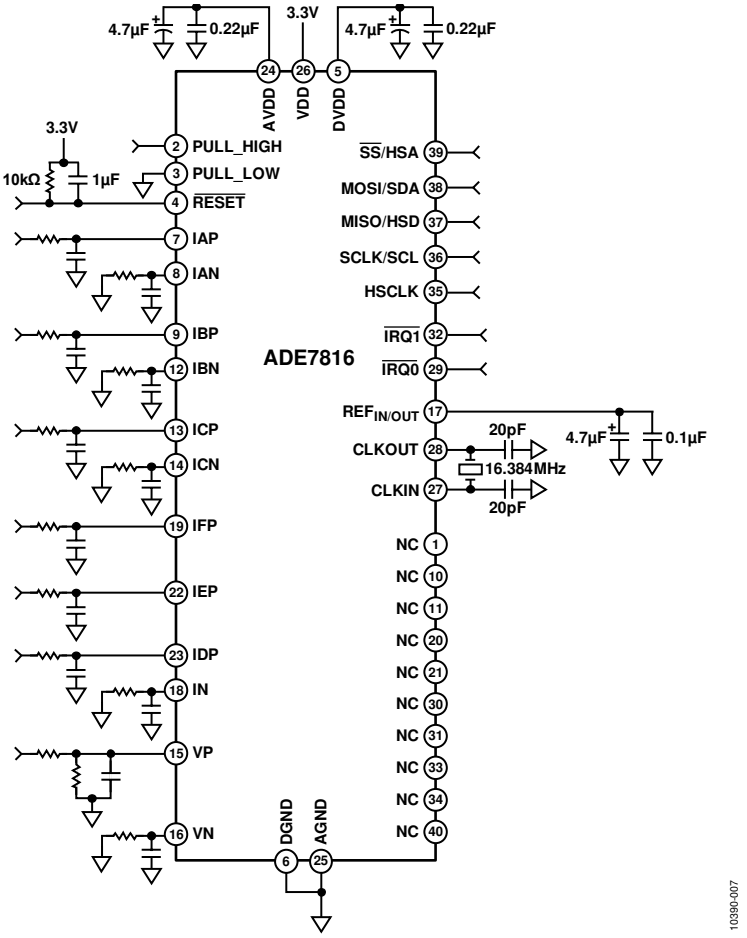


Figure 22. Test Circuit

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7816 is defined by the following equation:

$$Measurement\ Error = \frac{Energy\ Registered\ by\ ADE7816 - True\ Energy}{True\ Energy} \times 100\%$$

Phase Error Between Channels

The high-pass filter (HPF) and digital integrator introduce a slight phase mismatch between the current channels and the voltage channel. The all digital design ensures that the phase matching between the current channels and voltage channel in all three phases is within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range of 40 Hz to 1 kHz. This internal phase mismatch can be combined with the external phase error (from current sensor or component tolerance) and calibrated with the phase calibration registers.

Power Supply Rejection (PSR)

PSR quantifies the ADE7816 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at 100 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading (see the Measurement Error definition).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±10%. Any error introduced is expressed as a percentage of the reading.

ADC Offset Error

ADC offset error refers to the dc offset that is associated with the analog inputs to the ADCs. It means that, with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection (see the Typical Performance Characteristics section). However, the HPF removes the offset from the current channels and voltage channel, and the power calculation remains unaffected by this offset.

Gain Error

The gain error in the ADCs of the ADE7816 is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code. The difference is expressed as a percentage of the ideal code.

QUICK START

This section outlines the procedure for powering up and initializing the ADE7816. Figure 23 shows a flow diagram of the initialization steps. For detailed information, refer to the section of the data sheet that pertains to each step, as indicated in Figure 23.

After power is supplied to the ADE7816 and communication is established, a set of registers must be written (see Figure 23). Table 8 lists details about each register.

The registers listed in Table 8 are essential for correct operation. After these registers are set, enable any meter-specific features before enabling the DSP to begin the energy calculations.

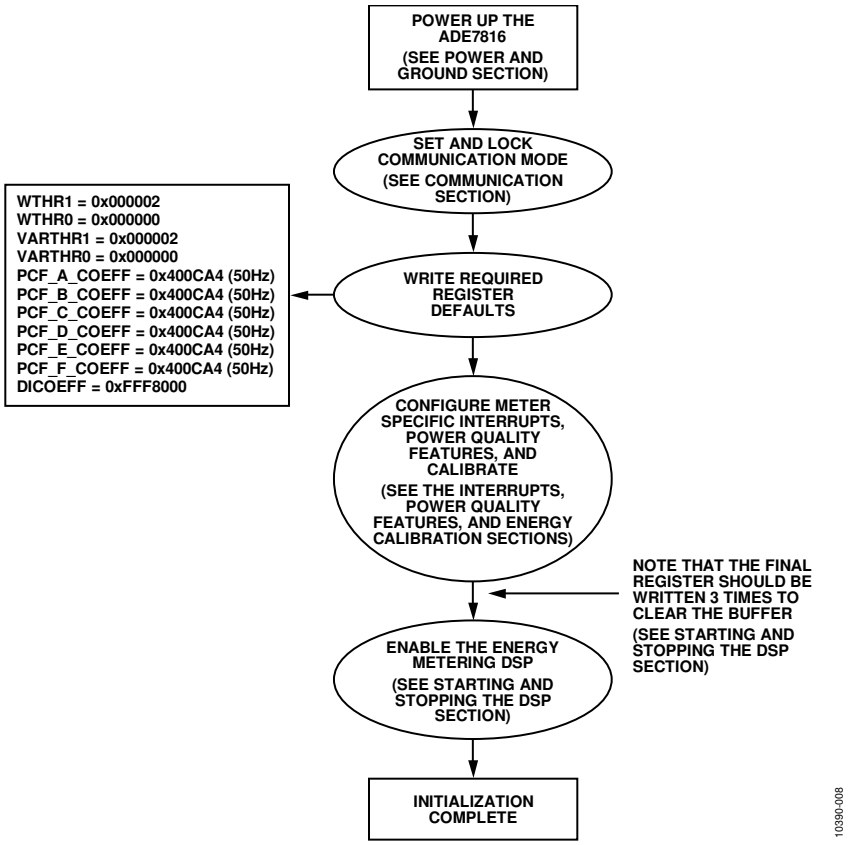


Figure 23. Quick Start

Table 8. Required Register Defaults

Register Address	Register Name	Register Description	Required Value	Reference Information
0x43AB	WTHR1	Threshold register for active energy	0x000002	Refer to the Active Energy Threshold section.
0x43AC	WTHR0	Threshold register for active energy	0x000000	Refer to the Active Energy Threshold section.
0x43AD	VARTHR1	Threshold register for reactive energy	0x000002	Refer to the Reactive Energy Threshold section.
0x43AE	VARTHR0	Threshold register for reactive energy	0x000000	Refer to the Reactive Energy Threshold section.
0x43B1	PCF_A_COEFF	Phase calibration for Current Channel A	0x400CA4 (50 Hz)	Refer to the Energy Phase Calibration section.
0x43B2	PCF_B_COEFF	Phase calibration for Current Channel B	0x400CA4 (50 Hz)	Refer to the Energy Phase Calibration section.
0x43B3	PCF_C_COEFF	Phase calibration for Current Channel C	0x400CA4 (50 Hz)	Refer to the Energy Phase Calibration section.
0x43B4	PCF_D_COEFF	Phase calibration for Current Channel D	0x400CA4 (50 Hz)	Refer to the Energy Phase Calibration section.
0x43B5	PCF_E_COEFF	Phase calibration for Current Channel E	0x400CA4 (50 Hz)	Refer to the Energy Phase Calibration section.
0x43B6	PCF_F_COEFF	Phase calibration for Current Channel F	0x400CA4 (50 Hz)	Refer to the Energy Phase Calibration section.
0x4388	DICOEFF	Digital integrator algorithm; required only if using di/dt sensors	0xFFF8000	Refer to the Digital Integrator section.

INPUTS

The following section provides details on the ADE7816 input connections that are required for correct functionality.

POWER AND GROUND

VDD and AGND, DGND

To power the ADE7816, a 3.3 V dc input voltage should be provided between the VDD pin and the AGND and DGND pins. In addition, the PULL_HIGH and PULL_LOW pins must be connected to 3.3 V and AGND, respectively. This configuration is shown in Figure 24.

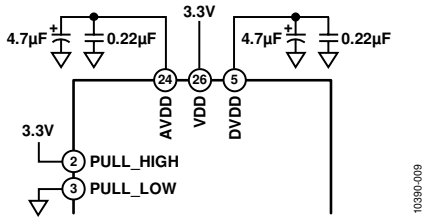


Figure 24. Applying Power to the ADE7816

The ADE7816 contains an on-chip power supply monitor that supervises the power supply (VDD). When the voltage applied to the VDD pin is below 2 V ± 10%, the chip is in an inactive state. After VDD crosses the 2 V ± 10% threshold, the power supply monitor keeps the ADE7816 in an inactive state for an additional 26 ms. This time delay allows VDD to reach the minimum specified operating voltage of 3.3 V − 10%. When the minimum specified operating voltage is met and the PULL_HIGH and PULL_LOW pins are tied to VDD and AGND, respectively, the internal circuitry is enabled. This process is accomplished in approximately 40 ms.

When the start-up sequence is complete and the ADE7816 is ready to receive communication from a microcontroller, the RSTDONE flag is set in the STATUS1 register (Address 0xE503). An external interrupt is triggered on the $\overline{\text{IRQ1}}$ pin. The RSTDONE interrupt is enabled by default and cannot be disabled; therefore, an external interrupt always occurs at the end of a power-up procedure or hardware or software reset.

It is highly recommended that the RSTDONE interrupt be used by the microcontroller to gate the first communication with the ADE7816. If the interrupt is not used, a timeout can be implemented. However, because the start-up sequence can vary from part to part and over temperature, a timeout of a least 100 ms is recommended. The RSTDONE interrupt provides the most time-efficient way of monitoring the completion of the ADE7816 start-up sequence.

The AVDD and DVDD output pins provide access to the on-chip analog and digital LDOs. When the ADE7816 is fully powered up, these pins are at 2.5 V. If the internal reference is being used, the $\text{REF}_{\text{IN/OUT}}$ pin outputs 1.2 V (see the Reference Circuit section).

When the start-up sequence is complete, all registers are at their default value, and the I^2C port is the active serial port. Communication with the ADE7816 can begin. See the Communication section for more details.

To start the energy and rms computations, the internal DSP must be powered up after all configuration registers are set to their desired values. The DSP is started by setting the run register (Address 0xE228) to 0x0001. See the Starting and Stopping the DSP section for more information.

REFERENCE CIRCUIT

$\text{REF}_{\text{IN/OUT}}$

The nominal reference voltage at the $\text{REF}_{\text{IN/OUT}}$ pin is 1.2 V ± 0.075%. The $\text{REF}_{\text{IN/OUT}}$ pin can be overdriven by an external 1.2 V reference source. If Bit 0 (EXTREFEN) in the CONFIG2 register (Address 0xEC01) is cleared to 0 (the default value), the ADE7816 uses the internal voltage reference. If Bit 0 is set to 1, the external voltage reference is used.

The voltage of the ADE7816 internal reference drifts slightly with temperature; see the Specifications section for the temperature coefficient specification (in ppm/°C). The value of the temperature drift varies from part to part. Because the reference is used for all ADCs, any x% drift in the reference results in a 2x% deviation of the meter accuracy.

RESET

Hardware Reset

To initiate a hardware reset of the ADE7816, the $\overline{\text{RESET}}$ pin must be pulled low for at least 10 µs. After the $\overline{\text{RESET}}$ pin returns high, all registers return to their default values. The ADE7816 signals the end of the transition period by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is set to 0 during the transition period and changes to 1 when the transition ends.

Software Reset Functionality

Bit 7 (SWRST) in the CONFIG register (Address 0xE618) manages the software reset functionality in the ADE7816. The default value of this bit is 0. If Bit 7 is set to 1, the ADE7816 enters the software reset state. In this state, all internal registers are set to their default values, with the exception of the CONFIG2 register, which retains its existing value. In addition, the choice of which serial port is in use (I^2C or SPI) remains unchanged if the lock-in procedure was executed previously (see the Communication section for details).

When the software reset ends, Bit 7 (SWRST) in the CONFIG register is cleared to 0, the $\overline{\text{IRQ1}}$ interrupt pin is set low, and Bit 15 (RSTDONE) in the STATUS1 register is set to 1. RSTDONE is set to 0 during the transition period and changes to 1 when the transition ends.

It is recommended that all meters be designed to have both software and hardware reset capability.

CLKIN AND CLKOUT

An external clock or parallel resonant crystal is required to clock the ADE7816. If an external clock source is being used, it should be connected to the CLKIN pin. The required clock frequency for specified operation is 16.384 MHz. Alternatively, a parallel resonant AT-cut crystal can be connected across the CLKIN and CLKOUT pins. The ADE7816 has no internal load capacitance and, therefore, load capacitors based on the data sheet of the crystal manufacturer should be added on each pin.

ANALOG INPUTS

Input Pins

The ADE7816 has seven analog inputs that form six current channels and one voltage channel. Current Channel A, Current Channel B, and Current Channel C each consist of a pair of differential input pins: IAP and IAN, IBP and IBN, and ICP and ICN. Current Channel D, Current Channel E, and Current Channel F all share a common reference, IN, and, therefore, are single-ended. For consistency, it is recommended that all six current inputs be connected in a single-ended configuration (see Figure 26 and Figure 27). The voltage channel is a fully differential input that consists of a pair of inputs: VP and VN. The voltage channel is typically connected in a single-ended configuration.

The maximum input voltage that should be applied to any input channel is ±500 mV. The maximum common-mode signal that is allowed on the inputs is ±25 mV. Figure 25 shows a schematic of the inputs and their relation to the maximum common-mode voltage.

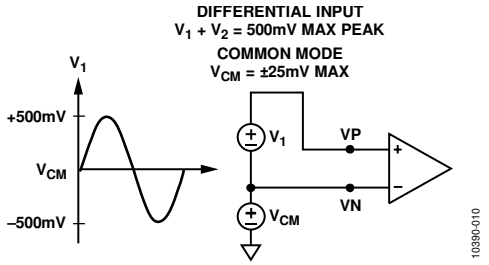


Figure 25. Maximum Input Level

PGA Gain

The ADE7816 has three internal PGA gain amplifiers that can be used to amplify the input signals by ×2, ×4, ×8 or ×16. The PGA gain stage is often required when using a current sensor that produces a low output voltage, such as Rogowski coils. PGA1 affects Current Channel A, Current Channel B, and Current Channel C and is controlled by Bits[2:0] (PGA1) of the gain register (Address 0xE60F). PGA2 affects the voltage channel and is controlled by Bits[5:3] (PGA2) of the gain register. PGA3 affects Current Channel D, Current Channel E, and Current Channel F and is controlled by Bits[8:6] (PGA3) of the gain register.

Table 9 lists details on how the PGA gain affects the full-scale input voltage.

Table 9. PGA Gain

Gain	Full-Scale Single-Ended Input (mV)	Gain Register (Address 0xE60F)		
		PGA1[2:0]	PGA2[5:3]	PGA3[8:6]
1	±500	000	000	000
2	±250	001	001	001
4	±125	010	010	010
8	±62.5	011	011	011
16	±31.25	100	100	100

Digital Integrator

The ADE7816 includes a digital integrator that must be enabled when using a di/dt sensor such as a Rogowski coil. This integrator is enabled by setting the INTEN bit (Bit 0) of the CONFIG register (Address 0xE618) to 1. When using the digital integrator, the DICOEFF register (Address 0x4388) should be written to 0xFFF8000. For more details on the theory behind the digital integrator, refer to the AN-1137 Application Note.

Antialiasing Filters

Each analog input pin requires that a simple RC filter be connected to the input. The role of the RC filter is to prevent aliasing. The aliasing effect is caused by frequency components (which are higher than half the sampling rate of the ADC) folding back and appearing in the sampled signal at a frequency that is below half the sampling rate. Aliasing is an artifact of all sampled systems. For conventional current sensors, it is recommended that one RC filter with a corner frequency of 5 kHz be used for the attenuation to be sufficiently high at the sampling frequency of 1.024 MHz. The 20 dB per decade attenuation of this filter is usually sufficient to eliminate the effects of aliasing for conventional current sensors (see Figure 26).

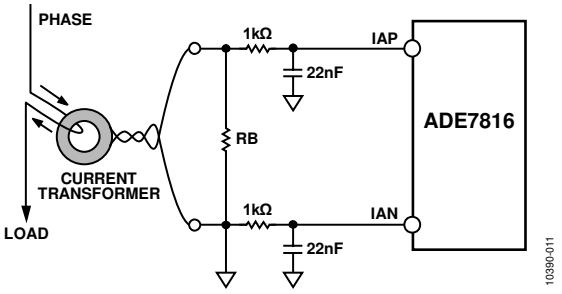


Figure 26. Current Transformer Input Connections

However, a di/dt sensor, such as a Rogowski coil, has a 20 dB per decade gain. This neutralizes the 20 dB per decade attenuation produced by the low-pass filter (LPF). Therefore, when using a di/dt sensor, a second pole is required. One simple approach is to cascade one additional RC filter, thereby producing a −40 dB per decade attenuation (see Figure 27).

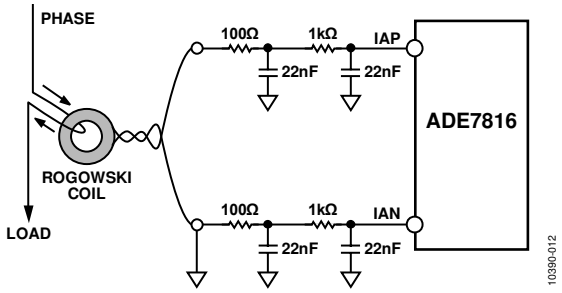


Figure 27. Rogowski Coil Input Connections

ENERGY MEASUREMENTS

This section describes the energy measurements available in the ADE7816. For information about the theory behind these measurements, refer to the AN-1137 Application Note.

STARTING AND STOPPING THE DSP

To obtain energy measurements, the internal processor must first be started by setting the run register (Address 0xE228) to 0x0001. It is recommended that all registers be initialized before starting the DSP and that the last register in the queue be written three times to flush the pipeline. When this procedure is complete, the DSP should be started. There is no reason to stop the DSP, once started, because all of the registers can be modified while the DSP is running. The DSP can be stopped, however, by writing 0x0000 to the run register.

Within the DSP core, there is a two-stage pipeline. This means that when a single register must be initialized, two or more writes are required to ensure that the value has been written. If two or more registers must be initialized, the last register must be written two more times to ensure that the value is written into the RAM. It is recommended that the last register be written three times to ensure successful communication. See the Register Protection section for details on protecting these registers.

ACTIVE ENERGY MEASUREMENT

Definition of Active Power and Active Energy

Active power is the product of voltage and current and is the power dissipated in a purely resistive load. Active energy is the accumulation of active power over time and is measured in watts.

The average power over an integral number of line cycles (n) is given by the following expression:

$$P = \frac{1}{nT}\int_0^{nT} P(t)dt = VI \quad (1)$$

where:
V is the rms voltage.
I is the rms current.
P is the active or real power.
T is the line cycle period.

Active Energy Registers

The ADE7816 has six active energy registers, where the active energy is accumulated for each of the six channels separately: AWATTHR (Address 0xE400), BWATTHR (Address 0xE401), CWATTHR (Address 0xE402), DWATTHR (Address 0xE403), EWATTHR (Address 0xE404) and FWATTHR (Address 0xE405). All active energy registers are in 32-bit, signed format. The ADE7816 accumulates both positive and negative power. Negative power indicates that the angle between the voltage and current is greater than 90°, and power is being injected back into the grid. The ADE7816 provides a signed accumulation of the power; positive power is added and negative power is subtracted. Figure 28 shows the configurations of the active energy signal path.

Active Energy Threshold

The ADE7816 accumulates energy in two steps (see Figure 28). The first step occurs internally, using the two threshold registers, WTHR1 (Address 0x43AB) and WTHR0 (Address 0x43AC). These registers make up the most significant and least significant 24 bits, respectively, of an internal threshold register that is used to control the frequency at which the external xWATTHR registers are updated. The WTHR1 and WTHR0 registers affect all six active energy measurements. For standard operation, the WTHR1 register should be set to 0x2 and the WTHR0 register set to 0x0. Thus, the update rate of the xWATTHR registers is set to slightly below the maximum of 8 kHz with full-scale inputs. If the rate at which energy is accumulated in the xWATTHR registers must be reduced, the WTHR1and WTHR0 registers can be modified.

$$Threshold = 0x2000000 \times \frac{8\text{ kHz}}{Required\ Update\ Rate\ (\text{kHz})} \quad (2)$$

Note that the maximum output with full scale inputs is 8 kHz. Do not adjust the threshold to try to produce more than 8 kHz. Such an adjustment may result in saturation of the output frequency and, therefore, a loss of accuracy.

The second stage of the accumulation occurs in the external registers, xWATTHR. With the recommended values provided in Equation 2, the energy updates at a rate of 8 kHz with full-scale inputs (see Figure 28).

Energy Accumulation and Register Roll-Over

As shown in Equation 2, the active energy accumulates at a maximum rate of 8 kHz with full-scale inputs. The maximum positive value that the 32-bit, signed xWATTHR registers can store before they overflow is 0x7FFFFFFF. Assuming steady accumulation with full-scale inputs, the accumulation time is

$$Time = 0x7FFFFFFF \times 125\ \mu s = 74\text{ hr, }33\text{ min, }55\text{ sec}$$

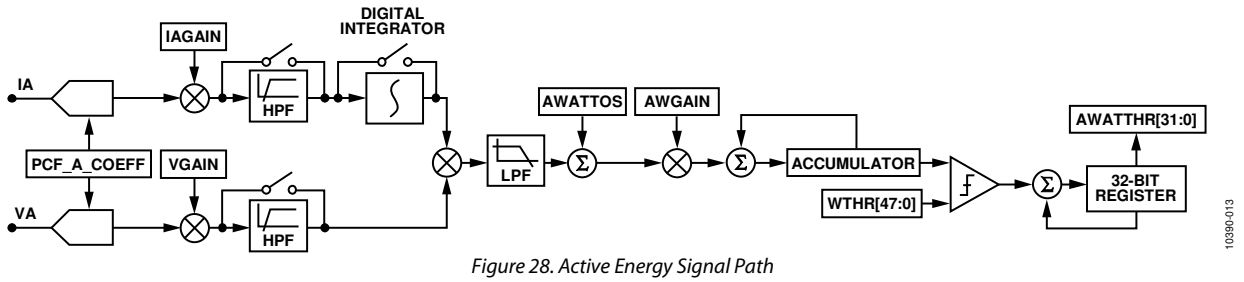


Figure 28. Active Energy Signal Path

The content of the active energy register overflows from full-scale positive (0x7FFFFFFF) to full-scale negative (0x80000000) and continues to increase in value when the active power is positive. Conversely, if the active power is negative, the energy register underflows from full-scale negative (0x80000000) to full-scale positive (0x7FFFFFFF) and continues decreasing in value. Bit 0 (AEHF1) in the STATUS0 register (Address 0xE502) is set when Bit 30 in the AWATTHR, BWATTHR, or CWATTHR register changes, signifying that one of these registers is half full. Similarly, Bit 1 (AEHF2) in the STATUS0 register is set when Bit 30 in the DWATTHR, EWATTHR, or FWATTHR register changes, signifying that one of these registers is half full.

Setting Bit 6 (RSTREAD) in the LCYCMODE register (Address 0xE702) enables a read-with-reset for all watt-hour accumulation registers. When this bit is set, all energy accumulation registers are set to 0 following a read operation.

REACTIVE ENERGY MEASUREMENT

Definition of Reactive Power and Reactive Energy

Reactive power is the product of the voltage and current when all harmonic components of one of these signals are phase shifted by 90°. Reactive power is the power dissipated in an induc-tive or capacitive load and is measured as volt-ampere reactive (var). Reactive energy is the accumulation of reactive power over time.

$$RP = \frac{1}{nT}\int_{0}^{nT} RP(t)dt = VI \times \sin(\theta) \quad (3)$$

where:
V is the rms voltage.
I is the rms current.
RP is the reactive or real power.
T is the line cycle period.

Reactive Energy Registers

The ADE7816 has six reactive energy registers that accumulate active energy for each of the six channels separately: AVARHR (Address 0xE406), BVARHR (Address 0xE407), CVARHR (Address 0xE408), DVARHR (Address 0xE409), EVARHR (Address 0xE40A), and FVARHR (Address 0xE40B). All reactive energy registers are in 32-bit, signed format. The ADE7816 accumulates both positive and negative reactive power. Negative reactive power indicates that the current is leading the voltage by up to 180°. The ADE7816 provides a signed accumulation of the power, where positive power is added and negative is subtracted.

Reactive Energy Threshold

The ADE7816 accumulates energy in two steps. The first is done internally using the threshold registers, VARTHR1 (Address 0x43AD) and VARTHR0 (Address 0x43AE). These registers make up the most significant and least significant 24 bits, respectively, of an internal threshold register that is used to control the frequency at which the external xVARHR registers are updated. The VARTHR1 and VARTHR0 registers affect all six reactive energy measurements. For standard operation, the VARTHR1 register should be set to 0x2 and the VARTHR0 register set to 0x0. This sets the update rate of the xVARHR registers to the maximum of 8 kHz with full-scale inputs.

If the rate at which energy is accumulated in the xVARHR registers must be reduced, VARTHR1 and VARTHR0 can be modified as follows:

$$Threshold = 0x2000000 \times \frac{8\text{ kHz}}{Required\ Update\ Rate\ (\text{kHz})} \quad (4)$$

Note that the maximum output with full scale inputs is 8 kHz. The threshold should not be adjusted to try to produce more than 8 kHz. Such an adjustment could result in saturation of the output frequency and, therefore, a loss of accuracy.

The second stage of the accumulation is done in the external registers, xVARHR. With the recommended values provided in Equation 4, the reactive energy updates at a rate of 8 kHz with full-scale inputs (see Figure 29).

Reactive Energy Accumulation and Register Roll-Over

The reactive energy accumulates at a maximum rate of 8 kHz with full-scale inputs. The maximum positive value that the 32-bit, signed xVARHR registers can store before they overflow is 0x7FFFFFFF. Assuming steady accumulation with full-scale reactive energy inputs, the accumulation time is

$$Time = 0x7FFFFFFF \times 125\ \mu s = 74\text{ hr, }33\text{ min, }55\text{ sec}$$

Conversely, if the reactive power is negative, the energy register underflows from full-scale negative (0x80000000) to full-scale positive (0x7FFFFFFF) and continues decreasing in value. Bit 2 (REHF1) in the STATUS0 register is set when Bit 30 of the AVARHR, BVARHR, or CVARHR register changes, signifying that one of these registers is half full. Similarly, Bit 3 (REHF2) in the STATUS0 register is set when Bit 30 of the DVARHR, EVARHR, or FVARHR register changes, signifying that one of these registers is half full.

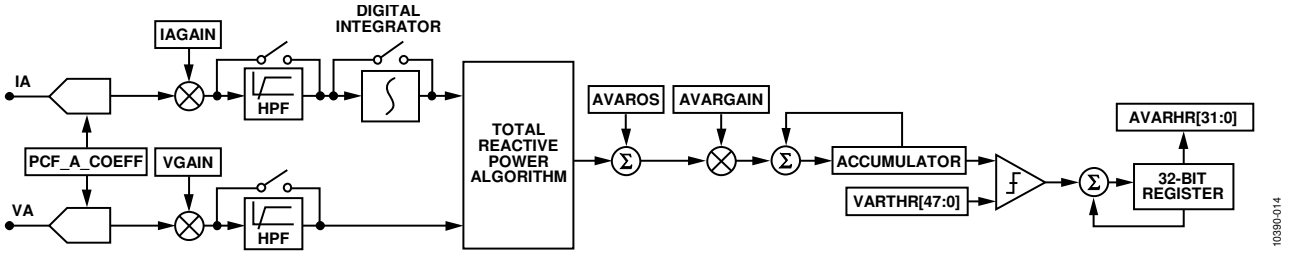


Figure 29. Reactive Energy Signal Path

The reactive energy register content overflows from full-scale positive (0x7FFFFFFF) to full-scale negative (0x80000000) and continues to increase in value when the reactive power is positive.

Setting Bit 6 (RSTREAD) of the LCYCMODE (Address 0xE702) register enables a read-with-reset for all reactive energy accumulation registers. When this bit is set, all energy accumulation registers are set to 0 following a read operation.

LINE CYCLE ACCUMULATION MODE

In the active and reactive line cycle accumulation mode, the energy accumulation of the ADE7816 is synchronized to the voltage channel zero crossing, so that the active and reactive energy can be accumulated over an integral number of half line cycles. This feature is available for the active and reactive energy accumulation on all six channels. The advantage of summing the active and reactive energy over an integral number of half line cycles is that the sinusoidal component of the energy is reduced to 0. This eliminates any ripple in the energy calculation. Accurate energy is calculated in a shorter time because the integration period can be shortened. The line cycle accumulation mode can be used for fast calibration and to obtain the average power over a specified time period. Figure 30 shows a diagram of the active energy line cycle accumulation mode signal path.

Active and reactive energy line cycle accumulation modes are disabled by default and can be enabled on all six channels by setting Bit 0 (LWATT) and Bit 1 (LVAR), respectively, in the LCYCMODE register. Bit 3 (ZX_SEL) of the LCYCMODE register must also be set to enable the voltage channel zero-crossing counter to be used in the line cycle accumulation measurement. The accumulation time should be written to the LINECYC register (Address 0xE60C) as an integer number of half line cycles. The ADE7816 can accumulate energy for up to 65,535 half line cycles. This equates to an accumulation period of approximately 655 sec with 50 Hz inputs, and 546 sec with 60 Hz inputs.

The number of half line cycles written to the LINECYC register is used for the active and reactive line cycle accumulation on all six channels. At the end of a line cycle accumulation period, the xWATTHR and xVARHR registers are updated and the LENERGY flag is set in the STATUS0 register (Address 0xE502). If the LENERGY bit in the MASK0 register (Address 0xE50A) is set, an external interrupt is issued on the $\overline{\text{IRQ0}}$ pin. Another accumulation cycle begins immediately, as long as the LWATT and LVAR bits in the LCYCMODE register remain set.

The contents of the xWATTHR and xVARHR registers are updated synchronous to the LENERGY flag. The xWATTHR and xVARHR registers hold their current values until the end of the next line cycle period, when the contents are replaced with the new reading (see Figure 30 and Figure 31). When using the line cycle accumulation mode, Bit 6 (RSTREAD) of the LCYCMODE register should be set to Logic 0 because the read-with-reset function of the energy registers is not available in this mode.

Note that, when line cycle accumulation mode is first enabled, the reading after the first LENERGY flag should be ignored because it may be inaccurate. This inaccuracy is due to the line cycle accumulation mode not being synchronized to the zero crossing. As a result, the first reading may not be taken over a complete number of half line cycles. After the first line cycle accumulation is completed, all successive readings are correct.

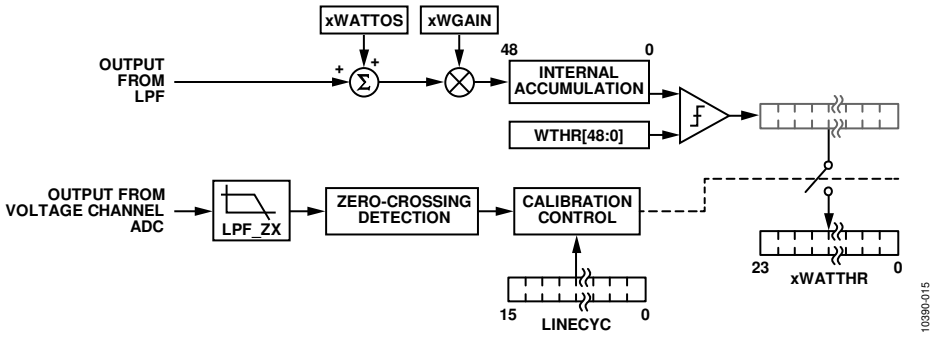


Figure 30. Line Cycle Accumulation for xWATTHR

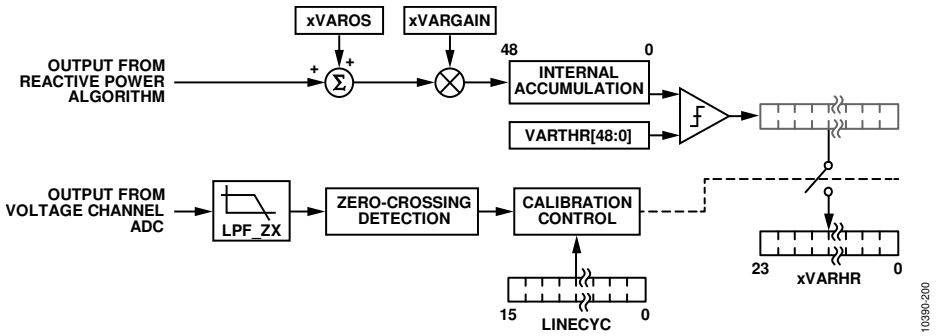


Figure 31. Line Cycle Accumulation for xVARHR

ROOT MEAN SQUARE MEASUREMENT

Root mean square (rms) is a measurement of the magnitude of an ac signal. Specifically, the rms of an ac signal is equal to the amount of dc required to produce an equivalent amount of power in the load. The ADE7816 provides rms measurements on the six current channels and the voltage channel simultaneously. These measurements have a settling time of approximately 440 ms with the integrator off and 500 ms with the integrator on. The registers are updated every 125 µs. The rms value is measured over a 2 kHz bandwidth.

The 24-bit, unsigned voltage rms measurement is available in the VRMS register (Address 0x43C0). Similarly, the six current channel rms measurements are available in the IARMS (Address 0x43C1), IBRMS (Address 0x43C2), ICRMS (Address 0x43C3), IDRMS (Address 0x43C4), IERMS (0x43C5), and IFRMS (Address 0x43C6) registers. All registers are updated at a rate of 8 kHz. Figure 32 shows the IxRMS signal path. A similar signal path is used on the voltage channel to compute the VRMS measurement.

Due to nonidealities in the internal filtering, it is recommended that the IxRMS registers be read synchronously to the zero-crossing signal (see the Zero-Crossing Detection section). This helps to stabilize reading-to-reading variation by removing the effect of any 2ω ripple that is present on the rms measurement.

With the specified full-scale analog input signal of 0.5 V, the rms value of a sinusoidal signal is 4,191,910 (0x3FF6A6), independent of line frequency. If the integrator is enabled on the current channels, the equivalent current rms value of a full-scale sinusoidal signal at 50 Hz is 4,191,910 (0x3FF6A6). At 60 Hz, it is 3,493,258 (0x354D8A).

NO LOAD DETECTION

The ADE7816 includes a no load detection feature that eliminates meter creep. Meter creep is defined as excess energy that is accumulated by the meter when there is no load attached. The ADE7816 warns of this condition and stops energy accumulation if the energy falls below a programmable threshold. The ADE7816 includes a no load feature on the active and reactive energy measurements. This allows a true no load condition to be detected.

The no load condition is triggered when the absolute values of the active and reactive powers are less than or equal to a threshold that is specified in the APNOLOAD (Address 0x43AF) and VARNOLOAD (Address 0x43B0) registers. When in the no load condition, the active and reactive energies are no longer accumulated in the energy registers. Note that each of the six channels has a separate no load circuit.

Setting the No Load Thresholds

The APNOLOAD and VARNOLOAD registers are compared to the active and reactive powers, respectively, to set the no load threshold. With full-scale inputs on both the current and voltage channel, the maximum power is 0x1FF6A6B. The no load threshold should, therefore, be set with respect to this maximum power, as follows:

$$APNOLOAD = 0x1FF6A6B \times V_{\%\ of\ Full\_Scale} \times I_{(noload)\%\ of\ Full\_Scale} \quad (5)$$

For example, if the nominal voltage is set to 50% of full scale and the current channel no load threshold is required to be at 0.01% of full scale, the APNOLOAD threshold is

$$APNOLOAD = 0x1FF6A6B \times 50\% \times 0.01\% = 0x68C \quad (6)$$

The VARNOLOAD register is usually set to the same value as that of the APNOLOAD register. When the APNOLOAD and VARNOLOAD registers are set to negative values, the no load detection circuit is disabled.

Bit 0 (NLOAD1) in the STATUS1 register (Address 0xE503) is set when the no load condition occurs on the A, B, or C current channel. Bit 1 (NLOAD2) in the STATUS1 register is set when the load condition occurs on the D, E, or F current channel. Bits[5:0] (NOLOADx) in the CHNOLOAD register (Address 0xE608) can be used to determine which channel caused the no load condition. When NOLOADx is cleared to 0, the channel is not in a no load condition. When NOLOADx is set to 1, the channel is in a no load condition.

No Load Interrupt

The ADE7816 includes two interrupts that are associated with the no load feature. The first is associated with the A, B, and C current channels, and it can be enabled by setting Bit 0 (NLOAD1) in the MASK1 register (Address 0xE50B). The second interrupt is associated with the D, E, and F current channels; it can be enabled by setting Bit 1 (NLOAD2) in the MASK1 register. If the corresponding interrupt is enabled, the no load condition causes the external $\overline{\text{IRQ1}}$ pin to go low (see the Interrupts section).

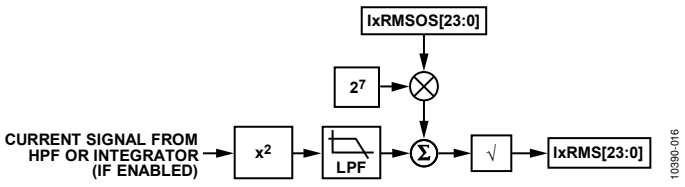


Figure 32. IxRMS Signal Path

ENERGY CALIBRATION

CHANNEL MATCHING

The ADE7816 provides individual channel gain registers that allow the six current channels and the voltage channel to be matched. Matching the channels simplifies the calibration process. The IAGAIN (Address 0x4381), IBGAIN (Address 0x4382), ICGAIN (Address 0x4383), IDGAIN (Address 0x4384), IEGAIN (Address 0x4385), and IFGAIN (Address 0x4386) registers adjust the A through F current channels, respectively, whereas the VGAIN register (Address 0x4380) can be used to adjust the voltage channel. The default value of the IxGAIN registers is 0x00000, which corresponds to no channel gain. The IxGAIN can adjust the channel gain by up to ±100%. The channel is scaled by −50% by writing 0xC00000 to the corresponding IxGAIN register, and it is increased by +50% by writing 0x400000. Equation 7 shows the relationship between the IxGAIN register and the rms measurement.

$$I_{rms} = I_{rms_0} \times \left(1 + \frac{IxGAIN}{2^{23}}\right) \quad (7)$$

$$V_{rms} = V_{rms_0} \times \left(1 + \frac{VGAIN}{2^{23}}\right)$$

where I_{rms_0} and V_{rms_0} are the current and voltage rms measurements, respectively, without offset correction.

Changing the content of the IxGAIN registers affects all calculations based off that channel, including the active and reactive energy. Therefore, it is recommended that the channel matching be performed first in the calibration procedure.

ENERGY GAIN CALIBRATION

The active and reactive energy measurements can be calibrated on all six channels separately. This separate calibration allows compensation for meter-to-meter gain variation.

The AWGAIN register (Address 0x4391) controls the active power gain calibration on Current Channel A. The BWGAIN (Address 0x4393), CWGAIN (Address 0x4395), DWGAIN (Address 0x4397), EWGAIN (Address 0x4399), and FWGAIN (Address 0x439B) registers control the active power gain calibration on the B through F current channels, respectively. The default value of the xWGAIN registers is 0x00000, which corresponds to no gain calibration. The xWGAIN registers can adjust the active power by up to ±100%. The output is scaled by −50% by writing 0xC00000 to the watt gain registers, and it is increased by +50% by writing 0x400000 to them. Equation 8 shows the relationship between the gain adjustment and the xWGAIN registers.

$$Active\ Power = Active\ Power_0 \times \left(\frac{xWGAIN}{0x800000} + 1\right) \quad (8)$$

Similar gain calibration registers are available for the reactive power. The reactive power on Current Channel A can be gain calibrated using the AVARGAIN (Address 0x439D) register. The BVARGAIN (Address 0x439F), CVARGAIN (Address 0x43A1), DVARGAIN (Address 0x43A3), EVARGAIN (Address 0x43A5), and FVARGAIN (Address 0x43A7) registers control the reactive power gain calibration on the B through F current channels, respectively. The xVARGAIN registers affect the reactive power in the same way that the xWGAIN registers affect the active power. Equation 9 shows the relationship between gain adjustment and the xVARGAIN registers.

$$Reactive\ Power = Reactive\ Power_0 \times \left(\frac{xVARGAIN}{0x800000} + 1\right) \quad (9)$$

ENERGY OFFSET CALIBRATION

The ADE7816 includes offset calibration registers for the active and reactive powers on all six channels. Offsets can exist in the power calculations due to crosstalk between channels on the PCB and in the ADE7816. The offset calibration allows these offsets to be removed to increase the accuracy of the measurement at low input levels.

The active power offset can be corrected on Current Channel A by adjusting the AWATTOS (Address 0x4392) register. The BWATTOS (Address 0x4394), CWATTOS (Address 0x4396), DWATTOS (Address 0x4398), EWATTOS (Address 0x439A), and FWATTOS (Address 0x439C) registers control the active power offset calibration on the B through F current channels, respectively. The xWATTOS registers are 24-bit, signed, twos complement registers with default values of 0. One LSB in the active power offset register is equivalent to 1 LSB in the active power multiplier output. With full-scale current and voltage inputs, the maximum power output is equal to 1FF6A6B = 33,516,139. At −80 dB down from full scale (active power scaled down 10^4 times), one LSB of the xWATTOS registers represents 0.0298%. Equation 10 shows the relationship between the xWATTOS registers and the active energy reading.

$$xWATTHR = xWATTHR_0 + \left(\frac{8000}{WTHR} \times xWATTOS \times AccumulationTime(s)\right) \quad (10)$$

Similar offset calibration registers are available for the reactive power. The reactive power on Current Channel A can be offset calibrated using the AVAROS (Address 0x439E). The BVAROS (Address 0x43A0), CVAROS (Address 0x43A2), DVAROS (Address 0x43A4), EVAROS (Address 0x43A6), and FVAROS (Address 0x43A8) registers control the reactive power gain calibration on the B through F current channels, respectively. The xVAROS registers affect the reactive powers in the same way that the xWATTOS registers affect the active power. Equation 11 shows the relationship between the xVAROS registers and the reactive energy reading.

$$xVARHR = xVARHR_0 + \left(\frac{8000}{VARTHR} \times xVAROS \times AccumulationTime(s)\right) \quad (11)$$