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# Polyphase Multifunction Energy Metering IC with Harmonic and Fundamental Information

Data Sheet

# ADE7854/ADE7858/ADE7868/ADE7878

## FEATURES

- Highly accurate; supports EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-22, and IEC 62053-23 standards
- Compatible with 3-phase, 3- or 4-wire (delta or wye), and other 3-phase services
- Supplies total (fundamental and harmonic) active, reactive (ADE7878, ADE7868, and ADE7858 only), and apparent energy, and fundamental active/reactive energy (ADE7878 only) on each phase and on the overall system
- Less than 0.1% error in active and reactive energy over a dynamic range of 1000 to 1 at $T_A$ = 25°C
- Less than 0.2% error in active and reactive energy over a dynamic range of 3000 to 1 at $T_A$ = 25°C
- Supports current transformer and di/dt current sensors
- Dedicated ADC channel for neutral current input (ADE7868 and ADE7878 only)
- Less than 0.1% error in voltage and current rms over a dynamic range of 1000 to 1 at $T_A$ = 25°C
- Supplies sampled waveform data on all three phases and on neutral current
- Selectable no load threshold levels for total and fundamental active and reactive powers, as well as for apparent powers
- Low power battery mode monitors phase currents for antitampering detection (ADE7868 and ADE7878 only)
- Battery supply input for missing neutral operation
- Phase angle measurements in both current and voltage channels with a typical 0.3° error
- Wide-supply voltage operation: 2.4 V to 3.7 V
- Reference: 1.2 V (drift ±5 ppm/°C typical) with external overdrive capability
- Single 3.3 V supply
- 40-lead lead frame chip scale package (LFCSP), Pb-free
- Operating temperature: −40°C to +85°C
- Flexible I²C, SPI, and HSDC serial interfaces

## APPLICATIONS

- Energy metering systems

## GENERAL DESCRIPTION

The ADE7854/ADE7858/ADE7868/ADE7878 are high accuracy, 3-phase electrical energy measurement ICs with serial interfaces and three flexible pulse outputs. The ADE78xx devices incorporate second-order sigma-delta (Σ-Δ) analog-to-digital converters (ADCs), a digital integrator, reference circuitry, and all of the signal processing required to perform total (fundamental and harmonic) active, reactive (ADE7878, ADE7868, and ADE7858), and apparent energy measurement and rms calculations, as well as fundamental-only active and reactive energy measurement (ADE7878) and rms calculations. A fixed function digital signal processor (DSP) executes this signal processing. The DSP program is stored in the internal ROM memory.

The ADE7854/ADE7858/ADE7868/ADE7878 are suitable for measuring active, reactive, and apparent energy in various 3-phase configurations, such as wye or delta services, with both three and four wires. The ADE78xx devices provide system calibration features for each phase, that is, rms offset correction, phase calibration, and gain calibration. The CF1, CF2, and CF3 logic outputs provide a wide choice of power information: total active, reactive, and apparent powers, or the sum of the current rms values, and fundamental active and reactive powers.

The ADE7854/ADE7858/ADE7868/ADE7878 contain waveform sample registers that allow access to all ADC outputs. The devices also incorporate power quality measurements, such as short duration low or high voltage detections, short duration high current variations, line voltage period measurement, and angles between phase voltages and currents. Two serial interfaces, SPI and I²C, can be used to communicate with the ADE78xx. A dedicated high speed interface, the high speed data capture (HSDC) port, can be used in conjunction with I²C to provide access to the ADC outputs and real-time power information. The ADE7854/ADE7858/ADE7868/ADE7878 also have two interrupt request pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$, to indicate that an enabled interrupt event has occurred. For the ADE7868/ADE7878, three specially designed low power modes ensure the continuity of energy accumulation when the ADE7868/ADE7878 is in a tampering situation. See Table 1 for a quick reference chart listing each part and its functions. The ADE78xx are available in the 40-lead LFCSP, Pb-free package.

**Table 1. Part Comparison**

| Part No. | WATT | VAR | IRMS, VRMS, and VA | di/dt | Fundamental WATT and VAR | Tamper Detect and Low Power Modes |
|---|---|---|---|---|---|---|
| ADE7878 | Yes | Yes | Yes | Yes | Yes | Yes |
| ADE7868 | Yes | Yes | Yes | Yes | No | Yes |
| ADE7858 | Yes | Yes | Yes | Yes | No | No |
| ADE7854 | Yes | No | Yes | Yes | No | No |

Rev. H
Document Feedback


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**2/10—Revision 0: Initial Version**

# FUNCTIONAL BLOCK DIAGRAMS

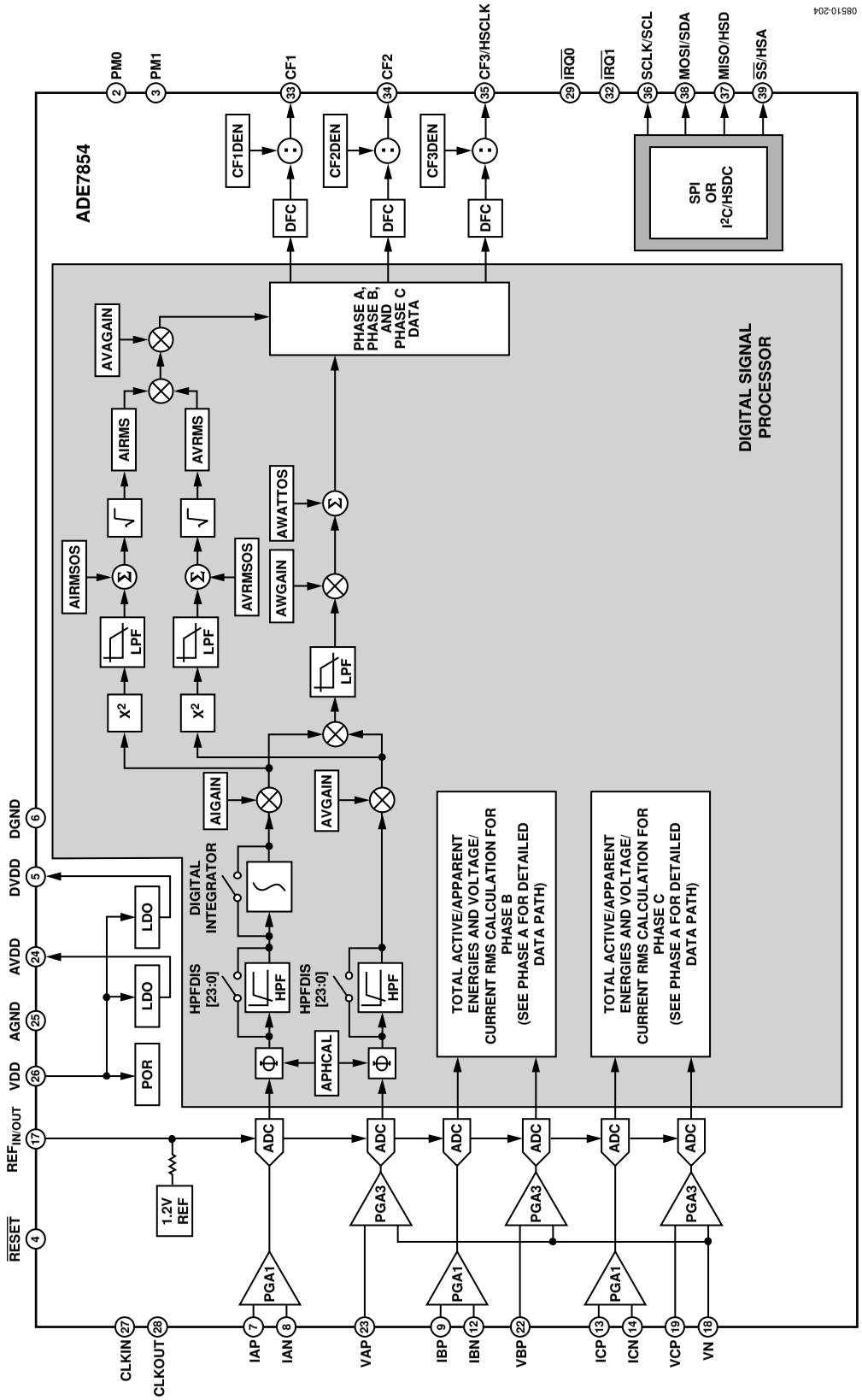


*Figure 1. ADE7854 Functional Block Diagram*

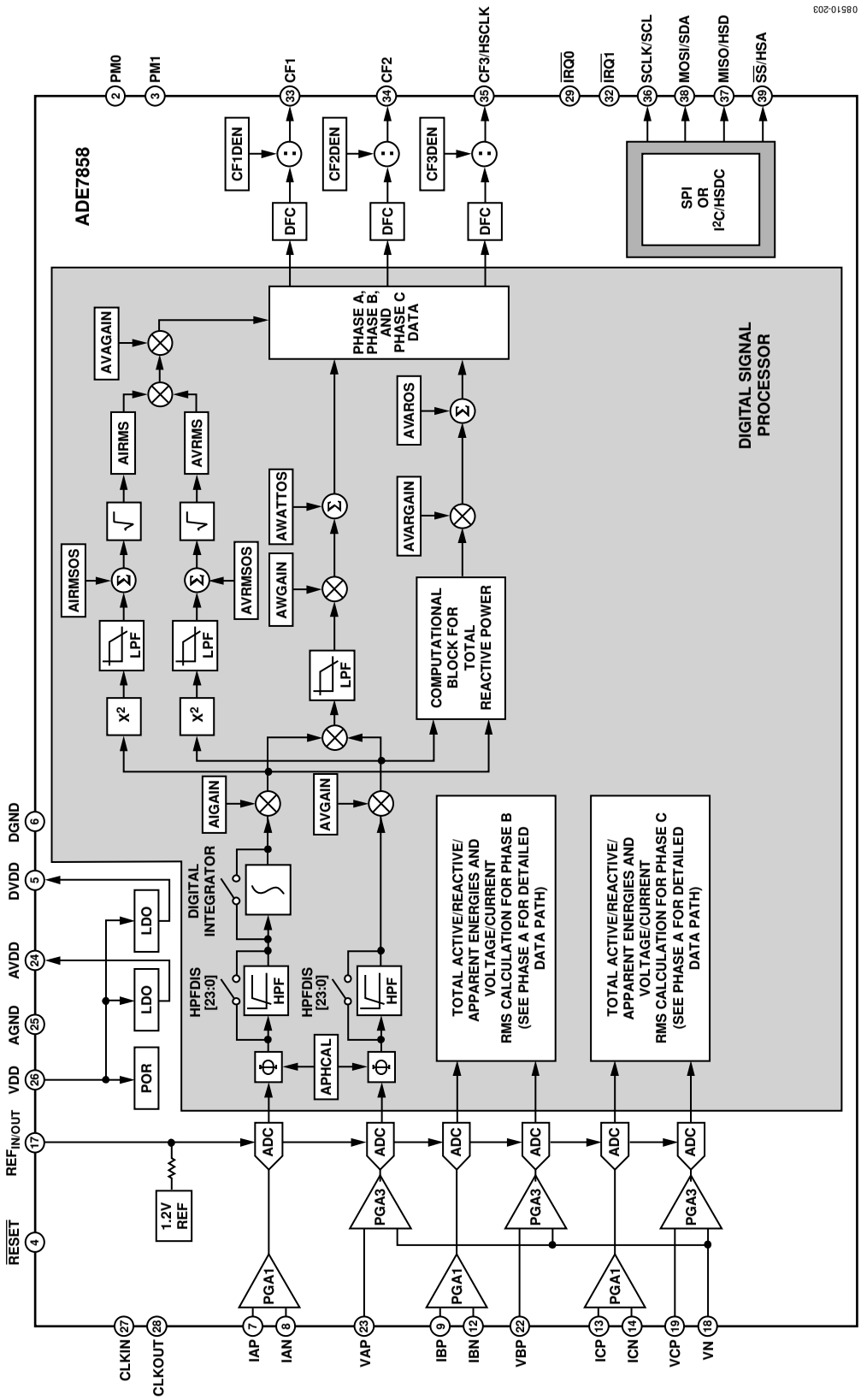


*Figure 2. ADE7858 Functional Block Diagram*

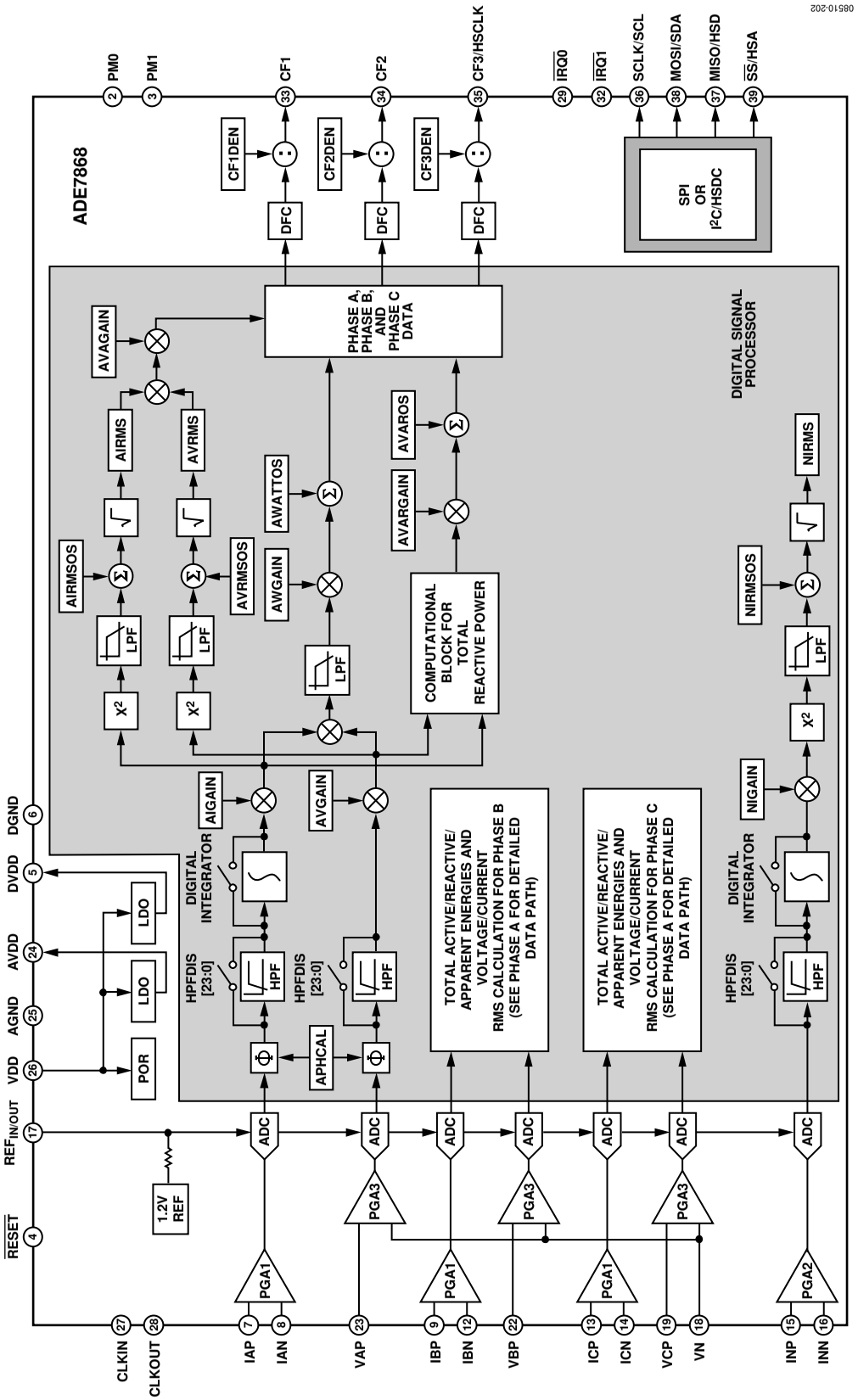


*Figure 3. ADE7868 Functional Block Diagram*

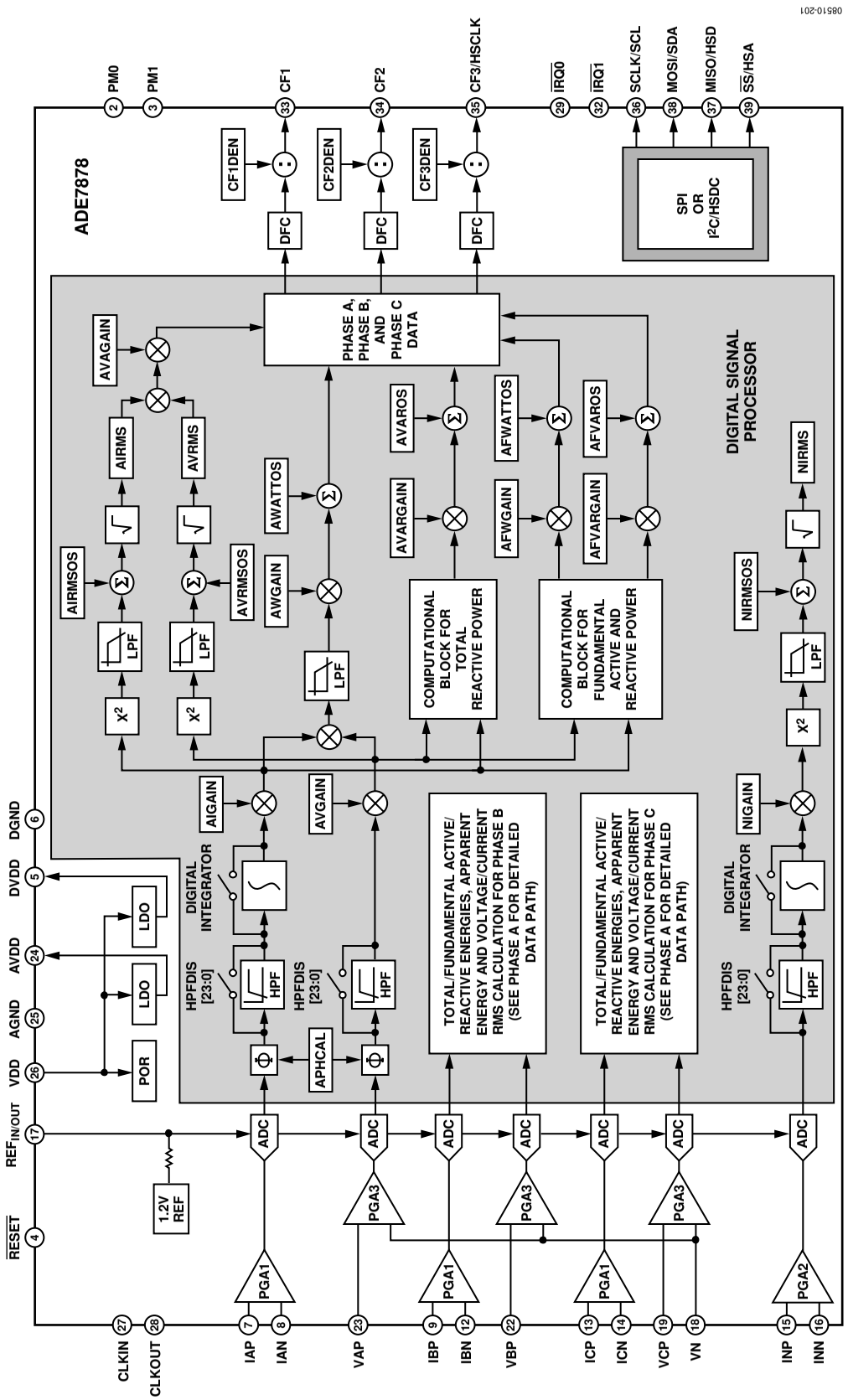


*Figure 4. ADE7878 Functional Block Diagram*

# SPECIFICATIONS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, $T_{MIN}$ to $T_{MAX}$ = −40°C to +85°C, $T_{TYP}$= 25°C.

**Table 2.**

| Parameter[1, 2] | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ACCURACY | | | | | |
| Active Energy Measurement | | | | | |
| Active Energy Measurement Error (per Phase) | | | | | |
| Total Active Energy | | 0.1 | | % | Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off |
| | | 0.2 | | % | Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off |
| | | 0.1 | | % | Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on |
| Fundamental Active Energy (ADE7878 Only) | | 0.1 | | % | Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off |
| | | 0.2 | | % | Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off |
| | | 0.1 | | % | Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on |
| AC Power Supply Rejection | | | | | VDD = 3.3 V + 120 mV rms/120 Hz/100 Hz, IPx = VPx = ±100 mV rms |
| Output Frequency Variation | | 0.01 | | % | |
| DC Power Supply Rejection | | | | | VDD = 3.3 V ± 330 mV dc; IPx = VPx = ±100 mV rms |
| Output Frequency Variation | | 0.01 | | % | |
| Total Active Energy Measurement Bandwidth | | 2 | | kHz | |
| REACTIVE ENERGY MEASUREMENT (ADE7858, ADE7868, AND ADE7878) | | | | | |
| Reactive Energy Measurement Error (per Phase) | | | | | |
| Total Reactive Energy | | 0.1 | | % | Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off |
| | | 0.2 | | % | Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off |
| | | 0.1 | | % | Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on |
| Fundamental Reactive Energy (ADE7878 Only) | | 0.1 | | % | Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off |
| | | 0.2 | | % | Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off |
| | | 0.1 | | % | Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on |
| AC Power Supply Rejection | | | | | VDD = 3.3 V + 120 mV rms/120 Hz/100 Hz, IPx = VPx = ±100 mV rms |
| Output Frequency Variation | | 0.01 | | % | |
| DC Power Supply Rejection | | | | | VDD = 3.3 V ± 330 mV dc; IPx = VPx = ±100 mV rms |
| Output Frequency Variation | | 0.01 | | % | |
| Total Reactive Energy Measurement Bandwidth | | 2 | | kHz | |
| RMS MEASUREMENTS | | | | | |
| I rms and V rms Measurement Bandwidth | | 2 | | kHz | |
| I rms and V rms Measurement Error (PSM0 Mode) | | 0.1 | | % | Over a dynamic range of 1000 to 1, PGA = 1 |

| Parameter[1, 2] | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| MEAN ABSOLUTE VALUE (MAV) MEASUREMENT (ADE7868 AND ADE7878) | | | | | |
| I mav Measurement Bandwidth (PSM1 Mode) | | 260 | | Hz | |
| I mav Measurement Error (PSM1 Mode) | | 0.5 | | % | Over a dynamic range of 100 to 1, PGA = 1, 2, 4, 8 |
| ANALOG INPUTS | | | | | |
| Maximum Signal Levels | | | ±500 | mV peak | PGA = 1, differential inputs between the following pins: IAP and IAN, IBP and IBN, ICP and ICN; single-ended inputs between the following pins: VAP and VN, VBP and VN, VCP, and VN |
| Input Impedance (DC) | | | | | |
| IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, and VCP Pins | 400 | | | kΩ | |
| VN Pin | 130 | | | kΩ | |
| ADC Offset | | −24 | | mV | PGA = 1, uncalibrated error, see the Terminology section |
| Gain Error | | ±4 | | % | External 1.2 V reference |
| WAVEFORM SAMPLING | | | | | Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS |
| Current and Voltage Channels | | | | | See the Waveform Sampling Mode section |
| Signal-to-Noise Ratio, SNR | | 74 | | dB | PGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology section |
| Signal-to-Noise-and-Distortion Ratio, SINAD | | 74 | | dB | PGA = 1; fundamental frequency: 45 Hz to 65 Hz, see the Terminology section |
| Bandwidth (−3 dB) | | 2 | | kHz | |
| TIME INTERVAL BETWEEN PHASES | | | | | |
| Measurement Error | | 0.3 | | Degrees | Line frequency = 45 Hz to 65 Hz, HPF on |
| CF1, CF2, CF3 PULSE OUTPUTS | | | | | |
| Maximum Output Frequency | | 8 | | kHz | WTHR = VARTHR = VATHR = PMAX = 33,516,139 |
| Duty Cycle | | 50 | | % | If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1 |
| | | (1 + 1/CFDEN) × 50% | | | If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1 |
| Active Low Pulse Width | | 80 | | ms | If CF1, CF2, or CF3 frequency < 6.25 Hz |
| Jitter | | 0.04 | | % | For CF1, CF2, or CF3 frequency = 1 Hz and nominal phase currents are larger than 10% of full scale |
| REFERENCE INPUT | | | | | |
| $REF_{IN/OUT}$ Input Voltage Range | 1.1 | | 1.3 | V | Minimum = 1.2 V − 8%; maximum = 1.2 V + 8% |
| Input Capacitance | | | 10 | pF | |
| ON-CHIP REFERENCE | | | | | Nominal 1.2 V at the $REF_{IN/OUT}$ pin at $T_A$ = 25°C |
| PSM0 and PSM1 Modes | | | | | |
| Temperature Coefficient | −50 | ±5 | +50 | ppm/°C | Drift across the entire temperature range of −40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more details |
| CLKIN | | | | | All specifications CLKIN of 16.384 MHz. See the Crystal Circuit section for more details. |
| Input Clock Frequency | 16.22 | 16.384 | 16.55 | MHz | |
| LOGIC INPUTS—MOSI/SDA, SCLK/SCL, $\overline{SS}$, $\overline{RESET}$, PM0, AND PM1 | | | | | |
| Input High Voltage, $V_{INH}$ | 2.0 | | | V | VDD = 3.3 V ± 10% |
| Input Low Voltage, $V_{INL}$ | | | 0.8 | V | VDD = 3.3 V ± 10% |
| Input Current, $I_{IN}$ | | | −8.7 | µA | Input = 0 V, VDD = 3.3 V |
| | | | 3 | µA | Input = VDD = 3.3 V |
| Input Capacitance, $C_{IN}$ | | 10 | | pF | |

| Parameter[1, 2] | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| LOGIC OUTPUTS—$\overline{IRQ0}$, $\overline{IRQ1}$, MISO/HSD | | | | | VDD = 3.3 V ± 10% |
| Output High Voltage, $V_{OH}$ | 2.4 | | | V | VDD = 3.3 V ± 10% |
| $I_{SOURCE}$ | | | 800 | µA | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | VDD = 3.3 V ± 10% |
| $I_{SINK}$ | | | 2 | mA | |
| CF1, CF2, CF3/HSCLK | | | | | |
| Output High Voltage, $V_{OH}$ | 2.4 | | | V | VDD = 3.3 V ± 10% |
| $I_{SOURCE}$ | | | 500 | µA | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | VDD = 3.3 V ± 10% |
| $I_{SINK}$ | | | 2 | mA | |
| POWER SUPPLY | | | | | For specified performance |
| PSM0 Mode | | | | | |
| VDD Pin | 2.97 | | 3.63 | V | Minimum = 3.3 V − 10%; maximum = 3.3 V + 10% |
| $I_{DD}$ | | 24.4 | 27.2 | mA | |
| PSM1 and PSM2 Modes (ADE7868 and ADE7878) | | | | | |
| VDD Pin | 2.4 | | 3.7 | V | |
| $I_{DD}$ | | | | | |
| PSM1 Mode | | 6.0 | | mA | |
| PSM2 Mode | | 0.2 | | mA | |
| PSM3 Mode | | | | | |
| VDD Pin | 2.4 | | 3.7 | V | |
| $I_{DD}$ in PSM3 Mode | | 1.7 | | µA | |

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for a definition of the parameters.

## TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, $T_{MIN}$ to $T_{MAX}$ = −40°C to +85°C. Note that dual function pin names are referenced by the relevant function only within the timing tables and diagrams; see the Pin Configuration and Function Descriptions section for full pin mnemonics and descriptions.

**Table 3. I²C-Compatible Interface Timing Parameter**

| | | Standard Mode | | Fast Mode | | |
|---|---|---|---|---|---|---|
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| SCL Clock Frequency | $f_{SCL}$ | 0 | 100 | 0 | 400 | kHz |
| Hold Time (Repeated) Start Condition | $t_{HD;STA}$ | 4.0 | | 0.6 | | µs |
| Low Period of SCL Clock | $t_{LOW}$ | 4.7 | | 1.3 | | µs |
| High Period of SCL Clock | $t_{HIGH}$ | 4.0 | | 0.6 | | µs |
| Set-Up Time for Repeated Start Condition | $t_{SU;STA}$ | 4.7 | | 0.6 | | µs |
| Data Hold Time | $t_{HD;DAT}$ | 0 | 3.45 | 0 | 0.9 | µs |
| Data Setup Time | $t_{SU;DAT}$ | 250 | | 100 | | ns |
| Rise Time of Both SDA and SCL Signals | $t_R$ | | 1000 | 20 | 300 | ns |
| Fall Time of Both SDA and SCL Signals | $t_F$ | | 300 | 20 | 300 | ns |
| Setup Time for Stop Condition | $t_{SU;STO}$ | 4.0 | | 0.6 | | µs |
| Bus Free Time Between a Stop and Start Condition | $t_{BUF}$ | 4.7 | | 1.3 | | µs |
| Pulse Width of Suppressed Spikes | $t_{SP}$ | N/A[1] | | | 50 | ns |

[1] N/A means not applicable.

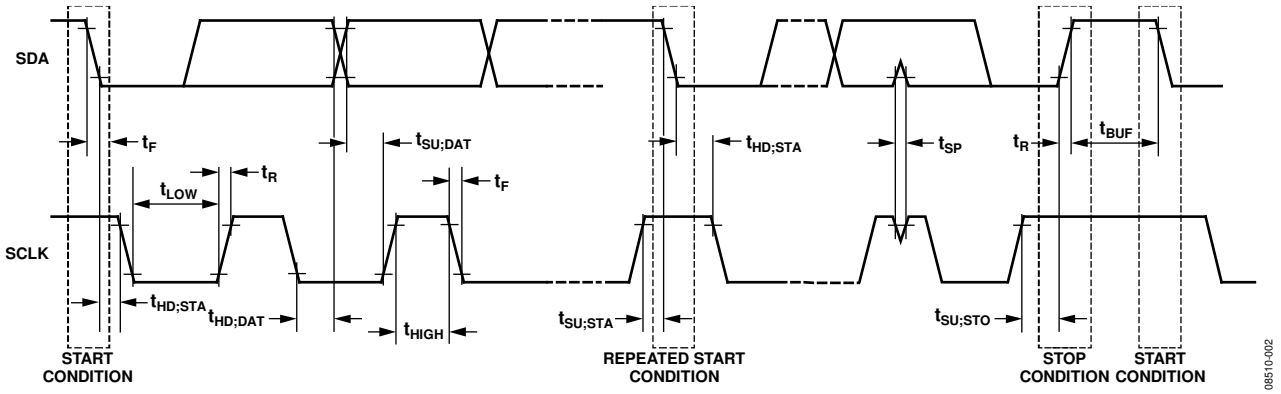


*Figure 5. I²C-Compatible Interface Timing*

**Table 4. SPI Interface Timing Parameters**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| $\overline{SS}$ to SCLK Edge | $t_{SS}$ | 50 | | ns |
| SCLK Period | | 0.4 | 4000[1] | µs |
| SCLK Low Pulse Width | $t_{SL}$ | 175 | | ns |
| SCLK High Pulse Width | $t_{SH}$ | 175 | | ns |
| Data Output Valid After SCLK Edge | $t_{DAV}$ | | 100 | ns |
| Data Input Setup Time Before SCLK Edge | $t_{DSU}$ | 100 | | ns |
| Data Input Hold Time After SCLK Edge | $t_{DHD}$ | 5 | | ns |
| Data Output Fall Time | $t_{DF}$ | | 20 | ns |
| Data Output Rise Time | $t_{DR}$ | | 20 | ns |
| SCLK Rise Time | $t_{SR}$ | | 20 | ns |
| SCLK Fall Time | $t_{SF}$ | | 20 | ns |
| MISO Disable After $\overline{SS}$ Rising Edge | $t_{DIS}$ | | 200 | ns |
| $\overline{SS}$ High After SCLK Edge | $t_{SFS}$ | 0 | | ns |

[1] Guaranteed by design.

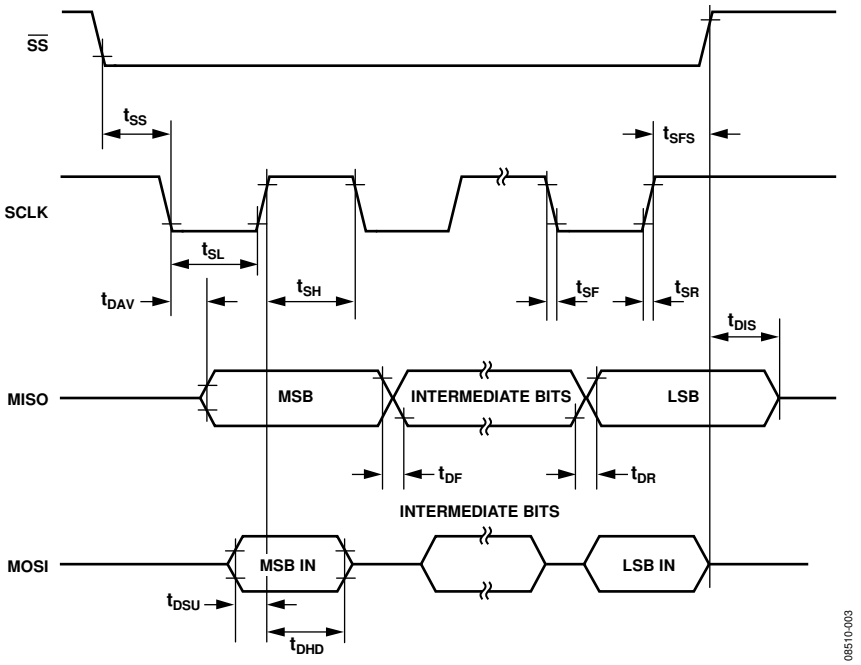


*Figure 6. SPI Interface Timing*

**Table 5. HSDC Interface Timing Parameter**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| HSA to HSCLK Edge | $t_{SS}$ | 0 | | ns |
| HSCLK Period | | 125 | | ns |
| HSCLK Low Pulse Width | $t_{SL}$ | 50 | | ns |
| HSCLK High Pulse Width | $t_{SH}$ | 50 | | ns |
| Data Output Valid After HSCLK Edge | $t_{DAV}$ | | 40 | ns |
| Data Output Fall Time | $t_{DF}$ | | 20 | ns |
| Data Output Rise Time | $t_{DR}$ | | 20 | ns |
| HSCLK Rise Time | $t_{SR}$ | | 10 | ns |
| HSCLK Fall Time | $t_{SF}$ | | 10 | ns |
| HSD Disable After HSA Rising Edge | $t_{DIS}$ | 5 | | ns |
| HSA High After HSCLK Edge | $t_{SFS}$ | 0 | | ns |

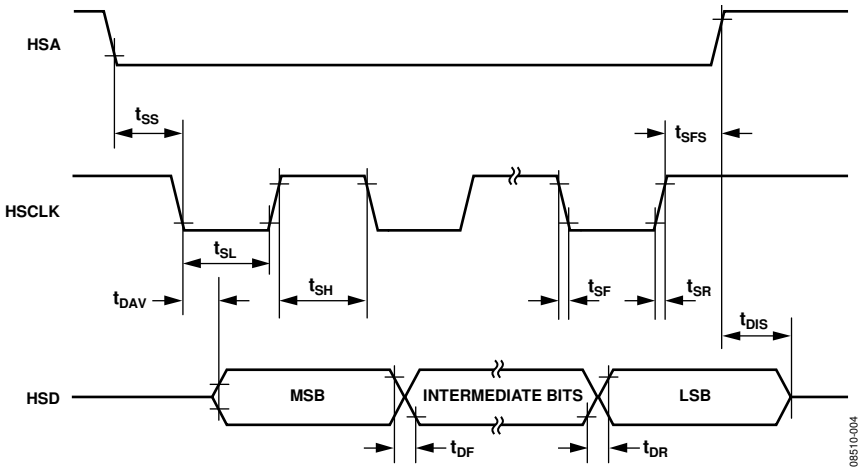


*Figure 7. HSDC Interface Timing*

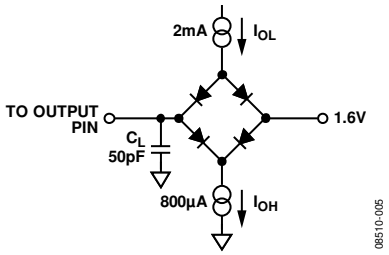


*Figure 8. Load Circuit for Timing Specifications*

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 6.**

| Parameter | Rating |
|---|---|
| VDD to AGND | −0.3 V to +3.7 V |
| VDD to DGND | −0.3 V to +3.7 V |
| Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, VCP, VN | −2 V to +2 V |
| Analog Input Voltage to INP and INN | −2 V to +2 V |
| Reference Input Voltage to AGND | −0.3 V to VDD + 0.3 V |
| Digital Input Voltage to DGND | −0.3 V to VDD + 0.3 V |
| Digital Output Voltage to DGND | −0.3 V to VDD + 0.3 V |
| Operating Temperature | |
| Industrial Range | −40°C to +85°C |
| Storage Temperature Range | −65°C to +150°C |
| Lead Temperature (Soldering, 10 sec) | 300°C |

Note that, regarding the temperature profile used in soldering RoHS compliant parts, Analog Devices advises that reflow profiles should conform to J-STD 20 from JEDEC. Refer to www.jedec.org for the latest revision.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$ is specified equal to 29.3°C/W; $\theta_{JC}$ is specified equal to 1.8°C/W.

**Table 7. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 40-Lead LFCSP | 29.3 | 1.8 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

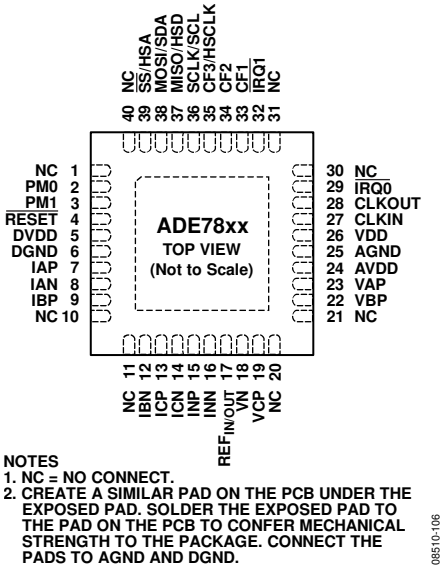


*Figure 9. Pin Configuration*

**Table 8. Pin Function Descriptions**

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1, 10, 11, 20, 21, 30, 31, 40 | NC | No Connect. These pins are not connected internally. It is recommended to ground these pins. |
| 2 | PM0 | Power Mode Pin 0. This pin, combined with PM1, defines the power mode of the ADE7854/ADE7858/ADE7868/ADE7878, as described in Table 9. |
| 3 | PM1 | Power Mode Pin 1. This pin defines the power mode of the ADE7854/ADE7858/ADE7868/ADE7878 when combined with PM0, as described in Table 9. |
| 4 | $\overline{\text{RESET}}$ | Reset Input, Active Low. In PSM0 mode, this pin should stay low for at least 10 µs to trigger a hardware reset. |
| 5 | DVDD | 2.5 V output of the digital low dropout regulator (LDO). Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin. |
| 6 | DGND | Ground Reference. This pin provides the ground reference for the digital circuitry. |
| 7, 8 | IAP, IAN | Analog Inputs for Current Channel A. This channel is used with the current transducers and is referenced in this document as Current Channel A. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel B and Channel C. |
| 9, 12 | IBP, IBN | Analog Inputs for Current Channel B. This channel is used with the current transducers and is referenced in this document as Current Channel B. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel C and Channel A. |
| 13, 14 | ICP, ICN | Analog Inputs for Current Channel C. This channel is used with the current transducers and is referenced in this document as Current Channel C. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel A and Channel B. |
| 15, 16 | INP, INN | Analog Inputs for Neutral Current Channel N. This channel is used with the current transducers and is referenced in this document as Current Channel N. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA, different from the ones found on the A, B, and C channels. The neutral current channel is available in the ADE7878 and ADE7868. In the ADE7858 and ADE7854, connect these pins to AGND. |
| 17 | $\text{REF}_{\text{IN/OUT}}$ | This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. An external reference source with 1.2 V ± 8% can also be connected at this pin. In either case, decouple this pin to AGND with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor. After reset, the on-chip reference is enabled. |

| Pin No. | Mnemonic | Description |
|---|---|---|
| 18, 19, 22, 23 | VN, VCP, VBP, VAP | Analog Inputs for the Voltage Channel. This channel is used with the voltage transducer and is referenced as the voltage channel in this document. These inputs are single-ended voltage inputs with a maximum signal level of ±0.5 V with respect to VN for specified operation. This channel also has an internal PGA. |
| 24 | AVDD | 2.5 V output of the analog low dropout regulator (LDO). Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin. |
| 25 | AGND | Ground Reference. This pin provides the ground reference for the analog circuitry. Tie this pin to the analog ground plane or to the quietest ground reference in the system. Use this quiet ground reference for all analog circuitry, for example, antialiasing filters, current, and voltage transducers. |
| 26 | VDD | Supply Voltage. This pin provides the supply voltage. In PSM0 (normal power mode), maintain the supply voltage at 3.3 V ± 10% for specified operation. In PSM1 (reduced power mode), PSM2 (low power mode), and PSM3 (sleep mode), when the ADE7868/ADE7878 is supplied from a battery, maintain the supply voltage between 2.4 V and 3.7 V. Decouple this pin to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. The only modes available on the ADE7858 and ADE7854 are the PSM0 and PSM3 power modes. |
| 27 | CLKIN | Master Clock. An external clock can be provided at this logic input. Alternatively, a crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7854/ADE7858/ADE7868/ADE7878. The clock frequency for specified operation is 16.384 MHz. See the Crystal Circuit section for details on choosing a suitable crystal. |
| 28 | CLKOUT | A crystal can be connected across this pin and CLKIN (as previously described with Pin 27 in this table) to provide a clock source for the ADE7854/ADE7858/ADE7868/ADE7878. |
| 29, 32 | $\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$ | Interrupt Request Outputs. These are active low logic outputs. See the Interrupts section for a detailed presentation of the events that can trigger interrupts. |
| 33, 34, 35 | CF1, CF2, CF3/HSCLK | Calibration Frequency (CF) Logic Outputs. These outputs provide power information based on the CF1SEL[2:0], CF2SEL[2:0], and CF3SEL[2:0] bits in the CFMODE register. These outputs are used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the CF1DEN, CF2DEN, and CF3DEN registers, respectively (see the Energy-to-Frequency Conversion section). CF3 is multiplexed with the serial clock output of the HSDC port. |
| 36 | SCLK/SCL | Serial Clock Input for SPI Port/Serial Clock Input for $I^2C$ Port. All serial data transfers are synchronized to this clock (see the Serial Interfaces section). This pin has a Schmidt trigger input for use with a clock source that has a slow edge transition time, for example, opto-isolator outputs. |
| 37 | MISO/HSD | Data Out for SPI Port/Data Out for HSDC Port. |
| 38 | MOSI/SDA | Data In for SPI Port/Data Out for $I^2C$ Port. |
| 39 | $\overline{\text{SS}}$/HSA | Slave Select for SPI Port/HSDC Port Active. |
| EP | Exposed Pad | Create a similar pad on the PCB under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package. Connect the pads to AGND and DGND. |

# TYPICAL PERFORMANCE CHARACTERISTICS

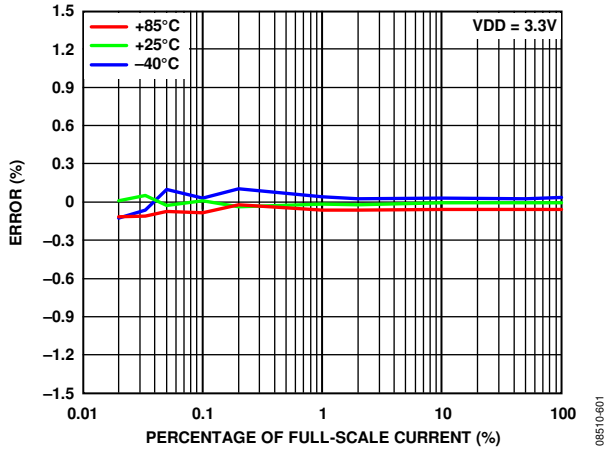


Figure 10. Total Active Energy Error As Percentage of Reading (Gain = +1, Power Factor = 1) over Temperature with Internal Reference and Integrator Off

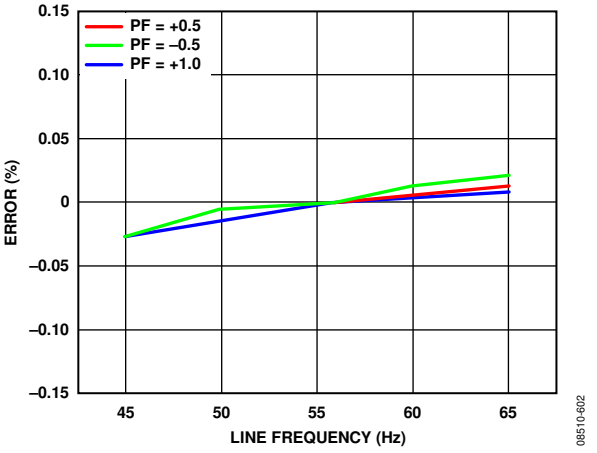


Figure 11. Total Active Energy Error As Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

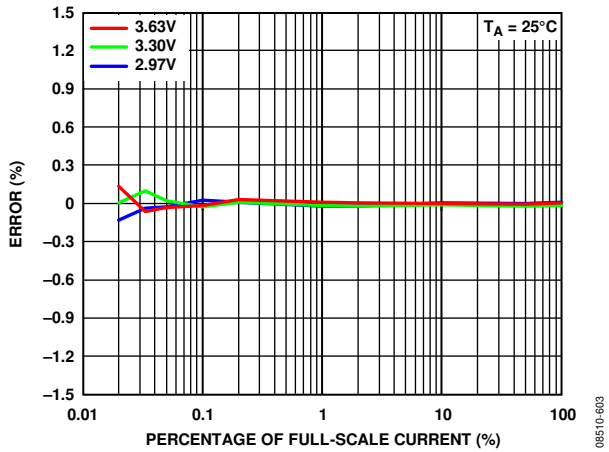


Figure 12. Total Active Energy Error As Percentage of Reading (Gain = +1, Power Factor = 1) over Power Supply with Internal Reference and Integrator Off

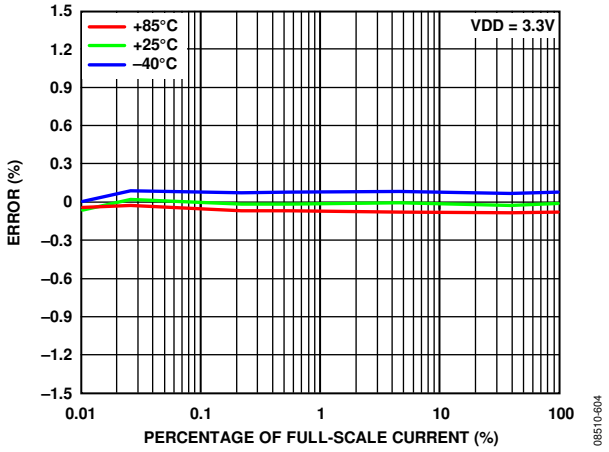


Figure 13. Total Active Energy Error As Percentage of Reading (Gain = +16, Power Factor = 1) over Temperature with Internal Reference and Integrator On

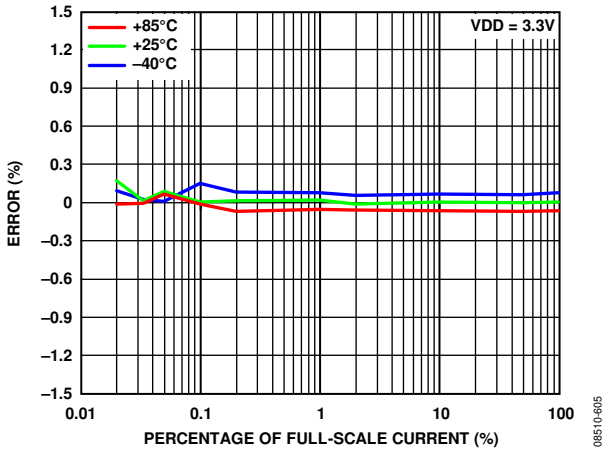


Figure 14. Total Reactive Energy Error As Percentage of Reading (Gain = +1, Power Factor = 0) over Temperature with Internal Reference and Integrator Off

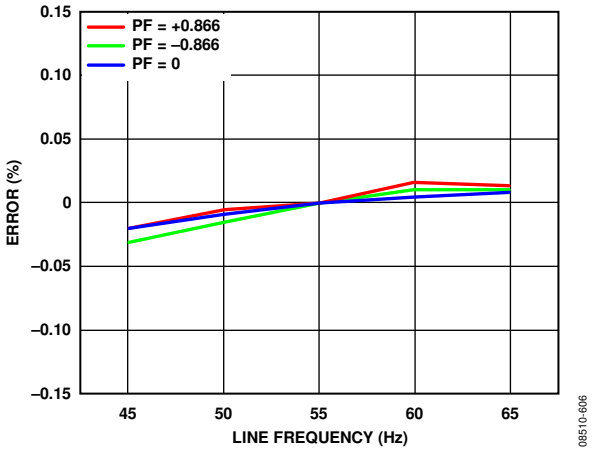


Figure 15. Total Reactive Energy Error As Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

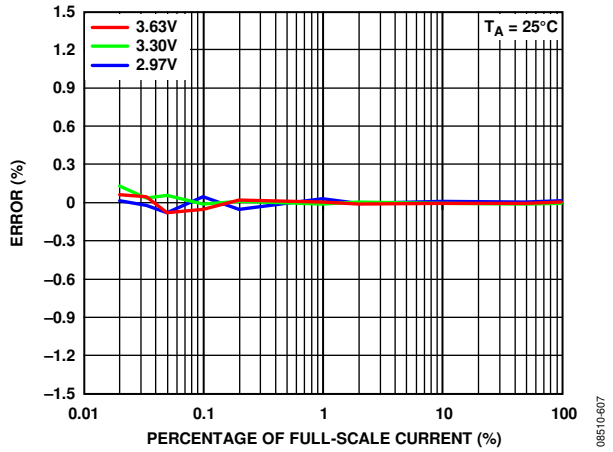


Figure 16. Total Reactive Energy Error As Percentage of Reading (Gain = +1, Power Factor = 0) over Power Supply with Internal Reference and Integrator Off

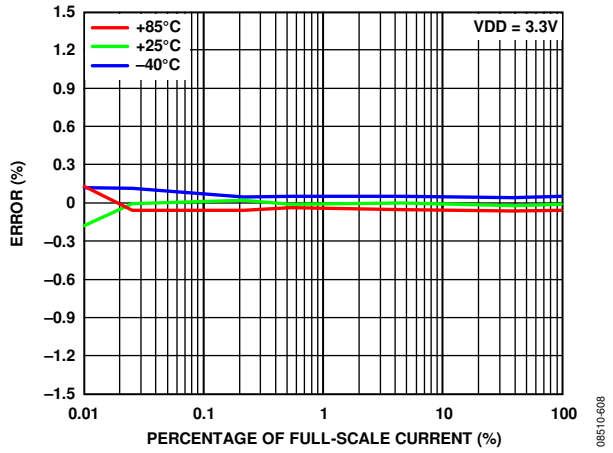


Figure 17. Total Reactive Energy Error As Percentage of Reading (Gain = +16, Power Factor = 0) over Temperature with Internal Reference and Integrator On

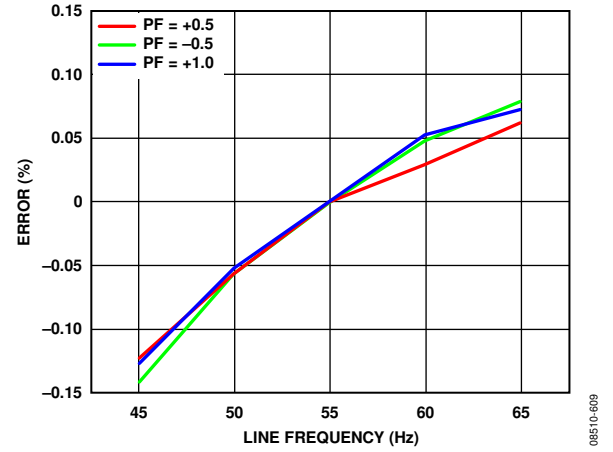


Figure 18. Fundamental Active Energy Error As Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

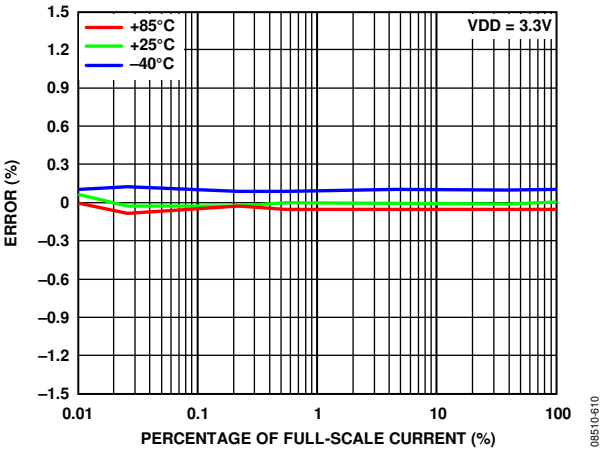


Figure 19. Fundamental Active Energy Error As Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On

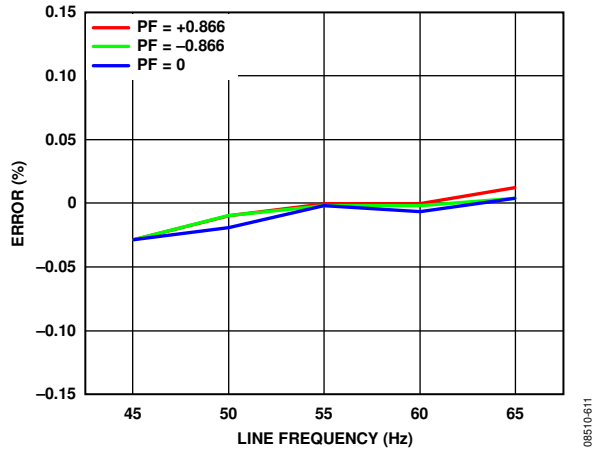


Figure 20. Fundamental Reactive Energy Error As Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

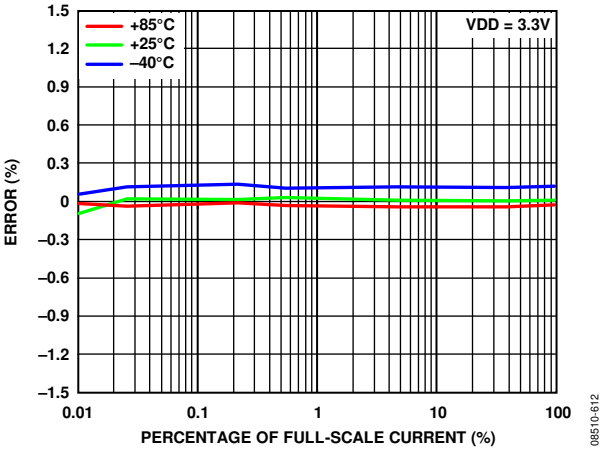


Figure 21. Fundamental Reactive Energy Error As Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On

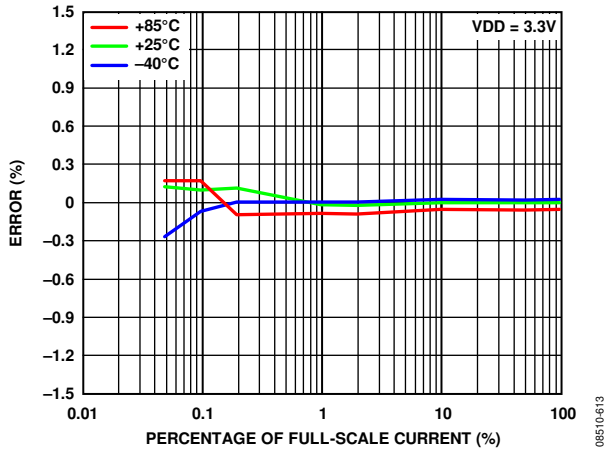


*Figure 22. IRMS Error as Percentage of Reading (Gain = +1, Power Factor = 1) over Temperature with Internal Reference and Integrator Off*

# TEST CIRCUIT

Note that in Figure 23, the PM1 and PM0 pins are pulled up internally to 3.3 V. Select the mode of operation by using a microcontroller to programmatically change the pin values.

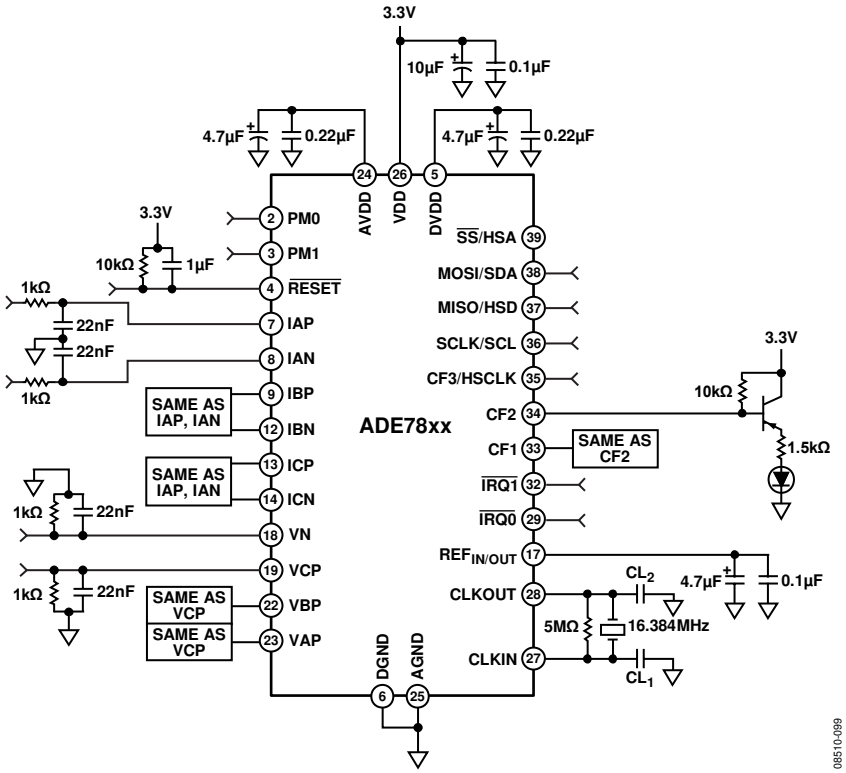


*Figure 23. Test Circuit*

# TERMINOLOGY

**Measurement Error**

The error associated with the energy measurement made by the ADE7854/ADE7858/ADE7868/ADE7878 is defined by

$$Measurement\ Error = \frac{Energy\ Registered\ by\ ADE78xx - True\ Energy}{True\ Energy} \times 100\% \quad (1)$$

**Power Supply Rejection (PSR)**

This quantifies the ADE7854/ADE7858/ADE7868/ADE7878 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at twice the fundamental frequency) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see the Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±10%. Any error introduced is expressed as a percentage of the reading.

**ADC Offset Error**

This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection However, the HPF removes the offset from the current and voltage channels and the power calculation remains unaffected by this offset.

**Gain Error**

The gain error in the ADCs of the ADE7854/ADE7858/ADE7868/ADE7878 is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC section and the Voltage Channel ADC section). The difference is expressed as a percentage of the ideal code.

**CF Jitter**

The period of pulses at one of the CF1, CF2, or CF3 pins is continuously measured. The maximum, minimum, and average values of four consecutive pulses are computed as follows:

$$Maximum = max(Period_0, Period_1, Period_2, Period_3)$$

$$Minimum = min(Period_0, Period_1, Period_2, Period_3)$$

$$Average = \frac{Period_0 + Period_1 + Period_2 + Period_3}{4}$$

The CF jitter is then computed as

$$CF_{JITTER} = \frac{Maximum - Minimum}{Average} \times 100\% \quad (2)$$

**Signal-to-Noise Ratio (SNR)**

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below 2 kHz, excluding harmonics and dc. The input signal contains only the fundamental component. The spectral components are calculated over a 2 sec window. The value for SNR is expressed in decibels.

**Signal-to-(Noise and Distortion) Ratio (SINAD)**

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below 2 kHz, including harmonics but excluding dc. The input signal contains only the fundamental component. The spectral components are calculated over a 2 sec window. The value for SINAD is expressed in decibels.

# POWER MANAGEMENT

The ADE7868/ADE7878 have four modes of operation, determined by the state of the PM0 and PM1 pins (see Table 9). The ADE7854/ADE7858 have two modes of operation. These pins provide complete control of the ADE7854/ADE7858/ADE7868/ADE7878 operation and can easily be connected to an external microprocessor I/O. The PM0 and PM1 pins have internal pull-up resistors. See Table 11 and Table 12 for a list of actions that are recommended before and after setting a new power mode.

**Table 9. Power Supply Modes**

| Power Supply Modes | PM1 | PM0 |
|---|---|---|
| PSM0, Normal Power Mode | 0 | 1 |
| PSM1, Reduced Power Mode[1] | 0 | 0 |
| PSM2, Low Power Mode[1] | 1 | 0 |
| PSM3, Sleep Mode | 1 | 1 |

[1] Available in the ADE7868 and ADE7878.

## PSM0—NORMAL POWER MODE (ALL PARTS)

In PSM0 mode, the ADE7854/ADE7858/ADE7868/ADE7878 are fully functional. The PM0 pin is set to high and the PM1 pin is set to low for the ADE78xx to enter this mode. If the ADE78xx is in one of PSM1, PSM2, or PSM3 modes and is switched into PSM0 mode, then all control registers take the default values with the exception of the threshold register, LPOILVL, which is used in PSM2 mode, and the CONFIG2 register, both of which maintain their values.

The ADE7854/ADE7858/ADE7868/ADE7878 signal the end of the transition period by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is 0 during the transition period and becomes 1 when the transition is finished. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set back to high by writing to the STATUS1 register with the corresponding bit set to 1. Bit 15 (RSTDONE) in the interrupt mask register does not have any functionality attached even if the $\overline{\text{IRQ1}}$ pin goes low when Bit 15 (RSTDONE) in the STATUS1 register is set to 1. This makes the RSTDONE interrupt unmaskable.

## PSM1—REDUCED POWER MODE (ADE7868, ADE7878 ONLY)

The reduced power mode, PSM1, is available on the ADE7868 and ADE7878 only. In this mode, the ADE7868/ADE7878 measure the mean absolute values (mav) of the 3-phase currents and store the results in the AIMAV, BIMAV, and CIMAV 20-bit registers. This mode is useful in missing neutral cases in which the voltage supply of the ADE7868 or ADE7878 is provided by an external battery. The serial ports, $I^2C$ or SPI, are enabled in this mode; the active port can be used to read the AIMAV, BIMAV, and CIMAV registers. It is not recommended to read any of the other registers because their values are not guaranteed in this mode. Similarly, a write operation is not taken into account by the ADE7868/ADE7878 in this mode.

In summary, in this mode, it is not recommended to access any register other than AIMAV, BIMAV, and CIMAV. The circuit that measures these estimates of rms values is also active during PSM0; therefore, its calibration can be completed in either PSM0 mode or in PSM1 mode. Note that the ADE7868 and ADE7878 do not provide any register to store or process the corrections resulting from the calibration process. The external microprocessor stores the gain values in connection with these measurements and uses them during PSM1 (see the Current Mean Absolute Value Calculation—ADE7868 and ADE7878 Only section for more details on the xIMAV registers).

The 20-bit mean absolute value measurements done in PSM1, although available also in PSM0, are different from the rms measurements of phase currents and voltages executed only in PSM0 and stored in the xIRMS and xVRMS 24-bit registers. See the Current Mean Absolute Value Calculation—ADE7868 and ADE7878 Only section for details.

If the ADE7868/ADE7878 is set in PSM1 mode while still in the PSM0 mode, the ADE7868/ADE7878 immediately begin the mean absolute value calculations without any delay. The xIMAV registers are accessible at any time; however, if the ADE7878 or ADE7868 is set in PSM1 mode while still in PSM2 or PSM3 modes, the ADE7868/ADE7878 signal the start of the mean absolute value computations by triggering the $\overline{\text{IRQ1}}$ pin low. The xIMAV registers can be accessed only after this moment.

## PSM2—LOW POWER MODE (ADE7868, ADE7878 ONLY)

The low power mode, PSM2, is available on the ADE7868 and ADE7878 only. In this mode, the ADE7868/ADE7878 compare all phase currents against a threshold for a period of 0.02 × (LPLINE[4:0] + 1) seconds, independent of the line frequency. LPLINE[4:0] are Bits[7:3] of the LPOILVL register (see Table 10).

**Table 10. LPOILVL Register**

| Bit | Mnemonic | Default | Description |
|---|---|---|---|
| [2:0] | LPOIL[2:0] | 111 | Threshold is put at a value corresponding to full scale multiplied by LPOIL/8. |
| [7:3] | LPLINE[4:0] | 00000 | The measurement period is (LPLINE[4:0] + 1)/50 sec. |

The threshold is derived from Bits[2:0] (LPOIL[2:0]) of the LPOILVL register as LPOIL[2:0]/8 of full scale. Every time one phase current becomes greater than the threshold, a counter is incremented. If every phase counter remains below LPLINE[4:0] + 1 at the end of the measurement period, then the $\overline{\text{IRQ0}}$ pin is triggered low. If a single phase counter becomes greater or equal to LPLINE[4:0] + 1 at the end of the measurement period, the $\overline{\text{IRQ1}}$ pin is triggered low. Figure 24 illustrates how the ADE7868/ADE7878 behave in PSM2 mode when LPLINE[4:0] = 2 and LPOIL[2:0] = 3. The test period is three 50 Hz cycles (60 ms), and the Phase A current rises above the LPOIL[2:0] threshold three times. At the end of the test period, the $\overline{\text{IRQ1}}$ pin is triggered low.

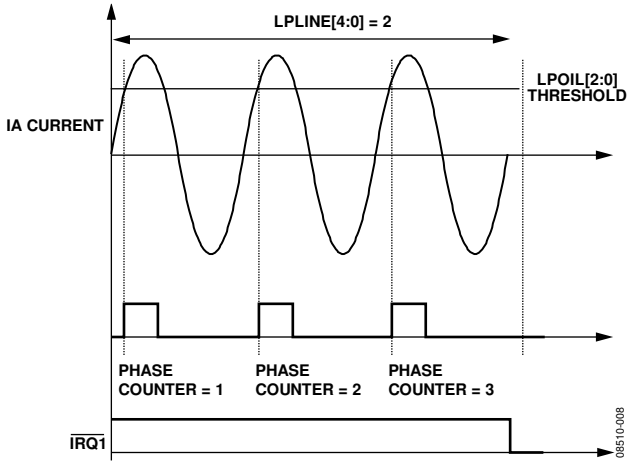


*Figure 24. PSM2 Mode Triggering $\overline{\text{IRQ1}}$ Pin for LPLINE[4:0] = 2 (50 Hz Systems)*

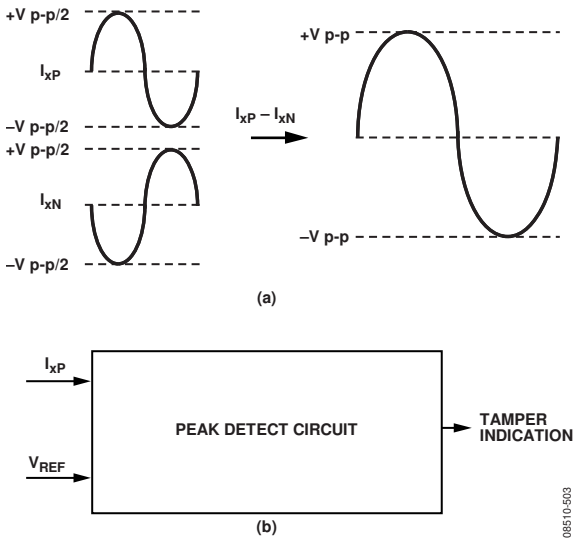


*Figure 25. PSM2 Low Power Mode Peak Detection*

The PSM2 level threshold comparison works based on a peak detection methodology. The peak detect circuit makes the comparison based on the positive terminal current channel input, $I_{AP}$, $I_{BP}$, and $I_{CP}$ (see Figure 25). In case of differential inputs being applied to the current channels, Figure 25 shows the differential antiphase signals at each of the current input terminals, $I_{xP}$ and $I_{xN}$, and the net differential current, $I_{xP} - I_{xN}$.

The I²C or SPI port is not functional during this mode. The PSM2 mode reduces the power consumption required to monitor the currents when there is no voltage input and the voltage supply of the ADE7868/ADE7878 is provided by an external battery. If the $\overline{\text{IRQ0}}$ pin is triggered low at the end of a measurement period, this signifies all phase currents stayed below threshold and, therefore, there is no current flowing through the system. At this point, the external microprocessor sets the ADE7868/ADE7878 into Sleep Mode PSM3. If the $\overline{\text{IRQ1}}$ pin is triggered low at the end of the measurement period, this signifies that at least one current input is above the defined threshold and current is flowing through the system, although no voltage is present at the ADE7868/ADE7878 pins. This situation is often called missing neutral and is considered a tampering situation, at which point the external microprocessor sets the ADE7868/ADE7878into PSM1 mode, measures the mean absolute values of phase currents, and integrates the energy based on their values and the nominal voltage.

It is recommended to use the ADE7868/ADE7878 in PSM2 mode when Bits[2:0] (PGA1[2:0]) of the gain register are equal to 1 or 2. These bits represent the gain in the current channel datapath. It is not recommended to use the ADE7868/ADE7878 in PSM2 mode when the PGA1[2:0] bits are equal to 4, 8, or 16.

## PSM3—SLEEP MODE (ALL PARTS)

The sleep mode is available on all parts (ADE7854, ADE7858, ADE7868, and ADE7878). In this mode, the ADE78xx has most of its internal circuits turned off and the current consumption is at its lowest level. The I²C, HSDC, and SPI ports are not functional during this mode, and the $\overline{\text{RESET}}$, SCLK/SCL, MOSI/SDA, and $\overline{\text{SS}}$/HSA pins should be set high.

**Table 11. Power Modes and Related Characteristics**

| Power Mode | All Registers[1] | LPOILVL, CONFIG2 | I²C/SPI | Functionality |
|---|---|---|---|---|
| PSM0 | | | | |
| State After Hardware Reset | Set to default | Set to default | I²C enabled | All circuits are active and DSP is in idle mode. |
| State After Software Reset | Set to default | Unchanged | Active serial port is unchanged if lock-in procedure has been previously executed | All circuits are active and DSP is in idle mode. |
| PSM1—ADE7878, ADE7868 Only | Not available | Values set during PSM0 unchanged | Enabled | Current mean absolute values are computed and the results are stored in the AIMAV, BIMAV, and CIMAV registers. The I²C or SPI serial port is enabled with limited functionality. |
| PSM2—ADE7878, ADE7868 Only | Not available | Values set during PSM0 unchanged | Disabled | Compares phase currents against the threshold set in LPOILVL. Triggers $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pins accordingly. The serial ports are not available. |
| PSM3 | Not available | Values set during PSM0 unchanged | Disabled | Internal circuits shut down and the serial ports are not available. |

[1] Setting for all registers except the LPOILVL and CONFIG2 registers.

**Table 12. Recommended Actions When Changing Power Modes**

| Initial Power Mode | Recommended Actions Before Setting Next Power Mode | Next Power Mode | | | |
|---|---|---|---|---|---|
| | | PSM0 | PSM1 | PSM2 | PSM3 |
| PSM0 | Stop DSP by setting the run register = 0x0000.<br>Disable HSDC by clearing Bit 6 (HSDEN) to 0 in the CONFIG register.<br>Mask interrupts by setting MASK0 = 0x0 and MASK1 = 0x0.<br>Erase interrupt status flags in the STATUS0 and STATUS1 registers. | | Current mean absolute values (mav) computed immediately.<br>xIMAV registers can be accessed immediately. | Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly. | No action necessary. |
| PSM1—ADE7878, ADE7868 Only | No action necessary. | Wait until the $\overline{\text{IRQ1}}$ pin is triggered low.<br>Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1. | | Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly. | No action necessary. |
| PSM2—ADE7878, ADE7868 Only | No action necessary. | Wait until the $\overline{\text{IRQ1}}$ pin is triggered low.<br>Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1. | Wait until the $\overline{\text{IRQ1}}$ pin triggered low.<br>Current mean absolute values compute at this moment.<br>xIMAV registers may be accessed from this moment. | | No action necessary. |
| PSM3 | No action necessary. | Wait until the $\overline{\text{IRQ1}}$ pin is triggered low.<br>Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1. | Wait until the $\overline{\text{IRQ1}}$ pin is triggered low.<br>Current mav circuit begins computations at this time.<br>xIMAV registers can be accessed from this moment. | Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly. | |