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# **ANALOG** Polyphase Multifunction Energy Metering IC with Harmonic and Fundamental Information

**Data Sheet** 

# ADE7854/ADE7858/ADE7868/ADE7878

### **FEATURES**

Highly accurate; supports EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-22, and IEC 62053-23 standards Compatible with 3-phase, 3- or 4-wire (delta or wye), and other 3-phase services Supplies total (fundamental and harmonic) active, reactive (ADE7878, ADE7868, and ADE7858 only), and apparent energy, and fundamental active/reactive energy (ADE7878 only) on each phase and on the overall system Less than 0.1% error in active and reactive energy over a dynamic range of 1000 to 1 at  $T_A = 25^{\circ}C$ Less than 0.2% error in active and reactive energy over a dynamic range of 3000 to 1 at  $T_A = 25^{\circ}C$ Supports current transformer and di/dt current sensors Dedicated ADC channel for neutral current input (ADE7868 and ADE7878 only) Less than 0.1% error in voltage and current rms over a dynamic range of 1000 to 1 at  $T_A = 25^{\circ}C$ Supplies sampled waveform data on all three phases and on neutral current Selectable no load threshold levels for total and fundamental active and reactive powers, as well as for apparent powers Low power battery mode monitors phase currents for antitampering detection (ADE7868 and ADE7878 only) Battery supply input for missing neutral operation Phase angle measurements in both current and voltage channels with a typical 0.3° error Wide-supply voltage operation: 2.4 V to 3.7 V Reference: 1.2 V (drift +5 ppm/°C typical) with external overdrive capability Single 3.3 V supply

40-lead lead frame chip scale package (LFCSP), Pb-free Operating temperature: –40°C to +85°C Flexible I<sup>2</sup>C, SPI, and HSDC serial interfaces

### APPLICATIONS

**Energy metering systems** 

### **GENERAL DESCRIPTION**

The ADE7854/ADE7858/ADE7868/ADE7878 are high accuracy, 3-phase electrical energy measurement ICs with serial interfaces and three flexible pulse outputs. The ADE78xx devices incorporate second-order sigma-delta ( $\Sigma$ - $\Delta$ ) analog-to-digital converters (ADCs), a digital integrator, reference circuitry, and all of the signal processing required to perform total (fundamental and

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harmonic) active, reactive (ADE7878, ADE7868, and ADE7858), and apparent energy measurement and rms calculations, as well as fundamental-only active and reactive energy measurement (ADE7878) and rms calculations. A fixed function digital signal processor (DSP) executes this signal processing. The DSP program is stored in the internal ROM memory.

The ADE7854/ADE7858/ADE7868/ADE7878 are suitable for measuring active, reactive, and apparent energy in various 3-phase configurations, such as wye or delta services, with both three and four wires. The ADE78xx devices provide system calibration features for each phase, that is, rms offset correction, phase calibration, and gain calibration. The CF1, CF2, and CF3 logic outputs provide a wide choice of power information: total active, reactive, and apparent powers, or the sum of the current rms values, and fundamental active and reactive powers.

The ADE7854/ADE7858/ADE7868/ADE7878 contain waveform sample registers that allow access to all ADC outputs. The devices also incorporate power quality measurements, such as short duration low or high voltage detections, short duration high current variations, line voltage period measurement, and angles between phase voltages and currents. Two serial interfaces, SPI and I<sup>2</sup>C, can be used to communicate with the ADE78xx. A dedicated high speed interface, the high speed data capture (HSDC) port, can be used in conjunction with I<sup>2</sup>C to provide access to the ADC outputs and real-time power information. The ADE7854/ADE7858/ADE7868/ADE7878 also have two interrupt request pins, IRQ0 and IRQ1, to indicate that an enabled interrupt event has occurred. For the ADE7868/ADE7878, three specially designed low power modes ensure the continuity of energy accumulation when the ADE7868/ADE7878 is in a tampering situation. See Table 1 for a quick reference chart listing each part and its functions. The ADE78xx are available in the 40-lead LFCSP, Pb-free package.

### Table 1. Part Comparison

Part No.	WATT	VAR	IRMS, VRMS, and VA	di/dt	Fundamental WATT and VAR	Tamper Detect and Low Power Modes
ADE7878	Yes	Yes	Yes	Yes	Yes	Yes
ADE7868	Yes	Yes	Yes	Yes	No	Yes
ADE7858	Yes	Yes	Yes	Yes	No	No
ADE7854	Yes	No	Yes	Yes	No	No

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### 10/13—Rev. F to Rev. G

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Deleted Junction Temperature; Table 6	15
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Replaced Typical Performance Characteristics Section	18
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Reorganized Layout	Universal
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### 2/10—Revision 0: Initial Version

# FUNCTIONAL BLOCK DIAGRAMS



Figure 1. ADE7854 Functional Block Diagram

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Figure 4. ADE7878 Functional Block Diagram

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# **SPECIFICATIONS**

 $VDD = 3.3 V \pm 10\%$ , AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T<sub>MIN</sub> to T<sub>MAX</sub> = -40°C to +85°C, T<sub>TYP</sub>= 25°C.

### Table 2.

Parameter <sup>1, 2</sup>	Min	Тур М	lax	Unit	Test Conditions/Comments
ACCURACY					
Active Energy Measurement					
Active Energy Measurement Error (per Phase)					
Total Active Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
Fundamental Active Energy (ADE7878 Only)		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz/100 Hz, IPx =
Output Frequency Variation		0.01		%	$VPx = \pm 100 \text{ mV rms}$
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc; IPx = VPx = ±100 mV rms
Output Frequency Variation		0.01		%	
Total Active Energy Measurement Bandwidth		2		kHz	
REACTIVE ENERGY MEASUREMENT (ADE7858, ADE7868, AND ADE7878)					
Reactive Energy Measurement Error (per Phase)					
Total Reactive Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
Fundamental Reactive Energy (ADE7878 Only)		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz/100 Hz, IPx =
Output Frequency Variation		0.01		%	$VPx = \pm 100 \text{ mV rms}$
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc; IPx = VPx = ±100 mV rms
Output Frequency Variation		0.01		%	
Total Reactive Energy Measurement Bandwidth		2		kHz	
RMS MEASUREMENTS					
l rms and V rms Measurement Bandwidth		2		kHz	
l rms and V rms Measurement Error (PSM0 Mode)		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1

MEAN ASSOLITE VALUE (MAV) MEASUREMENT DOLE 7:068 AND ADE 7878) 260 Hz   Imay Measurement Bandwidth (PSM1 Mode) 0.5 % Over a dynamic range of 100 to 1, PGA = 1, 2, 4, 8   ANALOG INPUTS may measurement Error (PSM1 Mode) 0.5 % Over a dynamic range of 100 to 1, PGA = 1, 2, 4, 8   ANALOG INPUTS may measurement Error (PSM1 Mode) 0.5 % Over a dynamic range of 100 to 1, PGA = 1, 2, 4, 8   ANALOG INPUTS may measurement Error (PSM1 Mode) 0.5 % PGA = 1, differential inputs between the following pins: VAP and VN, VBP and VN, VCP, and VN, VDP	Parameter <sup>1, 2</sup>	Min	Тур	Max	Unit	Test Conditions/Comments
MEASUREMENT (ADE7368 AND ADE7378)     Maximum Signal Levels     260     Hz       ANL76780     0.5     %     Over a dynamic range of 100 to 1, PGA = 1, 2,4,8       ANL0G INPUTS     maximum Signal Levels     ±500     mV peak Following pins: VAP and VN, VEP and VN, VEP and VN, VEP and VN     PGA = 1, differential inputs between the following pins: VAP and VN, VEP and VN, VEP and VN, VEP and VN       Input Impedance (DC)     400     KO       MALOG INPUTS     400     KO       Gain Error     ±4     %     External 1.2 V reference       Gain Error     0.3     Core 1 (A tre	MEAN ABSOLUTE VALUE (MAV)					
ADC 9789     260     Hz       Imax Measurement Entror (PSM1 Mode)     0.5     %     Over a dynamic range of 100 to 1, PGA = 1, 2, 4.8       ANALGG INPUTS     Maximum Signal Levels     ±500     mV peak     PGA = 1, differential inputs between the following pins: VAP and VN, VBP and VN, VCP, and VCP Pins       Input Impedance (DC)     IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, and VCP Pins     400     KQ       ADC Coffset     -24     %     External 1.2 V reference       WPEROM SAMPLING     Sampling CLMX2048, 16.384 MHz/2048 = 8.495     See the Waveform Sampling Mode section PGA = 1, incalibrated error, see the Terminology section       Signal-to-Noise Ratio, SNR     74     dB     PGA = 1, incalibrated error, see the Terminology section       Signal-to-Noise Ratio, SNR     74     dB     PGA = 1, incalibrated error, see the Terminology section       TIME INTERVILE ENTWEEN PHASES     0.3     Degrees     Line frequency = 45 Hz to 65 Hz, HPF on       CT, CT, CT, DELSE OUTPUTS     KHz     Maximum Output Frequency     80     WTHR = WATRR = WATRR = WATRR = PMAX = 33.516.139       Muticurve Low Pulse Width     1.1     1.3     V	MEASUREMENT (ADE7868 AND					
Imax Measurement Brandwidth (PSM1 Made)     260     Hz       Imax Measurement Error (PSM1 Mode)     0.5     %     Over a dynamic range of 100 to 1, PGA = 1, 2, 4, 8       MANLOG INPUTS     mW peak     pGA = 1, differential inputs between the following pins: VP and IAN, IBP and IBN, ICP and ICN; single-ended inputs between the following pins: VP and VN, VEP, and ICN; single-ended inputs between the following pins: VP and VN, VEP, and VN       Input Impedance (DC)     iAP     400     kΩ       iAPC Offset     -24     mV     PGA = 1, uncalibrated enor, see the Terminology section       Gain Error     +4     %     External 1.2 V reference       WAVEFORM SAMPLING     -24     mV     Sampling CLKIN/2048, 16.344 MHz/2048 = 8 kSPS See the Waveform Sampling Mode section PGA = 1, fundamental frequency - 54 Hz to 65 Hz, see the Terminology section       Signal-to-Noise Antio, SNR     74     dB     PGA = 1, fundamental frequency - 54 Hz to 65 Hz, see the Terminology section       Signal-to-Noise Antio, SNR     74     dB     PGA = 1, concentral frequency - 54 Hz to 65 Hz, see the Terminology section       Signal-to-Noise Antio, SNR     2     Hz     6       Maximum Output Frequency     8     Hz     67 L, 2, cr 2 Hz to 65 Hz, see the Terminology section       Duty Cycle <t< td=""><td>ADE7878)</td><td></td><td></td><td></td><td></td><td></td></t<>	ADE7878)					
Model Imax Measurement Error (PSM1 Mode)     0.5     %     Over a dynamic range of 100 to 1, PGA = 1, 2, 4, 8       ANALOG INPUTS     Maximum Signal Levels     ±500     mV peak     PGA = 1, differential inputs between the following pins: I/P and IAN, IPP and VN, VCP, and VN, VCP pins       Input Impedance (DC)     IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, and VCP Pins     400     KO       Gain Error     130     -24     mV     External 1.2 V reference       WWEPORM SAMPLING     -24     %     Sampling CLINI2048, IS.834 MH/z2048 = 8 KSPS       Current and Voltage Channels     signal to Avise faito, SNR     74     dB     PGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology section       Signal to Avise faito, SNR     74     dB     PGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology section       Signal-to-Noise and-Distortion Ratio, SNR     74     dB     PGA = 1, fundamental frequency: 45 Hz to 65 Hz, HPF on       CFL, CF2, CF3 PULSE OUTPUTS     Maxium Output Frequency     8     Hz     HZ       Maxium Output Frequency     8     KHz     WTHR = WRTHR = VATHR = PMAX = 33,516,139       Utfy CF	I mav Measurement Bandwidth (PSM1		260		Hz	
Time Meaduration (Figure 1) (Fash in Nobe) 0.3 1000 a dynamic angle of Nobe 7, Fash 5, ANLOG INPUTS   Maximum Signal Levels ±500 mV peak PGA = 1, differential inputs between the following pins: MP and IAN, IBP and ISN, ICP and ISN, ICP and ISN, ICP and ICN, ISP and ISN, ICP and ICN, ISP and ISN, ICP and ICN, ISP and ICN, IS	Mode)		0.5		0/	Over a durancia reason of 100 to 1 DCA 1 2 4 9
Adduct Num Gigan Levels ±500 mV peak PGA = 1, differential inputs between the following pins: VP and VN, VCP and VN and VN VCP			0.5		70	Over a dynamic range of 100 to 1, PGA = 1, 2, 4, 8
maximum Signal Levels 2.300 In V peak FOA = 1, Uncellent inputs Detween the following pins: LAP and IAN, IBP and IBN, ICP and ICN's ingle-metel inputs Detween the following pins: VAP and VN, VCP, and VN   input Impedance (DC) IAP, IAN, IBP, IBN, ICP (CN, VAP, VBP, and VA, VCP 400 KQ   and VCP Pins 130 KQ   ADC Offset -24 %   External 1.2 V reference Sampling CLKIN/2048, 16.384 MHz/2048 = 8 KSPS   Current and Voltage Channels signal-to-Noise Ratio, SNN 74   Signal-to-Noise Ratio, SNN 74 dB   Bandwidth (-3 dB) 2 KHz   TIME INTERVAL BETWEEN PHASES 0.3 Degrees   Maximum Output Frequency 8 KHz   Maximum Output Frequency 8 KHz   Outy Cycle 50 %   FEFERNCE INPUT 8   REFERNCE INPUT 0.04   REFERENCE INPUT -50   REFERENCE INP	ANALOG INPUTS			1500	m\/ nool/	PCA = 1 differential inputs between the
Input Impedance (DC) AD kΩ   Input Impedance (DC) IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, and VCP Pins 400 kΩ   ADC Offset -24 KΩ   Gain Error -24 %   WAFFORM SAMPLING Sampling CLRIV2048 = 8 KSPS   Current and Voltage Channels Signal-to-Noise Ratio, SNR 74   Signal-to-Noise Ratio, SNR 74   Bandwidth (-3 dB) 2   TIME. INTERVAL BETWEEN PHASES Bandwidth (-3 dB)   Maximum Output Frequency 8   Maximum Output Frequency 8   Active Low Pulse Width 80   JItter 0.04   Sofik rs   Active Low Pulse Width 80   Maximum Output Frequency 8   Active Low Pulse Width 80   JItter 0.04   Noninal 12V at the REFrequency = 0.25 Hz and CFD. CF2, or CF3 frequency = 0.25 Hz and CFD. CF2, or CF3 frequency = 0.25 Hz and CFD. CF2, or CF3 frequency = 0.25 Hz and CFD. CF3 requency = 0.25 Hz and CF3 CF3 requen	Maximum Signal Levels			±300	пі реак	following pins: IAP and IAN, IBP and IBN, ICP
Input impedance (DC)     APL AND MAY VEP, and VN, VEP, and VLP, VEP, and VEP, VEP, and Veltaper, VEP, and Veltaper, Vertaper, assessible, and Veltaper, Vertaper, assessible, and Veltaper, Vertaper, ve						and ICN; single-ended inputs between the
Input impedance (DC)     IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, and VCP Pins     400     KΩ       VN Pin     130     KΩ       Gain Error     ±4     %     External 1.2 verference       WVEFORK SAMPLING     -24     %     External 1.2 verference       Signal-to-Noise-and-Distortion Ratio, Signal-to-Noise-and-Distortion Ratio, Sig						following pins: VAP and VN, VBP and VN, VCP,
Input impedance (UC) IAP, IAN, IRP, IBN, ICP, ICN, VAP, VBP, and VCP Pins400KONP Pin130NCKOADC Offset $-24$ mVPGA = 1, uncalibrated error, see the Terminology sectionGain Error144%External 1.2 V referenceWWEPORM SAMPLINGSampling CUNV2048, 16.384 MHz/2048 = 8 kSPSCurrent and Voltage ChannelsSampling CUNV2048, 16.384 MHz/2048 = 8 kSPSSignal-to-Noise-and-Distortion Ratio, SINAD74dBPGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology sectionBandwidth (-3 dB)2kHzKHzTIME INTERVAL BETWEEN PHASES0.3DegreesLine frequency: 45 Hz to 65 Hz, HPF onCFI, CF2, CF3 PULSE OUTPUTS8KHzWTHR = WATHR = WAX = 33,516,139Maximum Output Frequency8KHzWTHR = WATHR = WAX = 33,516,139Juty Cycle50%If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDN is odd and > 1If cF1, CF2, Or CF3 frequency > 6.25 Hz and CFDN is odd and > 1If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDN is odd and > 1REFERENCE INPUT80msIf CF1, CF2, or CF3 frequency = 1.11REFERENCE INPUT-50 $\pm 5$ $\pm 50$ ppm/°CREFERENCE INPUT-50 $\pm 5$ $\pm 50$ ppm/°CREFERENCE INPUT16.2216.38416.55MHzREFERENCE-50 $\pm 5$ $\pm 50$ ppm/°CDrift across the entire temperature range of $-40^\circ$ to $\pm 85^\circ$ to $\pm 35$ CLNN16.2216.38416.55MHz <td></td> <td></td> <td></td> <td></td> <td></td> <td>and VN</td>						and VN
IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP; and VCP Prins400K1VN Pin130KQADC Offset-24mVGain Error $\pm 4$ %External 1.2 V referenceSampling CLNN208, 16.384 MHz/2048 = 8 KSPSCurrent and Voltage ChannelsSampling CLNN208, 16.384 MHz/2048 = 8 KSPSSignal-to-Noise Ratio, SNR74dBSignal-to-Noise-and-Distortion Ratio, SINAD74dBBandwidth (-3 dB)2kHzTIME INTERVAL BETWEEN PHASES0.3Measurement Error0.3DegreesCF1, CF2, CF3 PULSE OUTPUTS8Maximum Output Frequency8Maximum Output Frequency8Active Low Pulse Width80JItter0.04%FCF1, CF2, or CF3 frequency < 6.25 Hz and CFDEN is even and > 1Ifter0.04%FCF1, CF2, or CF3 frequency < 6.25 Hz and cFDEN is odd and > 1REFERENCE INPUT $\pm 50\%$ REFERENCE INPUT $\pm 50\%$ REFE	Input Impedance (DC)					
and VC Yms130KDADC Offset130 $K\Omega$ Gain Error±4%WAVEFORM SAMPLINGExternal 1.2 V referenceCurrent and Voltage ChannelsSampling Mode sectionSignal-to-Noise Ratio, SNR74Signal-to-Noise-and-Distortion Ratio,74Bandwidth (-3 dB)2LTIME INTERVAL BETWEEN PHASESKHzMeasurement Error0.3CF1, CF2, CF3 PULSE OUTPUTS8Maximum Output Frequency8Maximum Output Frequency8Jutter50Soft50Active Low Pulse Width80Jitter0.04REFERENCE INPUT8Reference10Reference11LIN13VMinimum = 1.2V – 8%; maximum = 1.2V + 8%Input Clock Frequency16.22Input Clock Frequency16.24Input Clock Frequency <td>IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP,</td> <td>400</td> <td></td> <td></td> <td>kΩ</td> <td></td>	IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP,	400			kΩ	
ADC Offset IJS PGA = 1, uncalibrated error, see the Terminology section   Gain Error ±4 % External 1.2 V reference   WAVEFORM SAMPLING Sampling CLKIN/2048, 16.384 MHz/2048 = 8 LSPS See the Waveform Sampling Mode section   Signal-to-Noise Ratio, SNR 74 dB GGA = 1, fundamental frequency: 45 Hz to   Signal-to-Noise and-Distortion Ratio, SINAD 74 dB PGA = 1, fundamental frequency: 45 Hz to   Bandwidth (-3 dB) 2 kHz VHR = VARTHR = VATHR	VN Pin	130			k0	
Constant Constant Constant Constant Constant   Gain Error ±4 % External 1.2 V reference   WWEFORM SAMPLING External 1.2 V reference Section   Current and Voltage Channels Signal-to-Noise Attain SNR 74   Signal-to-Noise and-Distortion Ratio, Signal-to-Noise Attained Signal-to-Noise and-Distortion Ratio, Signal-to-Noise Attained Signal-to-Noise Attained Sig		150	_24		m\/	PGA = 1 uncalibrated error see the Terminology
Gain Error $\pm 4$ %External 1.2 V referenceWAVEFORM SAMPLING Current and Voltage Channels Signal-to-Noise Ratio, SNR3See the Waveform Sampling Mode section $CG = 1$ , fundamental frequency: 45 Hz to 65 Hz, see the Terminology sectionSignal-to-Noise-and-Distortion Ratio, SINAD74dB $PGA = 1$ ; fundamental frequency: 45 Hz to 65 Hz, see the Terminology sectionBandwidth (-3 dB)2kHz $PGA = 1$ ; fundamental frequency: 45 Hz to 65 Hz, see the Terminology sectionBandwidth (-3 dB)2kHz $PGA = 1$ ; fundamental frequency: 45 Hz to 65 Hz, see the Terminology sectionMaximum Output Error0.3DegreesLine frequency = 45 Hz to 65 Hz, HPF onCF1, CF2, CF3 PlUSE OUTPUTS Maximum Output Frequency8kHzWTHR = VARTHR = VARTHR = PMAX = 33,516,139Muther Voltage Volte50%If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1Active Low Pulse Width Jitter80msmsREFERENCE INPUT REFERENCE INPUT REFERENCE INPUT1.11.3VREFERENCE INPUT REFERENCE-50 $\pm 5$ $\pm 50$ PSM0 and PSMI Modes Temperature Coefficient-50 $\pm 5$ $\pm 50$ PSM0 and PSMI Modes Temperature Coefficient-50 $\pm 5$ $\pm 50$ PSM0 and PSMI Modes Temperature Coefficient-50 $\pm 5$ $\pm 50$ PSM0 and PSMI Modes Temperature Coefficient-50 $\pm 5$ $\pm 50$ PSM0 and PSMI Modes Temperature Coefficient-50 $\pm 5$ $\pm 50$ PSM0 and PSMI Modes Te	Abeonset		27		1110	section
WAVEFORM SAMPLING Current and Voltage Channels Signal-to-Noise Ratio, SNR74Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS See the Waveform Sampling Mode section PGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology section PGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology section PGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology sectionBandwidth (-3 dB)2kHzTIME INTERVAL BETWEEN PHASES Measurement Error0.3DegreesCF1, CF2, CF3 PULSE OUTPUTS Maximum Output Frequency8kHzMaximum Output Frequency S0%8kHzDuty Cycle50%If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1 If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1 If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1 If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1REFERENCE INPUT REFewour Input Voltage Range Input Capacitance1.11.3VMinimum = 1.2V - 8%; maximum = 1.2V + 8% Input Capacitance-50 $\pm 5$ $\pm 50$ ON-CHIP REFERENCE PSM0 and PSM1 Modes Temperature Coefficient-50 $\pm 5$ $\pm 50$ CLIN-50 $\pm 5$ $\pm 50$ Drift across the entire temperature range of -40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more detailsCLIN-50 $\pm 5$ $\pm 50$ Drift across the entire temperature range of -40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more detailsCLIN-50 $\pm 5$ $\pm 50$ Drift across the ent	Gain Error		±4		%	External 1.2 V reference
Current and Voltage Channels Signal-to-Noise Ratio, SNR   74   dB   See the Waveform Sampling Mode section PGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology section     Bandwidth (-3 dB)   2   kHz   PGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology section     Bandwidth (-3 dB)   2   kHz   Interminology section     TIME INTERVAL BETWEEN PHASES   0.3   Degrees   Line frequency: 45 Hz to 65 Hz, HPF on     CF1, CF2, CF3 FULSE OUTPUTS   KHz   WTHR = VARTHR = VAITHR = PMAX = 33,516,139     Maximum Output Frequency   8   KHz   WTHR = VARTHR = VAITHR = PMAX = 33,516,139     Duty Cycle   50   %   If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDE N is odd and > 1     Active Low Pulse Width   80   ms   If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDE N is odd and > 1     Jitter   0.04   %   FCF1, CF2, or CF3 frequency < 6.25 Hz and crEDE N is odd and > 1     REFERENCE INPUT   1.1   1.3   V   Minimum = 1.2V – 8%; maximum = 1.2V + 8%     Input Capacitance   -50   ±5   +50   pf   Drift across the entire temperature range of -40°C to +85°C is calculated with reference to 25°C; see the Reference Cincuit section for more details     CLKIN   -50   ±5   +5	WAVEFORM SAMPLING					Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS
Signal-to-Noise Ratio, SNR 74 dB PGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology section   Signal-to-Noise-and-Distortion Ratio, SINAD 74 dB PGA = 1, fundamental frequency: 45 Hz to 65 Hz, see the Terminology section   Bandwidth (-3 dB) 2 kHz   TIME INTERVAL BETWEEN PHASES 0.3 Degrees   Maximum Output Frequency 8 kHz   Maximum Output Frequency 6.25 Hz and CFDEN is even and > 1   If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1   If CF1, CF2, or CF3 frequency > 6.25 Hz   Active Low Pulse Width 80   Jitter 0.04   REFERENCE INPUT   REFERENCE INPUT   REFERENCE INPUT   REFERENCE INPUT   REFERENCE   PSM0 and PSM1 Modes   Temperature Coefficient   -50 ±5   +50   pmm/CC   Drift across the entire temperature range of -40°C to +85°C is calculated with re	Current and Voltage Channels					See the Waveform Sampling Mode section
Signal-to-Noise-and-Distortion Ratio, SINAD 74 65 Hz, see the Terminology section   Bandwidth (-3 dB) 2 kHz   TIME INTERVAL BETWEEN PHASES 0.3 Degrees Line frequency = 45 Hz to 65 Hz, HPF on   CF1, CF2, CF3 PULSE OUTPUTS 8 kHz WTHR = VARTHR = PMAX = 33,516,139   Maximum Output Frequency 8 kHz WTHR = VARTHR = PMAX = 33,516,139   Duty Cycle 50 % If CF1, CF2, OF3 Frequency > 6.25 Hz and CFDEN is even and > 1   Active Low Pulse Width 80 ms If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1   Jitter 0.04 % For CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1   REFERENCE INPUT 80 ms If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1   REFERENCE INPUT 80 ms If CF1, CF2, or CF3 frequency > 6.25 Hz   REFERENCE INPUT 1.1 1.3 V Minimum = 1.2V - 8%; maximum = 1.2V + 8%   Input Capacitance 10 pF Drift across the entire temperature range of -40°C to -85°C is calculated with reference to 25°C; see the Reference Circuit section for more details.   CLKIN Input Capacitance -50 ±5 +50 ppm/°C   Input Clock Frequency 16.22 16.384 16.55 MHz   LOGIC INPUTS	Signal-to-Noise Ratio, SNR		74		dB	PGA = 1, fundamental frequency: 45 Hz to
Signal-to-Noise-and-Distortion Ratio, SiNAD 74 dB PGA = 1; fundamental frequency: 45 Hz to 65 Hz, see the Terminology section   Bandwidth (-3 dB) 2 kHz   TIME INTERVAL BETWEEN PHASES 0.3 Degrees   Measurement Error 0.3 Degrees   CF1, CF2, CF3 PULSE OUTPUTS KHz   Maximum Output Frequency 8 KHz   Duty Cycle 50 %   If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1 If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1   Active Low Pulse Width 80 ms If CF1, CF2, or CF3 frequency > 6.25 Hz   Jitter 0.04 % For CF1, CF2, or CF3 frequency > 6.25 Hz   Nominal phase currents are larger than 10% of full scale full scale   REFERENCE INPUT 1.1 1.3 V   REFERENCE INPUT -50 ±5 +50   ON-CHIP REFERENCE pF Nominal 1.2V at the REFwour pin at T <sub>A</sub> = 25°C   PSM0 and PSM1 Modes -50 ±5 +50   Temperature Coefficient -50 ±5 +50   Input Clock Frequency 16.22 16.384 16.55   Input High Voltage, Vest 2.0 V VDD = 3.3 V ± 10%   Input High Voltage, Vest 0.8 V VDD = 3.						65 Hz, see the Terminology section
SINAD 65 Hz, see the Terminology section   Bandwidth (-3 dB) 2   TIME INTERVAL BETWEEN PHASES Line frequency = 45 Hz to 65 Hz, HPF on   CF1, CF2, CF3 PULSE OUTPUTS Bandwidth   Maximum Output Frequency 8   Duty Cycle 50   V If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1   If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1   If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1   If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1   If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1   Jitter 0.04   % If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1   Input Capacitance 10   Input Capacitance 10   ON-CHIP REFERENCE INPUT ±5   REFRENCE INPUT ±5   REFRENCE INPUT 50   CLKIN -50   UCGCI INPUTS-MOSI/SDA, SCLK/SCL, SS, RESET, PMO, AND PM1   Input Clock Frequency 16.22   Input High Voltage, Vimit 2.0   V VDD = 3.3 V ± 10%   Input High Voltage, Vimit 2.0   V VDD = 3.3 V ± 10%   Input Low Voltage, Vimit 0.8   V VDD = 3.3 V ± 10%   Input Low Voltage, V	Signal-to-Noise-and-Distortion Ratio,		74		dB	PGA = 1; fundamental frequency: 45 Hz to
Lindowith (-3 db)2KH2TIME INTERVAL BETWEEN PHASES0.3DegreesLine frequency = 45 Hz to 65 Hz, HPF onMeasurement Error0.3DegreesLine frequency = 45 Hz to 65 Hz, HPF onCF1, CF2, CF3 PULSE OUTPUTS8KHzWTHR = VARTHR = VATHR = PMAX = 33,516,139Maximum Output Frequency8KHzWTHR = VARTHR = VARTHR = PMAX = 33,516,139Duty Cycle50%If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1Active Low Pulse Width80msIf CF1, CF2, or CF3 frequency > 6.25 HzJitter0.04%For CF1, CF2, or CF3 frequency > 6.25 HzNaminal phase currents are larger than 10% of full scaleFor CF1, CF2, or CF3 frequency > 6.25 HzREFERENCE INPUT80msIf CF1, CF2, or CF3 frequency > 6.25 HzNoninal phase currents are larger than 10% of full scaleNominal phase currents are larger than 10% of full scaleREFERENCE INPUT1.11.3VREFERENCENominal 1.2 V at the REFerence to 25°CPSM0 and PSM1 Modes Temperature Coefficient-50 $\pm 5$ -50 $\pm 5$ $\pm 50$ ppm/°CCLKINInput Clock Frequency16.22Input Clock Frequency16.2216.384Input High Voltage, Visit0.8VVDD = 3.3 V $\pm 10\%$ Input = 0, VDD = 3.3 VInput Low Voltage, Visit0.8VNoncillar Capacitance Circuit frequency Input = VDD = 3.3 VInput Covoltage, Visit0.8VInput Covoltage, Visit <t< td=""><td>SINAD</td><td></td><td>2</td><td></td><td></td><td>65 Hz, see the Terminology section</td></t<>	SINAD		2			65 Hz, see the Terminology section
IIME INTERVAL BET WEEN PHASESDegreesLine frequency = 45 Hz to 65 Hz, HPF onMeasurement Error0.3DegreesLine frequency = 45 Hz to 65 Hz, HPF onCF1, CF2, CF3 PULSE OUTPUTS8KHzWTHR = VARTHR = VARTHR = PMAX = 33,516,139Duty Cycle50%If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1Active Low Pulse Width80msIf CF1, CF2, or CF3 frequency > 6.25 HzJitter0.04%For CF1, CF2, or CF3 frequency > 6.25 HzJitter0.04%For CF1, CF2, or CF3 frequency > 6.25 HzInput Capacitance10msIf CF1, CF2, or CF3 frequency = 1 Hz and nominal phase currents are larger than 10% of full scaleREFERENCE INPUT1.11.3VREFERENCE INPUTFor CF1, CF2, or CF3 frequency = 1 Hz and nominal phase currents are larger than 10% of full scaleON-CHIP REFERENCEpFPSM0 and PSM1 Modes-50 $\pm 5$ Temperature Coefficient-50 $\pm 5$ -50 $\pm 5$ $+50$ Input Clock Frequency16.2216.384Input Clock Frequency16.2216.384Input High Voltage, VmH2.0VVD = 3.3 V $\pm 10\%$ Input = 0V, VDD = 3.3 VInput Low Voltage, VmL0.8VVDD = 3.3 V $\pm 10\%$ Input = VDD = 3.3 VInput Corrent, Im-8.7 $\mu A$ Input Corrent, Im-8.7 $\mu A$ Input Corrent, Im-8.7Input Corrent, Im-9.6			2		KHZ	
Measurement Prof0.3DegreesLine frequency $43$ fr2 to 55 H2, HPF onCF1, CF2, CF3 PULSE OUTPUTS Maximum Output Frequency Duty Cycle8kHzWTHR = VARTHR = VATHR = PMAX = 33,516,139Maximum Output Frequency Duty Cycle50%If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1(1 + 1/CFDEN) x 50%(1 + 1/CFDEN) x 50%If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1Active Low Pulse Width Jitter80msIf CF1, CF2, or CF3 frequency < 6.25 Hz For CF1, CF2, or CF3 frequency < 6.25 Hz and CFDEN is odd and > 1REFERENCE INPUT REFerence1.11.3VREFERENCE INPUT REFerence1.11.3VREFERENCE INPUT REFERENCE PSM0 and PSM1 Modes Temperature Coefficient-50 $\pm 5$ $\pm 50$ PSM0 and PSM1 Modes Temperature Coefficient-50 $\pm 5$ $\pm 50$ ppm/°CCLKIN16.2216.38416.55MHzInput Clock Frequency16.2216.38416.55Input High Voltage, VmH Input Low Voltage, VmH Input Low Voltage, VmL Input Low Voltage, VmL Input Low Voltage, VmL Input Low Voltage, VmL2.0VVDD = 3.3 V $\pm 10\%$ Input = 0V, VDD = 3.3 VInput Concertainer Cm109FNeptNotage, VmL Input = VDD = 3.3 VInput = VDD = 3.3 V			0.2		Deersee	
CLT, CP2, CF3 PULSE OUTPOTS88HzWTHR = VARTHR = VARTHR = PMAX = 33,516,139Maximum Output Frequency50%If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1CFDEN is even and > 1Active Low Pulse Width80msIf CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1CFDEN is odd and > 1Jitter0.04%For CF1, CF2, or CF3 frequency < 6.25 Hz			0.3		Degrees	Line frequency = 45 Hz to 65 Hz, HPF on
Maximum Output Frequency6KH2WIRE - WAIR = WAIR = WAR = 35, 16, 139Duty Cycle50%If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1 $(1 + 1/CFDEN)$ × 50%(1 + 1/CFDEN) × 50%If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1Active Low Pulse Width80msJitter0.04%REFERENCE INPUT REFINIOUT Input Voltage Range1.11.3REFERENCE INPUT REFERENCE1.11.3ON-CHIP REFERENCE PSM0 and PSM1 Modes Temperature Coefficient-50 $\pm 5$ -50 $\pm 5$ $\pm 50$ ppm/°CDift across the entire temperature range of $-40^{\circ}C$ to $+85^{\circ}C$ is calculated with reference to $25^{\circ}C$ ; see the Reference Circuit section for more details.CLKIN16.2216.38416.55Input Clock Frequency16.2216.384Input Clock Frequency2.0VVDD = 3.3 V ± 10% Input High Voltage, VmL Input High Voltage, VmL Input Low Voltage, VmL Input Low Voltage, VmL Input High Voltage, VmL Input Low Voltage, VmL Input High Voltage, VmL Input Low Voltage, VmL Input High Voltage, VmL Input Capacitance CmVVVDD = 3.3 V ± 10% VDD = 3.3 VInput = 0V, VDD = 3.3 VInput Capacitance Cm10pF	CF1, CF2, CF3 PULSE OUTPUTS		0		LU =	
Duty Cycle   30   %   If CF1, CF2, Of CF3 frequency > 6.25 H2 and CFDEN is seven and > 1 If CF1, CF2, or CF3 frequency > 6.25 H2 and CFDEN is odd and > 1     Active Low Pulse Width   80   ms   If CF1, CF2, or CF3 frequency > 6.25 H2 or CF1, CF2, or CF3 frequency < 6.25 H2 For CF1, CF2, or CF3 frequency < 6.25 H2	Maximum Output Frequency		8		КПZ 0/	WIAK = VALHK = VALHK = PMAX = $33,510,139$
Active Low Pulse Width Jitter $(1 + 1/CFDEN)$ $\times 50%$ If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1Jitter80 0.04msIf CF1, CF2, or CF3 frequency < 6.25 Hz For CF1, CF2, or CF3 frequency < 6.25 Hz and nominal phase currents are larger than 10% of full scaleREFERENCE INPUT REFENCUT Input Voltage Range Input Capacitance1.11.3VMinimum = 1.2 V - 8%; maximum = 1.2 V + 8% Input Capacitance10pFON-CHIP REFERENCE PSM0 and PSM1 Modes Temperature Coefficient-50 $\pm 5$ $+50$ ppm/°CCLKIN-50 $\pm 5$ $+50$ ppm/°CDrift across the entire temperature range of -40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more detailsCLKIN16.2216.38416.55MHzLOGIC INPUTSMOSI/SDA, SCLK/SCL, SS, RESET, PM0, AND PM1 	Duty Cycle		50		%	$\Gamma$ CF1, CF2, of CF3 frequency > 0.25 H2 and CFDFN is even and > 1
Active Low Pulse Width Jitter $\times 50\%$ $CFDEN is odd and > 1Active Low Pulse WidthJitter800.04msIf CF1, CF2, or CF3 frequency < 6.25 HzFor CF1, CF2, or CF3 frequency = 1 Hz andnominal phase currents are larger than 10% offull scaleREFERENCE INPUTREFINIOUT Input Voltage RangeInput Capacitance1.11.3VMinimum = 1.2 V - 8%; maximum = 1.2 V + 8%ON-CHIP REFERENCEPSM0 and PSM1 ModesTemperature Coefficient-50\pm 5+50ppm/°CDiff across the entire temperature range of -40°Cto +85°C is calculated with reference to 25°C;see the Reference Circuit section for more detailsAll specifications CLKIN of 16.384 MHz. See theCrystal Circuit section for more details.CLKIN16.2216.38416.55MHzLOGIC INPUTS-MOSI/SDA, SCLK/SCL, SS,RESET, PM0, AND PM1Input High Voltage, VINHInput Low Voltage, VINH2.0VVDD = 3.3 V \pm 10\%UDD = 3.3 V \pm 10\%Input Capacitance CapInput Capacitance CapInput CapacitanceUDDIT Capacitance10-8.7µAµAInput = 0V, VDD = 3.3 VInput = VDD = 3.3 V$			(1 + 1/CFDEN)			If CF1, CF2, or CF3 frequency $> 6.25$ Hz and
Active Low Pulse Width Jitter80msIf CF1, CF2, or CF3 frequency < 6.25 HzJitter0.04%For CF1, CF2, or CF3 frequency < 1 Hz and nominal phase currents are larger than 10% of full scaleREFERENCE INPUT REFINIOUT Input Voltage Range Input Capacitance1.11.3VREFERENCE PSM0 and PSM1 Modes Temperature Coefficient-50±5+50ppm/°CDN-CHIP REFERENCE PSM0 and PSM1 Modes-50±5+50ppm/°CCLKIN-50±5+50ppm/°CDrift across the entire temperature range of -40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more detailsCLKIN16.2216.38416.55MHzInput Clock Frequency16.2216.38416.55MHzLOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PM0, AND PM1 Input High Voltage, VINH Input Low Voltage, VINH2.0VVDD = 3.3 V ± 10% Input Current, INInput Capacitance Cru10-8.7 3µAInput = 0V, VDD = 3.3 V Input = VDD = 3.3 V			× 50%			CFDEN is odd and > 1
Jitter   0.04   %   For CF1, CF2, or CF3 frequency = 1 Hz and nominal phase currents are larger than 10% of full scale     REFERENCE INPUT   Input Capacitance   11   1.3   V   Minimum = 1.2 V - 8%; maximum = 1.2 V + 8%     Input Capacitance   10   pF   PS   Nominal 1.2 V at the REFINIOUT pin at TA = 25°C     ON-CHIP REFERENCE   PSM0 and PSM1 Modes   -50   ±5   +50   ppm/°C   Drift across the entire temperature range of -40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more details     CLKIN   -50   ±5   +50   ppm/°C   Drift across the entire temperature range of -40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more details     CLKIN   -50   ±5   +50   ppm/°C   Drift across the entire temperature range of -40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more details     CLKIN   -52   16.22   16.384   16.55   MHz     LOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PMO, AND PM1   0.8   V   VDD = 3.3 V ± 10%     Input Low Voltage, VINL   0.8   V   VDD = 3.3 V ± 10%     Input Current, IN   -8.7   µA   Input = 0 V, VDD = 3.3 V     Input C	Active Low Pulse Width		80		ms	If CF1, CF2, or CF3 frequency < 6.25 Hz
REFERENCE INPUT nominal phase currents are larger than 10% of full scale   REFINOUT Input Voltage Range 1.1 1.3 V   Input Capacitance 10 pF   ON-CHIP REFERENCE pSM0 and PSM1 Modes -50 ±5 +50 ppm/°C Nominal 1.2 V at the REF <sub>INVOUT</sub> pin at T <sub>A</sub> = 25°C   PSM0 and PSM1 Modes -50 ±5 +50 ppm/°C Drift across the entire temperature range of -40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more details   CLKIN Input Clock Frequency 16.22 16.384 16.55 MHz   LOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PM0, AND PM1 2.0 V VDD = 3.3 V ± 10%   Input Low Voltage, VINL 0.8 V VDD = 3.3 V ± 10%   Input Current, IN -8.7 µA Input = 0 V, VDD = 3.3 V   Input Capacitance Cav 10 pF 0.8 V	Jitter		0.04		%	For CF1, CF2, or CF3 frequency = 1 Hz and
Tull scaleTull scaleREFERENCE INPUT REFIN/OUT Input Voltage Range Input Capacitance1.11.3V pFMinimum = 1.2 V - 8%; maximum = 1.2 V + 8%ON-CHIP REFERENCE PSM0 and PSM1 Modes Temperature Coefficient $-50 \pm 5$ $+50$ ppm/°CNominal 1.2 V at the REFINIOUT pin at TA = 25°CON-CHIP REFERENCE PSM0 and PSM1 Modes $-50 \pm 5$ $+50$ ppm/°CDrift across the entire temperature range of $-40^{\circ}C$ to $+85^{\circ}C$ is calculated with reference to $25^{\circ}C$ ; see the Reference Circuit section for more detailsCLKINInput Clock Frequency16.2216.38416.55MHzLOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PM0, AND PM1 Input High Voltage, VINH Input Low Voltage, VINL2.0VVDD = $3.3 V \pm 10\%$ HA Input Current, INInput Capacitance Cm10 $-8.7$ M $\mu A$ Input $= 0V, VDD = 3.3 V$ Input $= VDD = 3.3 V$						nominal phase currents are larger than 10% of
REFERENCE INPOLInput Voltage Range1.11.3VMinimum = $1.2 \text{ V} - 8\%$ ; maximum = $1.2 \text{ V} + 8\%$ Input Capacitance10pFNominal $1.2 \text{ V}$ at the REF_INCOUT pin at $T_A = 25^{\circ}\text{C}$ ON-CHIP REFERENCEPSM0 and PSM1 Modes-50 $\pm 5$ $+50$ ppm/°CDrift across the entire temperature range of $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ is calculated with reference to $25^{\circ}\text{C}$ ; see the Reference Circuit section for more detailsCLKINInput Clock Frequency16.2216.38416.55MHzLOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PM0, AND PM12.0VVDD = $3.3 \text{ V} \pm 10\%$ Input Low Voltage, VINH2.00.8VVDD = $3.3 \text{ V} \pm 10\%$ Input Current, Im-8.7 $\mu A$ Input = 0V, VDD = $3.3 \text{ V}$ Input Capacitance Conv10 $pF$ $PF$						
REFINOUT Input Voitage Range1.11.5VMinimum 1.2 V = 5% (Indexindum = 1.2 V = 5%)Input Capacitance10pFON-CHIP REFERENCEPSM0 and PSM1 ModesNominal 1.2 V at the REF <sub>INVOUT</sub> pin at $T_A = 25^{\circ}$ CPSM0 and PSM1 Modes-50 $\pm 5$ $+50$ ppm/°CTemperature Coefficient-50 $\pm 5$ $+50$ ppm/°CCLKIN-50 $\pm 5$ $+50$ ppm/°CDrift across the entire temperature range of $-40^{\circ}$ C to $+85^{\circ}$ C is calculated with reference to $25^{\circ}$ C; see the Reference Circuit section for more detailsCLKINInput Clock Frequency16.2216.38416.55Input Clock Frequency16.2216.38416.55MHzLOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PM0, AND PM12.0VVDD = 3.3 V ± 10%Input Low Voltage, VINH2.00.8VVDD = 3.3 V ± 10%Input Current, IN-8.7 $\mu A$ Input = 0 V, VDD = 3.3 VInput Capacitance Circuit Capacitance Circ	REFERENCE INPUT	1 1		1 2	V	Minimum = 1.2 V = 90% maximum = 1.2 V + 90%
Input CapacitanceIOprON-CHIP REFERENCE PSM0 and PSM1 Modes Temperature Coefficient $-50 \pm 5$ $+50$ $ppm/^{\circ}C$ Nominal 1.2 V at the REF <sub>IN/OUT</sub> pin at T <sub>A</sub> = 25°CDrift across the entire temperature range of $-40^{\circ}C$ to $+85^{\circ}C$ is calculated with reference to $25^{\circ}C$ ; see the Reference Circuit section for more detailsCLKINInput Clock Frequency16.2216.38416.55MHzLOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PM0, AND PM12.0VVDD = $3.3 V \pm 10\%$ Input Low Voltage, VINH Input Low Voltage, VINL2.0VVDD = $3.3 V \pm 10\%$ Input Current, IN $-8.7$ MA $\mu$ AInput = 0 V, VDD = $3.3 V$ Input Capacitance Cav10 $\mu$ AInput = VDD = $3.3 V$		1.1		1.5	v	1000000000000000000000000000000000000
ONVERTING NET EXERCIC PSM0 and PSM1 Modes Temperature Coefficient-50 $\pm 5$ $+50$ ppm/°CDrift across the entire temperature range of -40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more detailsCLKINInput Clock Frequency16.2216.38416.55MHzLOGIC INPUTS—MOSI/SDA, SCLK/SCL, $\overline{SS}$ , RESET, PM0, AND PM12.0VVDD = 3.3 V ± 10%Input Low Voltage, VINH Input Low Voltage, VINL2.0VVDD = 3.3 V ± 10%Input Current, IN-8.7 $\mu A$ Input = 0 V, VDD = 3.3 VInput Capacitance Cm10 $\mu A$ Input = VDD = 3.3 V				10	рі	Nominal 1.2 V at the REF word pin at $T_{1} = 25^{\circ}$
Temperature Coefficient $-50 \pm 5$ $\pm 50$ $ppm/^{\circ}C$ Drift across the entire temperature range of $-40^{\circ}C$ to $+85^{\circ}C$ is calculated with reference to $25^{\circ}C$ ; see the Reference Circuit section for more detailsCLKINInput Clock Frequency16.2216.38416.55MHzLOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PMO, AND PM1 Input Low Voltage, VINH2.0VVDD = $3.3 V \pm 10\%$ UDD = $3.3 V \pm 10\%$ Input Current, $I_{IN}$ Input Capacitance Circuit2.0VVDD = $3.3 V \pm 10\%$ Input Current, $I_{IN}$ Input Capacitance Circuit10 $pE$	PSM0 and PSM1 Modes					
Interference ContractingIso<	Temperature Coefficient	-50	+5	+50	nnm/°C	Drift across the entire temperature range of $-40^{\circ}$ C
CLKIN   see the Reference Circuit section for more details     Input Clock Frequency   16.22   16.384   16.55   MHz     LOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PM0, AND PM1   16.22   16.384   16.55   MHz     Input High Voltage, VINH Input Low Voltage, VINL   2.0   V   VDD = 3.3 V ± 10%     Input Current, IN   -8.7   µA   Input = 0 V, VDD = 3.3 V     Input Capacitance Circuit Capacitance Circuit Section for more details   10   pE		50		150	ppin/ C	to $+85^{\circ}$ C is calculated with reference to $25^{\circ}$ C;
CLKINAll specifications CLKIN of 16.384 MHz. See the Crystal Circuit section for more details.Input Clock Frequency16.2216.38416.55MHzLOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PM0, AND PM116.2216.38416.55MHzInput High Voltage, V_INH Input Low Voltage, V_INL2.0VVDD = 3.3 V ± 10%Input Current, I <sub>IN</sub> 0.8VVDD = 3.3 V ± 10%Input Capacitance Circuit10pE						see the Reference Circuit section for more details
Input Clock Frequency16.2216.38416.55MHzCrystal Circuit section for more details.LOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PM0, AND PM116.25MHzVVDD = $3.3 V \pm 10\%$ Input High Voltage, V <sub>INH</sub> 2.0VVDD = $3.3 V \pm 10\%$ VDD = $3.3 V \pm 10\%$ Input Low Voltage, V <sub>INL</sub> 0.8VVDD = $3.3 V \pm 10\%$ Input Current, I <sub>IN</sub> -8.7 $\mu A$ Input = $0 V, VDD = 3.3 V$ Input Capacitance C <sub>IN</sub> 10pE	CLKIN					All specifications CLKIN of 16.384 MHz. See the
Input Clock Frequency16.2216.38416.55MHzLOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PM0, AND PM12.0VVDD = $3.3 V \pm 10\%$ Input High Voltage, VINH2.00.8VVDD = $3.3 V \pm 10\%$ Input Low Voltage, VINL0.8VVDD = $3.3 V \pm 10\%$ Input Current, IN-8.7 $\mu A$ Input = $0 V, VDD = 3.3 V$ Input Capacitance Cinic10pE		44.00	44.204			Crystal Circuit section for more details.
LOGIC INPUTS—MOSI/SDA, SCLK/SCL, SS, RESET, PM0, AND PM12.0VVDD = $3.3 V \pm 10\%$ Input High Voltage, V_INH2.00.8VVDD = $3.3 V \pm 10\%$ Input Low Voltage, V_INL0.8VVDD = $3.3 V \pm 10\%$ Input Current, I <sub>IN</sub> -8.7 $\mu A$ Input = $0 V, VDD = 3.3 V$ Input Capacitance Cinic10pE		16.22	16.384	16.55	MHz	
RESET, PM0, AND PM12.0VVDD = $3.3 V \pm 10\%$ Input High Voltage, V_{INL}0.8VVDD = $3.3 V \pm 10\%$ Input Current, I <sub>IN</sub> -8.7 $\mu A$ Input = $0 V, VDD = 3.3 V$ Input Capacitance C <sub>IN</sub> 10pE	LOGIC INPUTS-MOSI/SDA, SCLK/SCL, SS,					
Input High Voltage, VINH2.0V $VDD = 3.3 V \pm 10\%$ Input Low Voltage, VINL0.8V $VDD = 3.3 V \pm 10\%$ Input Current, IIN-8.7 $\mu A$ Input = 0 V, VDD = 3.3 VInput Capacitance Cinic10 $\mu A$ Input = VDD = 3.3 V		2.0			V	
Input Cov voltage, VINL0.8V $VDD = 3.3 V \pm 10\%$ Input Current, In-8.7 $\mu A$ Input = 0 V, VDD = 3.3 V3 $\mu A$ Input = VDD = 3.3 V	Input High voltage, VINH	2.0		<u>^ </u>	v	$VDD = 3.3 V \pm 10\%$
Input Capacitance $C_{N}$ 10 $-6.7$ $\mu$ A Input = 0 V, VDD = 3.3 V $\mu$ A Input = VDD = 3.3 V				U.0	v uA	$V \cup V = 2.5 V \pm 10\%$
Input Capacitance $C_{N}$ 10 pE	input current, in			-0./ 3	μΑ	$ \text{Input} - V \nabla \nabla - 3.3 \text{ V}$
	Input Capacitance C		10	ر.	pF	

**Data Sheet** 

# ADE7854/ADE7858/ADE7868/ADE7878

Parameter <sup>1, 2</sup>	Min	Тур	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS-IRQ0, IRQ1, MISO/HSD					VDD = 3.3 V ± 10%
Output High Voltage, Vон	2.4			V	VDD = 3.3 V ± 10%
Isource			800	μΑ	
Output Low Voltage, Vo∟			0.4	V	$VDD = 3.3 V \pm 10\%$
Isink			2	mA	
CF1, CF2, CF3/HSCLK					
Output High Voltage, Vон	2.4			V	$VDD = 3.3 V \pm 10\%$
Isource			500	μΑ	
Output Low Voltage, Vol			0.4	V	VDD = 3.3 V ± 10%
Isink			2	mA	
POWER SUPPLY					For specified performance
PSM0 Mode					
VDD Pin	2.97		3.63	V	Minimum = 3.3 V – 10%; maximum = 3.3 V + 10%
lod		24.4	27.2	mA	
PSM1 and PSM2 Modes (ADE7868 and					
ADE7878)					
VDD Pin	2.4		3.7	V	
I <sub>DD</sub>					
PSM1 Mode		6.0		mA	
PSM2 Mode		0.2		mA	
PSM3 Mode					
VDD Pin	2.4		3.7	V	
IDD in PSM3 Mode		1.7		μA	

<sup>1</sup> See the Typical Performance Characteristics section.
<sup>2</sup> See the Terminology section for a definition of the parameters.

### **TIMING CHARACTERISTICS**

 $VDD = 3.3 V \pm 10\%$ , AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz,  $T_{MIN}$  to  $T_{MAX} = -40^{\circ}C$  to +85°C. Note that dual function pin names are referenced by the relevant function only within the timing tables and diagrams; see the Pin Configuration and Function Descriptions section for full pin mnemonics and descriptions.

### Table 3. I<sup>2</sup>C-Compatible Interface Timing Parameter

		Standard Mode Fast Mode		Mode		
Parameter	Symbol	Min	Max	Min	Max	Unit
SCL Clock Frequency	f <sub>scl</sub>	0	100	0	400	kHz
Hold Time (Repeated) Start Condition	<b>t</b> hd;sta	4.0		0.6		μs
Low Period of SCL Clock	t <sub>LOW</sub>	4.7		1.3		μs
High Period of SCL Clock	tніgн	4.0		0.6		μs
Set-Up Time for Repeated Start Condition	t <sub>su;sta</sub>	4.7		0.6		μs
Data Hold Time	thd;dat	0	3.45	0	0.9	μs
Data Setup Time	t <sub>su;dat</sub>	250		100		ns
Rise Time of Both SDA and SCL Signals	t <sub>R</sub>		1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t <sub>F</sub>		300	20	300	ns
Setup Time for Stop Condition	tsu;sto	4.0		0.6		μs
Bus Free Time Between a Stop and Start Condition	t <sub>BUF</sub>	4.7		1.3		μs
Pulse Width of Suppressed Spikes	t <sub>SP</sub>	N/A <sup>1</sup>			50	ns

<sup>1</sup> N/A means not applicable.



*Figure 5. I<sup>2</sup>C-Compatible Interface Timing* 

### Table 4. SPI Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
SS to SCLK Edge	tss	50		ns
SCLK Period		0.4	4000 <sup>1</sup>	μs
SCLK Low Pulse Width	tsl	175		ns
SCLK High Pulse Width	t <sub>sH</sub>	175		ns
Data Output Valid After SCLK Edge	t <sub>DAV</sub>		100	ns
Data Input Setup Time Before SCLK Edge	t <sub>DSU</sub>	100		ns
Data Input Hold Time After SCLK Edge	<b>t</b> DHD	5		ns
Data Output Fall Time	t <sub>DF</sub>		20	ns
Data Output Rise Time	t <sub>DR</sub>		20	ns
SCLK Rise Time	t <sub>sr</sub>		20	ns
SCLK Fall Time	t <sub>SF</sub>		20	ns
MISO Disable After SS Rising Edge	t <sub>DIS</sub>		200	ns
SS High After SCLK Edge	t <sub>SFS</sub>	0		ns

<sup>1</sup> Guaranteed by design.

.



Figure 6. SPI Interface Timing

### Table 5. HSDC Interface Timing Parameter

Parameter	Symbol	Min	Max	Unit
HSA to HSCLK Edge	tss	0		ns
HSCLK Period		125		ns
HSCLK Low Pulse Width	tsL	50		ns
HSCLK High Pulse Width	t <sub>sн</sub>	50		ns
Data Output Valid After HSCLK Edge	t <sub>DAV</sub>		40	ns
Data Output Fall Time	t <sub>DF</sub>		20	ns
Data Output Rise Time	t <sub>DR</sub>		20	ns
HSCLK Rise Time	t <sub>sr</sub>		10	ns
HSCLK Fall Time	t <sub>sF</sub>		10	ns
HSD Disable After HSA Rising Edge	t <sub>DIS</sub>	5		ns
HSA High After HSCLK Edge	t <sub>sFs</sub>	0		ns



Figure 7. HSDC Interface Timing



Figure 8. Load Circuit for Timing Specifications

# **ABSOLUTE MAXIMUM RATINGS**

 $T_A = 25^{\circ}C$ , unless otherwise noted.

### Table 6.

Parameter	Rating
VDD to AGND	–0.3 V to +3.7 V
VDD to DGND	–0.3 V to +3.7 V
Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, VCP, VN	–2 V to +2 V
Analog Input Voltage to INP and INN	–2 V to +2 V
Reference Input Voltage to AGND	–0.3 V to VDD + 0.3 V
Digital Input Voltage to DGND	–0.3 V to VDD + 0.3 V
Digital Output Voltage to DGND	–0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	-40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Note that, regarding the temperature profile used in soldering RoHS compliant parts, Analog Devices advises that reflow profiles should conform to J-STD 20 from JEDEC. Refer to www.jedec.org for the latest revision.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL RESISTANCE

 $\theta_{JA}$  is specified equal to 29.3°C/W;  $\theta_{JC}$  is specified equal to 1.8°C/W.

### Table 7. Thermal Resistance

Package Type	Αιθ	οıc	Unit
40-Lead LFCSP	29.3	1.8	°C/W

### **ESD CAUTION**



**ESD** (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# **PIN CONFIGURATION AND FUNCTION DESCRIPTIONS**



### Figure 9. Pin Configuration

### **Table 8. Pin Function Descriptions**

Pin No.	Mnemonic	Description
1, 10, 11, 20, 21, 30, 31, 40	NC	No Connect. These pins are not connected internally. It is recommended to ground these pins.
2	PM0	Power Mode Pin 0. This pin, combined with PM1, defines the power mode of the ADE7854/ADE7858/ADE7868/ADE7878, as described in Table 9.
3	PM1	Power Mode Pin 1. This pin defines the power mode of the ADE7854/ADE7858/ADE7868/ADE7878 when combined with PM0, as described in Table 9.
4	RESET	Reset Input, Active Low. In PSM0 mode, this pin should stay low for at least 10 $\mu$ s to trigger a hardware reset.
5	DVDD	2.5 V output of the digital low dropout regulator (LDO). Decouple this pin with a 4.7 μF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin.
6	DGND	Ground Reference. This pin provides the ground reference for the digital circuitry.
7,8	IAP, IAN	Analog Inputs for Current Channel A. This channel is used with the current transducers and is referenced in this document as Current Channel A. These inputs are fully differential voltage inputs with a maximum differential level of $\pm 0.5$ V. This channel also has an internal PGA equal to the ones on Channel B and Channel C.
9, 12	IBP, IBN	Analog Inputs for Current Channel B. This channel is used with the current transducers and is referenced in this document as Current Channel B. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel C and Channel A.
13, 14	ICP, ICN	Analog Inputs for Current Channel C. This channel is used with the current transducers and is referenced in this document as Current Channel C. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel A and Channel B.
15, 16	INP, INN	Analog Inputs for Neutral Current Channel N. This channel is used with the current transducers and is referenced in this document as Current Channel N. These inputs are fully differential voltage inputs with a maximum differential level of $\pm 0.5$ V. This channel also has an internal PGA, different from the ones found on the A, B, and C channels. The neutral current channel is available in the ADE7878 and ADE7868. In the ADE7858 and ADE7854, connect these pins to AGND.
17	REFIN/OUT	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. An external reference source with 1.2 V $\pm$ 8% can also be connected at this pin. In either case, decouple this pin to AGND with a 4.7 $\mu$ F capacitor in parallel with a ceramic 100 nF capacitor. After reset, the on-chip reference is enabled.

Pin No.	Mnemonic	Description
18, 19, 22, 23	VN, VCP, VBP, VAP	Analog Inputs for the Voltage Channel. This channel is used with the voltage transducer and is referenced as the voltage channel in this document. These inputs are single-ended voltage inputs with a maximum signal level of $\pm 0.5$ V with respect to VN for specified operation. This channel also has an internal PGA.
24	AVDD	2.5 V output of the analog low dropout regulator (LDO). Decouple this pin with a 4.7 μF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin.
25	AGND	Ground Reference. This pin provides the ground reference for the analog circuitry. Tie this pin to the analog ground plane or to the quietest ground reference in the system. Use this quiet ground reference for all analog circuitry, for example, antialiasing filters, current, and voltage transducers.
26	VDD	Supply Voltage. This pin provides the supply voltage. In PSM0 (normal power mode), maintain the supply voltage at 3.3 V $\pm$ 10% for specified operation. In PSM1 (reduced power mode), PSM2 (low power mode), and PSM3 (sleep mode), when the ADE7868/ADE7878 is supplied from a battery, maintain the supply voltage between 2.4 V and 3.7 V. Decouple this pin to AGND with a 10 $\mu$ F capacitor in parallel with a ceramic 100 nF capacitor. The only modes available on the ADE7858 and ADE7854 are the PSM0 and PSM3 power modes.
27	CLKIN	Master Clock. An external clock can be provided at this logic input. Alternatively, a crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7854/ADE7858/ ADE7868/ADE7878. The clock frequency for specified operation is 16.384 MHz. See the Crystal Circuit section for details on choosing a suitable crystal.
28	CLKOUT	A crystal can be connected across this pin and CLKIN (as previously described with Pin 27 in this table) to provide a clock source for the ADE7854/ADE7858/ADE7868/ADE7878.
29, 32	IRQ0, IRQ1	Interrupt Request Outputs. These are active low logic outputs. See the Interrupts section for a detailed presentation of the events that can trigger interrupts.
33, 34, 35	CF1, CF2, CF3/HSCLK	Calibration Frequency (CF) Logic Outputs. These outputs provide power information based on the CF1SEL[2:0], CF2SEL[2:0], and CF3SEL[2:0] bits in the CFMODE register. These outputs are used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the CF1DEN, CF2DEN, and CF3DEN registers, respectively (see the Energy-to-Frequency Conversion section). CF3 is multiplexed with the serial clock output of the HSDC port.
36	SCLK/SCL	Serial Clock Input for SPI Port/Serial Clock Input for I <sup>2</sup> C Port. All serial data transfers are synchronized to this clock (see the Serial Interfaces section). This pin has a Schmidt trigger input for use with a clock source that has a slow edge transition time, for example, opto-isolator outputs.
37	MISO/HSD	Data Out for SPI Port/Data Out for HSDC Port.
38	MOSI/SDA	Data In for SPI Port/Data Out for I <sup>2</sup> C Port.
39	SS/HSA	Slave Select for SPI Port/HSDC Port Active.
EP	Exposed Pad	Create a similar pad on the PCB under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package. Connect the pads to AGND and DGND.

# **TYPICAL PERFORMANCE CHARACTERISTICS**







Figure 11. Total Active Energy Error As Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off



Figure 12. Total Active Energy Error As Percentage of Reading (Gain = +1, Power Factor = 1) over Power Supply with Internal Reference and Integrator Off



Figure 13. Total Active Energy Error As Percentage of Reading (Gain = +16, Power Factor = 1) over Temperature with Internal Reference and Integrator On



Figure 14. Total Reactive Energy Error As Percentage of Reading (Gain = +1, Power Factor = 0) over Temperature with Internal Reference and Integrator Off







Figure 16. Total Reactive Energy Error As Percentage of Reading (Gain = +1, Power Factor = 0) over Power Supply with Internal Reference and Integrator Off



Figure 17. Total Reactive Energy Error As Percentage of Reading (Gain = +16, Power Factor = 0) over Temperature with Internal Reference and Integrator On



Figure 18. Fundamental Active Energy Error As Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off



Figure 19. Fundamental Active Energy Error As Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On



Figure 20. Fundamental Reactive Energy Error As Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off



Figure 21. Fundamental Reactive Energy Error As Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On





# **TEST CIRCUIT**

Note that in Figure 23, the PM1 and PM0 pins are pulled up internally to 3.3 V. Select the mode of operation by using a microcontroller to programmatically change the pin values.



Figure 23. Test Circuit

## **TERMINOLOGY**

### Measurement Error

The error associated with the energy measurement made by the ADE7854/ADE7858/ADE7868/ADE7878 is defined by

```
\frac{Measurement \ Error =}{\frac{Energy \ Registered \ by \ ADE78xx - True \ Energy}{True \ Energy} \times 100\% (1)
```

### Power Supply Rejection (PSR)

This quantifies the ADE7854/ADE7858/ADE7868/ADE7878 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at twice the fundamental frequency) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading—see the Measurement Error definition.

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied  $\pm 10\%$ . Any error introduced is expressed as a percentage of the reading.

### ADC Offset Error

This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection However, the HPF removes the offset from the current and voltage channels and the power calculation remains unaffected by this offset.

### **Gain Error**

### The gain error in the ADCs of the ADE7854/ADE7858/

ADE7868/ADE7878 is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC section and the Voltage Channel ADC section). The difference is expressed as a percentage of the ideal code.

### **CF** Jitter

The period of pulses at one of the CF1, CF2, or CF3 pins is continuously measured. The maximum, minimum, and average values of four consecutive pulses are computed as follows:

$$Maximum = max(Period_0, Period_1, Period_2, Period_3)$$
$$Minimum = min(Period_0, Period_1, Period_2, Period_3)$$
$$Average = \frac{Period_0 + Period_1 + Period_2 + Period_3}{4}$$

The CF jitter is then computed as

$$CF_{JITTER} = \frac{Maximum - Minimum}{Average} \times 100\%$$
(2)

### Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below 2 kHz, excluding harmonics and dc. The input signal contains only the fundamental component. The spectral components are calculated over a 2 sec window. The value for SNR is expressed in decibels.

### Signal-to-(Noise and Distortion) Ratio (SINAD)

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below 2 kHz, including harmonics but excluding dc. The input signal contains only the fundamental component. The spectral components are calculated over a 2 sec window. The value for SINAD is expressed in decibels.

# **POWER MANAGEMENT**

The ADE7868/ADE7878 have four modes of operation, determined by the state of the PM0 and PM1 pins (see Table 9). The ADE7854/ADE7858 have two modes of operation. These pins provide complete control of the ADE7854/ADE7858/ADE7868/ ADE7878 operation and can easily be connected to an external microprocessor I/O. The PM0 and PM1 pins have internal pullup resistors. See Table 11 and Table 12 for a list of actions that are recommended before and after setting a new power mode.

### Table 9. Power Supply Modes

Power Supply Modes	PM1	PM0
PSM0, Normal Power Mode	0	1
PSM1, Reduced Power Mode <sup>1</sup>	0	0
PSM2, Low Power Mode <sup>1</sup>	1	0
PSM3, Sleep Mode	1	1

<sup>1</sup> Available in the ADE7868 and ADE7878.

### PSM0—NORMAL POWER MODE (ALL PARTS)

In PSM0 mode, the ADE7854/ADE7858/ADE7868/ADE7878 are fully functional. The PM0 pin is set to high and the PM1 pin is set to low for the ADE78xx to enter this mode. If the ADE78xx is in one of PSM1, PSM2, or PSM3 modes and is switched into PSM0 mode, then all control registers take the default values with the exception of the threshold register, LPOILVL, which is used in PSM2 mode, and the CONFIG2 register, both of which maintain their values.

The ADE7854/ADE7858/ADE7868/ADE7878 signal the end of the transition period by triggering the IRQ1 interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is 0 during the transition period and becomes 1 when the transition is finished. The status bit is cleared and the IRQ1 pin is set back to high by writing to the STATUS1 register with the corresponding bit set to 1. Bit 15 (RSTDONE) in the interrupt mask register does not have any functionality attached even if the IRQ1 pin goes low when Bit 15 (RSTDONE) in the STATUS1 register is set to 1. This makes the RSTDONE interrupt unmaskable.

# PSM1—REDUCED POWER MODE (ADE7868, ADE7878 ONLY)

The reduced power mode, PSM1, is available on the ADE7868 and ADE7878 only. In this mode, the ADE7868/ADE7878 measure the mean absolute values (mav) of the 3-phase currents and store the results in the AIMAV, BIMAV, and CIMAV 20-bit registers. This mode is useful in missing neutral cases in which the voltage supply of the ADE7868 or ADE7878 is provided by an external battery. The serial ports, I<sup>2</sup>C or SPI, are enabled in this mode; the active port can be used to read the AIMAV, BIMAV, and CIMAV registers. It is not recommended to read any of the other registers because their values are not guaranteed in this mode. Similarly, a write operation is not taken into account by the ADE7868/ADE7878 in this mode. In summary, in this mode, it is not recommended to access any register other than AIMAV, BIMAV, and CIMAV. The circuit that measures these estimates of rms values is also active during PSM0; therefore, its calibration can be completed in either PSM0 mode or in PSM1 mode. Note that the ADE7868 and ADE7878 do not provide any register to store or process the corrections resulting from the calibration process. The external microprocessor stores the gain values in connection with these measurements and uses them during PSM1 (see the Current Mean Absolute Value Calculation—ADE7868 and ADE7878 Only section for more details on the xIMAV registers).

The 20-bit mean absolute value measurements done in PSM1, although available also in PSM0, are different from the rms measurements of phase currents and voltages executed only in PSM0 and stored in the xIRMS and xVRMS 24-bit registers. See the Current Mean Absolute Value Calculation—ADE7868 and ADE7878 Only section for details.

If the ADE7868/ADE7878 is set in PSM1 mode while still in the PSM0 mode, the ADE7868/ADE7878 immediately begin the mean absolute value calculations without any delay. The xIMAV registers are accessible at any time; however, if the ADE7878 or ADE7868 is set in PSM1 mode while still in PSM2 or PSM3 modes, the ADE7868/ADE7878 signal the start of the mean absolute value computations by triggering the IRQ1 pin low. The xIMAV registers can be accessed only after this moment.

### PSM2—LOW POWER MODE (ADE7868, ADE7878 ONLY)

The low power mode, PSM2, is available on the ADE7868 and ADE7878 only. In this mode, the ADE7868/ADE7878 compare all phase currents against a threshold for a period of  $0.02 \times$  (LPLINE[4:0] + 1) seconds, independent of the line frequency. LPLINE[4:0] are Bits[7:3] of the LPOILVL register (see Table 10).

Table 10. LPOILVL Register

Bit	Mnemonic	Default	Description
[2:0]	LPOIL[2:0]	111	Threshold is put at a value corresponding to full scale multiplied by LPOIL/8.
[7:3]	LPLINE[4:0]	00000	The measurement period is (LPLINE[4:0] + 1)/50 sec.

The threshold is derived from Bits[2:0] (LPOIL[2:0]) of the LPOILVL register as LPOIL[2:0]/8 of full scale. Every time one phase current becomes greater than the threshold, a counter is incremented. If every phase counter remains below LPLINE[4:0] + 1 at the end of the measurement period, then the IRQ0 pin is triggered low. If a single phase counter becomes greater or equal to LPLINE[4:0] + 1 at the end of the measurement period, the IRQ1 pin is triggered low. Figure 24 illustrates how the ADE7868/ADE7878 behave in PSM2 mode when LPLINE[4:0] = 2 and LPOIL[2:0] = 3. The test period is three 50 Hz cycles (60 ms), and the Phase A current rises above the LPOIL[2:0] threshold three times. At the end of the test period, the IRQ1 pin is triggered low.



The PSM2 level threshold comparison works based on a peak detection methodology. The peak detect circuit makes the comparison based on the positive terminal current channel input, I<sub>AP</sub>, I<sub>BP</sub>, and I<sub>CP</sub> (see Figure 25). In case of differential inputs being applied to the current channels, Figure 25 shows the differential antiphase signals at each of the current input terminals, I<sub>xP</sub> and I<sub>xN</sub>, and the net differential current, I<sub>xP</sub> – I<sub>xN</sub>.

The I<sup>2</sup>C or SPI port is not functional during this mode. The PSM2 mode reduces the power consumption required to monitor the currents when there is no voltage input and the voltage supply of the ADE7868/ADE7878 is provided by an external battery. If the IRQ0 pin is triggered low at the end of a measurement period, this signifies all phase currents stayed below threshold and, therefore, there is no current flowing through the system. At this point, the external microprocessor sets the ADE7868/ ADE7878 into Sleep Mode PSM3. If the IRQ1 pin is triggered low at the end of the measurement period, this signifies that at least one current input is above the defined threshold and current is flowing through the system, although no voltage is present at the ADE7868/ADE7878 pins. This situation is often called missing neutral and is considered a tampering situation, at which point the external microprocessor sets the ADE7868/ ADE7878into PSM1 mode, measures the mean absolute values of phase currents, and integrates the energy based on their values and the nominal voltage.

It is recommended to use the ADE7868/ADE7878 in PSM2 mode when Bits[2:0] (PGA1[2:0]) of the gain register are equal to 1 or 2. These bits represent the gain in the current channel datapath. It is not recommended to use the ADE7868/ADE7878 in PSM2 mode when the PGA1[2:0] bits are equal to 4, 8, or 16.

### PSM3—SLEEP MODE (ALL PARTS)

The sleep mode is available on all parts (ADE7854, ADE7858, ADE7868, and ADE7878). In this mode, the ADE78xx has most of its internal circuits turned off and the current consumption is at its lowest level. The I<sup>2</sup>C, HSDC, and SPI ports are not functional during this mode, and the RESET, SCLK/SCL, MOSI/SDA, and SS/HSA pins should be set high.

Power Mode	All Registers <sup>1</sup>	LPOILVL, CONFIG2	I <sup>2</sup> C/SPI	Functionality
PSM0	-			·
State After Hardware Reset	Set to default	Set to default	l <sup>2</sup> C enabled	All circuits are active and DSP is in idle mode.
State After Software Reset	Set to default	Unchanged	Active serial port is unchanged if lock-in procedure has been previously executed	All circuits are active and DSP is in idle mode.
PSM1—ADE7878, ADE7868 Only	Not available	Values set during PSM0 unchanged	Enabled	Current mean absolute values are computed and the results are stored in the AIMAV, BIMAV, and CIMAV registers. The I <sup>2</sup> C or SPI serial port is enabled with limited functionality.
PSM2—ADE7878, ADE7868 Only	Not available	Values set during PSM0 unchanged	Disabled	Compares phase currents against the threshold set in LPOILVL. Triggers IRQ0or IRQ1 pins accordingly. The serial ports are not available.
PSM3	Not available	Values set during PSM0 unchanged	Disabled	Internal circuits shut down and the serial ports are not available.

### Table 11. Power Modes and Related Characteristics

 $^{\scriptscriptstyle 1}$  Setting for all registers except the LPOILVL and CONFIG2 registers.

### Table 12. Recommended Actions When Changing Power Modes

	Recommended Actions	Next Power Mode			
Initial Power Mode	Before Setting Next Power Mode	PSM0	PSM1	PSM2	PSM3
PSM0	Stop DSP by setting the run register = 0x0000.		Current mean absolute values (mav) computed immediately.	Wait until the IRQ0 or IRQ1 pin is triggered accordingly.	No action necessary.
	Disable HSDC by clearing Bit 6 (HSDEN) to 0 in the CONFIG register.		xIMAV registers can be accessed immediately.		
	Mask interrupts by setting MASK0 = 0x0 and MASK1 = 0x0.				
	Erase interrupt status flags in the STATUS0 and STATUS1 registers.				
PSM1— ADE7878, ADE7868 Only	No action necessary.	Wait until the IRQ1 pin is triggered low. Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1.		Wait until the IRQ0 or IRQ1 pin is triggered accordingly.	No action necessary.
PSM2— ADE7878, ADE7868 Only	No action necessary.	Wait until the IRQ1 pin is triggered low. Poll the STATUS1 register until Bit 15 (RSTDONE) is	Wait until the IRQ1 pin triggered low. Current mean absolute values compute at this		No action necessary.
		set to 1.	moment. xIMAV registers may be accessed from this moment.		
PSM3	No action necessary.	Wait until the IRQ1 pin is triggered low. Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1.	Wait until the IRQ1 pin is triggered low. Current mav circuit begins computations at this time. xIMAV registers can be accessed from this	Wait until the IRQ0 or IRQ1 pin is triggered accordingly.	
			moment.		