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Polyphase Multifunction Energy Metering IC

Data Sheet

ADE7854A/ADE7858A/ADE7868A/ADE7878A

FEATURES

- **Highly accurate; supports EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-22, and IEC 62053-23 standards**
- **Compatible with 3-phase, 3- or 4-wire (delta or wye) meters, and other 3-phase services**
- **Supplies total (fundamental and harmonic) active, reactive, and apparent energy and fundamental active/reactive energy on each phase and on the overall system**
- **0.1% error (typical) in active and reactive energy over a dynamic range of 1000 to 1 at T_A = 25°C**
- **0.2% error (typical) in active and reactive energy over a dynamic range of 3000 to 1 at T_A = 25°C**
- **Averaged rms measurements available in low ripple rms registers**
- **Supports current transformer and di/dt current sensors**
- **Dedicated ADC channel for neutral current input**
- **Estimated neutral current measurement by calculating the rms of the sum of the phase currents in all 3 phases**
- **0.1% error (typical) in voltage and current rms over a dynamic range of 1000 to 1 at T_A = 25°C**
- **Supplies sampled waveform data on all 3 phases and on neutral current**
- **Selectable no load thresholds for total and fundamental active and reactive powers, as well as for apparent powers**
- **Highly accurate low power battery mode phase current monitoring for antitampering detection**
- **Battery supply input for missing neutral operation**
- **Phase angle measurements in current and voltage channels**
- **Calibration frequency (CF) output directly drives LED and opto-isolators**
- **Reference: 1.2 V (drift of ±5 ppm/°C typical) with external overdrive capability**
- **Single 3.3 V supply**
- **40-lead, Pb-free lead frame chip scale package (LFCSP)**
- **Operating temperature: −40°C to +85°C**
- **Flexible I²C, SPI, and HSDC serial interfaces**

GENERAL DESCRIPTION

The ADE7854A/ADE7858A/ADE7868A/ADE7878A are high accuracy, 3-phase electrical energy measurement ICs with serial interfaces and three flexible pulse outputs. The devices incorporate second-order Σ-Δ analog-to-digital converters (ADCs), a digital integrator, reference circuitry, and all signal processing required to perform total (fundamental and harmonic) active, reactive (ADE7858A, ADE7868A, and ADE7878A), and apparent energy measurement and rms calculations.

The ADE7878A can also perform fundamental-only active and reactive energy measurement and rms calculations. A fixed function digital signal processor (DSP) executes the signal processing. The DSP program is stored in the internal ROM memory.

The ADE7854A/ADE7858A/ADE7868A/ADE7878A can measure active, reactive, and apparent energy in various 3-phase configurations, such as wye or delta services, with both three and four wires. Aside from regular rms measurements, which are updated every 8 kHz, these devices measure low ripple rms values, which are averaged internally and updated every 1.024 sec. The devices provide system calibration features for each phase, that is, rms offset correction, phase calibration, and gain calibration.

The CF1, CF2, and CF3 logic outputs provide a wide selection of power information. All four devices provide total active and apparent powers, as well as the sum of the current rms values; the ADE7858A, ADE7868A, and ADE7878A also provide total reactive powers; whereas the ADE7878A provides fundamental active and reactive powers.

The ADE7854A/ADE7858A/ADE7868A/ADE7878A contain waveform sampling registers that allow access to all ADC outputs. The devices also incorporate power quality measurements, such as short duration low or high voltage detection, short duration high current variation, line voltage period measurement, and angles between phase voltages and currents.

Two serial interfaces, serial peripheral interface (SPI) and I²C, can communicate with the devices. A dedicated high speed interface, the high speed data capture (HSDC) port, can be used in conjunction with I²C to provide access to the ADC outputs and real-time power information.

The devices have two interrupt request pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$, to indicate that an enabled interrupt event has occurred. For the ADE7868A/ADE7878A, three specially designed low power modes ensure the continuity of energy accumulation when the ADE7868A/ADE7878A are in a tampering situation.

Table 1 lists each device and its functions. These devices are available in 40-lead, Pb-free LFCSP packages.

Table 1. Device Comparison

Part No.	WATT	VAR	I RMS, V RMS, and VA	di/dt	Fundamental WATT and VAR	Tamper Detect and Low Power Modes
ADE7854A	Yes	No	Yes	Yes	No	No
ADE7858A	Yes	Yes	Yes	Yes	No	No
ADE7868A	Yes	Yes	Yes	Yes	No	Yes
ADE7878A	Yes	Yes	Yes	Yes	Yes	Yes

Rev. C
Document Feedback

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REVISION HISTORY

5/2016—Rev. B to Rev. C

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Changes to Figure 23 ... 19
Changes to Figure 27 ... 25
Changes to Silicon Anomaly Section ... 70

7/2014—Revision A: Initial Version

FUNCTIONAL BLOCK DIAGRAMS

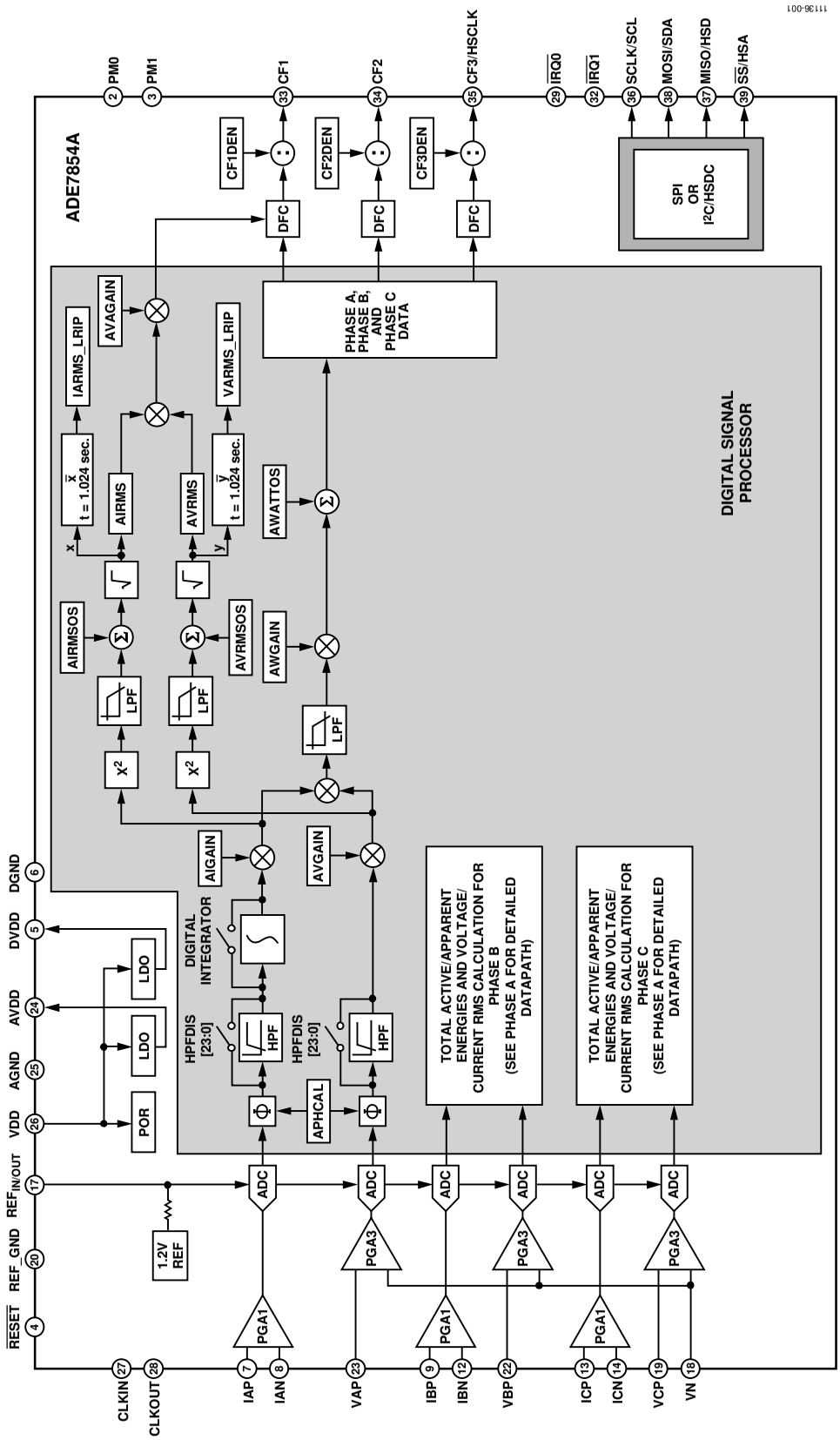

Figure 1. ADE7854A Functional Block Diagram

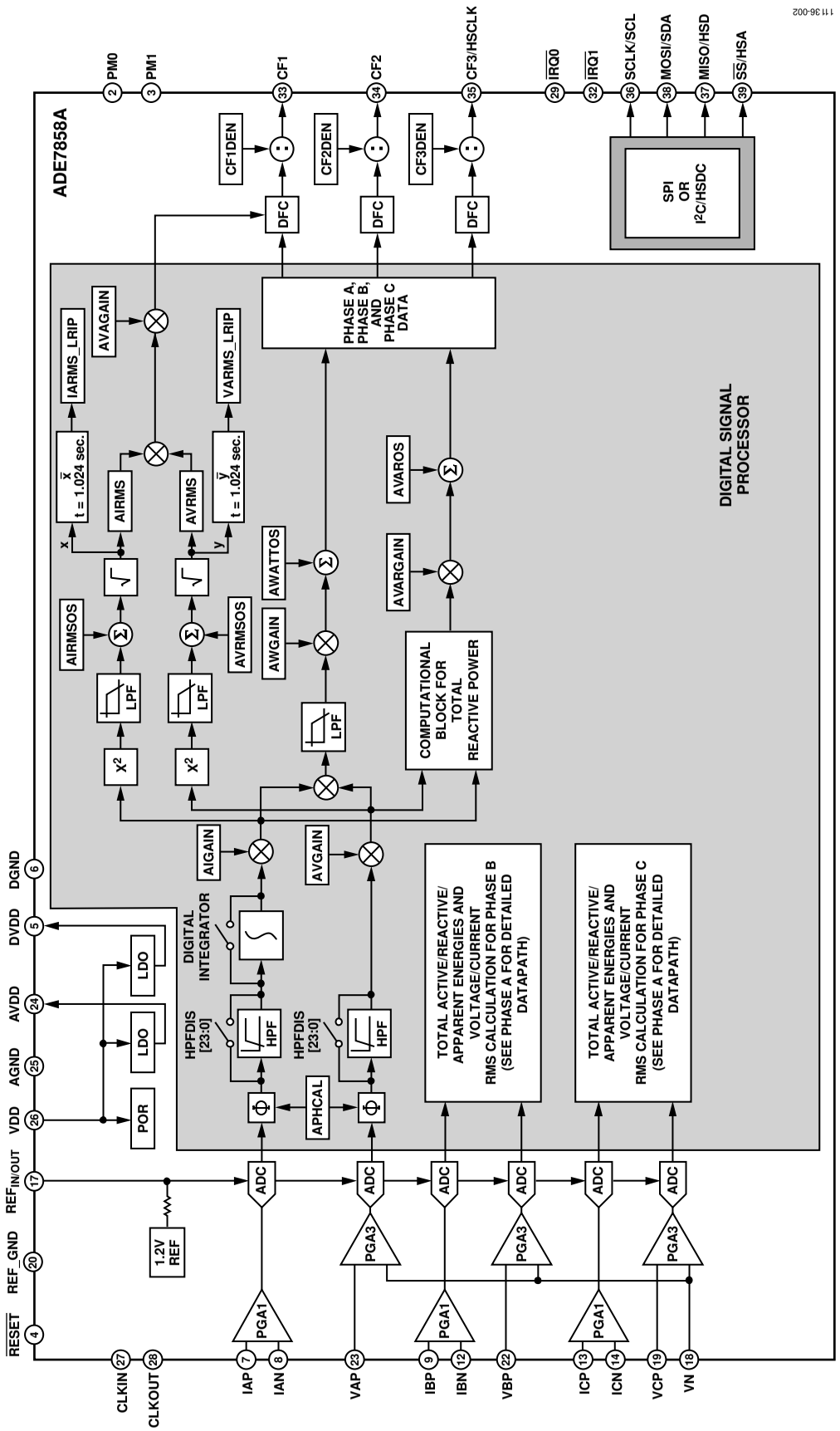

Figure 2. ADE7858A Functional Block Diagram

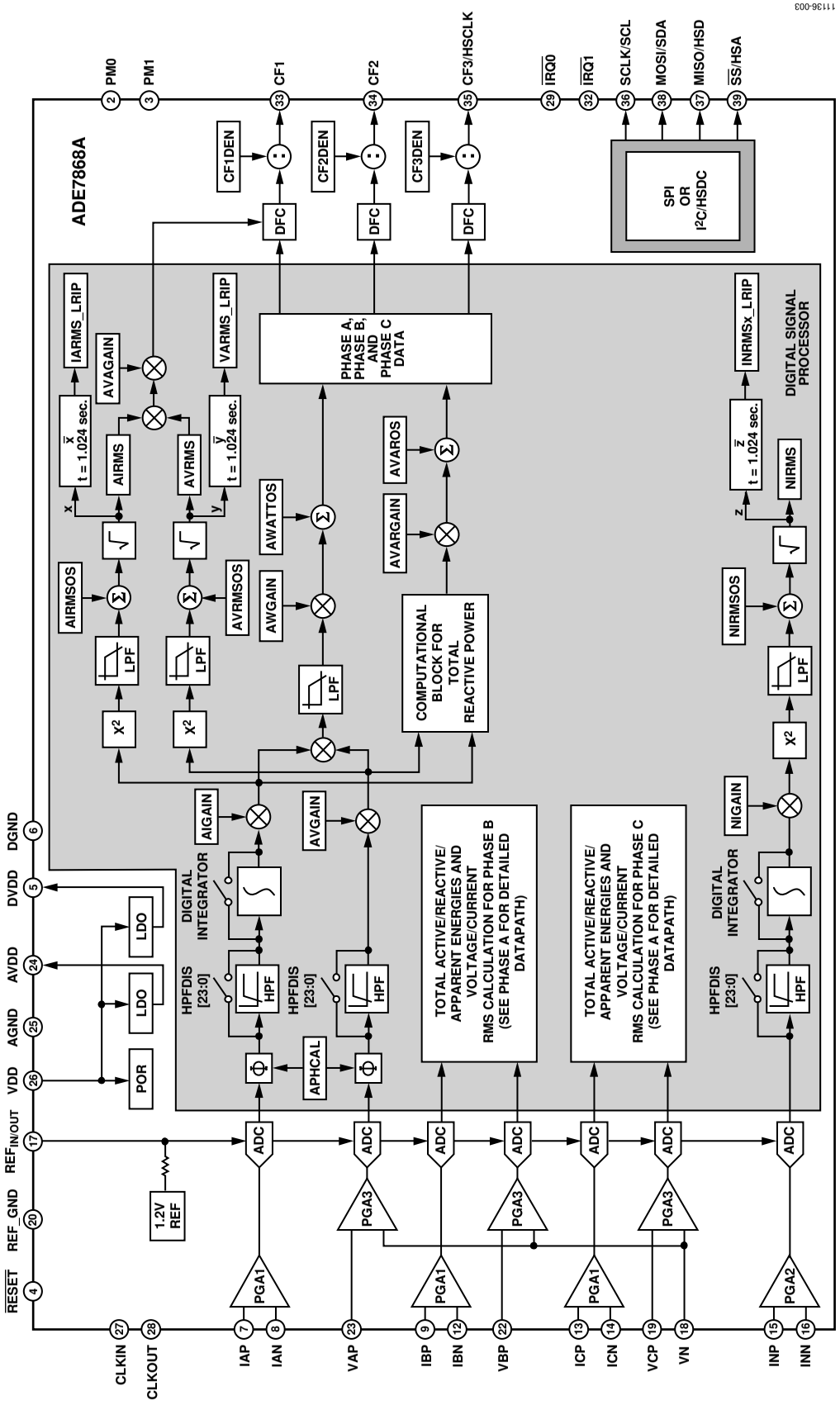

Figure 3. ADE7868A Functional Block Diagram

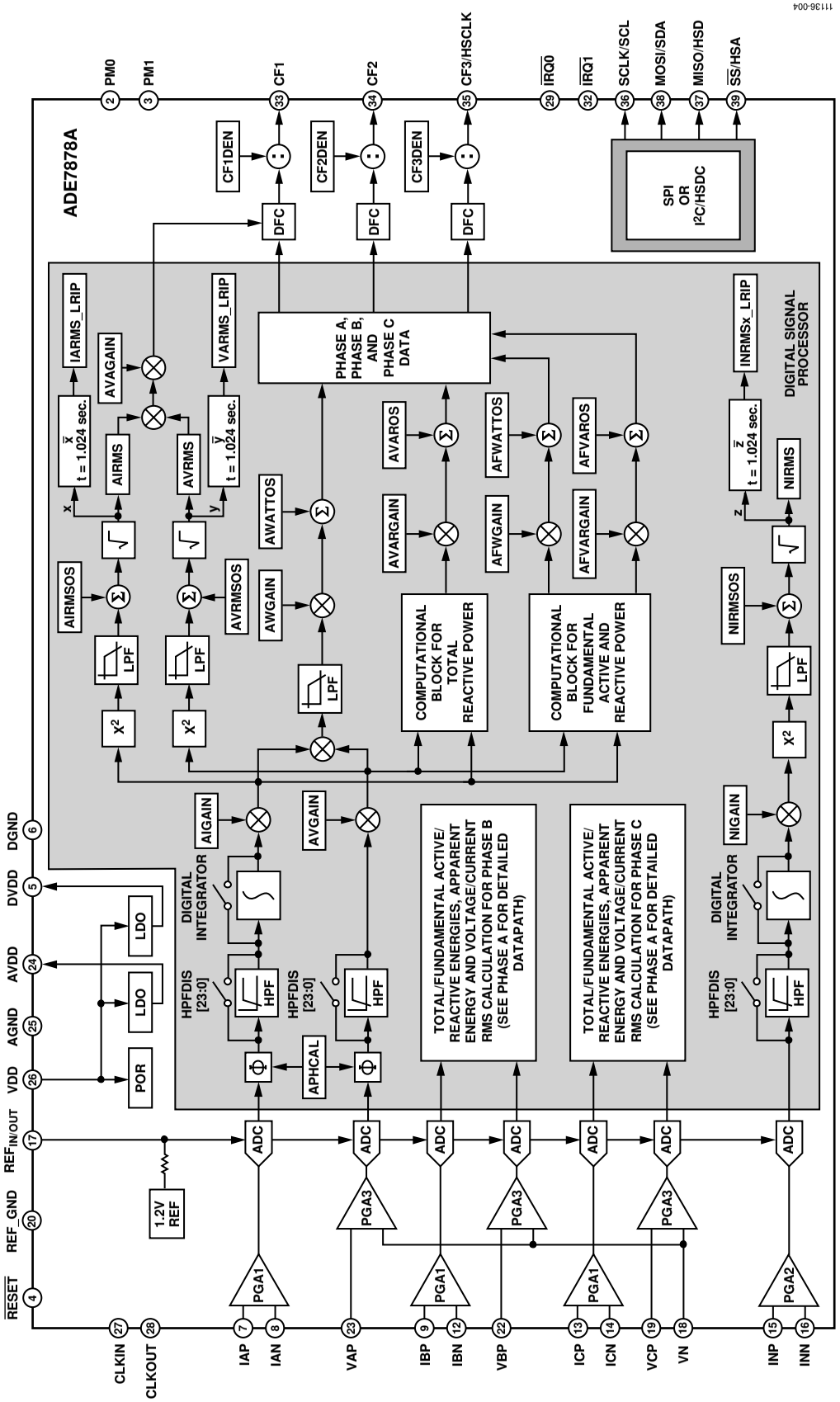

Figure 4. ADE7878A Functional Block Diagram

SPECIFICATIONS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP} = 25°C, unless otherwise noted.

Table 2.

Parameter[1, 2, 3]	Min	Typ	Max	Unit	Test Conditions/Comments
ACTIVE ENERGY MEASUREMENT (PSM0 MODE)					
Active Energy Measurement Error (Per Phase)					
Total Active Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
Fundamental Active Energy					ADE7878A only
		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms at 120 Hz/100 Hz, IxP = VxP = ±100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc, IxP = VxP = ±100 mV rms
Output Frequency Variation		0.01		%	
Total Active Energy Measurement Bandwidth		2		kHz	
REACTIVE ENERGY MEASUREMENT (PSM0 MODE)					ADE7858A, ADE7868A, and ADE7878A
Reactive Energy Measurement Error (Per Phase)					
Total Reactive Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
Fundamental Reactive Energy					ADE7878A only
		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off
		0.2		%	Over a dynamic range of 3000 to 1, PGA = 1, 2, 4; integrator off
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms at 120 Hz/100 Hz, IxP = VxP = ±100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc, IxP = VxP = ±100 mV rms
Output Frequency Variation		0.01		%	
Total Reactive Energy Measurement Bandwidth		2		kHz	
RMS MEASUREMENTS (PSM0 MODE)					
Current (I) RMS and Voltage (V) RMS Measurement Bandwidth		2		kHz	
I RMS and V RMS Measurement Error		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1
MEAN ABSOLUTE VALUE (MAV) MEASUREMENT (PSM1 Mode)					ADE7868A and ADE7878A
I MAV Measurement Bandwidth		260		Hz	
I MAV Measurement Error		0.5		%	Over a dynamic range of 100 to 1, PGA = 1, 2, 4, 8

Parameter[1, 2, 3]	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG INPUTS					
Maximum Signal Levels			±500	mV peak	PGA = 1, differential or single-ended inputs between the following pins: IAP and IAN, IBP and IBN, ICP and ICN, INP and INN; single-ended inputs between the following pins: VAP and VN, VBP and VN, VCP and VN
Input Impedance (DC)					
IAP, IAN, IBP, IBN, ICP, ICN, INP, INN, VAP, VBP, and VCP Pins	400			kΩ	
VN Pin	130			kΩ	
ADC Offset		−34		mV	PGA = 1; see the Terminology section
Gain Error		±4		%	External 1.2 V reference
WAVEFORM SAMPLING					Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS
Current and Voltage Channels					See the Waveform Sampling Mode section
Signal-to-Noise Ratio, SNR		74		dB	PGA = 1, fundamental frequency = 45 Hz to 65 Hz; see the Terminology section
Signal-to-Noise-and-Distortion (SINAD) Ratio		74		dB	PGA = 1, fundamental frequency = 45 Hz to 65 Hz; see the Terminology section
Bandwidth (−3 dB)		2		kHz	
TIME INTERVAL BETWEEN PHASES					
Measurement Error		0.3		Degrees	Line frequency = 45 Hz to 65 Hz, HPF on
CF1, CF2, CF3 PULSE OUTPUTS					
Maximum Output Frequency		8		kHz	WTHR = VARTHR = VATHR = PMAX = 33,516,139
Duty Cycle		50		%	CF1, CF2, or CF3 frequency > 6.25 Hz, CFDEN is even and > 1
		(1 + 1/CFDEN) × 50%			CF1, CF2, or CF3 frequency > 6.25 Hz, CFDEN is odd and > 1
Active Low Pulse Width		80		ms	CF1, CF2, or CF3 frequency < 6.25 Hz
Jitter		0.04		%	CF1, CF2, or CF3 frequency = 1 Hz, nominal phase currents larger than 10% of full scale
REFERENCE INPUT					
$REF_{IN/OUT}$ Input Voltage Range	1.1		1.3	V	Minimum = 1.2 V − 8%; maximum = 1.2 V + 8%
Input Capacitance			10	pF	
ON-CHIP REFERENCE, PSM0 AND PSM1 MODES					Nominal 1.2 V at the $REF_{IN/OUT}$ pin at T_A = 25°C
Temperature Coefficient	−32	±5	+32	ppm/°C	Drift across the entire temperature range of −40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section
CLKIN					CLKIN = 16.384 MHz; see the Crystal Circuit section
Input Clock Frequency	16.22	16.384	16.55	MHz	
LOGIC INPUTS—MOSI/SDA, SCLK/SCL, $\overline{SS}$/HSA, $\overline{RESET}$, PM0, AND PM1					
Input High Voltage, V_{INH}	2.0			V	VDD = 3.3 V ± 10%
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V ± 10%
Input Current, I_{IN}			−8.7	μA	Input = 0 V, VDD = 3.3 V
			3	μA	Input = VDD = 3.3 V
Input Capacitance, C_{IN}		10		pF	
LOGIC OUTPUTS, $\overline{IRQ0}$, $\overline{IRQ1}$, MISO/HSD					
Output High Voltage, V_{OH}	2.4			V	VDD = 3.3 V ± 10%
I_{SOURCE}			800	μA	
Output Low Voltage, V_{OL}			0.4	V	VDD = 3.3 V ± 10%
I_{SINK}			2	mA	

Parameter[1, 2, 3]	Min	Typ	Max	Unit	Test Conditions/Comments
CF1, CF2, CF3/HSCLK					
Output High Voltage, V_{OH}	2.4			V	VDD = 3.3 V ± 10%
I_{SOURCE}			500	µA	
Output Low Voltage, V_{OL}			0.4	V	VDD = 3.3 V ± 10%
I_{SINK}			8	mA	
POWER SUPPLY					For specified performance
PSM0 Mode					
VDD Pin	2.97		3.63	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
I_{DD}		20	23	mA	
PSM1 and PSM2 Modes					ADE7868A and ADE7878A
VDD Pin	2.8		3.7	V	
I_{DD}					
PSM1 Mode		4.5		mA	
PSM2 Mode		0.2		mA	
PSM3 Mode					
VDD Pin	2.8		3.7	V	
I_{DD}		1.7		µA	

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for a definition of the parameters.
[3] Note that dual function pin names are referenced by the relevant function only (see the Pin Configuration and Function Descriptions section for full pin mnemonics and descriptions).

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C. Note that within the timing tables and diagrams, dual function pin names are referenced by the relevant function only (see the Pin Configuration and Function Descriptions section for full pin mnemonics and descriptions).

I²C Interface Timing

Table 3.

		Standard Mode		Fast Mode		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time for Start and Repeated Start Conditions	$t_{HD;STA}$	4.0		0.6		µs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		µs
High Period of SCL Clock	t_{HIGH}	4.0		0.6		µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$	4.7		0.6		µs
Data Hold Time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data Setup Time	$t_{SU;DAT}$	250		100		ns
Rise Time of SDA and SCL Signals	t_R		1000	20	300	ns
Fall Time of SDA and SCL Signals	t_F		300	20	300	ns
Setup Time for Stop Condition	$t_{SU;STO}$	4.0		0.6		µs
Bus Free Time Between a Stop and Start Condition	t_{BUF}	4.7		1.3		µs
Pulse Width of Suppressed Spikes	t_{SP}	N/A[1]			50	ns

[1] N/A means not applicable.

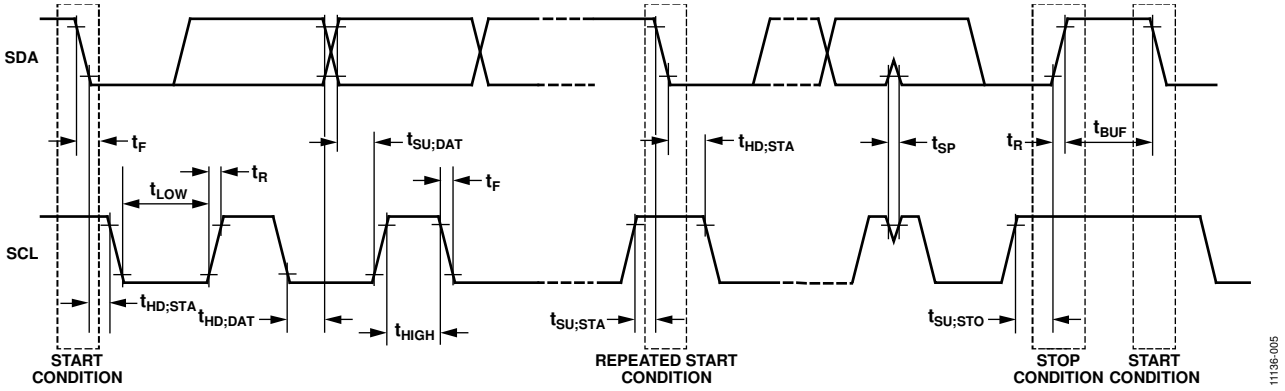

Figure 5. I²C Interface Timing

SPI Interface Timing

Table 4.

Parameter	Symbol	Min	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	50		ns
SCLK Period		0.4	4000[1]	µs
SCLK Low Pulse Width	t_{SL}	175		ns
SCLK High Pulse Width	t_{SH}	175		ns
Data Output Valid After SCLK Edge	t_{DAV}		100	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	100		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	5		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}		200	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0		ns

[1] Guaranteed by design.

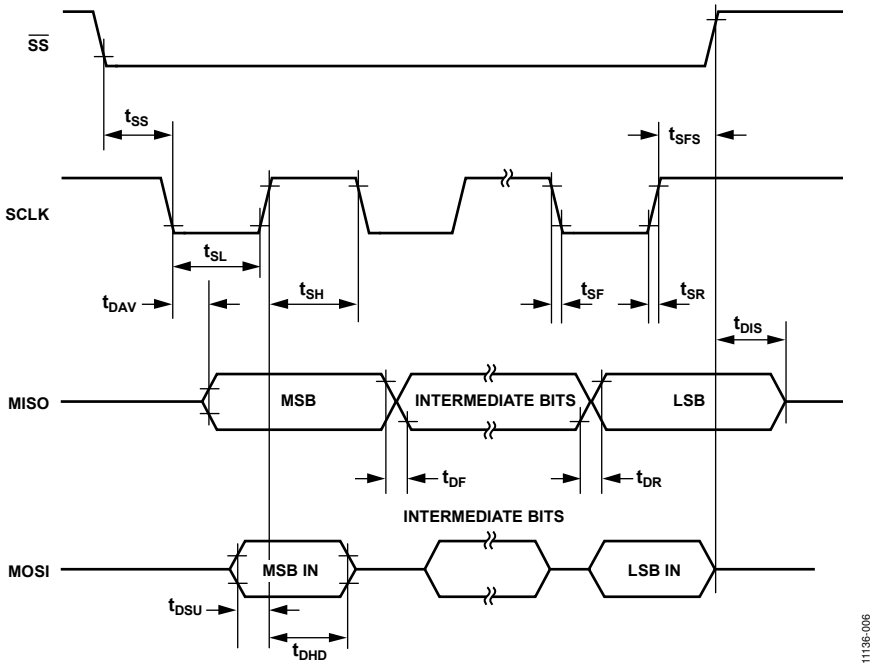

Figure 6. SPI Interface Timing

HSDC Interface Timing

Table 5.

Parameter	Symbol	Min	Max	Unit
HSA to HSCLK Edge	t_{SS}	0		ns
HSCLK Period		125		ns
HSCLK Low Pulse Width	t_{SL}	50		ns
HSCLK High Pulse Width	t_{SH}	50		ns
Data Output Valid After HSCLK Edge	t_{DAV}		40	ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
HSCLK Rise Time	t_{SR}		10	ns
HSCLK Fall Time	t_{SF}		10	ns
HSD Disable After HSA Rising Edge	t_{DIS}	5		ns
HSA High After HSCLK Edge	t_{SFS}	0		ns

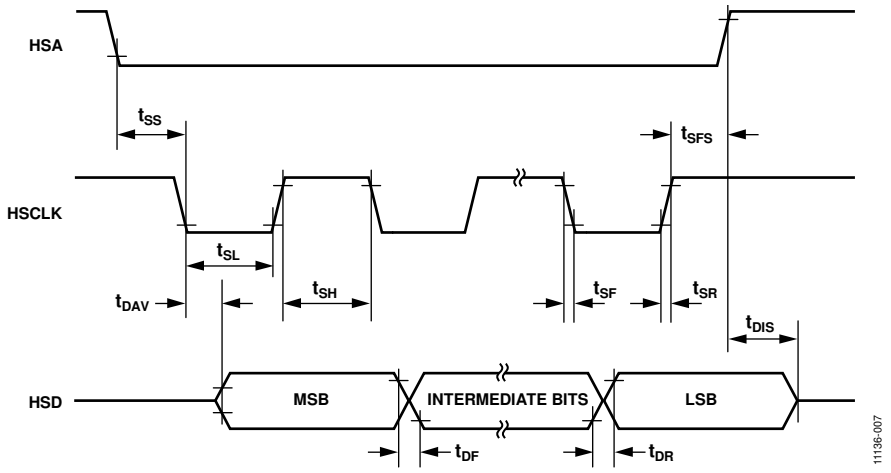

Figure 7. HSDC Interface Timing

Load Circuit for Timing Specifications

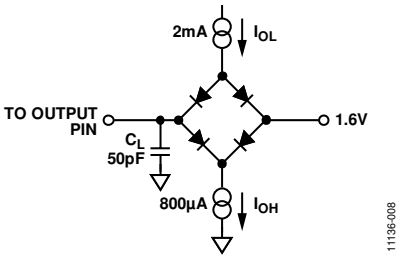

Figure 8. Load Circuit for Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
VDD to AGND	−0.3 V to +3.7 V
VDD to DGND	−0.3 V to +3.7 V
Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, VCP, VN	−2 V to +2 V
Analog Input Voltage to INP and INN	−2 V to +2 V
Reference Input Voltage to AGND	−0.3 V to VDD + 0.3 V
Digital Input Voltage to DGND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified at 29.3°C/W; θ_{JC} is specified at 1.8°C/W.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	29.3	1.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

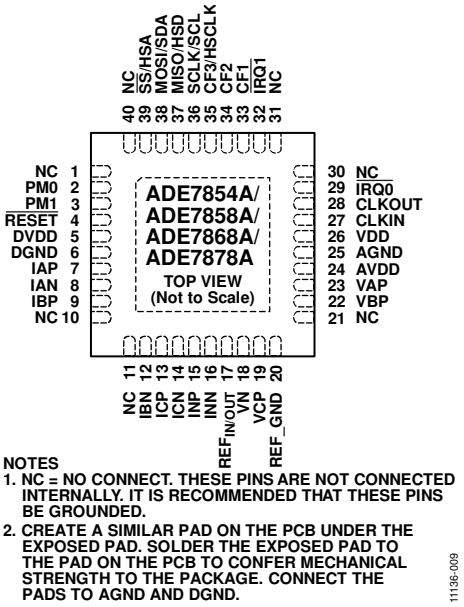

Figure 9. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10, 11, 21, 30, 31, 40	NC	No Connect. These pins are not connected internally. It is recommended that these pins be grounded.
2	PM0	Power Mode Pin 0. The PM0 and PM1 pins together specify the power mode of the ADE7854A, ADE7858A, ADE7868A, and ADE7878A (see Table 9).
3	PM1	Power Mode Pin 1. The PM1 and PM0 pins together specify the power mode of the ADE7854A, ADE7858A, ADE7868A, and ADE7878A (see Table 9).
4	$\overline{\text{RESET}}$	Reset Input, Active Low. In PSM0 mode, this pin must stay low for at least 10 µs to trigger a hardware reset.
5	DVDD	2.5 V Output of the Digital Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin.
6	DGND	Ground Reference for the Digital Circuitry.
7, 8	IAP, IAN	Analog Inputs, Current Channel A. Current Channel A is used with the current transducers. The IAP (positive) and IAN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V peak. Channel A also has an internal PGA, which is set to the same value as the PGAs used by Channel B and Channel C.
9, 12	IBP, IBN	Analog Inputs, Current Channel B. Current Channel B is used with the current transducers.. The IBP (positive) and IBN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V peak. Channel B also has an internal PGA, which is set to the same value as the PGAs used by Channel A and Channel C.
13, 14	ICP, ICN	Analog Inputs, Current Channel C. Current Channel C is used with the current transducers. The ICP (positive) and ICN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V peak. Channel C also has an internal PGA, which is set to the same value as the PGAs used by Channel A and Channel B.
15, 16	INP, INN	Analog Inputs, Neutral Current Channel N. Current Channel N is used with the current transducers. The INP (positive) and INN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V peak. Channel N also has an internal PGA, which is separate from the PGA used by Channel A, Channel B, and Channel C. The neutral current channel is available in the ADE7868A and ADE7878A only. In the ADE7854A and ADE7858A, connect the INP and INN pins to AGND.
17	$\text{REF}_{\text{IN/OUT}}$	The $\text{REF}_{\text{IN/OUT}}$ pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. An external reference source with 1.2 V ± 8% can also be connected at this pin. In either case, decouple $\text{REF}_{\text{IN/OUT}}$ to AGND with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor. After a reset, the on-chip reference is enabled.

Pin No.	Mnemonic	Description
18, 19, 22, 23	VN, VCP, VBP, VAP	Analog Inputs, Voltage Channels. These channels are used with the voltage transducer. The VN, VCP, VBP, and VAP inputs are single-ended voltage inputs with a maximum signal level of ±0.5 V peak with respect to VN for specified operation. Each voltage channel also has an internal PGA.
20	REF_GND	Ground Reference, Internal Voltage Reference. Connect REF_GND to the analog ground plane.
24	AVDD	2.5 V Output of the Analog Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin.
25	AGND	Ground Reference for the Analog Circuitry. Tie AGND to the analog ground plane or to the quietest ground reference in the system. Use this quiet ground reference for all analog circuitry, for example, antialiasing filters, current transducers, and voltage transducers.
26	VDD	Supply Voltage. The VDD pin provides the supply voltage. In PSM0 (normal power) mode, maintain the supply voltage at 3.3 V ± 10% for specified operation. In PSM1 (reduced power) mode, PSM2 (low power) mode, and PSM3 (sleep) mode, when the ADE7868A or ADE7878A is supplied from a battery, maintain the supply voltage from 2.8 V to 3.7 V. Decouple VDD to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor. The only power modes available on the ADE7858A and ADE7854A are the PSM0 and PSM3 modes.
27	CLKIN	Master Clock. An external clock can be provided at this logic input. Alternatively, a crystal can be connected across the CLKIN and CLKOUT pins to provide a clock source for the ADE7854A, ADE7858A, ADE7868A, or ADE7878A. The clock frequency for specified operation is 16.384 MHz. For information about choosing a suitable crystal, see the Crystal Circuit section.
28	CLKOUT	Crystal Output. A crystal can be connected across the CLKIN and CLKOUT pins to provide a clock source for the ADE7854A, ADE7858A, ADE7868A, or ADE7878A. The clock frequency for specified operation is 16.384 MHz. For information about choosing a suitable crystal, see the Crystal Circuit section.
29, 32	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$	Interrupt Request Outputs. These pins are active low logic outputs. For information about events that trigger interrupts, see the Interrupts section.
33, 34, 35	CF1, CF2, CF3/HSCLK	Calibration Frequency Logic Outputs/Serial Clock Output of the HSDC Port. The CF1, CF2, and CF3/HSCLK outputs provide power information based on the CF1SEL[2:0], CF2SEL[2:0], and CF3SEL[2:0] bits in the CFMODE register. Use these outputs for operational and calibration purposes. Scale the full-scale output frequency by writing to the CF1DEN, CF2DEN, and CF3DEN registers (see the Energy to Frequency Conversion section). CF3 is multiplexed with HSCLK.
36	SCLK/SCL	Serial Clock Input for the SPI Port/Serial Clock Input for the I^2C Port. All serial data transfers synchronize to this clock (see the Serial Interfaces section). The SCLK/SCL pin has a Schmitt trigger input for use with a clock source that has a slow edge transition time, for example, opto-isolator outputs.
37	MISO/HSD	Data Output for the SPI Port/Data Output for the HSDC Port.
38	MOSI/SDA	Data Input for the SPI Port/Data Input and Output for the I^2C Port.
39	$\overline{\text{SS}}$/HSA	Slave Select for the SPI Port/HSDC Port Active.
	EP	Exposed Pad. Create a similar pad on the printed circuit board (PCB) under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package. Connect the pads to AGND and DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

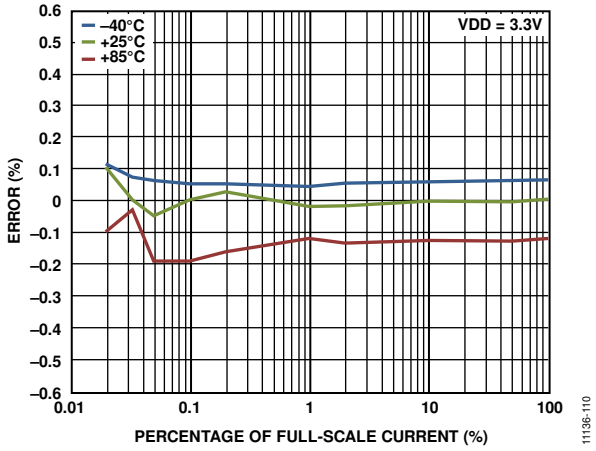

Figure 10. Total Active Energy Error as a Percentage of Reading (Gain = +1, Power Factor = 1) vs. Percentage of Full-Scale Current over Temperature with Internal Reference and Integrator Off

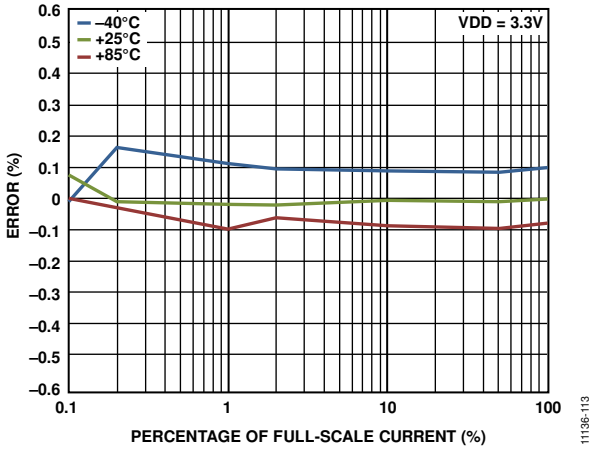

Figure 13. Total Active Energy Error as a Percentage of Reading (Gain = +16, Power Factor = 1) vs. Percentage of Full-Scale Current over Temperature with Internal Reference and Integrator On

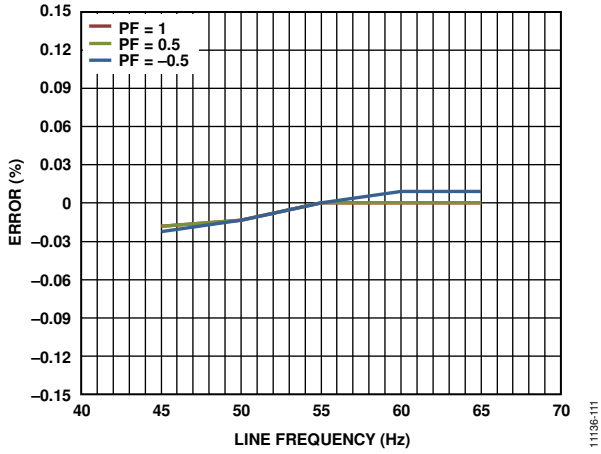

Figure 11. Total Active Energy Error as a Percentage of Reading (Gain = +1) vs. Line Frequency over Power Factor with Internal Reference and Integrator Off

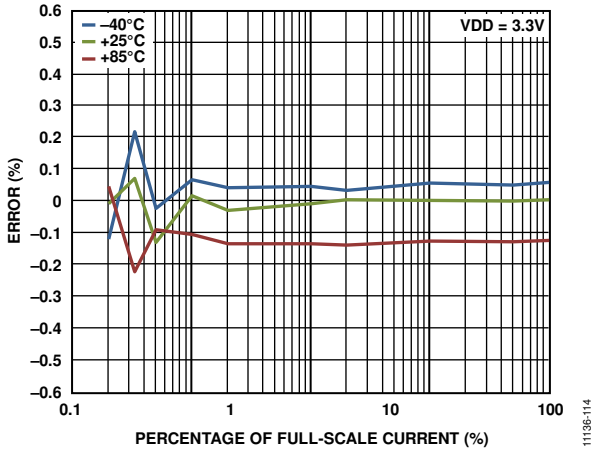

Figure 14. Total Reactive Energy Error as a Percentage of Reading (Gain = +1, Power Factor = 0) vs. Percentage of Full-Scale Current over Temperature with Internal Reference and Integrator Off

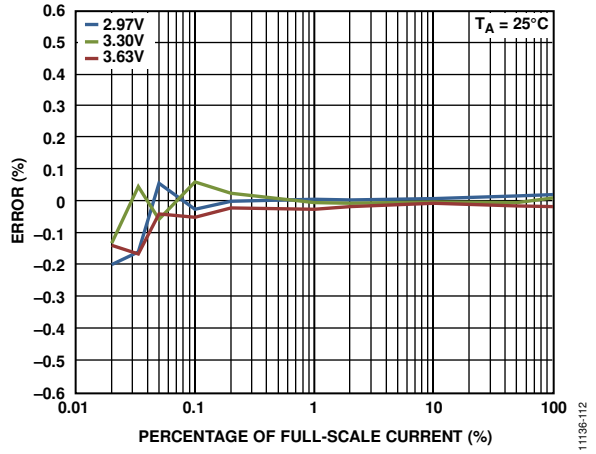

Figure 12. Total Active Energy Error as a Percentage of Reading (Gain = +1, Power Factor = 1) vs. Percentage of Full-Scale Current over Power Supply with Internal Reference and Integrator Off

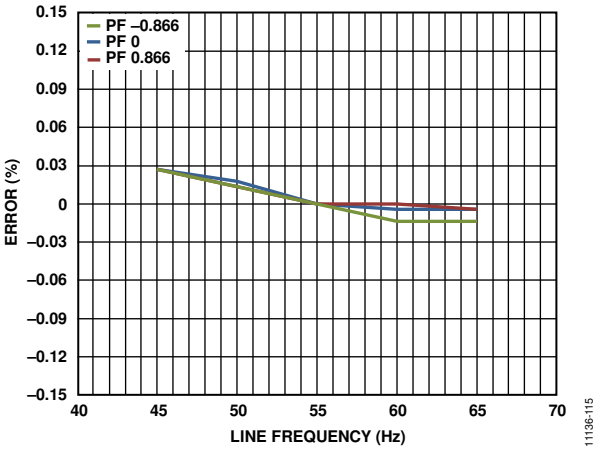

Figure 15. Total Reactive Energy Error as a Percentage of Reading (Gain = +1) vs. Line Frequency over Power Factor with Internal Reference and Integrator Off

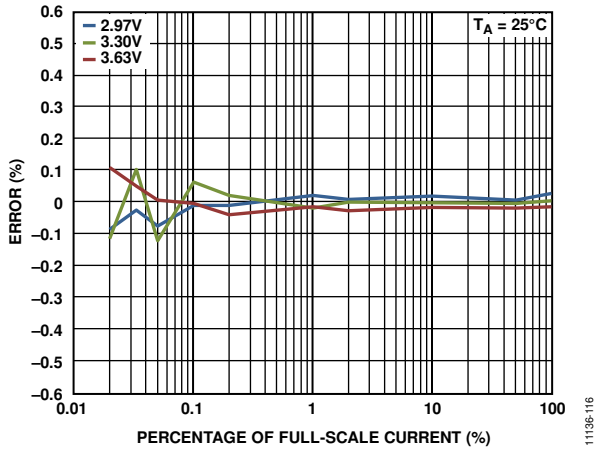

Figure 16. Total Reactive Energy Error as a Percentage of Reading (Gain = +1, Power Factor = 0) vs. Percentage of Full-Scale Current over Power Supply with Internal Reference and Integrator Off

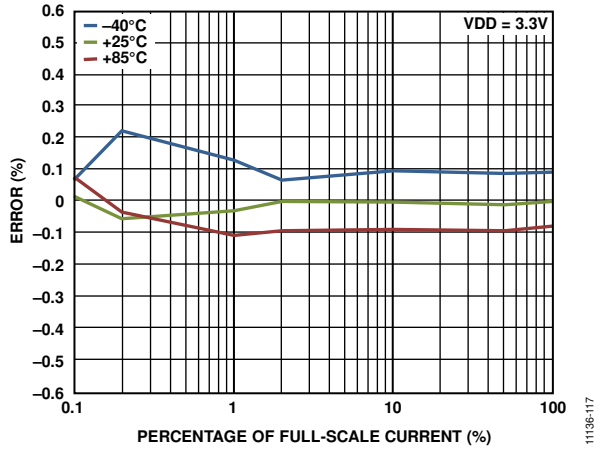

Figure 17. Total Reactive Energy Error as a Percentage of Reading (Gain = +16, Power Factor = 0) vs. Percentage of Full-Scale Current over Temperature with Internal Reference and Integrator On

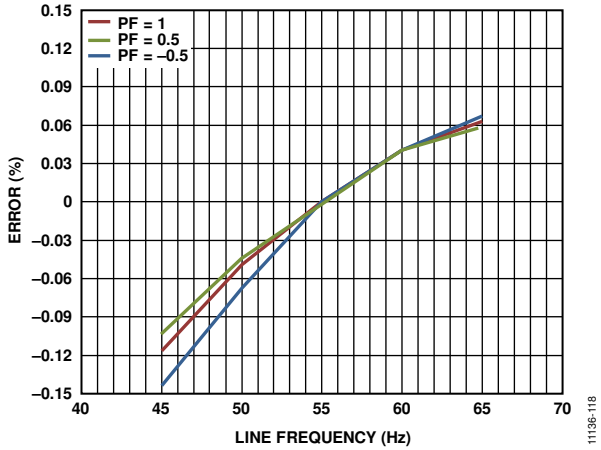

Figure 18. Fundamental Active Energy Error as a Percentage of Reading (Gain = +1) vs. Line Frequency over Power Factor over Frequency with Internal Reference and Integrator Off

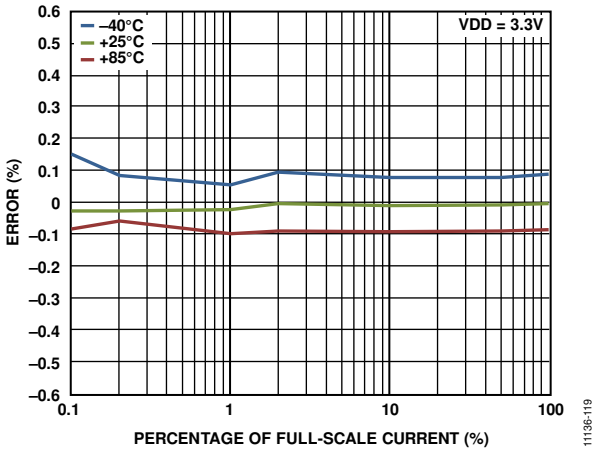

Figure 19. Fundamental Active Energy Error as a Percentage of Reading (Gain = +16) vs. Percentage of Full-Scale Current over Temperature with Internal Reference and Integrator On

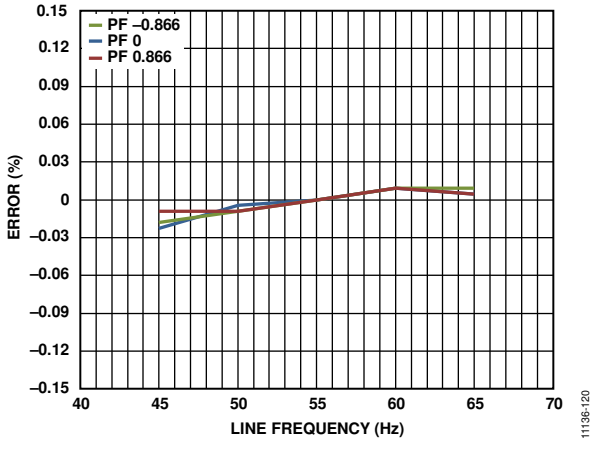

Figure 20. Fundamental Reactive Energy Error as a Percentage of Reading (Gain = +1) vs. Line Frequency over Power Factor with Internal Reference and Integrator Off

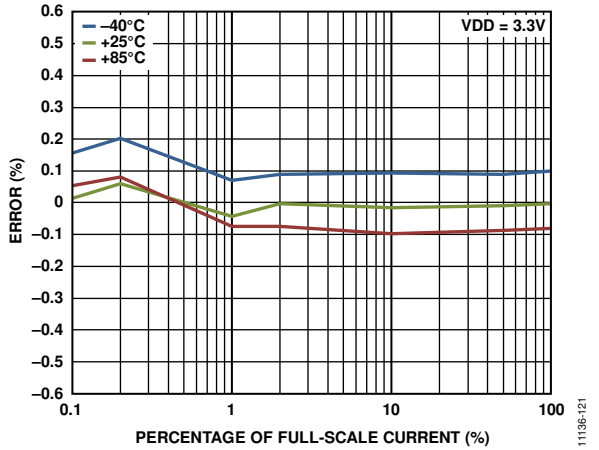

Figure 21. Fundamental Reactive Energy Error as a Percentage of Reading (Gain = +16) vs. Percentage of Full-Scale Current over Temperature with Internal Reference and Integrator On

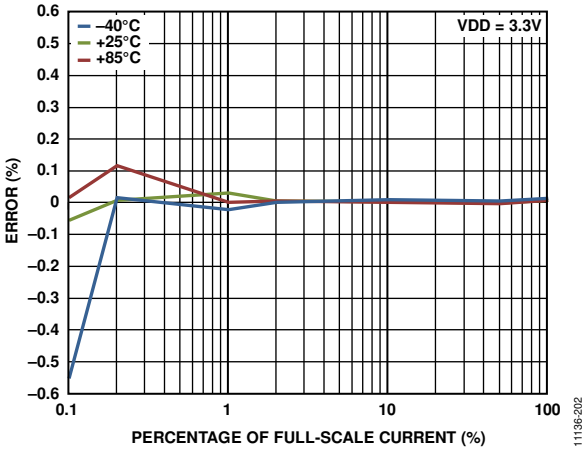

Figure 22. I RMS Error as a Percentage of Reading (Gain = +1, Power Factor = 1) vs. Percentage of Full-Scale Current over Temperature with Internal Reference and Integrator Off

TEST CIRCUIT

In Figure 23, the PM1 and PM0 pins are pulled up internally to VDD. Select the mode of operation by using a microcontroller to programmatically change the pin values (see the Power Management section).

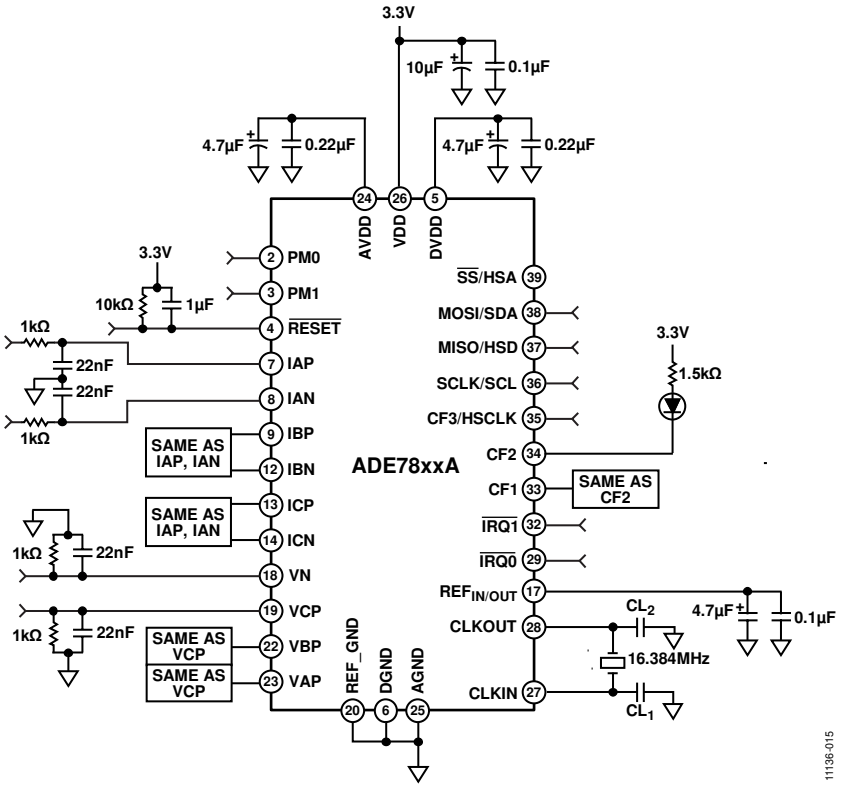

Figure 23. Test Circuit

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7854A/ADE7858A/ADE7868A/ADE7878A is defined as follows:

$$Measurement\ Error = \frac{Energy\ Registered\ by\ Device - True\ Energy}{True\ Energy} \times 100\% \quad (1)$$

where *Device* represents the ADE7854A, ADE7858A, ADE7868A, or ADE7878A.

Power Supply Rejection (PSR)

PSR quantifies the ADE7854A/ADE7858A/ADE7868A/ADE7878A measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at twice the fundamental frequency) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading.

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied by ±10%. Any error introduced is expressed as a percentage of the reading.

ADC Offset

ADC offset refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection. The high-pass filter (HPF) removes the offset from the current and voltage channels; therefore, the power calculation remains unaffected by this offset.

Gain Error

The gain error in the ADCs of the ADE7854A/ADE7858A/ADE7868A/ADE7878A is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC and Voltage Channel ADC sections). The difference is expressed as a percentage of the ideal code.

CF Jitter

The period of pulses at one of the CF1, CF2, or CF3/HSCLK pins is continuously measured. The maximum, minimum, and average values of four consecutive pulses are computed, as follows:

$$Maximum = max(Period_0, Period_1, Period_2, Period_3)$$

$$Minimum = min(Period_0, Period_1, Period_2, Period_3)$$

$$Average = \frac{Period_0 + Period_1 + Period_2 + Period_3}{4}$$

The CF jitter is then computed as follows:

$$CF_{JITTER} = \frac{Maximum - Minimum}{Average} \times 100\% \quad (2)$$

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below 2 kHz, excluding harmonics and dc. The input signal contains only the fundamental component. The spectral components are calculated over a 2 sec window. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below 2 kHz, including harmonics but excluding dc. The input signal contains only the fundamental component. The spectral components are calculated over a 2 sec window. The value for SINAD is expressed in decibels.

POWER MANAGEMENT

The ADE7868A/ADE7878A have four modes of operation and the ADE7854A/ADE7858A have two modes of operation; the modes of operation are determined by the state of the PM0 and PM1 pins (see Table 9).

Table 9. Power Supply Modes

Power Supply Mode	PM1 Pin	PM0 Pin
PSM0, Normal Power Mode	0	1
PSM1, Reduced Power Mode[1]	0	0
PSM2, Low Power Mode[1]	1	0
PSM3, Sleep Mode	1	1

[1] Available in the ADE7868A and ADE7878A only.

The PM1 and PM0 pins control the operation of the ADE7854A/ADE7858A/ADE7868A/ADE7878A. These pins are easily connected to an external microprocessor input/output. The PM1 and PM0 pins include internal pull-up resistors; therefore, the ADE7854A/ADE7858A/ADE7868A/ADE7878A are in sleep mode by default. For recommended actions to take before and after setting a new power mode, see Table 11 and Table 12.

PSM0 NORMAL POWER MODE (ALL DEVICES)

In PSM0 normal power mode (PSM0 mode), the ADE7854A/ADE7858A/ADE7868A/ADE7878A are fully functional. To enter PSM0 mode, the PM1 pin is set low and the PM0 pin is set high. When a device is in PSM1, PSM2, or PSM3 mode and switches to PSM0 mode, all control registers revert to their default values, except for the threshold register, LPOILVL (which is used in PSM2 mode), and the CONFIG2 register. These registers maintain their programmed values.

The ADE7854A/ADE7858A/ADE7868A/ADE7878A signal the completion of the power-up procedure by driving the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. Bit 15 is cleared to 0 during the power-up sequence and is set to 1 when the chip enters PSM0 mode. Writing to the STATUS1 register with the RSTDONE bit set to 1 clears the status bit and returns the $\overline{\text{IRQ1}}$ pin high.

The RSTDONE interrupt cannot be masked because Bit 15 (RSTDONE) in the interrupt mask register has no functionality.

PSM1 REDUCED POWER MODE (ADE7868A AND ADE7878A ONLY)

The PSM1 reduced power mode (PSM1 mode) is available on the ADE7868A and ADE7878A only. In PSM1 mode, the ADE7868A/ADE7878A measure the mean absolute values (MAV) of the 3-phase currents and store the results in the 20-bit AIMAV, BIMAV, and CIMAV registers. PSM1 mode is useful in missing neutral cases where an external battery provides the voltage supply for the ADE7868A or ADE7878A.

The I²C or SPI serial port is enabled in PSM1 mode and can be used to read the AIMAV, BIMAV, and CIMAV registers. Do not read any other registers because their values are not guaranteed in PSM1 mode. Similarly, a write operation in PSM1 mode is ignored by the ADE7868A/ADE7878A. In PSM1 mode, do not access any registers other than AIMAV, BIMAV, and CIMAV. For more information about the xIMAV registers, see the Current Mean Absolute Value Calculation—ADE7868A and ADE7878A Only section.

The circuit that measures the estimates of rms values is also active during PSM0 mode; therefore, the calibration of this circuit can be done in either PSM0 mode or PSM1 mode. Note that the ADE7868A and ADE7878A do not provide registers to store or process the corrections resulting from the calibration process. The external microprocessor stores the gain values from these measurements and uses them during PSM1 mode.

The 20-bit mean absolute value measurements that are completed in PSM1 mode are available in PSM0 mode. However, the MAV values are different from the rms measurements of phase currents and voltages that are executed only in PSM0 mode and stored in the xIRMS and xVRMS 24-bit registers. For more information, see the Current Mean Absolute Value Calculation—ADE7868A and ADE7878A Only section.

If the ADE7868A/ADE7878A are set to PSM1 mode while configured for PSM0 mode, the devices immediately begin the mean absolute value calculations. The xIMAV registers are accessible at any time; however, if the ADE7878A or ADE7868A is set to PSM1 mode while configured for PSM2 or PSM3 mode, the ADE7868A/ADE7878A signal the start of the mean absolute value computations by driving the $\overline{\text{IRQ1}}$ pin low. The xIMAV registers can be accessed only after the $\overline{\text{IRQ1}}$ pin is low.

PSM2 LOW POWER MODE (ADE7868A AND ADE7878A ONLY)

The PSM2 low power mode (PSM2 mode) is available on the ADE7868A and ADE7878A only. PSM2 mode reduces the power consumption required to monitor the currents when there is no voltage input, and an external battery provides the voltage supply for the ADE7868A/ADE7878A.

PSM2 mode detects a missing neutral tamper condition by monitoring all phase currents and comparing them with a programmable threshold. If any phase current rises above the programmable threshold for a programmable period, the device assumes that a tamper attack has occurred. If all currents remain below the programmable threshold, no tamper attack has taken place; instead, a simple power outage has occurred.

When a missing neutral tamper condition occurs, the external microprocessor sets the ADE7868A/ADE7878A to PSM1 mode, measures the mean absolute values of the phase currents, and integrates the energy based on these values and the nominal voltage. The I²C or SPI port is not functional during this mode.

It is best practice to use the ADE7868A/ADE7878A in PSM2 mode when the PGA1 gain is 1 or 2. PGA1 represents the gain in the current channel datapath. Do not use the ADE7868A or ADE7878A in PSM2 mode when the PGA1 gain is 4, 8, or 16.

Two PSM2 modes of operation are available: PSM2 interrupt mode and PSM2 $\overline{\text{IRQ1}}$ only mode. The PSM2 interrupt mode is the default mode. If the use of an external timer is possible, use the PSM2 $\overline{\text{IRQ1}}$ only mode.

The PSM2 level threshold comparison is based on a peak detection methodology. The peak detection circuit makes the comparison based on the positive terminal current channel input, I_{AP}, I_{BP}, and I_{CP} (see Figure 24). If differential inputs are applied to the current channels, Figure 24 shows the differential antiphase signals at each current input terminal, I_{xP} and I_{xN}, and the net differential current, $I_{xP} - I_{xN}$.

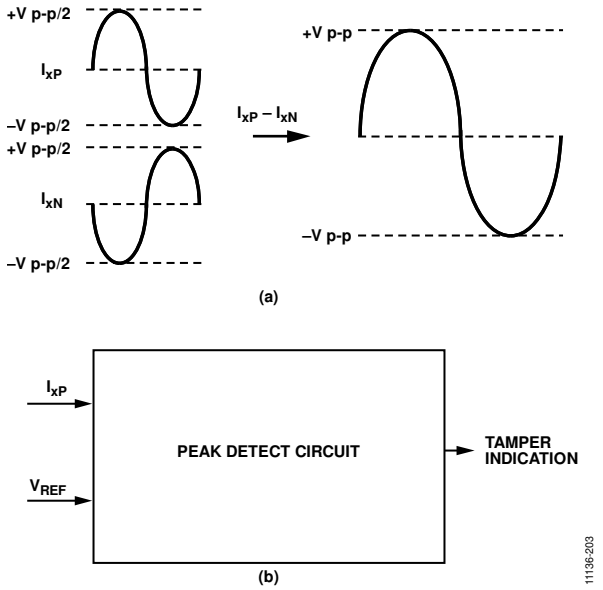

Figure 24. PSM2 Low Power Mode Peak Detection

PSM2 Interrupt Mode (Default)

In PSM2 interrupt mode, the ADE7868A/ADE7878A compare all phase currents against the programmable threshold for the programmable period of time. During this time, if one phase current exceeds the threshold, a counter is incremented. If a single phase counter is greater than or equal to LPLINE[4:0] + 1 at the end of the measurement period, the $\overline{\text{IRQ1}}$ pin is pulled low. If every phase counter remains below LPLINE[4:0] + 1 at the end of the measurement period, the $\overline{\text{IRQ0}}$ pin is pulled low.

In this way, a combination of the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ pins is used to determine the outcome of the measurement as follows:

- $\overline{\text{IRQ0}}$ pulled low: no tamper detected. When the $\overline{\text{IRQ0}}$ pin is pulled low at the end of a measurement period, it indicates that all phase currents are below the defined threshold and, therefore, no current is flowing through the system. In this case, the device does not detect a tamper condition. The external microprocessor sets the ADE7868A/ADE7878A to PSM3 sleep mode.
- $\overline{\text{IRQ1}}$ pulled low: missing neutral tamper condition detected. When the $\overline{\text{IRQ1}}$ pin is pulled low at the end of the measurement period, it indicates that at least one current input is above the defined threshold and current is flowing through the system, although no voltage is present at the ADE7868A/ADE7878A pins. This condition indicates the occurrence of a missing neutral tamper condition. At this point, the external microprocessor sets the ADE7868A/ADE7878A to PSM1 mode, measures the mean absolute values of the phase currents, and integrates the energy based on these values and the nominal voltage.

Setting the Measurement Period

The measurement period is defined by Bits[7:3] (LPLINE[4:0]) of the LPOILVL register (Address 0xEC00). The measurement period is independent of the line frequency and is defined as

Measurement Period (sec) = 0.02 × (*LPLINE[4:0]* + 10)

Setting the Threshold

The threshold is defined by Bits[2:0] (LPOIL[2:0]) of the LPOILVL register (see Table 10). The threshold level is for signal levels with the PGA set to 1. When LPOIL[2:0] = 111, the absolute value of the threshold typically varies by up to ±30%.

Table 10. LPOILVL Register

Bits	Bit Name	Value	Description
[2:0]	LPOIL[2:0]		Input signal levels that correspond to the following thresholds:
		000	71 mV rms
		001	Reserved
		010	Reserved
		011	1 mV rms
		100	Reserved
		101	Reserved
		110	Reserved
		111	0.471 mV rms
[7:3]	LPLINE[4:0]		Default value is 00000. Measurement period in PSM2 interrupt mode is 0.02 × (*LPLINE[4:0]* + 10) sec Measurement period in PSM2 $\overline{\text{IRQ1}}$ only mode is 0.02 × (*LPLINE[4:0]* + 1) sec

Figure 25 shows the typical variation around each threshold level; the gray regions in Figure 25 indicate where the feature may not yield expected and uniform results. The current levels outside this gray range help detect a tamper condition. For example, setting the threshold to 0.471 mV rms provides dependable tamper detection results for current levels above 0.707 mV rms and below 0.353 mV rms.

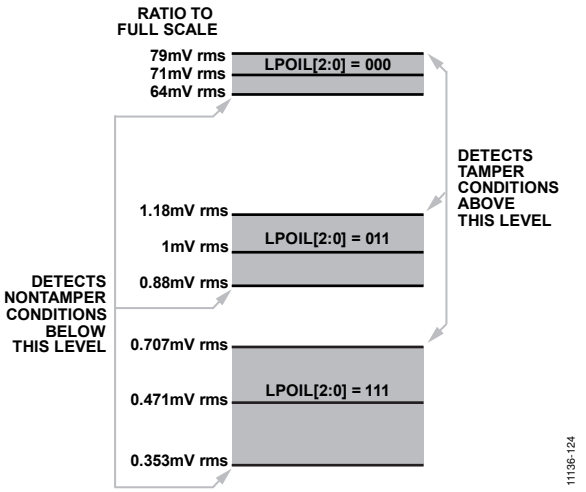

Figure 25. Variation Around Each Threshold Setting

Figure 26 shows the behavior of the ADE7868A/ADE7878A PSM2 mode when LPLINE[4:0] = 2. The test period is 12 cycles at 50 Hz (240 ms); the Phase A current rises above the LPOIL[2:0] threshold five times. Because the counter value is above the internal counter requirement of LPLINE[4:0] + 1, the $\overline{\text{IRQ1}}$ pin is pulled low at the end of the test period. This result suggests that a missing neutral tamper condition has occurred.

PSM2 $\overline{\text{IRQ1}}$ Only Mode

The PSM2 $\overline{\text{IRQ1}}$ only mode uses only the $\overline{\text{IRQ1}}$ pin to indicate a tamper event. If no tamper event has occurred, no signal is provided by the ADE7868A or ADE7878A.

To disable the $\overline{\text{IRQ0}}$ pin and thus enable the PSM2 $\overline{\text{IRQ1}}$ only mode, set Bit 2 (IRQ0_DIS) in the CONFIG2 register (Address 0xEC01) to 1. Selecting this mode defines the recommended measurement period using the following formula:

$$\textit{Recommended Measurement Period}\ (\text{sec}) = 0.02 \times (\textit{LPLINE[4:0]} + 1)$$

Because a wait is required during this measurement period, use an external timer before checking the status of the $\overline{\text{IRQ1}}$ interrupt. The measurement period can be longer than the recommended period because the internal phase counter continues to increment for the entire time that the device is in PSM2 mode. Switching to PSM3 mode and then back to PSM2 mode causes the device to enter the PSM2 interrupt mode (the default PSM2 mode).

PSM3 SLEEP MODE (ALL DEVICES)

PSM3 sleep mode is available on all devices: ADE7854A, ADE7858A, ADE7868A, and ADE7878A. In sleep mode, most of the internal circuits in the devices are turned off and the current consumption is at its lowest level. When configuring the device for sleep mode, set the $\overline{\text{RESET}}$, SCLK/SCL, MOSI/SDA, and $\overline{\text{SS}}$/HSA pins high.

In PSM3 sleep mode, the I²C, HSDC, and SPI ports are not functional.

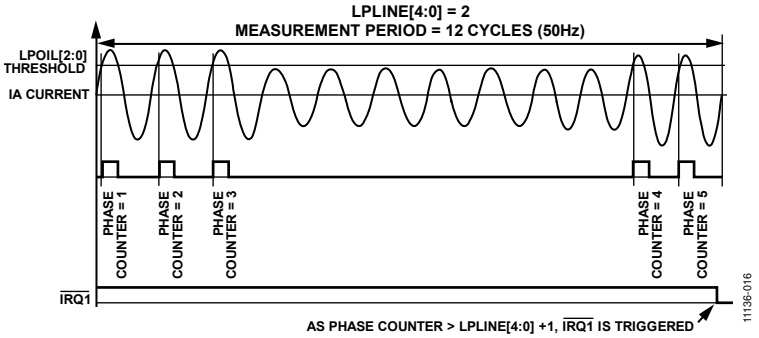

Figure 26. PSM2 Interrupt Mode Triggering $\overline{\text{IRQ1}}$ Pin for LPLINE[4:0] = 2 (50 Hz Systems)

Table 11. Power Modes and Related Characteristics

Power Mode	LPOILVL and CONFIG2 Registers	All Other Registers[1]	I²C/SPI Port	Functionality
PSM0				
After Hardware Reset	Set to default values	Set to default values	I²C port enabled	All circuits are active and DSP is in idle mode
After Software Reset	Unchanged	Set to default values	If the lock-in procedure was previously executed, the active serial port is unchanged	All circuits are active and DSP is in idle mode
PSM1 (ADE7868A and ADE7878A Only)	Values set during PSM0 mode are unchanged	Not available	I²C or SPI port enabled, but with limited functionality	Current mean absolute values are computed, and the results are stored in the AIMAV, BIMAV, and CIMAV registers
PSM2 (ADE7868A and ADE7878A Only)	Values set during PSM0 mode are unchanged	Not available	Serial port disabled	Compares phase currents against the threshold set in the LPOILVL register and triggers the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin accordingly
PSM3	Values set during PSM0 mode are unchanged	Not available	Serial port disabled	Internal circuits are shut down

[1] Setting for all registers except the LPOILVL and CONFIG2 registers.

Table 12. Recommended Actions When Changing Power Modes

Initial Power Mode	Recommended Actions Before Setting Next Power Mode	Next Power Mode			
		PSM0	PSM1	PSM2	PSM3
PSM0	Stop the DSP by setting the run register to 0x0000. Disable HSDC by clearing Bit 6 (HSDCEN) to 0 in the CONFIG register. Mask interrupts by setting MASK0 and MASK1 registers to 0x0. Erase interrupt status flags in the STATUS0 and STATUS1 registers.		Current mean absolute values (MAV) computed immediately. xIMAV registers immediately accessible.	Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is pulled low.	No action necessary.
PSM1 (ADE7868A and ADE7878A Only)	No action necessary.	Wait until the $\overline{\text{IRQ1}}$ pin is pulled low. Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1.		Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is pulled low.	No action necessary.
PSM2 (ADE7868A and ADE7878A Only)	No action necessary.	Wait until the $\overline{\text{IRQ1}}$ pin is pulled low. Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1.	Wait until the $\overline{\text{IRQ1}}$ pin is pulled low. Current mean absolute values computed after $\overline{\text{IRQ1}}$ pin is pulled low. xIMAV registers accessible after $\overline{\text{IRQ1}}$ pin is pulled low.		No action necessary.
PSM3	No action necessary.	Wait until the $\overline{\text{IRQ1}}$ pin is pulled low. Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1.	Wait until the $\overline{\text{IRQ1}}$ pin is pulled low. Current mean absolute values computed after $\overline{\text{IRQ1}}$ pin is pulled low. xIMAV registers accessible after $\overline{\text{IRQ1}}$ pin is pulled low.	Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is pulled low.	

POWER-UP PROCEDURE

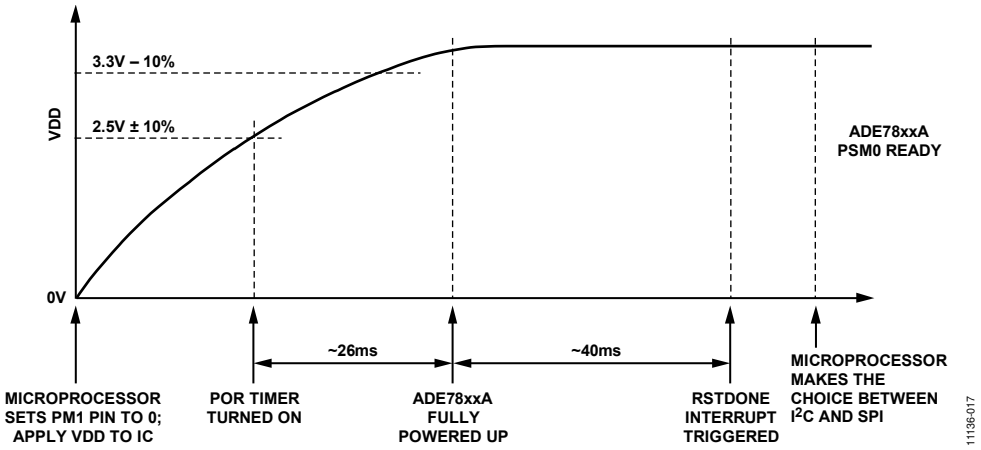

Figure 27. Power-Up Procedure

The ADE7854A/ADE7858A/ADE7868A/ADE7878A contain an on-chip power supply monitor that supervises the power supply (VDD). At power-up, the device is inactive until VDD reaches 2.5 V ± 10%. When VDD crosses this threshold, the power supply monitor keeps the device in the inactive state for an additional 26 ms to allow VDD to rise to 3.3 V − 10%, the minimum recommended supply voltage.

The PM0 and PM1 pins have internal pull-up resistors, but it is necessary to set the PM1 pin to Logic 0 either through a microcontroller or by grounding the PM1 pin externally, before powering up the chip. The PM0 pin can remain open as it is held high, due to the internal pull-up resistor. This ensures that ADE7854A/ADE7858A/ADE7868A/ADE7878A always power up in PSM0 (normal) mode. The time taken from the chip being powered up completely to the state where all functionality is enabled, is about 40 ms (see Figure 27). It is necessary to ensure that the $\overline{\text{RESET}}$ pin is held high during the entire power-up procedure.

If PSM0 mode is the only desired power mode, the PM1 pin can be tied to ground externally. When the ADE7854A/ADE7858A/ADE7868A/ADE7878A enter PSM0 mode, the I²C port is the active serial port. To use the SPI port, toggle the $\overline{\text{SS}}$/HSA pin three times from high to low.

To lock I²C as the active serial port, set Bit 1 (I2C_LOCK) of the CONFIG2 register to 1. From this moment, the device ignores spurious toggling of the $\overline{\text{SS}}$/HSA pin, and a switch to the SPI port is no longer possible.

If SPI is the active serial port, any write to the CONFIG2 register locks the port, and a switch to the I²C port is no longer possible. To use the I²C port, the ADE7854A/ADE7858A/ADE7868A/ADE7878A must be powered down or the device must be reset by setting the $\overline{\text{RESET}}$ pin low. After the serial port is locked, the serial port selection is maintained when the device changes from one PSMx power mode to another.

Immediately after entering PSM0 mode, all registers in the ADE7854A/ADE7858A/ADE7868A/ADE7878A are set to their default values, including the CONFIG2 and LPOILVL registers.

The ADE7854A/ADE7858A/ADE7868A/ADE7878A signal the end of the transition period by pulling the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is cleared to 0 during the transition period and is set to 1 when the transition ends. Writing the STATUS1 register with the RSTDONE bit set to 1 clears the status bit and returns the $\overline{\text{IRQ1}}$ pin high. Because RSTDONE is an unmaskable interrupt, Bit 15 (RSTDONE) in the STATUS1 register must be cancelled for the $\overline{\text{IRQ1}}$ pin to return high. Wait until the $\overline{\text{IRQ1}}$ pin goes low before accessing the STATUS1 register to test the state of the RSTDONE bit. At this point, as a good programming practice, cancel all other status flags in the STATUS1 and STATUS0 registers by writing the corresponding bits with 1.

Initially, the DSP is in idle mode and, therefore, does not execute any instructions. This is the moment to initialize all registers in the ADE7854A, ADE7858A, ADE7868A, or ADE7878A. See the Digital Signal Processor section for the proper procedure to initialize all registers and start the metering.

If the supply voltage, VDD, falls lower than 2.5 V ± 10%, the ADE7854A/ADE7858A/ADE7868A/ADE7878A enter an inactive state, which means that no measurements or computations are executed.

HARDWARE RESET

The ADE7854A, ADE7858A, ADE7868A, and ADE7878A have a $\overline{\text{RESET}}$ pin. When the ADE7854A, ADE7858A, ADE7868A, or ADE7878A is in PSM0 mode and the $\overline{\text{RESET}}$ pin is set low, the device enters the hardware reset state. The device must be in PSM0 mode to execute a hardware reset. Setting the $\overline{\text{RESET}}$ pin low while the device is in PSM1, PSM2, or PSM3 mode has no effect on the device.