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Polyphase Multifunction Energy Metering IC with Harmonic Monitoring

Data Sheet

ADE7880

FEATURES

- **Highly accurate; supports IEC 62053-21, IEC 62053-22, IEC 62053-23, EN 50470-1, EN 50470-3, ANSI C12.20, and IEEE1459 standards**
- **Supports IEC 61000-4-7 Class I and Class II accuracy specification**
- **Compatible with 3-phase, 3-wire or 4-wire (delta or wye), and other 3-phase services**
- **Supplies rms, active, reactive, and apparent powers, power factor, THD, and harmonic distortion of all harmonics within 2.8 kHz pass band on all phases**
- **Supplies rms and harmonic distortions of all harmonics within 2.8 kHz pass band on neutral current**
- **Less than 1% error in harmonic current and voltage rms, harmonic active and reactive powers over a dynamic range of 2000 to 1 at T_A = 25°C**
- **Supplies total (fundamental and harmonic) active and apparent energy and fundamental active/reactive energy on each phase and on the overall system**
- **Less than 0.1% error in active and fundamental reactive energy over a dynamic range of 1000 to 1 at T_A = 25°C**
- **Less than 0.2% error in active and fundamental reactive energy over a dynamic range of 5000 to 1 at T_A = 25°C**
- **Less than 0.1% error in voltage and current rms over a dynamic range of 1000 to 1 at T_A = 25°C**
- **Battery supply input for missing neutral operation**
- **Wide supply voltage operation: 2.4 V to 3.7 V**
- **Reference: 1.2 V (drift 20 ppm/°C typical) with external overdrive capability**
- **40-lead lead frame chip scale package (LFCSP), Pb-free, pin-for-pin compatible with ADE7854, ADE7858, ADE7868 and ADE7878**

APPLICATIONS

- **Energy metering systems**
- **Power quality monitoring**
- **Solar inverters**
- **Process monitoring**
- **Protective devices**

GENERAL DESCRIPTION

The ADE7880[1] is a high accuracy, 3-phase electrical energy measurement IC with serial interfaces and three flexible pulse outputs. The ADE7880 device incorporates second-order sigma-delta (Σ-Δ) analog-to-digital converters (ADCs), a digital integrator, reference circuitry, and all of the signal processing required to perform the total (fundamental and harmonic) active, and apparent energy measurements, rms calculations, as well as fundamental-only active and reactive energy measurements. In addition, the ADE7880 computes the rms of harmonics on the phase and neutral currents and on the phase voltages, together with the active, reactive and apparent powers, and the power factor and harmonic distortion on each harmonic for all phases. Total harmonic distortion (THD) is computed for all currents and voltages. A fixed function digital signal processor (DSP) executes this signal processing. The DSP program is stored in the internal ROM memory.

The ADE7880 is suitable for measuring active, reactive, and apparent energy in various 3-phase configurations, such as wye or delta services with, both, three and four wires. The ADE7880 provides system calibration features for each phase, that is, rms offset correction, phase calibration, and gain calibration. The CF1, CF2, and CF3 logic outputs provide a wide choice of power information: total active powers, apparent powers, or the sum of the current rms values, and fundamental active and reactive powers.

The ADE7880 contains waveform sample registers that allow access to all ADC outputs. The devices also incorporate power quality measurements, such as short duration low or high voltage detections, short duration high current variations, line voltage period measurement, and angles between phase voltages and currents. Two serial interfaces, SPI and I^2C, can be used to communicate with the ADE7880. A dedicated high speed interface, the high speed data capture (HSDC) port, can be used in conjunction with I^2C to provide access to the ADC outputs and real-time power information. The ADE7880 also has two interrupt request pins, $\overline{IRQ0}$ and $\overline{IRQ1}$, to indicate that an enabled interrupt event has occurred. Three specially designed low power modes ensure the continuity of energy accumulation when the ADE7880 is in a tampering situation. The ADE7880 is available in the 40-lead LFCSP, Pb-free package, pin-for-pin compatible with ADE7854, ADE7858, ADE7868, and ADE7878 devices.

[1] Protected by U.S. Patent 8,010,304 B2. Other patents pending.

Rev. C
Document Feedback

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ADE7880* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADE7880 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1127: Differences Between the ADE7880 and the ADE7878
- AN-1171: Calibrating a Three-Phase Energy Meter Based on the ADE7880
- AN-1334: Impact of Adding a Neutral Attenuation Network in a 3P4W Wye System
- AN-639: Frequently Asked Questions (FAQs) Analog Devices Energy (ADE) Products

Data Sheet

- ADE7880: Polyphase Multifunction Energy Metering IC with Harmonic Monitoring Data Sheet

Product Highlight

- ADE7880–Polyphase Energy Metering
- ADE78xx Polyphase Multifunction Energy Metering ICs

User Guides

- UG-356: Evaluating the ADE7880 Energy Metering IC

REFERENCE MATERIALS

Technical Articles

- MS-2250: Adaptive Real-Time DSP Architecture to Monitor Harmonic Components and Various Power Quality Factors in Electric Power Grids

DESIGN RESOURCES

- ADE7880 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADE7880 EngineerZone Discussions.

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FUNCTIONAL BLOCK DIAGRAM

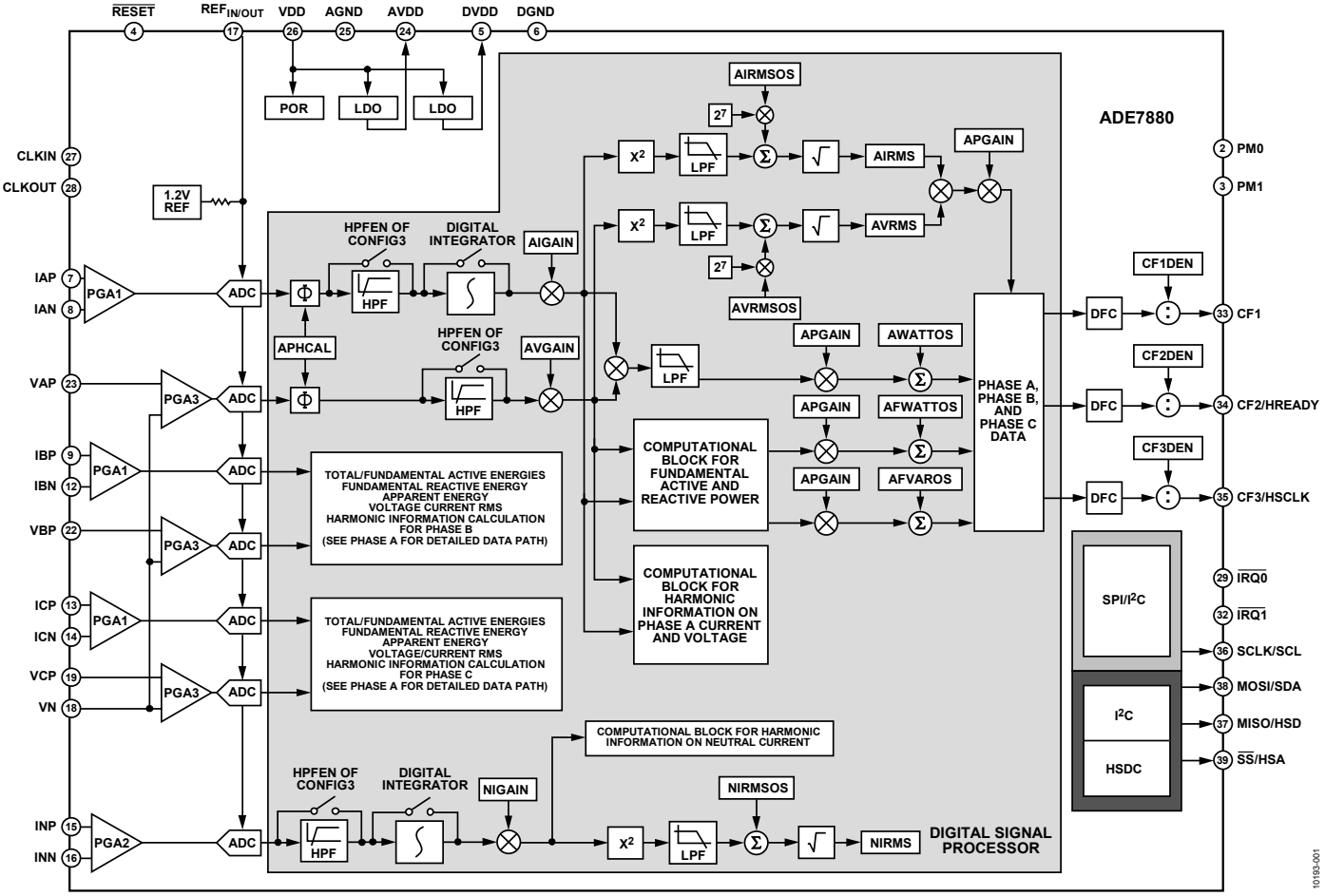

Figure 1. ADE7880 Functional Block Diagram

SPECIFICATIONS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP} = 25°C.

Table 1.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
ACTIVE ENERGY MEASUREMENT					
Active Energy Measurement Error (per Phase)					
Total Active Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off, pf = 1, gain compensation only
		0.2		%	Over a dynamic range of 5000 to 1, PGA = 1, 2, 4; integrator off, pf = 1
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on, pf = 1, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PGA = 8, 16; integrator on, pf = 1
Fundamental Active Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off, pf = 1, gain compensation only
		0.2		%	Over a dynamic range of 5000 to 1, PGA = 1, 2, 4; integrator off, pf = 1
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on, pf = 1, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PGA = 8, 16; integrator on, pf = 1
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz, IPx = VPx = ±100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Output Frequency Variation		0.01		%	
Total Active Energy Measurement Bandwidth (−3 dB)		3.3		kHz	
REACTIVE ENERGY MEASUREMENT					
Reactive Energy Measurement Error (per Phase)					
Fundamental Reactive Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off, pf = 0, gain compensation only
		0.2		%	Over a dynamic range of 5000 to 1, PGA = 1, 2, 4; integrator off, pf = 0
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on, pf = 0, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PGA = 8, 16; integrator on, pf = 0
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz, IPx = VPx = ± 100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Output Frequency Variation		0.01		%	
Fundamental Reactive Energy Measurement Bandwidth (−3 dB)		3.3		kHz	

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
RMS MEASUREMENTS (PSM0 Mode)					
I RMS and V RMS Measurement Bandwidth (−3 dB)		3.3		kHz	
I RMS and V RMS Measurement Error		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1
MEAN ABSOLUTE VALUE (MAV) MEASUREMENT (PSM1 Mode)					
I MAV Measurement Bandwidth		260		Hz	
I MAV Measurement Error		0.5		%	Over a dynamic range of 100 to 1, PGA = 1, 2, 4, 8
HARMONIC MEASUREMENTS					
Bandwidth (−3 dB)		3.3		kHz	
No attenuation Pass Band		2.8		kHz	
Fundamental Line Frequency, f_L	45		66	Hz	Voltage signal must have amplitudes greater than 100 mV peak at ADC stage. Set the SELFREQ bit of COMPMODE register based on the frequency. See the Managing Change in Fundamental Line Frequency section for details.
Maximum Number of Harmonics[3]			$\left[\frac{2800}{f_L}\right]$		
Absolute Maximum Number of Harmonics			63		
Harmonic RMS Measurement Error		1		%	Instantaneous reading accuracy over a dynamic range of 1000 to 1 for harmonics of frequencies within the pass band; after the initial 750 ms settling time; PGA = 1 Accuracy over a dynamic range of 2000:1 for harmonics of frequencies within the pass band; average of 10 readings at 128 ms update rate, after the initial 750 ms setting time; PGA = 1
Harmonic Active/Reactive Power Measurement Error		1		%	Instantaneous reading accuracy over a dynamic range of 1000 to 1 for harmonics of frequencies within the pass band; after the initial 750 ms settling time; PGA = 1 Accuracy over a dynamic range of 2000:1 for harmonics of frequencies within the pass band; average of 5 readings at 128 ms update rate, after the initial 750 ms setting time; PGA = 1
ANALOG INPUTS					
Maximum Signal Levels			±500	mV peak	PGA = 1, differential or single-ended inputs between the following pins: IAP and IAN, IBP and IBN, ICP and ICN, INP and INN; single-ended inputs between the following pins: VAP and VN, VBP and VN, VCP and VN
Input Impedance (DC)					
IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, and VCP Pins	490			kΩ	
VN Pin	170			kΩ	
ADC Offset		−35		mV	PGA = 1, uncalibrated error, see the Terminology section. Scales inversely proportional to the other PGA gains
Gain Error		±4		%	External 1.2 V reference

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
WAVEFORM SAMPLING					Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS
Current and Voltage Channels					See the Waveform Sampling Mode section
Signal-to-Noise Ratio, SNR		72		dB	PGA = 1, fundamental frequency = 45 Hz to 65 Hz, see the Terminology section
Signal-to-Noise-and-Distortion Ratio, SINAD		72		dB	PGA = 1, fundamental frequency = 45 Hz to 65 Hz, see the Terminology section
Bandwidth (−3 dB)		3.3		kHz	
TIME INTERVAL BETWEEN PHASES					
Measurement Error		0.3		Degrees	Line frequency = 45 Hz to 65 Hz, HPF on
CF1, CF2, CF3 PULSE OUTPUTS					
Maximum Output Frequency		68.818		kHz	WTHR = VARTHR = VATHR = 3
Duty Cycle		50		%	If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1
		(1 + 1/CFDEN) × 50		%	If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1
Active Low Pulse Width		80		ms	If CF1, CF2, or CF3 frequency < 6.25 Hz
Jitter		0.04		%	For CF1, CF2, or CF3 frequency = 1 Hz and nominal phase currents are larger than 10% of full scale
REFERENCE INPUT					
$REF_{IN/OUT}$ Input Voltage Range	1.1		1.3	V	Minimum = 1.2 V − 8%; maximum = 1.2 V + 8%
Input Capacitance			10	pF	
ON-CHIP REFERENCE					Nominal 1.2 V at the $REF_{IN/OUT}$ pin at T_A = 25°C
PSM0 and PSM1 Modes					
Temperature Coefficient	−50	±20	+50	ppm/°C	Drift across the entire temperature range of −40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more details
CLKIN					See the Crystal Circuit section for more details
Input Clock Frequency	16.22	16.384	16.55	MHz	
LOGIC INPUTS—MOSI/SDA, SCLK/SCL, $\overline{SS}$, $\overline{RESET}$, PM0, AND PM1					
Input High Voltage, V_{INH}	2.4			V	VDD = 3.3 V
Input Current, I_{IN}			82	nA	Input = VDD = 3.3 V
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V
Input Current, I_{IN}			−7.3	µA	Input = 0, VDD = 3.3 V
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS—$\overline{IRQ0}$, $\overline{IRQ1}$, AND MISO/HSD					VDD = 3.3 V
Output High Voltage, V_{OH}	3.0			V	I_{SOURCE} = 800 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
CF1, CF2, CF3/HSCLK					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 8 mA
POWER SUPPLY					For specified performance
PSM0 Mode					
VDD Pin	2.97		3.63	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
I_{DD}		25	28	mA	

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
PSM1 and PSM2 Modes					
VDD Pin	2.4		3.7	V	
I_{DD}					
PSM1 Mode		5.3	5.8	mA	
PSM2 Mode		0.2	0.27	mA	
PSM3 Mode					For specified performance
VDD Pin	2.4		3.7	V	
I_{DD} in PSM3 Mode		1.8	6	µA	

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for a definition of the parameters.
[3] $\left[\frac{2800}{f_L}\right]$ means the whole number of the division.

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C. Note that dual function pin names are referenced by the relevant function only within the timing tables and diagrams (see the Pin Configuration and Function Descriptions section for full pin mnemonics and descriptions).

Table 2. I²C-Compatible Interface Timing Parameter

		Standard Mode		Fast Mode		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) Start Condition	$t_{HD;STA}$	4.0		0.6		µs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		µs
High Period of SCL Clock	t_{HIGH}	4.0		0.6		µs
Set-Up Time for Repeated Start Condition	$t_{SU;STA}$	4.7		0.6		µs
Data Hold Time	$t_{HD;DAT}$	0.1	3.45	0.1	0.9	µs
Data Setup Time	$t_{SU;DAT}$	250		100		ns
Rise Time of Both SDA and SCL Signals	t_R		1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_F		300	20	300	ns
Setup Time for Stop Condition	$t_{SU;STO}$	4.0		0.6		µs
Bus Free Time Between a Stop and Start Condition	t_{BUF}	4.7		1.3		µs
Pulse Width of Suppressed Spikes	t_{SP}	N/A[1]			50	ns

[1] N/A means not applicable.

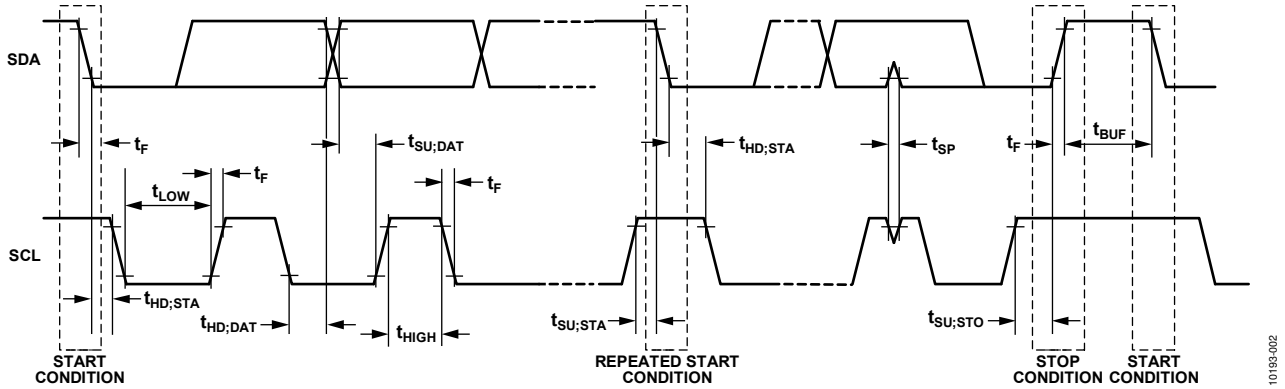

Figure 2. I²C-Compatible Interface Timing

Table 3. SPI Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	50		ns
SCLK Period		0.4	4000[1]	µs
SCLK Low Pulse Width	t_{SL}	175		ns
SCLK High Pulse Width	t_{SH}	175		ns
Data Output Valid After SCLK Edge	t_{DAV}		100	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	100		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	5		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}		200	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0		ns

[1] Guaranteed by design.

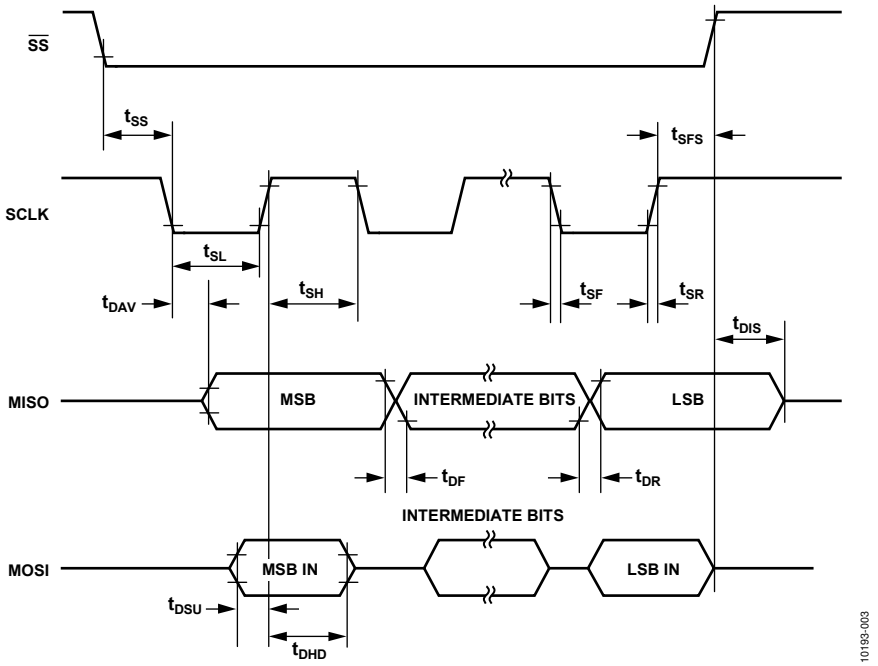

Figure 3. SPI Interface Timing

Table 4. HSDC Interface Timing Parameter

Parameter	Symbol	Min	Max	Unit
HSA to HSCLK Edge	t_{SS}	0		ns
HSCLK Period		125		ns
HSCLK Low Pulse Width	t_{SL}	50		ns
HSCLK High Pulse Width	t_{SH}	50		ns
Data Output Valid After HSCLK Edge	t_{DAV}		40	ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
HSCLK Rise Time	t_{SR}		10	ns
HSCLK Fall Time	t_{SF}		10	ns
HSD Disable After HSA Rising Edge	t_{DIS}	5		ns
HSA High After HSCLK Edge	t_{SFS}	0		ns

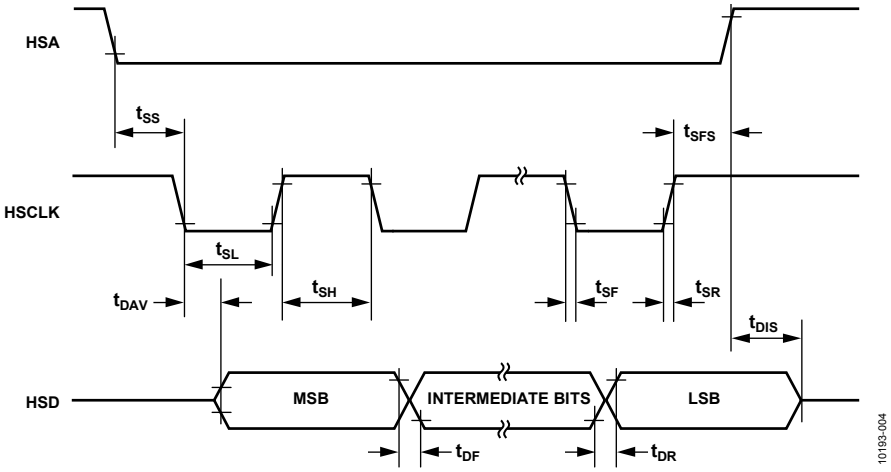

Figure 4. HSDC Interface Timing

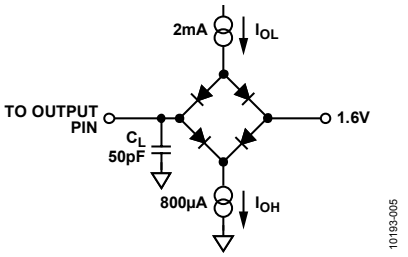

Figure 5. Load Circuit for Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter[1]	Rating
VDD to AGND	−0.3 V to +3.7 V
VDD to DGND	−0.3 V to +3.7 V
Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, VCP, VN	−2 V to +2 V
Analog Input Voltage to INP and INN	−2 V to +2 V
Reference Input Voltage to AGND	−0.3 V to VDD + 0.3 V
Digital Input Voltage to DGND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Regarding the temperature profile used in soldering RoHS Compliant Parts, Analog Devices, Inc. advises that reflow profiles conform to J-STD 20 from JEDEC. Refer to JEDEC website for the latest revision.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified equal to 29.3°C/W; θ_{JC} is specified equal to 1.8°C/W.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	29.3	1.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

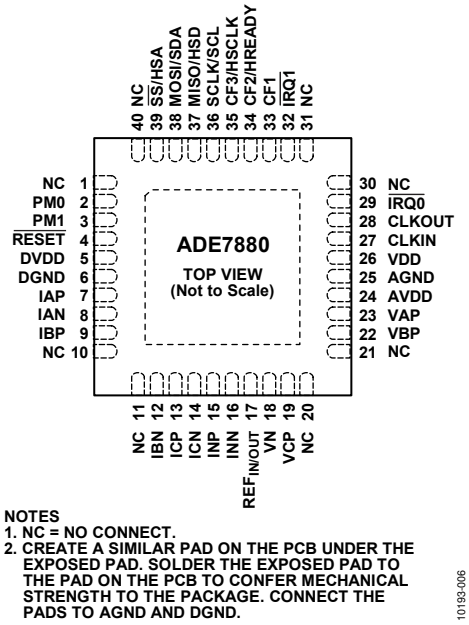

Figure 6. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10, 11, 20, 21, 30, 31, 40	NC	No Connect. Do not connect to these pins. These pins are not connected internally.
2	PM0	Power Mode Pin 0. This pin, combined with PM1, defines the power mode of the ADE7880, as described in Table 8.
3	PM1	Power Mode Pin 1. This pin defines the power mode of the ADE7880 when combined with PM0, as described in Table 8.
4	$\overline{\text{RESET}}$	Reset Input, Active Low. In PSM0 mode, this pin must stay low for at least 10 µs to trigger a hardware reset.
5	DVDD	2.5 V Output of the Digital Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin.
6	DGND	Ground Reference. This pin provides the ground reference for the digital circuitry.
7, 8	IAP, IAN	Analog Inputs for Current Channel A. This channel is used with the current transducers and is referenced in this data sheet as Current Channel A. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel B and Channel C.
9, 12	IBP, IBN	Analog Inputs for Current Channel B. This channel is used with the current transducers and is referenced in this data sheet as Current Channel B. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel C and Channel A.
13, 14	ICP, ICN	Analog Inputs for Current Channel C. This channel is used with the current transducers and is referenced in this data sheet as Current Channel C. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel A and Channel B.
15, 16	INP, INN	Analog Inputs for Neutral Current Channel N. This channel is used with the current transducers and is referenced in this data sheet as Current Channel N. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA, different from the ones found on the A, B, and C channels.
17	$\text{REF}_{\text{IN/OUT}}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. An external reference source with 1.2 V ± 8% can also be connected at this pin. In either case, decouple this pin to AGND with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor. After reset, the on-chip reference is enabled.

Pin No.	Mnemonic	Description
18, 19, 22, 23	VN, VCP, VBP, VAP	Analog Inputs for the Voltage Channel. This channel is used with the voltage transducer and is referenced as the voltage channel in this data sheet. These inputs are single-ended voltage inputs with a maximum signal level of ±0.5 V with respect to VN for specified operation. This channel also has an internal PGA.
24	AVDD	2.5 V Output of the Analog Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin.
25	AGND	Ground Reference. This pin provides the ground reference for the analog circuitry. Tie this pin to the analog ground plane or to the quietest ground reference in the system. Use this quiet ground reference for all analog circuitry, for example, antialiasing filters, current, and voltage transducers.
26	VDD	Supply Voltage. This pin provides the supply voltage. In PSM0 (normal power mode), maintain the supply voltage at 3.3 V ± 10% for specified operation. In PSM1 (reduced power mode), PSM2 (low power mode), and PSM3 (sleep mode), when the ADE7880 is supplied from a battery, maintain the supply voltage between 2.4 V and 3.7 V. Decouple this pin to DGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
27	CLKIN	Master Clock. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT-cut crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7880. The clock frequency for specified operation is 16.384 MHz. Use ceramic load capacitors of a few tens of picofarad with the gate oscillator circuit. Refer to the data sheet of the crystal manufacturer for load capacitance requirements.
28	CLKOUT	A crystal can be connected across this pin and CLKIN (as previously described with Pin 27 in this table) to provide a clock source for the ADE7880.
29, 32	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$	Interrupt Request Outputs. These are active low logic outputs. See the Interrupts section for a detailed presentation of the events that can trigger interrupts.
33, 34, 35	CF1, CF2/HREADY, CF3/HSCLK	Calibration Frequency (CF) Logic Outputs. These outputs provide power information based on the CF1SEL[2:0], CF2SEL[2:0], and CF3SEL[2:0] bits in the CFMODE register. These outputs are used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the CF1DEN, CF2DEN, and CF3DEN registers, respectively (see the Energy-to-Frequency Conversion section). CF2 is multiplexed with the HREADY signal generated by the harmonic calculations block. CF3 is multiplexed with the serial clock output of the HSDC port.
36	SCLK/SCL	Serial Clock Input for SPI Port/Serial Clock Input for I^2C Port. All serial data transfers are synchronized to this clock (see the Serial Interfaces section). This pin has a Schmidt trigger input for use with a clock source that has a slow edge transition time, for example, optoisolator outputs.
37	MISO/HSD	Data Out for SPI Port/Data Out for HSDC Port.
38	MOSI/SDA	Data In for SPI Port/Data Out for I^2C Port.
39	$\overline{\text{SS}}$/HSA	Slave Select for SPI Port/HSDC Port Active.
EP	Exposed Pad	Create a similar pad on the PCB under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package. Connect the pads to AGND and DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

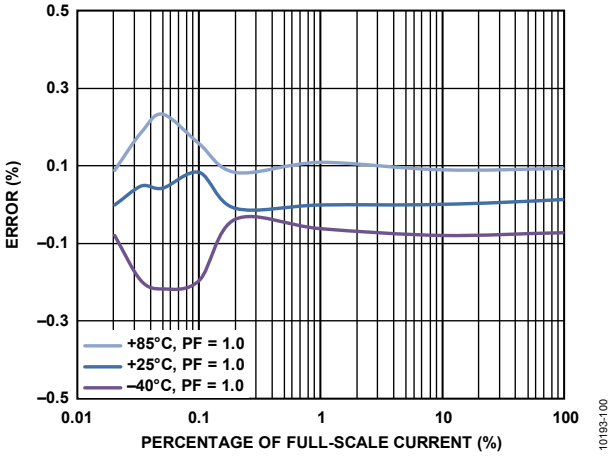

Figure 7. Total Active Energy Error as Percentage of Reading (Gain = +1, Power Factor = 1) over Temperature with Internal Reference and Integrator Off

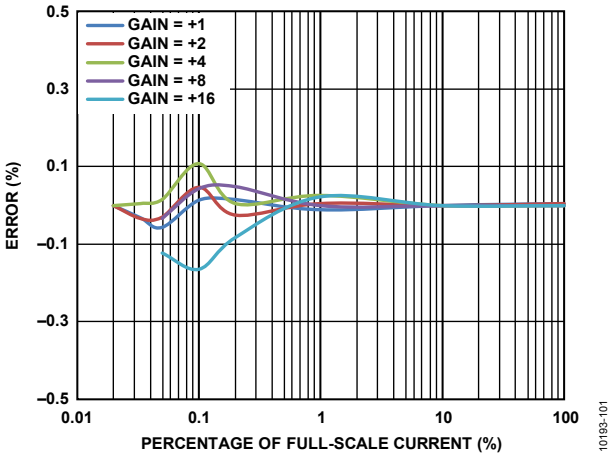

Figure 8. Total Active Energy Error as Percentage of Reading over Gain with Internal Reference and Integrator Off

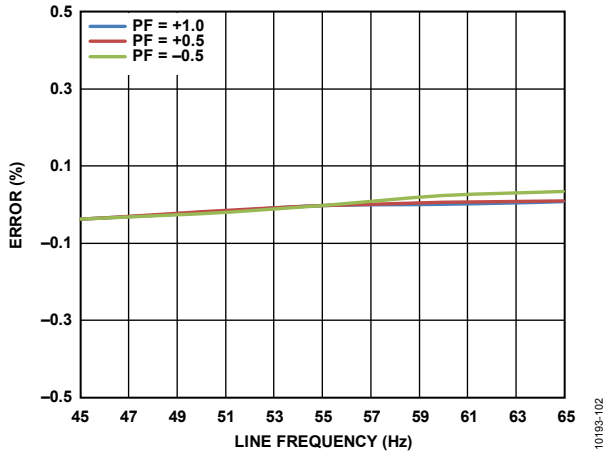

Figure 9. Total Active Energy Error as Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

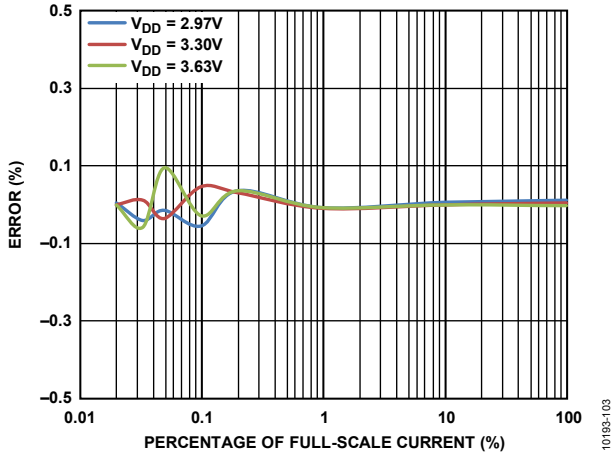

Figure 10. Total Active Energy Error as Percentage of Reading (Gain = +1) over Power Supply with Internal Reference and Integrator Off

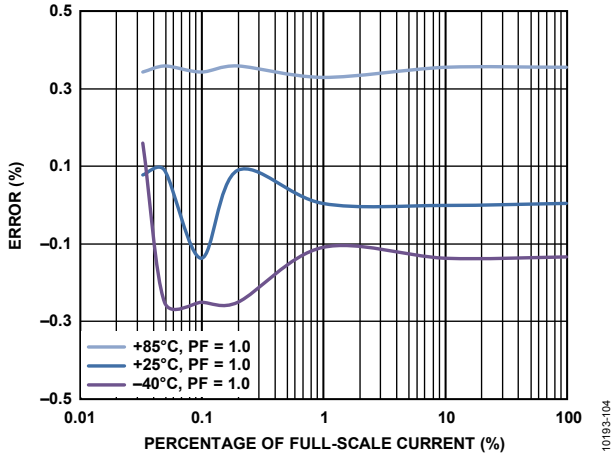

Figure 11. Total Active Energy Error as Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On

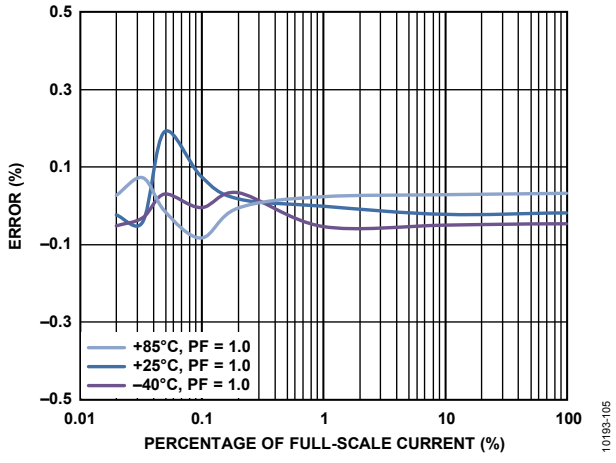

Figure 12. Fundamental Active Energy Error as Percentage of Reading (Gain = +1, Power Factor = 1) over Temperature with Internal Reference and Integrator Off

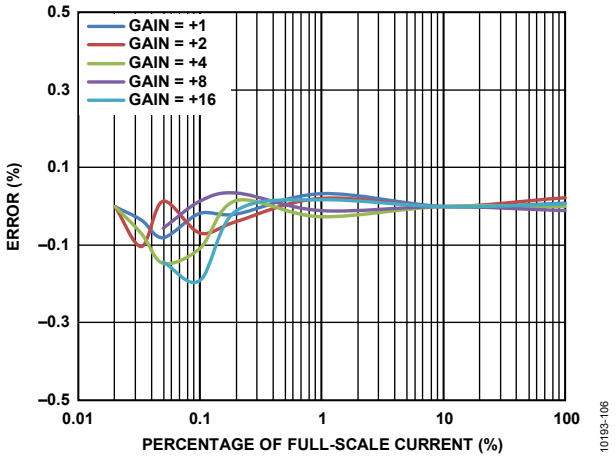

Figure 13. Fundamental Active Energy Error as Percentage of Reading over Gain with Internal Reference and Integrator Off

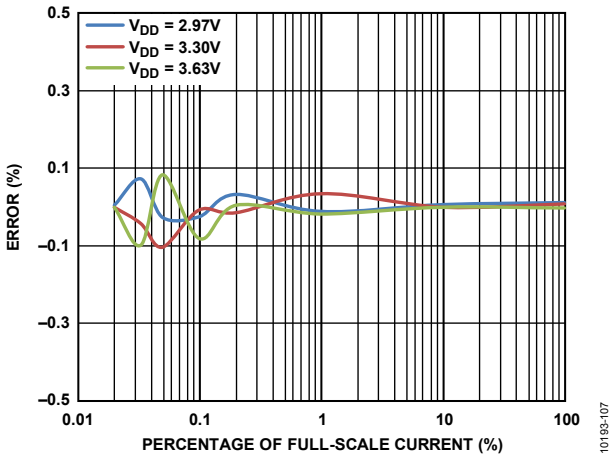

Figure 14. Fundamental Active Energy Error as Percentage of Reading (Gain = +1) over Power Supply with Internal Reference and Integrator Off

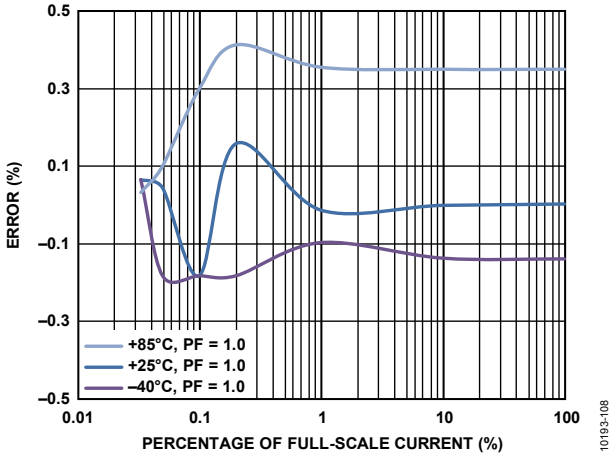

Figure 15. Fundamental Active Energy Error as Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator On

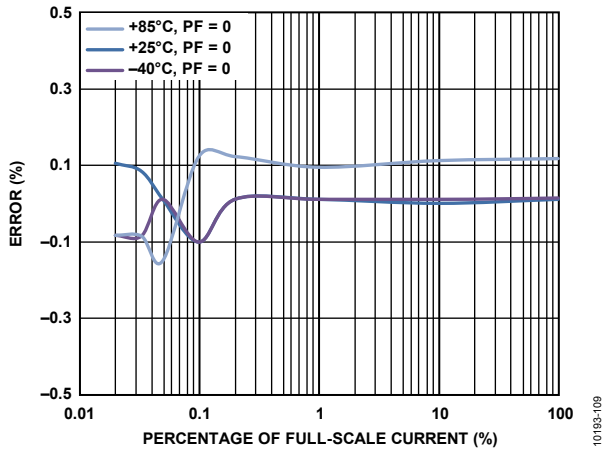

Figure 16. Fundamental Reactive Energy Error as Percentage of Reading (Gain = +1, Power Factor = 0) over Temperature with Internal Reference and Integrator Off

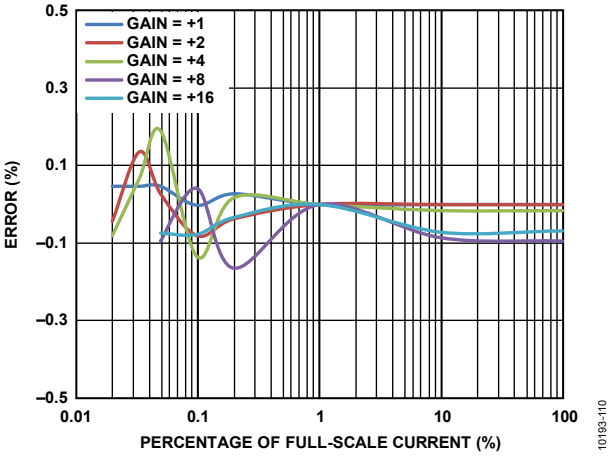

Figure 17. Fundamental Reactive Energy Error as Percentage of Reading over Gain with Internal Reference and Integrator Off

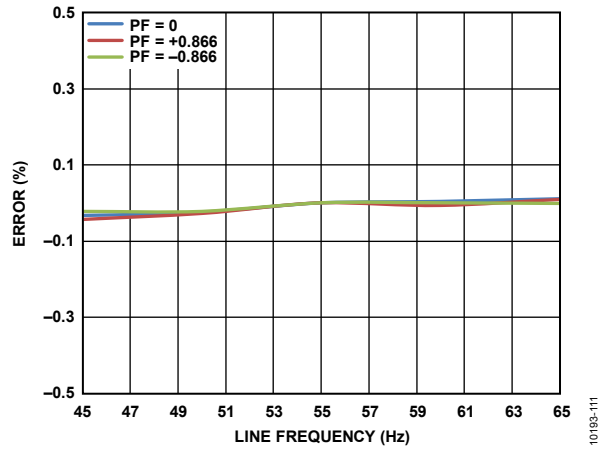

Figure 18. Fundamental Reactive Energy Error as Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

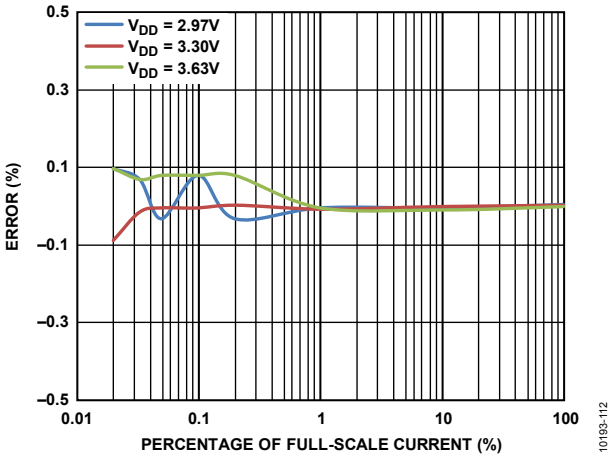

Figure 19. Fundamental Reactive Energy Error as Percentage of Reading (Gain = +1) over Power Supply with Internal Reference and Integrator Off

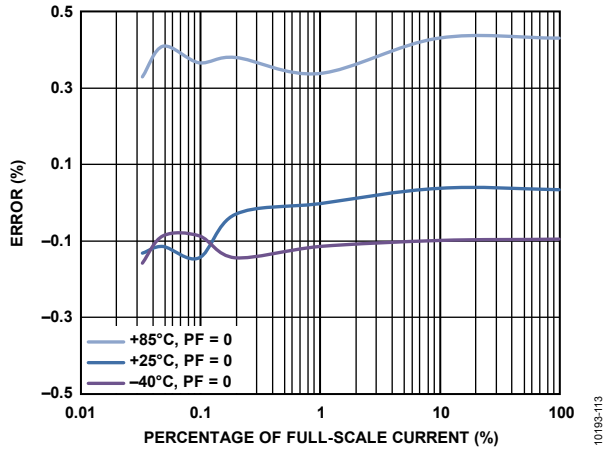

Figure 20. Fundamental Reactive Energy Error as Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On

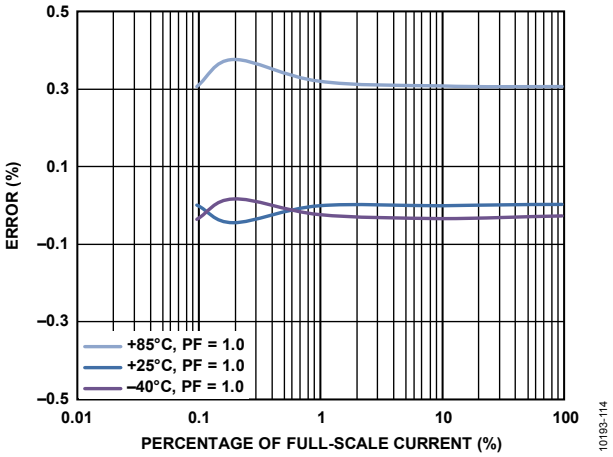

Figure 21. I RMS Error as Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator Off

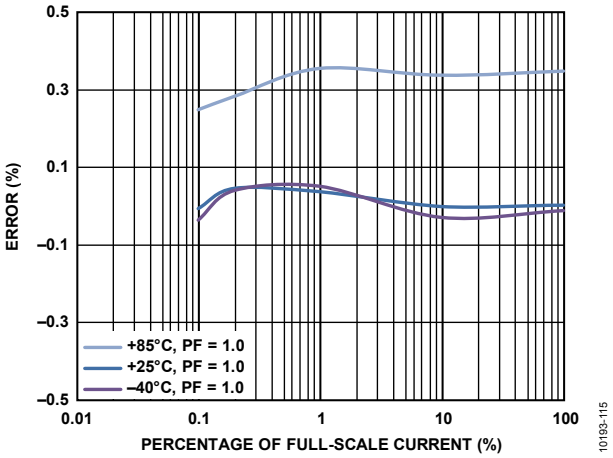

Figure 22. V RMS Error as a Percentage of Reading (Gain = +1) over Temperature with Internal Reference

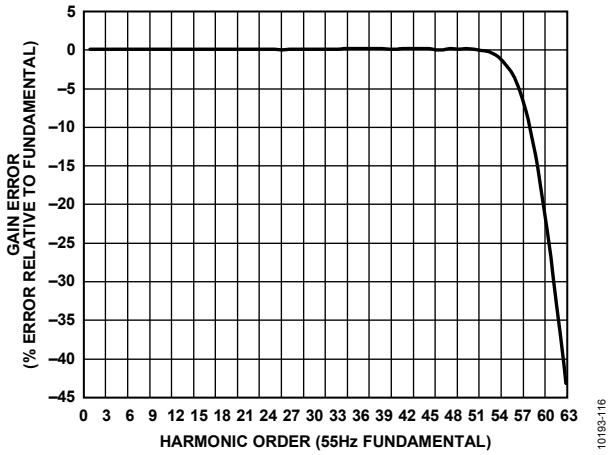

Figure 23. Harmonic I RMS Error as a Percentage of Reading over Harmonic Order, 63 Harmonics, 55 Hz Fundamental, 30 Averages per Reading, 750 ms Settling time, 125 µs Update Rate

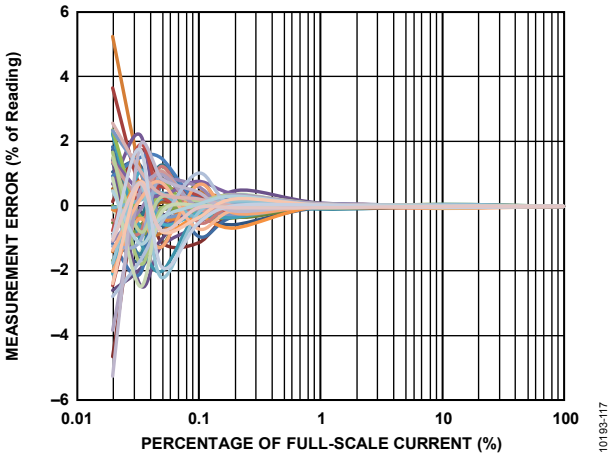

Figure 24. Harmonic I RMS Error as a Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, Single Reading, 750 ms Settling Time; 125 µs Update Rate

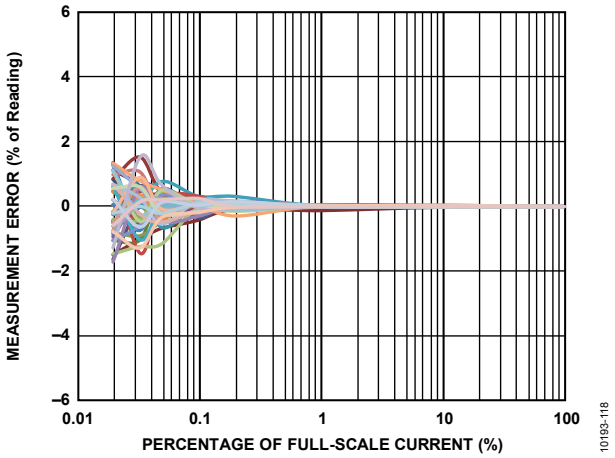

Figure 25. Harmonic I RMS Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, 10 Averages per Reading, 750 ms Settling Time, 125 µs Update Rate

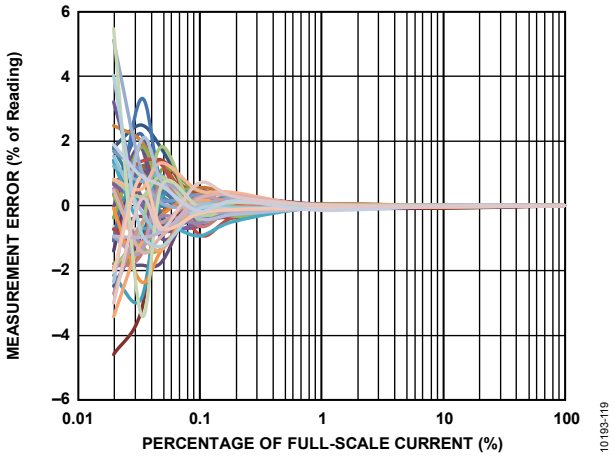

Figure 26. Harmonic Active Power Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, Single Reading, 750 ms Settling Time, 125 µs Update Rate

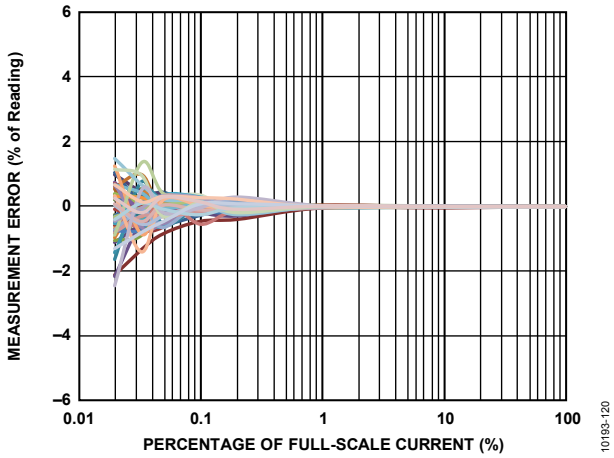

Figure 27. Harmonic Active Power Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, 10 Averages per Reading, 750 ms Settling Time, 125 µs Update Rate

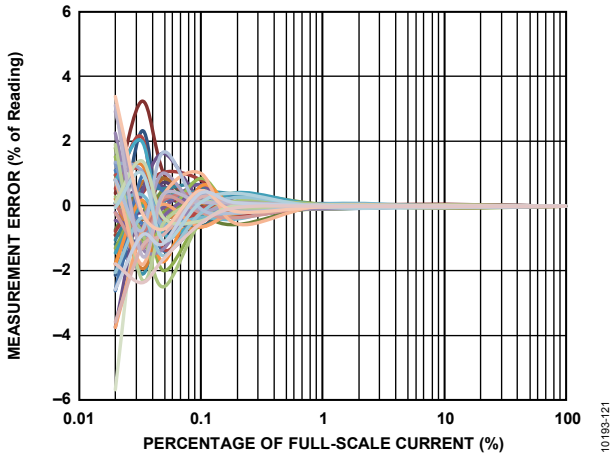

Figure 28. Harmonic Reactive Power Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, Single Reading, 750 ms Settling Time, 125 µs Update Rate

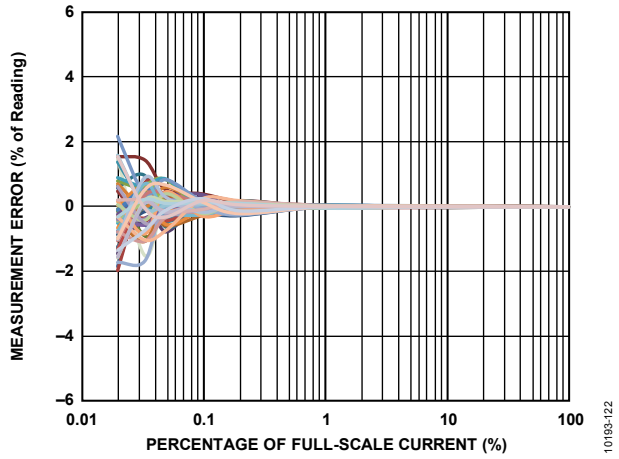

Figure 29. Harmonic Reactive Power Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, 10 Averages per Reading, 750 ms Settling Time, 125 µs Update Rate

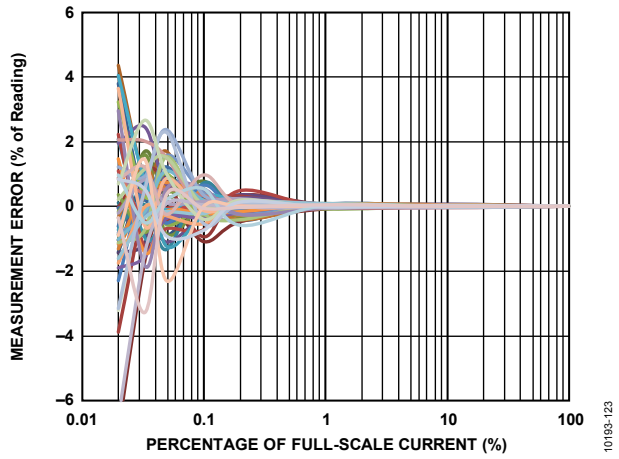

Figure 30. Harmonic Apparent Power Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, Single Reading, 750 ms Settling Time, 125 µs Update Rate

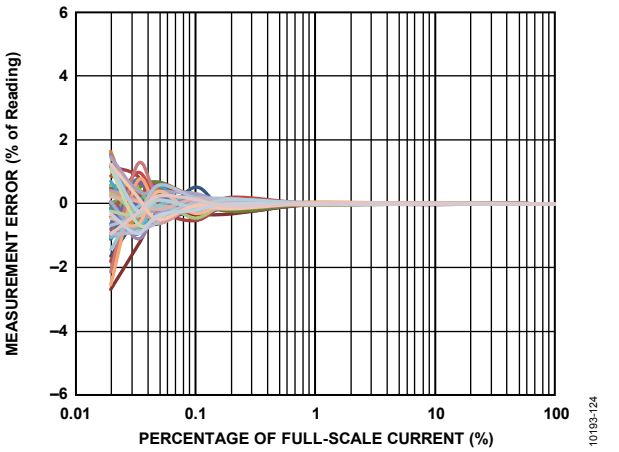

Figure 31. Harmonic Apparent Power Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, 10 Averages per Reading, 750 ms Settling Time, 125 µs Update Rate

TEST CIRCUIT

In Figure 32, the PM1 and PM0 pins are pulled up internally to VDD. Select the mode of operation by using a microcontroller to programmatically change the pin values. See the Power Management section for details.

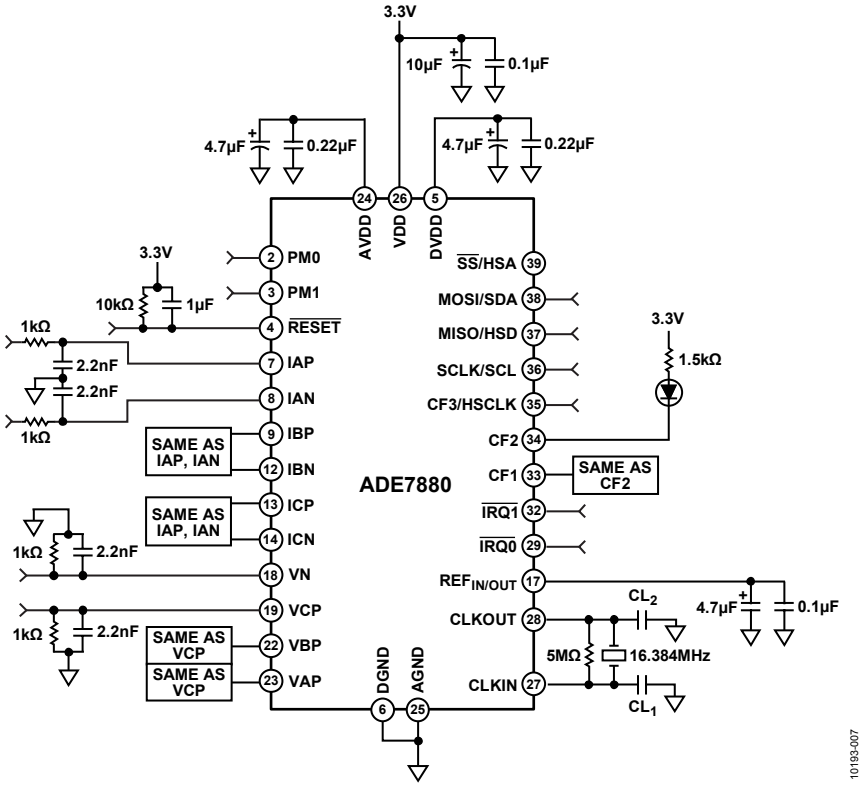

Figure 32. Test Circuit

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7880 is defined by

$$Measurement\ Error = \frac{Energy\ Registered\ by\ ADE7880 - True\ Energy}{True\ Energy} \times 100\% \quad (1)$$

Power Supply Rejection (PSR)

This quantifies the ADE7880 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at 100 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading (see the Measurement Error definition).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±10%. Any error introduced is expressed as a percentage of the reading.

ADC Offset

ADC offset refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection. The high-pass filter (HPF) removes the offset from the current and voltage channels; therefore, the power calculation remains unaffected by this offset.

Gain Error

The gain error in the ADCs of the ADE7880 is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC section and the Voltage Channel ADC section). The difference is expressed as a percentage of the ideal code.

CF Jitter

The period of pulses at one of the CF1, CF2, or CF3 pins is continuously measured. The maximum, minimum, and average values of four consecutive pulses are computed as follows:

$$Maximum = max(Period_0, Period_1, Period_2, Period_3)$$

$$Minimum = min(Period_0, Period_1, Period_2, Period_3)$$

$$Average = \frac{Period_0 + Period_1 + Period_2 + Period_3}{4}$$

The CF jitter is then computed as

$$CF_{JITTER} = \frac{Maximum - Minimum}{Average} \times 100\% \quad (2)$$

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below 3.3 kHz, excluding harmonics and dc. The input signal contains only the fundamental component. The spectral components are calculated over a 2 sec window. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below 3.3 kHz, including harmonics but excluding dc. The input signal contains only the fundamental component. The spectral components are calculated over a 2 sec window. The value for SINAD is expressed in decibels.

Harmonic Power Measurement Error

To measure the error in the harmonic active and reactive power calculations made by the ADE7880, the voltage channel is supplied with a signal comprising a fundamental and one harmonic component with amplitudes equal to 250 mV. The current channel is supplied with a signal comprising a fundamental with amplitude of 50 mV and one harmonic component of the same index as the one in the voltage channel. The amplitude of the harmonic is varied from 250 mV, down to 250 μV, 2000 times lower than full scale.

The error is defined by

$$Measurement\ Error = \frac{Power\ Registered\ by\ ADE7880 - True\ Power}{True\ Power} \times 100\% \quad (3)$$

POWER MANAGEMENT

The ADE7880 has four modes of operation, determined by the state of the PM0 and PM1 pins (see Table 8). These pins provide complete control of the ADE7880 operation and can easily be connected to an external microprocessor I/O. The PM0 and PM1 pins have internal pull-up resistors. See Table 10 and Table 11 for a list of actions that are recommended before and after setting a new power mode.

Table 8. Power Supply Modes

Power Supply Modes	PM1	PM0
PSM0, Normal Power Mode	0	1
PSM1, Reduced Power Mode	0	0
PSM2, Low Power Mode	1	0
PSM3, Sleep Mode	1	1

PSM0—NORMAL POWER MODE (ALL PARTS)

In PSM0 mode, the ADE7880 is fully functional. For the ADE7880 to enter this mode, the PM0 pin is set to high, and the PM1 pin is set to low. If the ADE7880 is in PSM1, PSM2, or PSM3 mode and is switched into PSM0 mode, then all control registers take the default values with the exception of the threshold register, LPOILVL, which is used in PSM2 mode, and the CONFIG2 register, both of which maintain their values.

The ADE7880 signals the end of the transition period by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is 0 during the transition period and becomes 1 when the transition is finished. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set back to high by writing to the STATUS1 register with the corresponding bit set to 1. Bit 15 (RSTDONE) in the interrupt mask register does not have any functionality attached even if the $\overline{\text{IRQ1}}$ pin goes low when Bit 15 (RSTDONE) in the STATUS1 register is set to 1. This makes the RSTDONE interrupt unmaskable.

PSM1—REDUCED POWER MODE

In the reduced power mode, PSM1, the ADE7880 measures the mean absolute values (mav) of the 3-phase currents and stores the results in the AIMAV, BIMAV, and CIMAV 20-bit registers. This mode is useful in missing neutral cases in which the voltage supply of the ADE7880 is provided by an external battery. The serial ports, I^2C or SPI, are enabled in this mode; the active port can be used to read the AIMAV, BIMAV, and CIMAV registers. Do not read any of the other registers as their values are not guaranteed in this mode. Similarly, the ADE7880 does not take a write operation into account by in this mode.

In summary, in this mode, it is not recommended to access any register other than AIMAV, BIMAV, and CIMAV. The circuit that computes the rms estimates is also active during PSM0; therefore, its calibration can be completed in either PSM0 mode or in PSM1 mode. Note that the ADE7880 does not provide any register to store or process the corrections resulting from the calibration process. The external microprocessor stores the gain values in connection with these measurements and uses them during PSM1 (see the Current Mean Absolute Value Calculation section for more details on the xIMAV registers).

The 20-bit mean absolute value measurements done in PSM1, although also available in PSM0, are different from the rms measurements of phase currents and voltages executed only in PSM0 and stored in the HxIRMS and HxVRMS 24-bit registers. See the Current Mean Absolute Value Calculation section for details.

If the ADE7880 is set in PSM1 mode after being in PSM0 mode, the ADE7880 begins the mean absolute value calculations without any delay. The xIMAV registers are accessible at any time; however, if the ADE7880 is set in PSM1 mode after being in PSM2 or PSM3 modes, the ADE7880 signals the start of the mean absolute value computations by triggering the $\overline{\text{IRQ1}}$ pin low. The xIMAV registers can be accessed only after this moment.

PSM2—LOW POWER MODE

In the low power mode, PSM2, the ADE7880 compares all phase currents against a threshold for a period of 0.02 × (LPLINE[4:0] + 1) seconds, independent of the line frequency. LPLINE[4:0] are Bits[7:3] of the LPOILVL register (see Table 9).

Table 9. LPOILVL Register

Bit	Mnemonic	Default	Description
[2:0]	LPOIL[2:0]	111	Threshold is put at a value corresponding to full scale multiplied by LPOIL/8
[7:3]	LPLINE[4:0]	00000	The measurement period is (LPLINE[4:0] + 1)/50 sec

The threshold is derived from Bits[2:0] (LPOIL[2:0]) of the LPOILVL register as LPOIL[2:0]/8 of full scale. Every time one phase current becomes greater than the threshold, a counter is incremented. If every phase counter remains below LPLINE[4:0] + 1 at the end of the measurement period, then the $\overline{\text{IRQ0}}$ pin is triggered low. If a single phase counter becomes greater or equal to LPLINE[4:0] + 1 at the end of the measurement period, the $\overline{\text{IRQ1}}$ pin is triggered low. Figure 33 illustrates how the ADE7880 behaves in PSM2 mode when LPLINE[4:0] = 2 and LPOIL[2:0] = 3. The test period is three 50 Hz cycles (60 ms), and the Phase A current rises above the LPOIL[2:0] threshold three times. At the end of the test period, the $\overline{\text{IRQ1}}$ pin is triggered low.

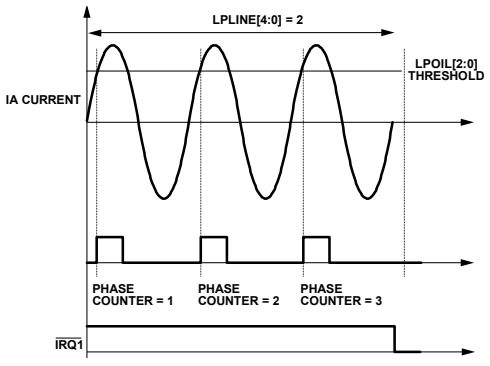

Figure 33. PSM2 Mode Triggering $\overline{\text{IRQ}}$ Pin for LPLINE[4:0] = 2 (50 Hz Systems)

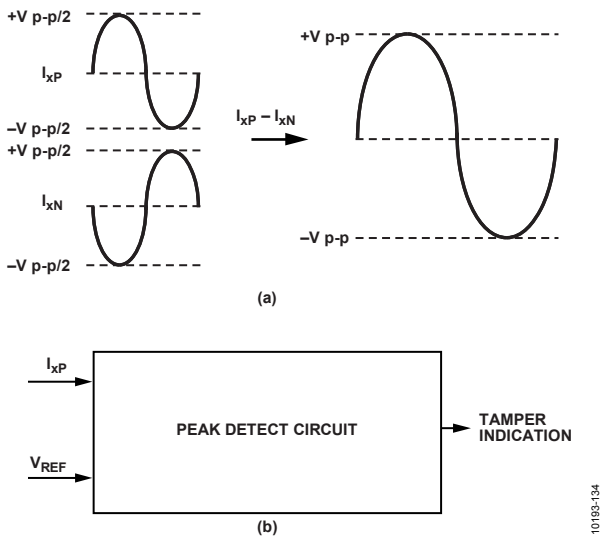

Figure 34. PSM2 Low Power Mode Peak Detection

The PSM2 level threshold comparison works based on a peak detection methodology. The peak detect circuit makes the comparison based on the positive terminal current channel input, I_{AP}, I_{BP}, and I_{CP} (see Figure 34). In case of differential inputs being applied to the current channels, Figure 34 shows the differential antiphase signals at each of the current input terminals, I_{xP} and I_{xN}, and the net differential current, $I_{xP} - I_{xN}$.

The I²C or SPI port is not functional during this mode. The PSM2 mode reduces the power consumption required to monitor the currents when there is no voltage input and the voltage supply of the ADE7880 is provided by an external battery. If the $\overline{\text{IRQ0}}$ pin is triggered low at the end of a measurement period, it signifies all phase currents stayed below threshold and, therefore, there is no current flowing through the system. At this point, the external microprocessor sets the ADE7880 into sleep mode PSM3. If the $\overline{\text{IRQ1}}$ pin is triggered low at the end of the measurement period, it signifies that at least one current input is above the defined threshold and current is flowing through the system, although no voltage is present at the ADE7880 pins. This situation is often called missing neutral and is considered a tampering situation, at which point the external microprocessor sets the ADE7880 into PSM1 mode, measures the mean absolute values of phase currents, and integrates the energy based on their values and the nominal voltage.

It is recommended to use the ADE7880 in PSM2 mode when Bits[2:0] (PGA1[2:0]) of the Gain register are equal to 1 or 2. These bits represent the gain in the current channel data path. It is not recommended to use the ADE7880 in PSM2 mode when the PGA1[2:0] bits are equal to 4, 8, or 16.

PSM3—SLEEP MODE (ALL PARTS)

In sleep mode, the ADE7880 has most of its internal circuits turned off and the current consumption is at its lowest level. The I²C, HSDC, and SPI ports are not functional during this mode, and the $\overline{\text{RESET}}$, SCLK/SCL, MOSI/SDA, and $\overline{\text{SS}}$/HSA pins must be set high.

Table 10. Power Modes and Related Characteristics

Power Mode	All Registers[1]	LPOILVL, CONFIG2	I²C/SPI	Functionality
PSM0				
State After Hardware Reset	Set to default	Set to default	I²C enabled	All circuits are active and DSP is in idle mode.
State After Software Reset	Set to default	Unchanged	Active serial port is unchanged if lock-in procedure has been previously executed	All circuits are active and DSP is in idle mode.
PSM1	Not available	PSM0 values retained	Enabled	Current mean absolute values are computed and the results are stored in the AIMAV, BIMAV, and CIMAV registers. The I²C or SPI serial port is enabled with limited functionality.
PSM2	Not available	PSM0 values retained	Disabled	Compares phase currents against the threshold set in LPOILVL. Triggers $\overline{\text{IRQ0}}$or $\overline{\text{IRQ1}}$ pins accordingly. The serial ports are not available.
PSM3	Not available	PSM0 values retained	Disabled	Internal circuits shut down and the serial ports are not available.

[1] Setting for all registers except the LPOILVL and CONFIG2 registers.

Table 11. Recommended Actions When Changing Power Modes

Initial Power Mode	Before Setting Next Power Mode	Next Power Mode			
		PSM0	PSM1	PSM2	PSM3
PSM0	Stop DSP by setting the Run register = 0x0000 Disable HSDC by clearing Bit 6 (HSDCEN) to 0 in the CONFIG register Mask interrupts by setting MASK0 = 0x0 and MASK1 = 0x0 Erase interrupt status flags in the STATUS0 and STATUS1 registers		Current mean absolute values (mav) computed immediately xIMAV registers can be accessed immediately	Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly	No action necessary
PSM1	No action necessary	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1		Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly	No action necessary
PSM2	No action necessary	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1	Wait until the $\overline{\text{IRQ1}}$ pin triggered low Current mean absolute values compute at this moment xIMAV registers may be accessed from this moment		No action necessary
PSM3	No action necessary	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Current mav circuit begins computations at this time xIMAV registers can be accessed from this moment	Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly	

POWER-UP PROCEDURE

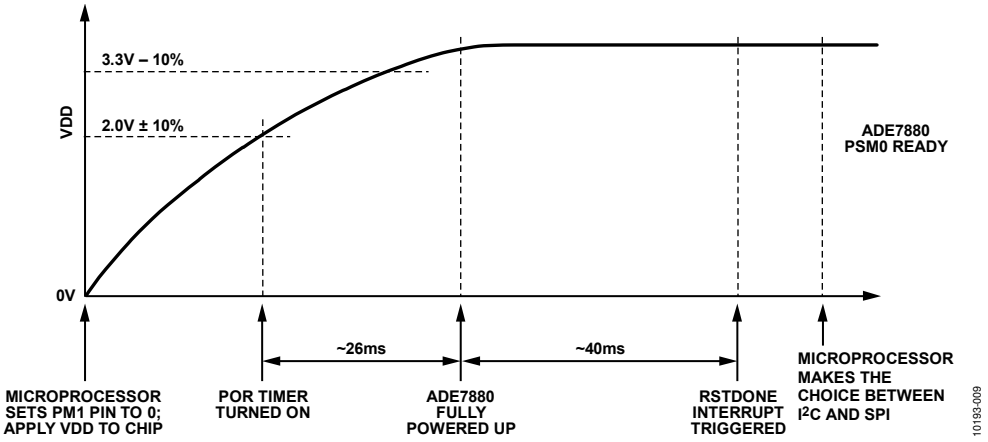

Figure 35. Power-Up Procedure

The ADE7880 contains an on-chip power supply monitor that supervises the power supply (VDD). At power-up, the device is inactive until VDD reaches 2.0 V ± 10%. When VDD crosses this threshold, the power supply monitor keeps the device in the inactive state for an additional 26 ms to allow VDD to rise to 3.3 V − 10%, the minimum recommended supply voltage.

The PM0 and PM1 pins have internal pull-up resistors, but it is necessary to set the PM1 pin to Logic 0, either through a microcontroller or by grounding the PM1 pin externally, before powering up the chip. The PM0 pin can remain open as it is held high, due to the internal pull-up resistor. This ensures that the ADE7880 always powers up in PSM0 (normal) mode. The time from the chip being powered up completely to all functionality being enabled is about 40 ms (see Figure 35). It is necessary to ensure that the $\overline{\text{RESET}}$ pin is held high during the entire power-up procedure.

If PSM0 mode is the only desired power mode, the PM1 pin can be tied to ground externally. When the ADE7880 enters PSM0 mode, the I²C port is the active serial port. To use the SPI port, toggle the $\overline{\text{SS}}$/HSA pin three times from high to low.

To lock I²C as the active serial port, set Bit 1 (I2C_LOCK) of the CONFIG2 register to 1. From this moment, the device ignores spurious toggling of the $\overline{\text{SS}}$/HSA pin, and a switch to the SPI port is no longer possible.

If SPI is the active serial port, any write to the CONFIG2 register locks the port, and a switch to the I²C port is no longer possible. To use the I²C port, the ADE7880 must be powered down or the device must be reset by setting the $\overline{\text{RESET}}$ pin low. After the serial port is locked, the serial port selection is maintained when the device changes from one PSMx power mode to another.

Immediately after entering PSM0 mode, all registers in the ADE7880 are set to their default values, including the CONFIG2 and LPOILVL registers.

The ADE7880 signals the end of the transition period by pulling the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is cleared to 0 during the transition period and is set to 1 when the transition ends. Writing the STATUS1 register with the RSTDONE bit set to 1 clears the status bit and returns the $\overline{\text{IRQ1}}$ pin high. Because RSTDONE is an unmaskable interrupt, Bit 15 (RSTDONE) in the STATUS1 register must be cancelled for the $\overline{\text{IRQ1}}$ pin to return high. Wait until the $\overline{\text{IRQ1}}$ pin goes low before accessing the STATUS1 register to test the state of the RSTDONE bit. At this point, as a good programming practice, cancel all other status flags in the STATUS1 and STATUS0 registers by writing the corresponding bits with 1.

Initially, the DSP is in idle mode and, therefore, does not execute any instructions. This is the moment to initialize all registers in the ADE7880. See the Digital Signal Processor section for the proper procedure to initialize all registers and start the metering.

If the supply voltage, VDD, falls lower than 2.0 V ± 10%, the ADE7880 enters an inactive state, which means that no measurements or computations are executed.

If the $\overline{\text{RESET}}$ pin is held low while the IC powers up or if the power-up sequence timing cannot be maintained as per Figure 35, perform the following sequence of write operations prior to starting the DSP (setting the RUN register to 0x01), to ensure that the modulators are reset properly.

1. 8-bit write: 0xAD is written at Address 0xE7FE.
2. 8-bit write: 0x14 is written at Address 0xE7E2.
3. Wait 200 µs.
4. 8-bit write: 0xAD is written at Address 0xE7FE.
5. 8-bit write: 0x04 is written at Address 0xE7E2.