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3-Channel, Isolated, Sigma-Delta ADC with SPI

ADE7912/ADE7913

FEATURES

Two (ADE7912) or three (ADE7913) isolated, Σ-Δ analog-to-digital converters (simultaneously sampling ADCs)
Integrated *iso*Power, isolated dc-to-dc converter
On-chip temperature sensor
4-wire SPI serial interface
Up to 4 ADE7912/ADE7913 devices clocked from a single crystal or an external clock
Synchronization of multiple ADE7912/ADE7913 devices
±31.25 mV peak input range for current channel
±500 mV peak input range for voltage channels
Reference drift: 10 ppm/°C typical
Single 3.3 V supply
20-lead, wide-body SOIC package with 8.3 mm creepage
Operating temperature: −40°C to +85°C
Safety and regulatory approvals
    UL recognition
        5000 V rms for 1 minute per UL 1577
    CSA Component Acceptance Notice 5A
        IEC 61010-1: 300 V rms
    VDE certificate of conformity
        DIN VDE V 0884-10 (VDE V 0884-10):2006-12
        V_{IORM} = 846 V peak

APPLICATIONS

Shunt-based polyphase meters
Power quality monitoring
Solar inverters
Process monitoring
Protective devices
Isolated sensor interfaces
Industrial PLCs

TYPICAL APPLICATIONS CIRCUIT

Figure 1.

GENERAL DESCRIPTION

The ADE7912/ADE7913[1] are isolated, 3-channel Σ-Δ ADCs for polyphase energy metering applications using shunt current sensors. Data and power isolation are based on the Analog Devices, Inc., *i*Coupler® technology. The ADE7912 features two ADCs, and the ADE7913 features three ADCs. The current ADC provides a 67 dB signal-to-noise ratio (SNR) over a 3 kHz signal bandwidth, whereas the voltage ADCs provide an SNR of 72 dB over 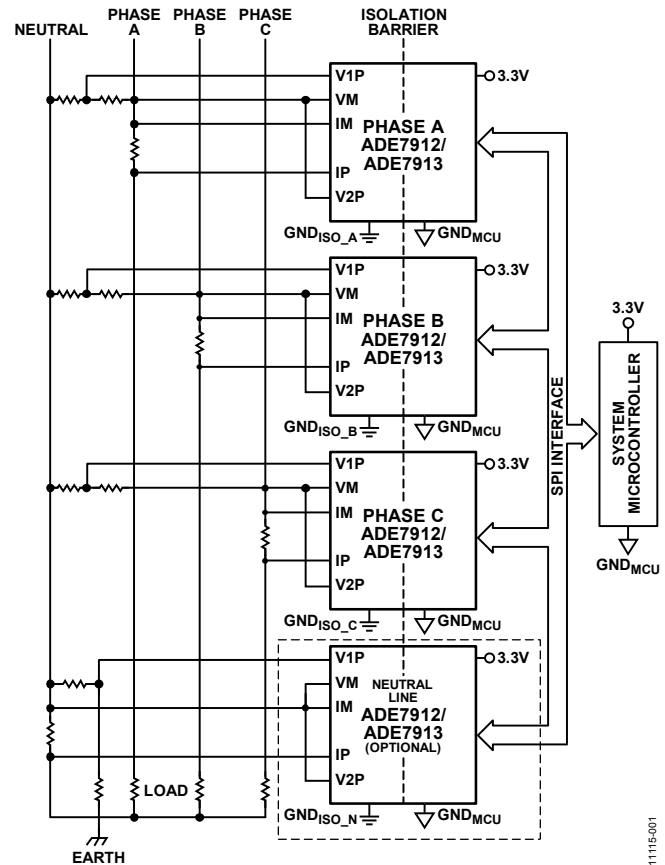the same bandwidth. One channel is dedicated to measuring the voltage across a shunt when the shunt is used for current sensing. Up to two additional channels are dedicated to measuring voltages, which are usually sensed using resistor dividers. One voltage channel can measure the temperature of the die via an internal sensor. The ADE7913 includes three channels: one current and two voltage channels. The ADE7912 has one voltage channel but is otherwise identical to the ADE7913.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329; 6,262,600; 7,489,526; 7,558,080; 8,892,933. Other patents are pending.

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REVISION HISTORY

The ADE7912/ADE7913 include *iso*Power®, an integrated, isolated dc-to-dc converter. Based on the Analog Devices *i*Coupler technology, the dc-to-dc converter provides the regulated power required by the first stage of the ADCs at a 3.3 V input supply. *iso*Power eliminates the need for an external dc-to-dc isolation block. The *i*Coupler chip scale transformer technology also isolates the logic signals between the first and second stages of the ADC. The result is a small form factor, total isolation solution.

The ADE7912/ADE7913 configuration and status registers are accessed via a bidirectional SPI serial port for easy interfacing with microcontrollers.

The ADE7912/ADE7913 can be clocked from a crystal or an external clock signal. To minimize the system bill of materials, the master ADE7912/ADE7913 can drive the clocks of up to three additional ADE7912/ADE7913 devices.

Multiple ADE7912/ADE7913 devices can be synchronized to sample at the same moment and provide coherent outputs.

The ADE7912/ADE7913 are available in a 20-lead, Pb-free, wide-body SOIC package with 8.3 mm creepage.
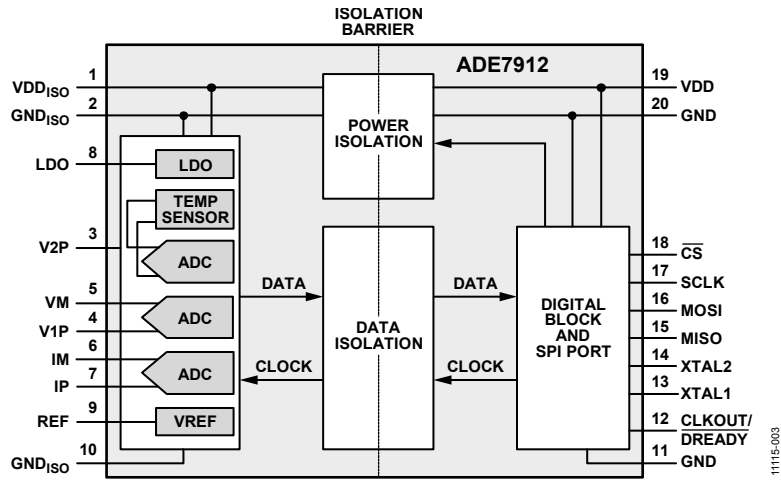
FUNCTIONAL BLOCK DIAGRAMS
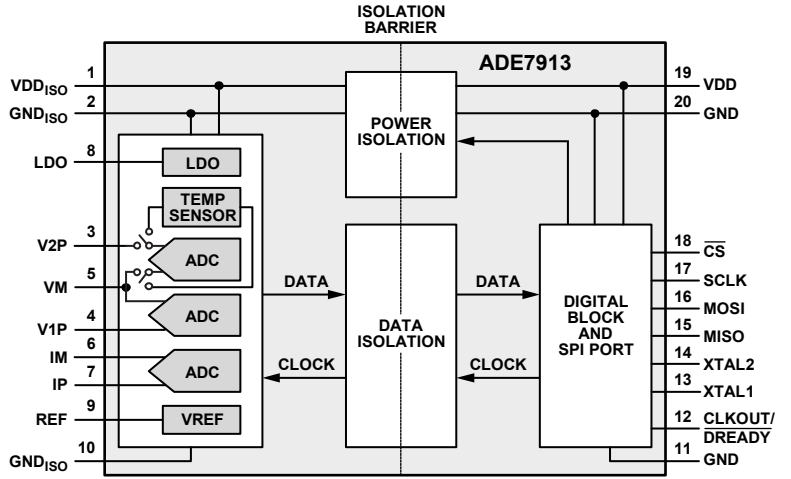

Figure 2. ADE7912 Functional Block Diagram

Figure 3. ADE7913 Functional Block Diagram

SPECIFICATIONS

VDD = 3.3 V ± 10%, GND = 0 V, on-chip reference, XTAL1 = 4.096 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_A = 25°C (typical).

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG INPUTS[1]					
Pseudo Differential Signal Voltage Range Between IP and IM Pins	−31.25		+31.25	mV peak	IM pin connected to GND_{ISO}
Pseudo Differential Signal Voltage Range Between V1P and VM Pins and Between V2P and VM Pins	−500		+500	mV peak	Pseudo differential inputs between V1P and VM pins and between V2P and VM pins; VM pin connected to GND_{ISO}
Maximum VM and IM Voltage	−25		+25	mV	
Crosstalk		−90		dB	IP and IM inputs set to 0 V (GND_{ISO}) when V1P and V2P inputs at full scale
		−105		dB	V2P and VM inputs set to 0 V (GND_{ISO}) when IP and V1P inputs at full scale; V1P and VM inputs set to 0 V (GND_{ISO}) when IP and V2P inputs at full scale
Input Impedance to GND_{ISO} (DC)					
IP, IM, V1P, and V2P Pins	480			kΩ	
VM Pin	240			kΩ	
Current Channel ADC Offset Error		−2		mV	
Voltage Channels ADC Offset Error		−35		mV	V2 channel applies to the ADE7913 only
ADC Offset Drift over Temperature		±200		ppm/°C	V1 channel only
Gain Error	−4		+4	%	
Gain Drift over Temperature	−135		+135	ppm/°C	Current channel
	−85		+85	ppm/°C	V1 and V2 channels
AC Power Supply Rejection (PSR)		−90		dB	VDD = 3.3 V + 120 mV rms (50 Hz/100 Hz), IP = V1P = V2P = GND_{ISO}
DC Power Supply Rejection (PSR)		−80		dB	VDD = 3.3 V ± 330 mV dc, IP = 6.25 mV rms, V1P = V2P = 100 mV rms
TEMPERATURE SENSOR					
Accuracy		±5		°C	
WAVEFORM SAMPLING—CURRENT CHANNEL[1]					
Signal-to-Noise Ratio (SNR)		67		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		68		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		72		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		74		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Signal-to-Noise-and-Distortion Ratio (SINAD)		66		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		68		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		72		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		73		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Total Harmonic Distortion (THD)		−79		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		−78		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		−82		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		−82		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Spurious-Free Dynamic Range (SFDR)		83		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		83		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		85		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		85		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
VOLTAGE CHANNELS[1]					
Signal-to-Noise Ratio (SNR)		72		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		74		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		77		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		79		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Signal-to-Noise-and-Distortion Ratio (SINAD)		72		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		74		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		77		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		78		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Total Harmonic Distortion (THD)		−83		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		−83		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		−85		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		−85		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
Spurious-Free Dynamic Range (SFDR)		86		dBFS	ADC_FREQ = 8 kHz, BW = 3300 Hz
		86		dBFS	ADC_FREQ = 8 kHz, BW = 2000 Hz
		87		dBFS	ADC_FREQ = 2 kHz, BW = 825 Hz
		87		dBFS	ADC_FREQ = 2 kHz, BW = 500 Hz
CLKIN[2]					All specifications for CLKIN = 4.096 MHz
Input Clock Frequency, CLKIN	3.6	4.096	4.21	MHz	
CLKIN Duty Cycle	45	50	55	%	
XTAL1 Logic Inputs					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	
XTAL1 Total Capacitance[3]		40		pF	
XTAL2 Total Capacitance[3]		40		pF	
CLKOUT Delay from XTAL1[4]			100	ns	
LOGIC INPUTS—MOSI, SCLK, $\overline{CS}$					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}		0.015	1	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS—CLKOUT/$\overline{DREADY}$ AND MISO					
Output High Voltage, V_{OH}	2.5			V	I_{SOURCE} = 800 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
POWER SUPPLY					For specified performance
VDD Pin	2.97		3.63	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
I_{DD}		12.5	19	mA	Bit 2 (PWRDWN_EN) in CONFIG register cleared to 0
		2.7	3	mA	Bit 2 (PWRDWN_EN) in CONFIG register set to 1
		50		µA	Bit 2 (PWRDWN_EN) in CONFIG register set to 1 and no CLKIN signal at XTAL1 pin

[1] See the Terminology section for a definition of the parameters.
[2] CLKIN is the internal clock of the ADE7912/ADE7913. It is the frequency at which the part is clocked at the XTAL1 pin.
[3] XTAL1/XTAL2 total capacitances refer to the net capacitances on each pin. Each capacitance is the sum of the parasitic capacitance at the pin and the capacitance of the ceramic capacitor connected between the pin and GND. See the ADE7912/ADE7913 Clock section for more details.
[4] CLKOUT delay from XTAL1 is the delay that occurs from a high to low transition at the XTAL1 pin to a synchronous high to low transition at the CLKOUT/$\overline{DREADY}$ pin when CLKOUT functionality is enabled.

REGULATORY APPROVALS

The ADE7912/ADE7913 are approved by the organizations listed in Table 2. Refer to Table 8 and the Insulation Lifetime section for more information about the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Note that Table 8 presents the maximum working voltages for 50-year minimum lifetime: 400 V rms for ac voltages and 1173 V peak for dc voltages. Greater working voltages shorten the lifetime of the product (see the Insulation Lifetime section). Some certifications in Table 2 state greater maximum working voltages than the values presented in Table 8. Therefore, use the ADE7912/ADE7913 only for working voltages lower than those presented in Table 8 (400 V rms for ac voltages and 1173 V peak for dc voltages).

Table 2. Regulatory Approvals

UL	CSA	VDE
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN VDE V 0884-10[2] (VDE V 0884-10):2006-12
Single Protection, 5000 V rms Isolation Voltage	Basic insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2:	Reinforced insulation, 846 V peak[4]
	830 V rms (1173 V peak) maximum working voltage[3]	
	Basic insulation per CSA 61010-1-12 and IEC 61010-1 3rd Ed. (Pollution Degree 2, Material Group III, Overvoltage Category II, III, and IV):	
	300 V rms (424 V peak) maximum working voltage.	
	Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2:	
	415 V rms (586 V peak) maximum working voltage	
	Reinforced insulation per CSA 61010-1-12 and IEC 61010-1 3rd Ed. (Pollution Degree 2, Material Group III, Overvoltage Category II, and III):	
	300 V rms (424 V peak) maximum working voltage.	
FILE E214100	FILE 2758945	FILE 2471900-4880-0001

[1] In accordance with UL 1577, each ADE7912/ADE7913 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 second (current leakage detection limit = 15 μA).
[2] In accordance with DIN V VDE V 0884-10, each ADE7912/ADE7913 is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN VDE V 0884-10 (VDE V 0884-10):2006-12 approval.
[3] At this maximum working voltage, the approximate predicted lifetime is 0.2 years under 50 Hz, 60 Hz ac voltages.
[4] At this maximum working voltage, the approximate predicted lifetime is 8 years under 50 Hz, 60 Hz ac voltages.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 3. Critical Safety Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(l01)	8.3	mm	Distance measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PCB layout
Minimum External Tracking (Creepage)	L(l02)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	400	V	IEC 60112
Isolation Group		II		Material group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

The [ADE7912](ADE7912)/[ADE7913](ADE7913) are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits.

Table 4. VDE Characteristics

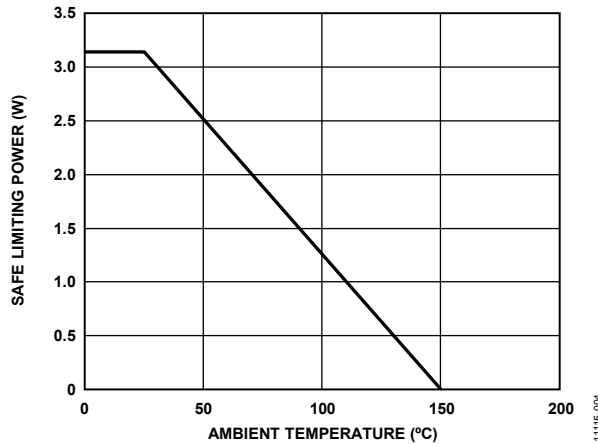| Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/085/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	846	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input-to-Output Test Voltage, Method A		$V_{pd(m)}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1273	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1018	V peak
Highest Allowable Overvoltage		V_{IOTM}	6000	V peak
Surge Isolation Voltage	$V_{PEAK} = 10$ kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	6250	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 4)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.78	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	>10⁹	Ω

Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-10

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, GND = 0 V, on-chip reference, CLKIN = 4.096 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 5. SPI Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
$\overline{CS}$ to SCLK Positive Edge	t_{SS}	50		ns
SCLK Frequency[1]		250	5600	kHz
SCLK Low Pulse Width	t_{SL}	80		ns
SCLK High Pulse Width	t_{SH}	80		ns
Data Output Valid After SCLK Edge	t_{DAV}		80	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	70		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	20		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{CS}$ Rising Edge	t_{DIS}	5	40	ns
$\overline{CS}$ High After SCLK Edge	t_{SFS}	0		ns

[1] Minimum and maximum specifications are guaranteed by design.
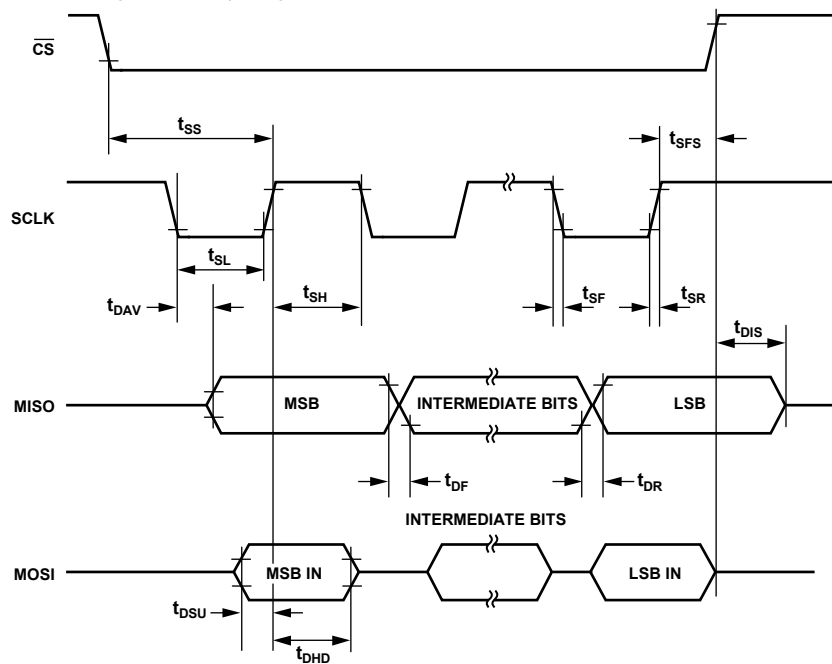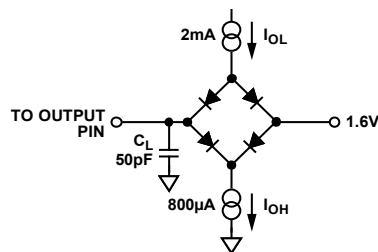

Figure 5. SPI Interface Timing

Figure 6. Load Circuit for Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
VDD to GND	−0.3 V to +3.7 V
Analog Input Voltage to GND$_{ISO}$, IP, IM, V1P, V2P, VM	−2 V to +2 V
Reference Input Voltage to GND$_{ISO}$	−0.3 V to VDD + 0.3 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.3 V
Common-Mode Transients[1]	−100 kV/µs to +100 kV/µs
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)[2]	260°C

[1] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

[2] Analog Devices recommends that reflow profiles used in soldering RoHS compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} and θ_{JC} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
20-Lead SOIC_IC	48.0	6.2	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 8. Maximum Continuous Working Voltage Supporting a 50-Year Minimum Lifetime[1]

Parameter	Max	Unit
AC Voltage, Bipolar Waveform	400	V rms
DC Voltage, Basic Insulation	1173	V peak

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Note that greater working voltages than the values presented in Table 8 shorten the lifetime of the product (see the Insulation Lifetime section). Therefore, although some certifications in Table 2 state bigger maximum working voltages, use the ADE7912/ADE7913 only for working voltages lower than the values presented in this Table 8.
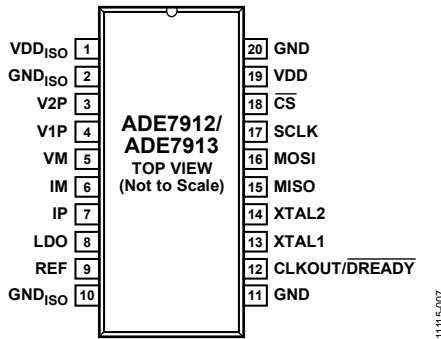
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Figure 7. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VDD$_{ISO}$	Isolated Secondary Side Power Supply. This pin provides access to the 2.8 V on-chip isolated power supply. Do not connect external load circuitry to this pin. Decouple this pin with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor using Pin 2, GND$_{ISO}$.
2, 10	GND$_{ISO}$	Ground Reference of the Isolated Secondary Side. These pins provide the ground reference for the analog circuitry. Use these quiet ground references for all analog circuitry. These two pins are connected together internally.
3, 4, 5	V2P, V1P, VM	Analog Inputs for the Voltage Channels. The voltage channels are used with the voltage transducers. V2P and V1P are pseudo differential voltage inputs with a maximum signal level of ±500 mV with respect to VM for specified operation. Use these pins with the related input circuitry, as shown in Figure 20. If V1P or V2P is not used, connect it to the VM pin. On the ADE7912, connect the V2P pin to the VM pin because the V2P voltage channel is not available. The second voltage channel is available on the ADE7913 only.
6, 7	IM, IP	Analog Inputs for the Current Channel. The current channel is used with shunts. IM and IP are pseudo differential voltage inputs with a maximum differential level of ±31.25 mV. Use these pins with the related input circuitry, as shown in Figure 20.
8	LDO	2.5 V Output of Analog Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor to GND$_{ISO}$, Pin 10. Do not connect external load circuitry to this pin.
9	REF	Voltage Reference. This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. Decouple this pin to GND$_{ISO}$, Pin 10, with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor.
11, 20	GND	Primary Ground Reference.
12	CLKOUT/$\overline{\text{DREADY}}$	Clock Output (CLKOUT). When CLKOUT functionality is selected (see the Synchronizing Multiple ADE7912/ADE7913 Devices section for details), the ADE7912/ADE7913 generate a digital signal synchronous to the master clock at the XTAL1 pin. Use CLKOUT to provide a clock to other ADE7912/ADE7913 devices on the board. Data Ready, Active Low ($\overline{\text{DREADY}}$). When $\overline{\text{DREADY}}$ functionality is selected (see the Synchronizing Multiple ADE7912/ADE7913 Devices section for details), the ADE7912/ADE7913 generate an active low signal synchronous to the ADC output frequency. Use this signal to start reading the ADC outputs of the ADE7912/ADE7913.
13	XTAL1	Master Clock Input. An external clock can be provided at this logic input. The CLKOUT/$\overline{\text{DREADY}}$ signal of another appropriately configured ADE7912/ADE7913 (see the Synchronizing Multiple ADE7912/ADE7913 Devices section for details) can be provided at this pin. Alternatively, a crystal with a maximum drive level of 0.5 mW and an equivalent series resistance (ESR) of 20 Ω can be connected across XTAL1 and XTAL2 to provide a clock source for the ADE7912/ADE7913. The clock frequency for specified operation is 4.096 MHz, but lower frequencies down to 3.6 MHz can be used. See the ADE7912/ADE7913 Clock section for more details.
14	XTAL2	Crystal, Second Input. A crystal with a maximum drive level of 0.5 mW and an ESR of 20 Ω can be connected across XTAL2 and XTAL1 to provide a clock source for the ADE7912/ADE7913.
15	MISO	Data Output for SPI Port. Pull up this pin with a 10 kΩ resistor (see the SPI-Compatible Interface section for details).
16	MOSI	Data Input for SPI Port.

Pin No.	Mnemonic	Description
17	SCLK	Serial Clock Input for SPI Port. All serial data transfers are synchronized to this clock (see the ADE7912/ADE7913 Clock section).
18	$\overline{CS}$	Chip Select for SPI Port.
19	VDD	Primary Supply Voltage. This pin provides the supply voltage for the ADE7912/ADE7913. Maintain the supply voltage at 3.3 V ± 10% for specified operation. Decouple this pin to GND, Pin 20, with a 10 μF capacitor in parallel with a ceramic 100 nF capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS
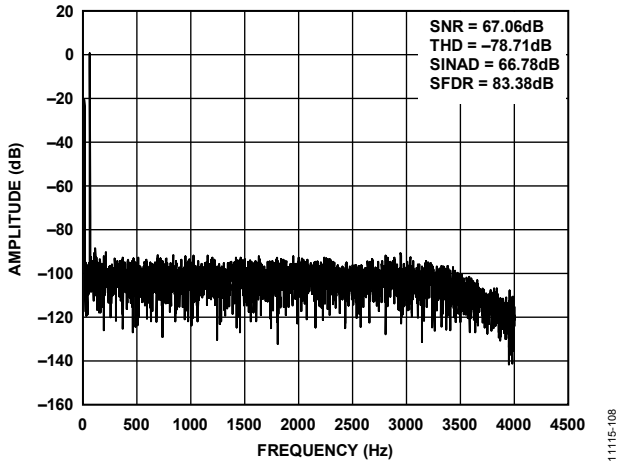
Figure 8. Current Channel FFT, ±31.25 mV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz
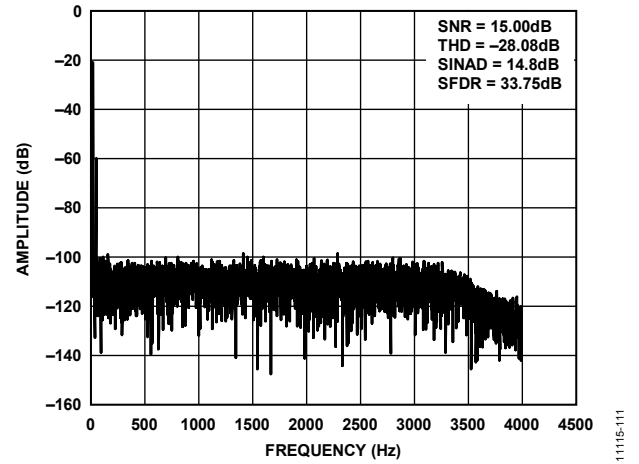

Figure 9. Current Channel FFT, ±31.25 µV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

Figure 10. Voltage Channel V1 FFT, ±500 mV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz
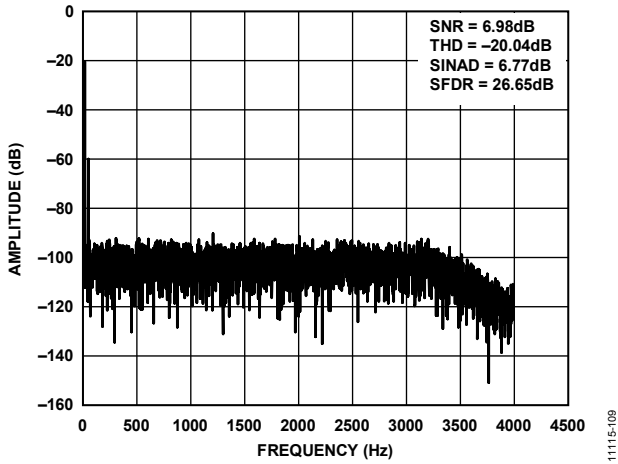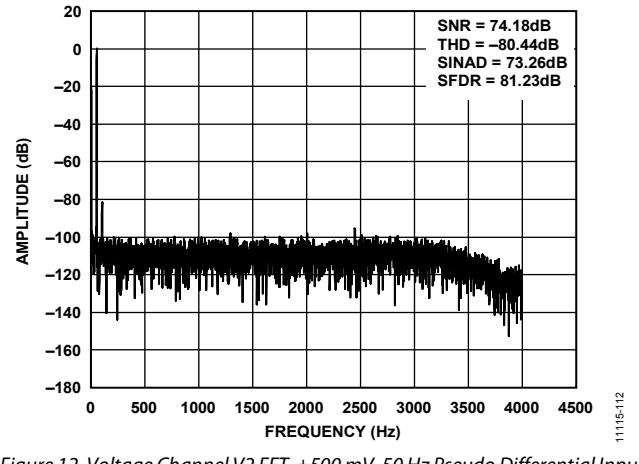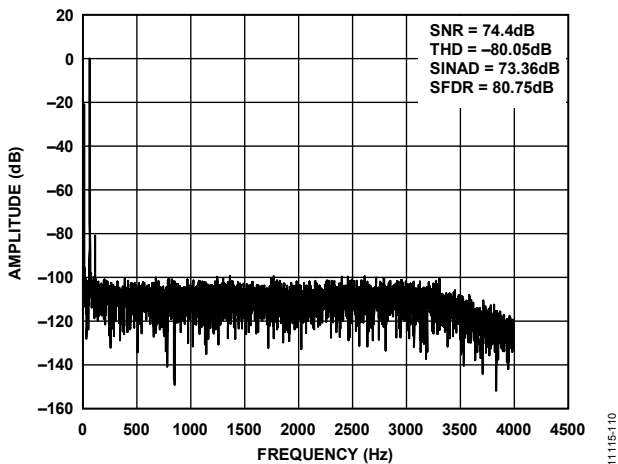

Figure 11. Voltage Channel V1 FFT, ±500 µV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz

Figure 12. Voltage Channel V2 FFT, ±500 mV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz
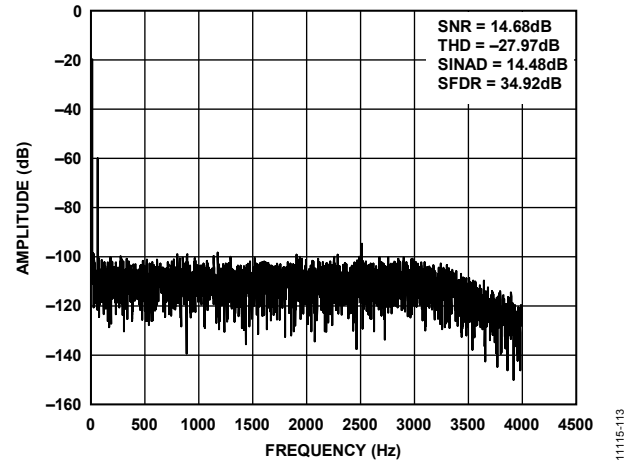

Figure 13. Voltage Channel V2 FFT, ±500 µV, 50 Hz Pseudo Differential Input Signal, ADC_FREQ = 8 kHz, BW = 3300 Hz
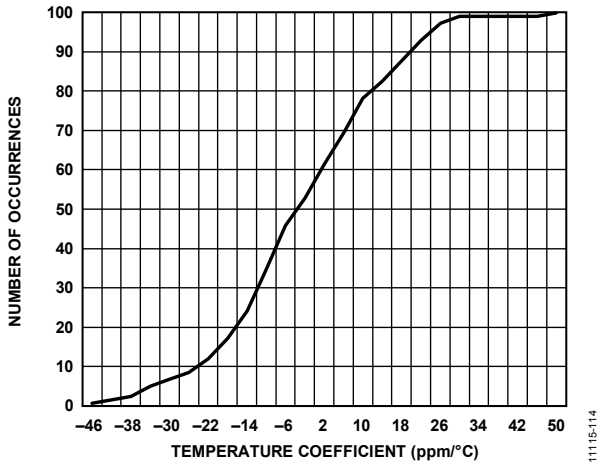
Figure 14. Cumulative Histogram of the Current Channel ADC Gain Temperature Coefficient for Temperatures Between −40°C and +25°C

Figure 15. Cumulative Histogram of the Current Channel ADC Gain Temperature Coefficient for Temperatures Between 25°C and 85°C

Figure 16. Cumulative Histogram of the Voltage Channel V1 ADC Gain Temperature Coefficient for Temperatures Between −40°C and +25°C
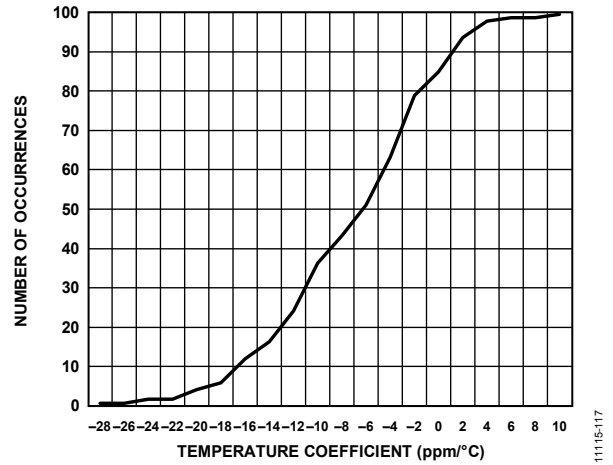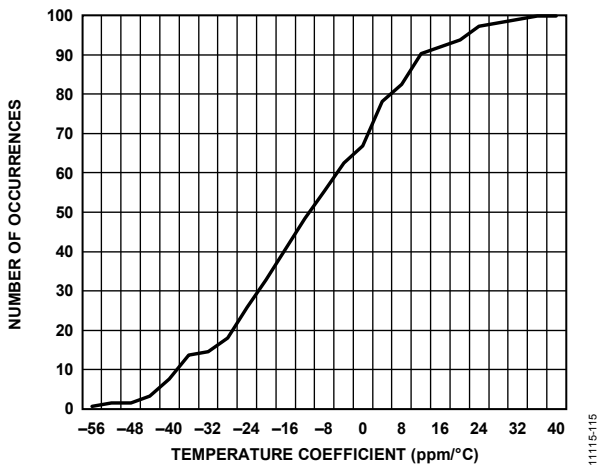

Figure 17. Cumulative Histogram of the Voltage Channel V1 ADC Gain Temperature Coefficient for Temperatures Between 25°C and 85°C

Figure 18. Cumulative Histogram of the Voltage Channel V2 ADC Gain Temperature Coefficient for Temperatures Between −40°C and +25°C
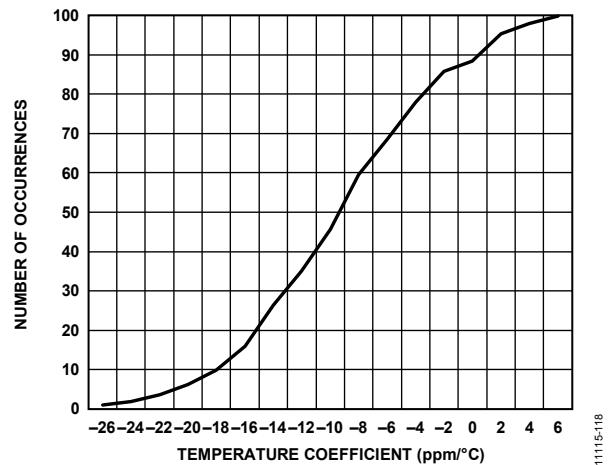

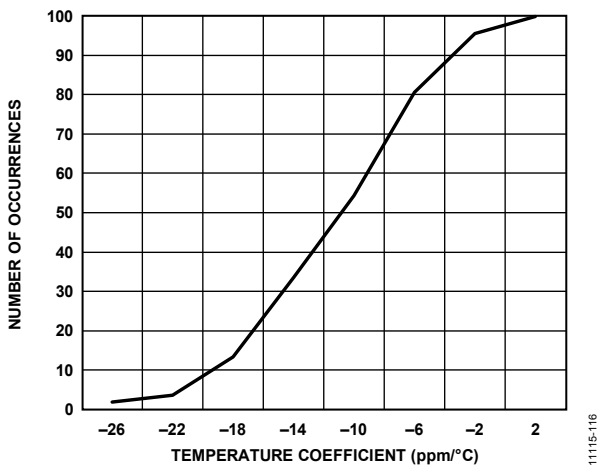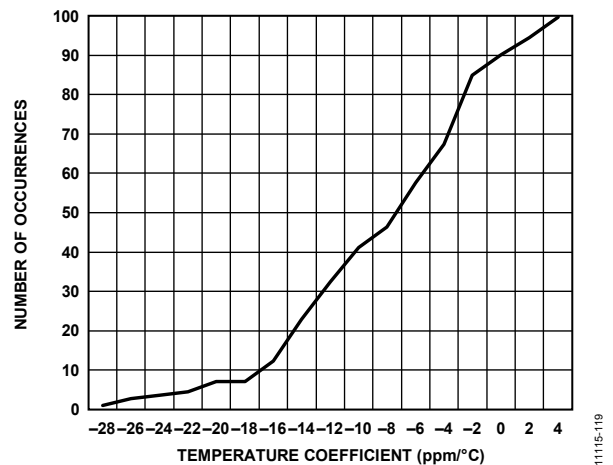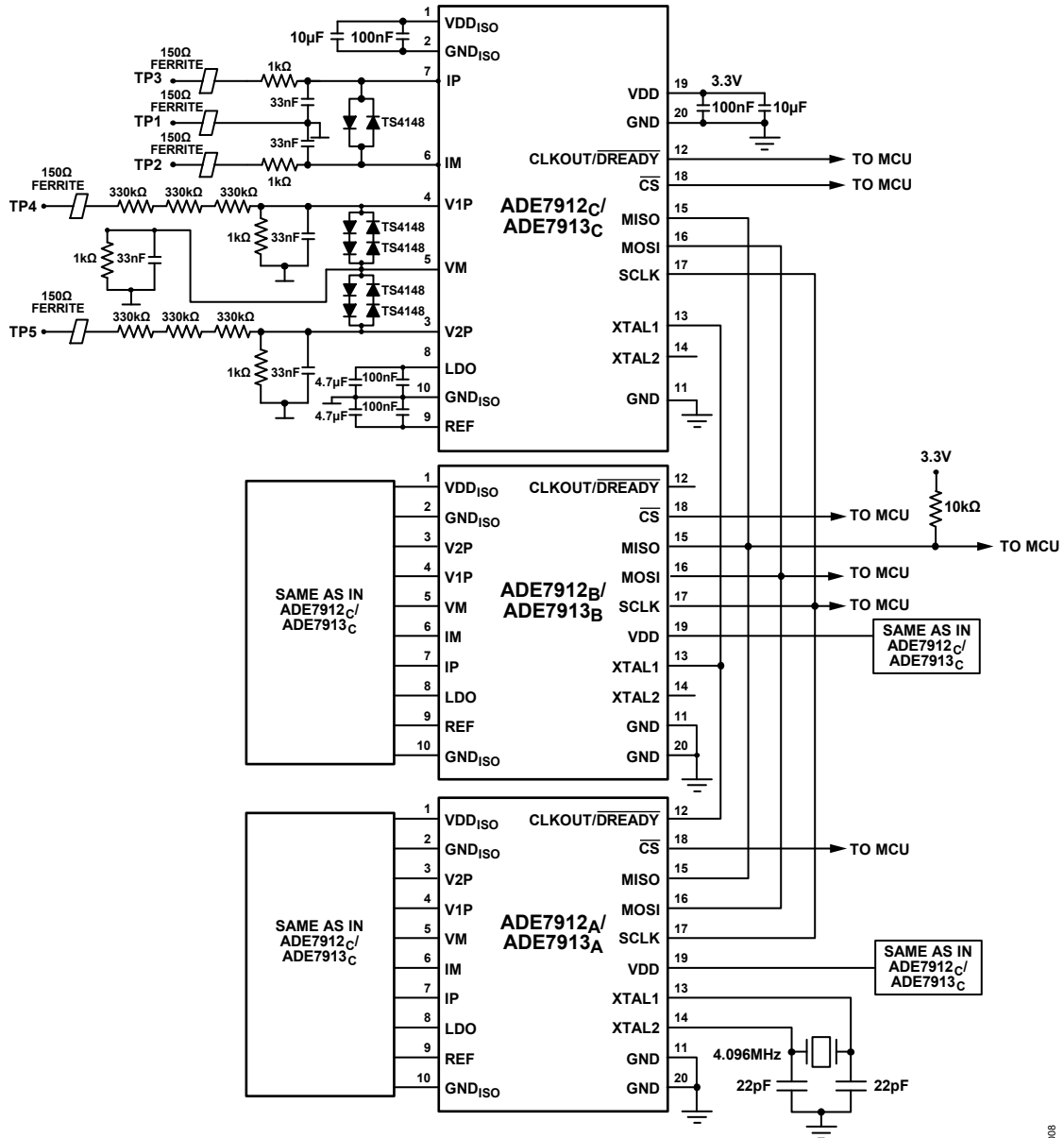Figure 19. Cumulative Histogram of the Voltage Channel V2 ADC Gain Temperature Coefficient for Temperatures Between 25°C and 85°C

TEST CIRCUIT

NOTES
1. ADE7912$_X$/ADE7913$_X$ = PHASE X ADE7912/ADE7913, WHERE X = A, B, OR C.

Figure 20. Test Circuit

TERMINOLOGY

Pseudo Differential Signal Voltage Range Between IP and IM, V1P and VM, and V2P and VM Pins

The range represents the peak-to-peak pseudo differential voltage that must be applied to the ADCs to generate a full-scale response when the IM and VM pins are connected to GND$_{ISO}$, Pin 2. The IM and VM pins are connected to GND$_{ISO}$ using antialiasing filters (see Figure 20). Figure 21 illustrates the input voltage range between IP and IM; Figure 22 illustrates the input voltage range between V1P and VM and between V2P and VM.
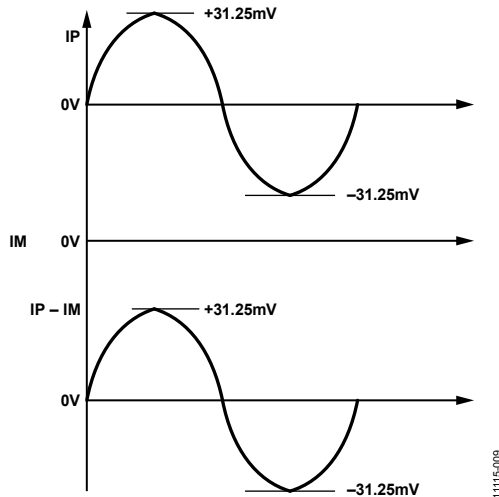

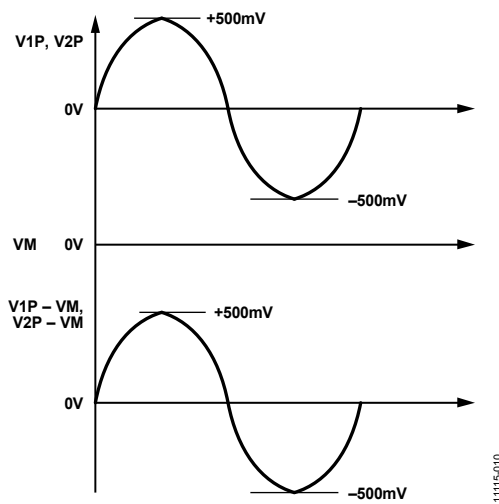*Figure 21. Pseudo Differential Input Voltage Range Between IP and IM Pins*

Figure 22. Pseudo Differential Input Voltage Range Between V1P and VM Pins and Between V2P and VM Pins

Maximum VM and IM Voltage Range

The range represents the maximum allowed voltage at VM and IM pins relative to GND$_{ISO}$, Pin 10.

Crosstalk

Crosstalk represents leakage of signals, usually via capacitance between circuits. Crosstalk is measured in the current channel by setting the IP and IM pins to GND$_{ISO}$, Pin 10, supplying a full-scale alternate differential voltage between the V1P and VM pins and between the V2P and VM pins of the voltage channel, and measuring the output of the current channel. It is measured in the V1P voltage channel by setting the V1P and VM pins to GND$_{ISO}$, Pin 10, supplying a full-scale alternate differential voltage at the IP and V2P pin, and measuring the output of the V1P channel. Crosstalk is measured in the V2P voltage channel by setting the V2P and VM pins to GND$_{ISO}$, Pin 10, supplying a full-scale alternate differential voltage at the IP and V1P pins, and measuring the output of the V2P channel. The crosstalk is equal to the ratio between the grounded ADC output value and the ADC full-scale output value. The ADC outputs are acquired for 2 sec. Crosstalk is expressed in decibels.

Input Impedance to Ground (DC)

The input impedance to ground represents the impedance measured at each ADC input pin (IP, IM, V1P, V2P, and VM) with respect to GND$_{ISO}$, Pin 10.

ADC Offset Error

ADC offset error is the difference between the average measured ADC output code with both inputs connected to GND$_{ISO}$ and the ideal ADC output code. The magnitude of the offset depends on the input range of each channel.

ADC Offset Drift over Temperature

The ADC offset drift is the change in offset over temperature. It is measured at −40°C, +25°C, and +85°C. The offset drift over temperature is computed as follows:

$$Drift = \max\left[\left|\frac{Offset(-40) - Offset(25)}{Offset(25) \times (-40 - 25)}\right|, \left|\frac{Offset(85) - Offset(25)}{Offset(25) \times (85 - 25)}\right|\right]$$

Offset drift is expressed in ppm/°C.

Gain Error

The gain error in the ADCs represents the difference between the measured ADC output code (minus the offset) and the ideal output code when the internal voltage reference is used (see the Analog-to-Digital Conversion section). The difference is expressed as a percentage of the ideal code. It represents the overall gain error of one current or voltage channel.

Gain Drift over Temperature

This temperature coefficient includes the temperature variation of the ADC gain and of the internal voltage reference. It represents the overall temperature coefficient of one current or voltage channel. With the internal voltage reference in use, the ADC gain is measured at −40°C, +25°C, and +85°C. The temperature coefficient is computed as follows:

$$Drift = \max \left[\left| \frac{Gain(-40) - Gain(25)}{Gain(25) \times (-40 - 25)} \right|, \left| \frac{Gain(85) - Gain(25)}{Gain(25) \times (85 - 25)} \right| \right]$$

Gain drift is measured in ppm/°C.

Power Supply Rejection (PSR)

PSR quantifies the measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken when the voltage at the input pins is 0 V. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at 50 Hz or 100 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of the reading (power supply rejection ratio, PSRR). PSR = 20 log$_{10}$ (PSRR).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken when the voltage between the IP and IM pins is 6.25 mV rms, and the voltages between the V1P and VM pins and between the V2P and VM pins are 100 mV rms. A second reading is obtained with the same input signal levels when the power supplies are varied by ±10%. Any error introduced is expressed as a percentage of the reading (PSRR). Then PSR = 20 log$_{10}$ (PSRR).

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The waveform samples are acquired over a 1 sec window, and then a Hanning window is applied. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The waveform samples are acquired over a 1 sec window, and then a Hanning window is applied. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of all harmonics (excluding the noise components) to the rms value of the fundamental. The waveform samples are acquired over a 1 sec window, and then a Hanning window is applied. The value for THD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the rms value of the actual input signal to the rms value of the peak spurious component over the measurement bandwidth of the waveform samples. The waveform samples are acquired over a 1 sec window, and then a Hanning window is applied. The value of SFDR is expressed in decibels relative to full scale, dBFS.

THEORY OF OPERATION

ANALOG INPUTS

The ADE7913 has three analog inputs: one current channel and two voltage channels. The ADE7912 does not include the second voltage channel. The current channel has two fully differential voltage input pins, IP and IM, that accept a maximum differential signal of ±31.25 mV.

The maximum V_{IP} signal level is also ±31.25 mV. The maximum V_{IM} signal level allowed at the IM input is ±25 mV. Figure 23 shows a schematic of the input for the current channel and the relation to the maximum IM pin voltage.
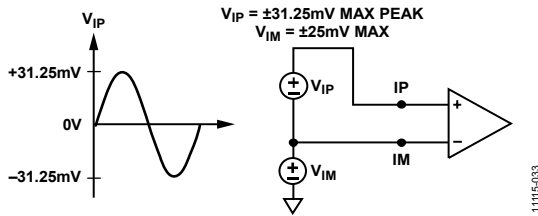
Figure 23. Maximum Input Level, Current Channel

Note that the current channel senses the voltage across a shunt. In this case, one pole of the shunt becomes the ground of the meter (see Figure 32) and, therefore, the current channel is used in a pseudo differential configuration, similar to the voltage channel configuration (see Figure 24).

The voltage channel has two pseudo differential, single-ended voltage input pins: V1P and V2P. These single-ended voltage inputs have a maximum input voltage of ±500 mV with respect to VM. The maximum signal allowed at the VM input is ±25 mV. Figure 24 shows a schematic of the voltage channel inputs and their relation to the maximum VM voltage.
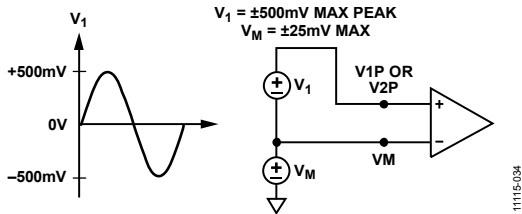
Figure 24. Maximum Input Level, Voltage Channels

ANALOG-TO-DIGITAL CONVERSION

The ADE7912/ADE7913 have three second-order Σ-Δ ADCs. For simplicity, the block diagram in Figure 25 shows a first-order Σ-Δ ADC. The converter is composed of the Σ-Δ modulator and the digital low-pass filter, separated by the digital isolation block.
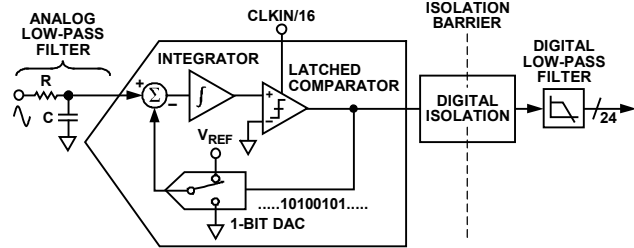
Figure 25. First-Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7912/ADE7913, the sampling clock is equal to CLKIN/4 (1.024 MHz when CLKIN = 4.096 MHz). The 1-bit DAC in the feedback loop is driven by the serial stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and, therefore, the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. A meaningful result is obtained only when a large number of samples is averaged. This averaging is completed in the second part of the ADC, the digital low-pass filter, after the data passes through the digital isolators. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first technique is oversampling. Oversampling means that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, when CLKIN = 4.096 MHz, the sampling rate in the ADE7912/ADE7913 is 1.024 MHz, and the bandwidth of interest is 40 Hz to 3.3 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the bandwidth of interest is lowered, as shown in Figure 26.

However, oversampling alone is not sufficient to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling factor of 4 is required to increase the SNR by a mere 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. Noise shaping is the second technique that achieves high resolution. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass type response for the quantization noise. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 26.
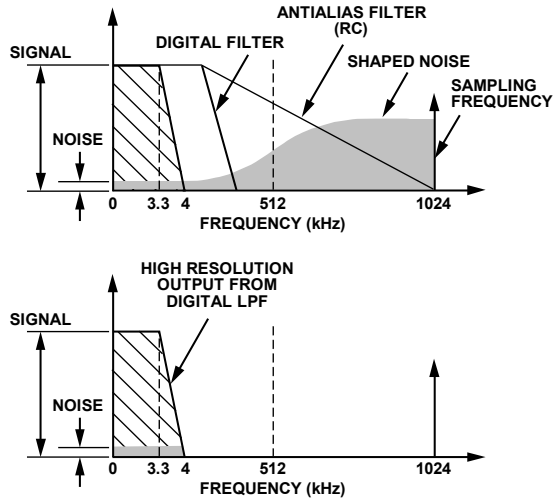
Figure 26. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

The bandwidth of interest is a function of the input clock frequency, the ADC output frequency (selectable by Bits[5:4] (ADC_FREQ) in the CONFIG register; see the ADC Output Values section for details), and Bit 7 (BW) of the CONFIG register. When CLKIN is 4.096 MHz and the ADC output frequency is 8 kHz, if BW is cleared to 0 (the default value) the ADC bandwidth is 3.3 kHz. If BW is set to 1, the ADC bandwidth is 2 kHz. Table 10 shows the ADC output frequencies and the ADC bandwidth function of the input clock (CLKIN) frequency. Three cases are shown: one for CLKIN = 4.096 MHz (the typical clock input frequency value), one for CLKIN = 4.21 MHz (the maximum clock input frequency), and one for CLKIN = 3.6 MHz (the minimum clock input frequency.)

Antialiasing Filter

Figure 25 also shows an analog low-pass filter (RC) on the input to the ADC. This filter is placed outside the ADE7912/ADE7913, and the role is to prevent aliasing. Aliasing is an artifact of all sampled systems, as shown in Figure 27. Aliasing refers to the frequency components in the input signal to the ADC that are higher than half the sampling rate of the ADC and appear in the sampled signal at a frequency below half the sampling rate. Frequency components above half the sampling frequency (also known as the Nyquist frequency, that is, 512 kHz) are imaged or folded back down below 512 kHz. This happens with all ADCs, regardless of the architecture. In Figure 27, only frequencies near the sampling frequency of 1.024 MHz move into the bandwidth of interest for metering, that is, 40 Hz to 3.3 kHz, or 40 Hz to 2 kHz. To attenuate the high frequency noise (near 1.024 MHz) and prevent the distortion of the bandwidth of interest, a low-pass filer (LPF) must be introduced. It is recommended that one RC filter with a corner frequency of 5 kHz be used for the attenuation to be sufficiently high at the sampling frequency of 1.024 MHz. The 20 dB per decade attenuation of this filter is usually sufficient to eliminate the effects of aliasing.
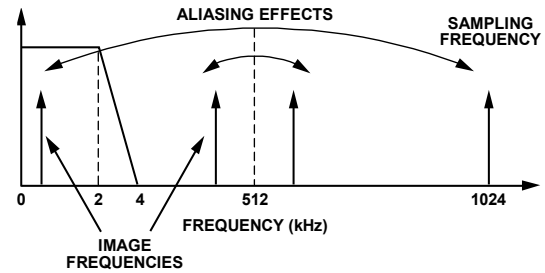

Figure 27. Aliasing Effects

Table 10. ADC Output Frequency and ADC Bandwidth as a Function of CLKIN Frequency

CLKIN (MHz)	Bits ADC_FREQ in CONFIG Register	ADC Output Frequency (Hz)	ADC Bandwidth When Bit BW in CONFIG Register Cleared to 0 (Hz)	ADC Bandwidth When Bit BW in CONFIG Register Set to 1 (Hz)
4.096	00	8000	3300	2000
	01	4000	1650	1000
	10	2000	825	500
	11	1000	412	250
4.21	00	8222	3391	2055
	01	4111	1695	1027
	10	2055	847	513
	11	1027	423	256
3.6	00	7031	2900	1757
	01	3515	1450	878
	10	1757	725	439
	11	878	362	219

ADC Transfer Function

All ADCs in the ADE7912/ADE7913 produce 24-bit signed output codes. With a full-scale input signal of 31.25 mV on the current channel and 0.5 V on the voltage channels, and with an internal reference of 1.2 V, the ADC output code is nominally 5,320,000 and usually varies for each AD E7912/ADE7913 around this value. The code from the ADC can vary between 0x800000 (−8,388,608) and 0x7FFFFF (+8,388,607); this is equivalent to an input signal level of ±49.27 mV on the current channel and ±0.788 V on the voltage channels. However, for specified performance, do not exceed the nominal range of ±31.25 mV for the current channel and ±500 mV for the voltage channels; ADC performance is guaranteed only for input signals within these limits. For input signals outside these limits, the digital low-pass filter of the ADCs (see Figure 25) overflows.

ADC Output Values

The ADC output values are stored in three 24-bit signed registers, IWV, V1WV, and V2WV, at a rate defined by Bits[5:4] (ADC_FREQ) in the CONFIG register. The output frequency is 8 kHz (CLKIN/512), 4 kHz (CLKIN/1024), 2 kHz (CLKIN/2048), or 1 kHz (CLKIN/4096) based on ADC_FREQ being equal to 00, 01, 10, or 11, respectively, when CLKIN is 4.096 MHz.

The microcontroller reads the ADC output registers one at a time or in burst mode. See the SPI Read Operation section and the SPI Read Operation in Burst Mode section for more information.

REFERENCE CIRCUIT

The nominal reference voltage at the REF pin is 1.2 V. This reference voltage is used for the ADCs in the ADE7912/ADE7913. Because the on-chip dc-to-dc converter cannot supply external loads, the REF pin cannot be overdriven by a standalone external voltage reference.

The voltage of the ADE7912/ADE7913 reference drifts slightly with temperature. Table 1 lists the gain drift over temperature specification of each ADC channel. This value includes the temperature variation of the ADC gain, together with the temperature variation of the internal voltage reference.

CRC OF ADC OUTPUT VALUES

Every output cycle, the ADE7912/ADE7913 compute the cyclic redundancy check (CRC) of the ADC output values stored in the IWV, V1WV, and V2WV registers. Bits[5:4] (ADC_FREQ) in the CONFIG register determine the ADC output frequency and, therefore, the update rate of the CRC.

The CRC algorithm is based on the CRC-16-CCITT algorithm. The registers are introduced into a linear feedback shift register (LFSR) based generator one byte at a time, least significant byte first, as shown in Figure 28. Each byte is then used with the most significant bit first. The 16-bit result is written in the ADC_CRC register.

When Bits[5:4] (ADC_FREQ) in the CONFIG register are set to 00, the ADC output frequency is 8 kHz and the ADC_CRC register contains the CRC of the IWV, V1WV, and V2WV registers generated during the same ADC output cycle. When ADC_FREQ bits are set to 01, 10 or 11, the ADC output frequency is 4 kHz, 2 kHz, and 1 kHz, respectively and the ADC_CRC register contains the CRC of the IWV, V1WV, and V2WV registers generated during the previous ADC output cycle.
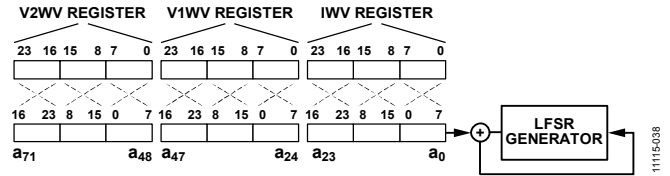

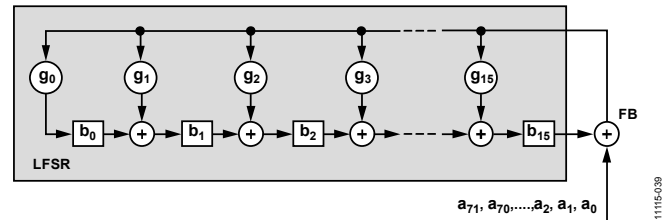*Figure 28. CRC Calculation of ADC Output Values*

Figure 29. LFSR Generator Used for ADC_CRC Calculation

Figure 29 shows how the LFSR works. The IWV, V1WV, and V2WV registers form the $[a_{71}, a_{70}, \ldots, a_0]$ bits used by the LFSR. Bit a_0 is Bit 7 of the first register to enter the LFSR; Bit a_{71} is Bit 16 of V2WV, the last register to enter the LFSR. The formulas that govern the LFSR are as follows:

$b_i(0) = 1$, where i = 0, 1, 2, …, 15, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{15} is the most significant bit.

g_i, where i = 0, 1, 2, …, 15 are the coefficients of the generating polynomial defined by the CRC-16-CCITT algorithm as follows:

$$G(x) = x^{16} + x^{12} + x^5 + 1 \tag{1}$$

$$g_0 = g_5 = g_{12} = 1 \tag{2}$$

All other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{15}(j-1) \tag{3}$$

$$b_0(j) = FB(j) \text{ AND } g_0 \tag{4}$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1), i = 1, 2, 3, \ldots, 15 \tag{5}$$

Equation 3, Equation 4, and Equation 5 must be repeated for j = 1, 2, …, 72. The value written into the ADC_CRC register contains Bit $b_i(72)$, i = 0, 1, …, 15.

The ADC_CRC register can be read by executing an SPI register read access or as part of the SPI burst mode read operation. See the SPI Read Operation section and the SPI Read Operation in Burst Mode section for more details.

TEMPERATURE SENSOR

The ADE7912/ADE7913 contain a temperature sensor that is multiplexed with the V2P input of the voltage channel. Bit 3 (TEMP_EN) of the CONFIG register selects what the third ADC of the ADE7913 measures. If the TEMP_EN bit is 0, the default value, the ADC measures the voltage between the V2P and VM pins. If the TEMP_EN bit is 1, the ADC measures the temperature sensor. In the case of the ADE7912, the ADC always measures the temperature sensor, and the state of the TEMP_EN bit has no significance. In both the ADE7912 and the ADE7913, the conversion result is stored in the V2WV register. The time it takes for the temperature sensor measurement to settle after the TEMP_EN bit is set to 1 is 5 ms.

In the microcontroller, the expression calculates the temperature in degrees Celsius is:

$$temperature =$$
$$gain \times V2WV + 8.72101 \times 10^{-5} \times TEMPOS \times 2^{11} - 306.47$$

where:
$temperature$ is the temperature value measured in degrees Celsius.
$gain$ is equal to 8.72101×10^{-5} when Bit 7 (BW) in the CONFIG register is 0 and 8.21015×10^{-5} when Bit 7 (BW) in the CONFIG register is 1. See Table 10 for details on Bit 7 (BW) significance in the context of ADC output frequency selection. The temperature measurement accuracy is ±5°C.

$TEMPOS$ is the 8-bit signed read-only register in which the temperature sensor offset is stored. The offset information is calculated during the manufacturing process, and it is stored with the opposite sign. For example, if the offset is 5, −5 is written into the ADE7912/ADE7913. One least significant bit (LSB) of the TEMPOS register is equivalent to 2^{11} LSBs of the V2WV register.

Instead of using the default temperature gain value, the gain can be calibrated as part of the overall meter calibration process. Measure the temperature, TEMP, of every ADE7912/ADE7913 using a thermocouple. Call it temperature and express it in degrees Celsius (see Equation 6). Read the V2WV register containing the temperature sensor reading of every ADE7912/ADE7913, and compute the gains as follows:

$$Temperature\ gain = gain = \frac{temperature + 306.47}{V2WV + k \times TEMPOS \times 2^{11}}\ (6)$$

where $k = 1$ when Bit 7 (BW) in CONFIG register is 0 and $k = 1.062223$ when Bit 7 (BW) in CONFIG register is 1.

PROTECTING THE INTEGRITY OF CONFIGURATION REGISTERS

The configuration registers of the ADE7912/ADE7913 are either user accessible registers (CONFIG, EMI_CTRL, SYNC_SNAP, COUNTER0, and COUNTER1) or internal registers. The internal registers are not user accessible, and they must remain at their default values. To protect the integrity of all configuration registers, a write protection mechanism is available.

By default, the protection is disabled and the user accessible configuration registers can be written without restriction. When the protection is enabled, no writes to any configuration register are allowed. The registers can always be read, without restriction, independent of the write protection state.

To enable the protection, write 0xCA to the 8-bit lock register (Address 0xA). To disable the protection, write 0x9C to the 8-bit lock register. It is recommended that the write protection be enabled after the CONFIG and EMI_CTRL registers are initialized. If any user accessible register must be changed, for example, during the synchronization process of multiple ADE7912/ADE7913 devices, disable the protection, change the value of the register, and then reenable the protection.

CRC OF CONFIGURATION REGISTERS

Every output cycle, the ADE7912/ADE7913 compute the CRC of the CONFIG, EMI_CTRL, and TEMPOS registers, as well as Bit 2 (IC_PROT) of the STATUS0 register, and Bit 7 of the STATUS1 register. The CRC algorithm is called CRC-16-CCITT. The 16-bit result is written in the CTRL_CRC register.

The input registers to the CRC circuit form a 64-bit array that is introduced bit by bit into an LFSR-based generator, similar to Figure 28 and Figure 29, with one byte at a time, least significant byte first. Each byte is then processed with the most significant bit first.

The formulas that govern the LFSR are as follows:

$b_i(0) = 1$, where $i = 0, 1, 2, …, 15$, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{15} is the most significant bit.

g_i, where $i = 0, 1, 2, …, 15$ are the coefficients of the generating polynomial defined by the CRC-16-CCITT algorithm in Equation 1 and Equation 2.

$$FB(j) = a_{j-1}\ \text{XOR}\ b_{15}(j-1)\ \ \ \ \ \ (7)$$
$$b_0(j) = FB(j)\ \text{AND}\ g_0\ \ \ \ \ \ (8)$$
$$b_i(j) = FB(j)\ \text{AND}\ g_i\ \text{XOR}\ b_{i-1}(j-1),\ i = 1, 2, 3, …, 15\ \ \ (9)$$

Equation 7, Equation 8, and Equation 9 must be repeated for $j = 1, 2, …, 64$. The value written into the CTRL_CRC register contains Bit $b_i(64)$, $i = 0, 1, …, 15$. Because each ADE7912/ADE7913 has a particular TEMPOS register value, each ADE7912/ADE7913 has a different CTRL_CRC register default value.

ADE7912/ADE7913 STATUS

The bits in the STATUS0 and STATUS1 registers of the ADE7912/ADE7913 characterize the state of the device.

If the value of the CTRL_CRC register changes, Bit 1 (CRC_STAT) is set to 1 in the STATUS0 register. This bit clears to 0 when the STATUS0 register is read.

After the configuration registers are protected by writing 0xCA into the lock register, Bit 2 (IC_PROT) in the STATUS0 register is set to 1. It clears to 0 when the STATUS0 register is read, and it is set back to 1 at the next ADC output cycle.

At power-up, or after a hardware or software reset, the ADE7912/ADE7913 signal the end of the reset period by clearing Bit 0 (RESET_ON) to 0 in the STATUS0 register.

If the ADC output values of IWV, V1WV, and V2WV are not read during an output cycle, Bit 3 (ADC_NA) in the STATUS1 register becomes 1. It clears to 0 when the STATUS1 register is read.

The STATUS0 and STATUS1 registers can be read by executing an SPI register read. STATUS0 can also be read as part of the SPI burst mode read operation. See the SPI Read Operation and the SPI Read Operation in Burst Mode sections for more information.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period of time. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADE7912/ADE7913 devices. Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 8 summarize the maximum working voltage for 50 years of service life for a bipolar ac operating condition. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADE7912/ADE7913 devices depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac or dc. Figure 30 and Figure 31 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the bipolar ac condition determines the maximum working voltage recommended by Analog Devices. In the case of dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life.

The working voltages listed in Table 8 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to the dc voltage case. Treat any cross-insulation voltage waveform that does not conform to Figure 31 as a bipolar ac waveform, and limit the peak voltage to the 50-year lifetime voltage value listed in Table 8.
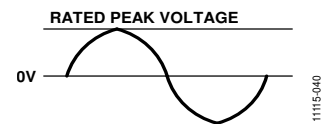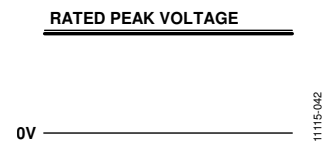

Figure 30. Bipolar AC Waveform

Figure 31. DC Waveform

APPLICATIONS INFORMATION

ADE7912/ADE7913 IN POLYPHASE ENERGY METERS

The ADE7912/ADE7913 are designed for use in 3-phase energy metering systems in which two, three, or four ADE7912/ADE7913 devices are managed by a master device containing an SPI interface, usually a microcontroller.
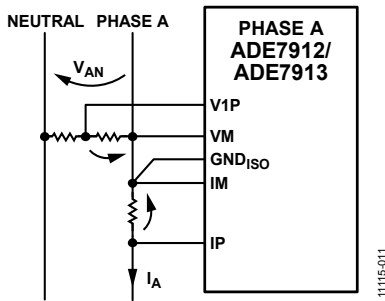

Figure 32. Phase A ADE7912/ADE7913 Current and Voltage Sensing

Figure 32 shows the Phase A of a 3-phase energy meter. The Phase A current, I_A, is sensed with a shunt. A pole of the shunt is connected to the IM pin of the ADE7912/ADE7913 and becomes the ground, GND_{ISO} (Pin 10), of the isolated side of the ADE7912/ADE7913. The Phase A to neutral voltage, V_{AN}, is sensed with a resistor divider, and the VM pin is also connected to the IM and GND_{ISO} pins. Note that the voltages measured by the ADCs of the ADE7912/ADE7913 are opposite to V_{AN} and I_A, a classic approach in single-phase metering. The other ADE7912/ADE7913 devices that monitor Phase B and Phase C are connected in a similar way.

The V2P voltage channel is intended to measure an auxiliary voltage, and it is available only on the ADE7913. If V2P is not used, as is the case of the ADE7912, connect V2P to VM.
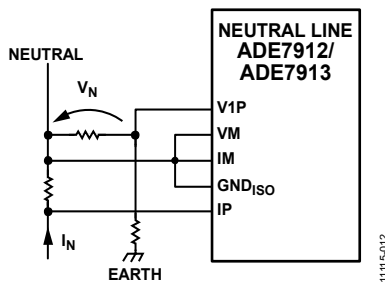

Figure 33. Neutral Line and Neutral to Earth Voltage Monitoring with the ADE7912/ADE7913

Figure 33 shows how the ADE7912/ADE7913 inputs are connected when the neutral line of a 3-phase system is monitored. The neutral current is sensed using a shunt and the voltage across the shunt is measured at the fully differential inputs, IP and IM. The earth to neutral voltage is sensed with a voltage divider at the single-ended inputs, V1P and VM.

Figure 34 shows a block diagram of a 3-phase energy meter that uses three ADE7912/ADE7913 devices and a microcontroller. The neutral current is not monitored in this example. One 4.096 MHz crystal provides the clock to the ADE7912/ADE7913 that senses the Phase A current and voltage. The ADE7912/ADE7913 devices that sense the Phase B and Phase C currents and voltages are clocked by a signal generated at the CLKOUT/DREADY pin of the ADE7912/ADE7913 that is placed to sense the Phase A current and voltage. As an alternative configuration, the microcontroller can generate a 4.096 MHz clock to all ADE7912/ADE7913 devices at the XTAL1 pin (see Figure 35). Note that the XTAL1 pin can receive a clock with a frequency within the 3.6 MHz to 4.21 MHz range, as specified in Table 1.

The microcontroller uses the SPI port to communicate with the ADE7912/ADE7913 devices. Three of the I/O pins, CS_A, CS_B, and CS_C, generate the SPI $\overline{CS}$ signals. The SCLK, MOSI, and MISO pins of the microcontroller are directly connected to the corresponding SCLK, MOSI, and MISO pins of each ADE7912/ADE7913 device (see Figure 38). To simplify Figure 34 to Figure 37, these connections are not shown.
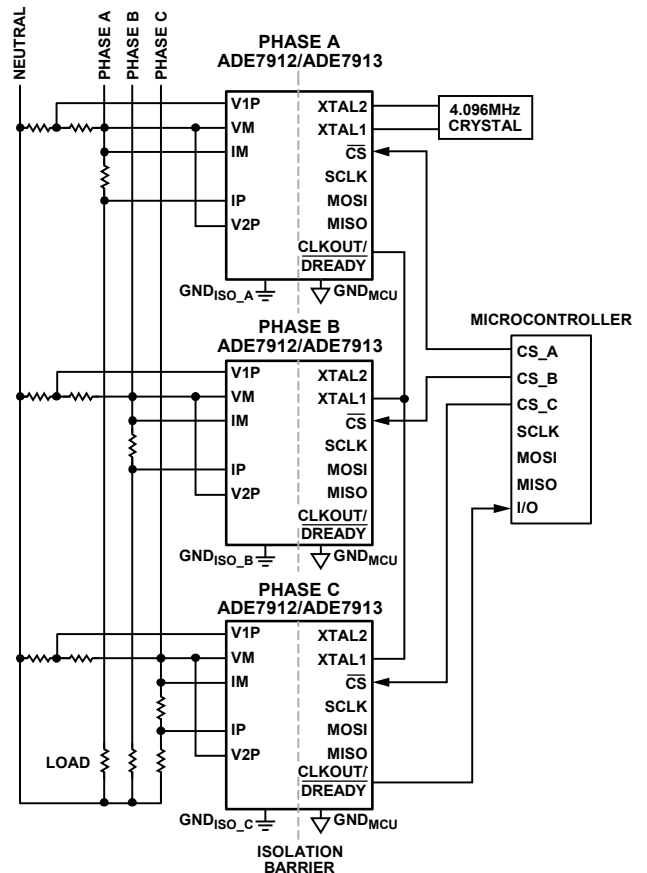

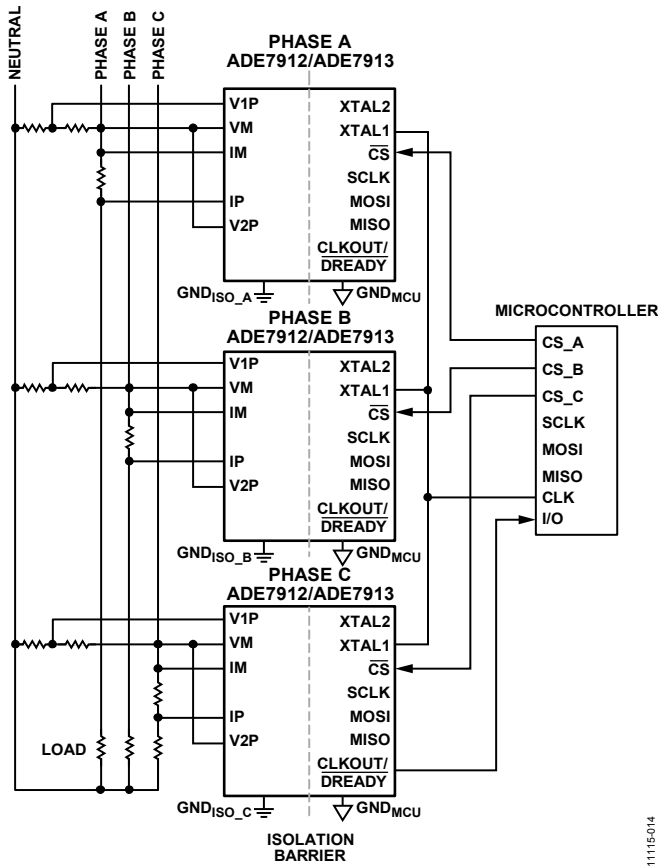Figure 34. 3-Phase Energy Meter Using Three ADE7912/ADE7913 Devices

Figure 35. Microcontroller Generating Clock to Three ADE7912/ADE7913 Devices

In Figure 35, the CLKOUT/DREADY pin of the ADE7912/ ADE7913 that senses the Phase C current and voltage is connected to the I/O pin of the microcontroller. CLKOUT/ DREADY provides an active low pulse for 64 CLKIN cycles (15.625 μs at CLKIN = 4.096 MHz) when the ADC conversion data is available. It signals when the ADC outputs of all ADE7912/ ADE7913 devices become available and when the microcontroller starts to read them. See the Synchronizing Multiple ADE7912/ADE7913 Devices section for more information about synchronizing multiple ADE7912/ADE7913 devices.

At power-up, or after a hardware or software reset, follow the procedure described in the Power-Up Procedure for Systems with Multiple Devices That Use a Single Crystal section or the Power-Up Procedure for Systems with Multiple Devices That Use Clock Generated from Microcontroller section to ensure that the ADE7912/ADE7913 devices function appropriately.

The configuration of an energy meter using four ADE7912/ ADE7913 devices is similar, shown in Figure 36. The micro-controller uses an additional I/O pin, CS_N, to generate the SPI $\overline{CS}$ signal to the ADE7912/ADE7913 device that is monitoring the neutral current.
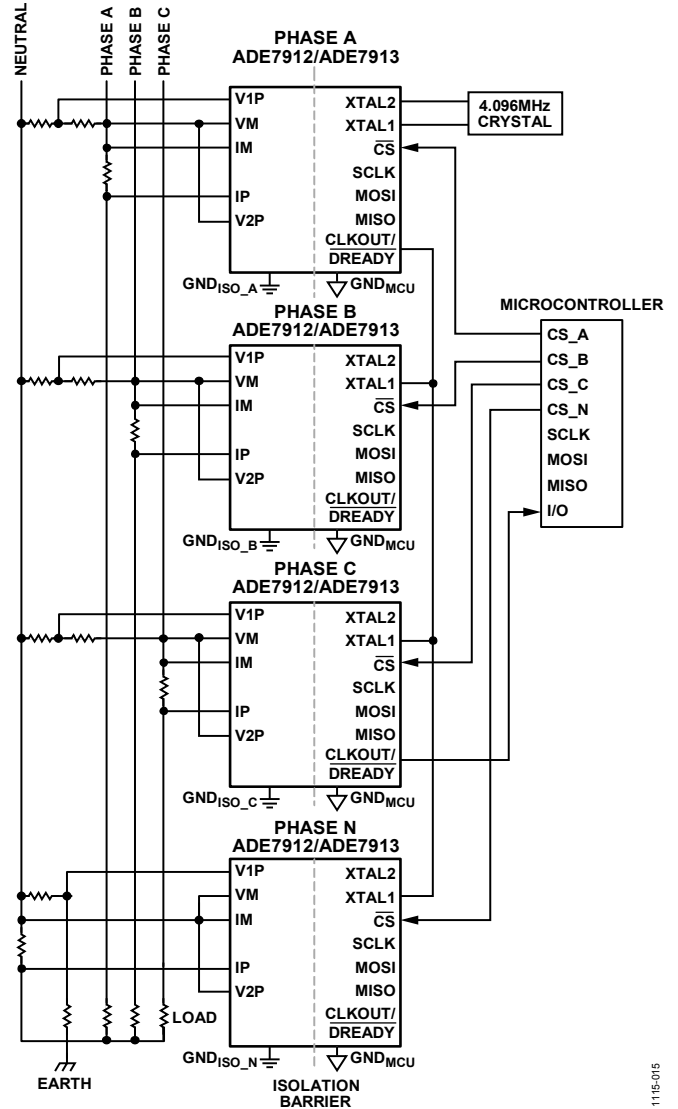

Figure 36. 3-Phase Energy Meter Using Four ADE7912/ADE7913 Devices

Figure 37 shows an energy meter using two ADE7912/ADE7913 devices in a delta configuration. The meter ground is on the Phase B line. One ADE7912/ADE7913 device measures Phase A current and Phase A to Phase B voltage. A second ADE7912/ADE7913 device measures Phase C current and Phase C to Phase B voltage. The system microcontroller computes the Phase B current and the Phase A to Phase C voltage.
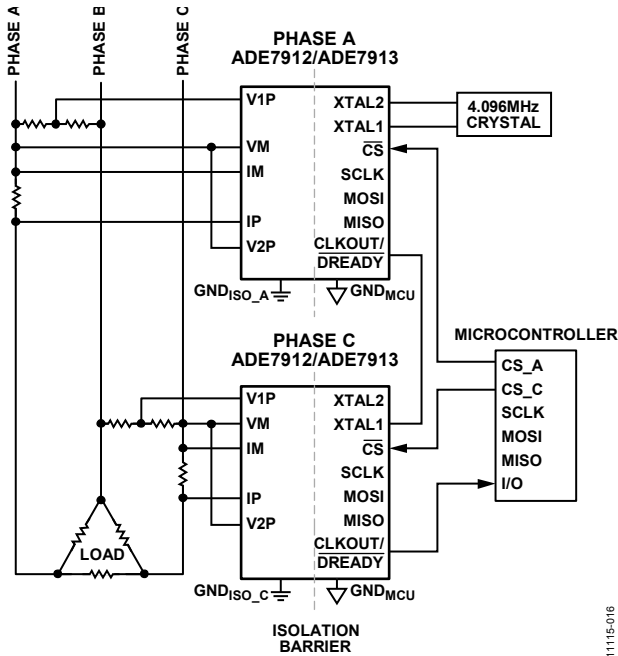

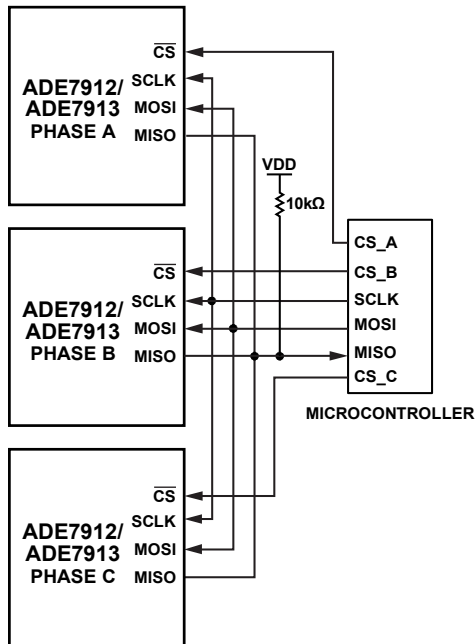Figure 37. 3-Phase Meter Using Two ADE7912/ADE7913 Devices in Delta Configuration

Figure 38. SPI Connections Between Three ADE7912/ADE7913 Devices and a Microcontroller

ADE7912/ADE7913 CLOCK

Provide a digital clock signal at the XTAL1 pin to clock the ADE7912/ADE7913. The frequency at which the ADE7912/ADE7913 are clocked at XTAL1 is called CLKIN. The ADE7912/ADE7913 are specified for CLKIN = 4.096 MHz, but frequencies between 3.6 MHz and 4.21 MHz are acceptable.

Alternatively, a 4.096 MHz crystal with a typical drive level of 0.5 mW and an equivalent series resistance (ESR) of 20 Ω can be connected across the XTAL1 and XTAL2 pins to provide a clock source for the ADE7912/ADE7913 (see Figure 39).

The total capacitance (TC) at the XTAL1 and XTAL2 pins is

$$TC = C1 + CP1 = C2 + CP2$$

where:
$C1$ and $C2$ are the ceramic capacitors between XTAL1 and GND and between XTAL2 and GND, respectively.
$CP1$ and $CP2$ are the parasitic capacitors of the wires connecting the crystal to the ADE7912/ADE7913.

The load capacitance (LC) of the crystal is equal to half the TC because it is the capacitance of the series circuit composed by C1 + CP1 and C2 + CP2.

$$LC = \frac{C1 + CP1}{2} = \frac{C2 + CP2}{2} = \frac{TC}{2}$$

Therefore, the value of the C1 and C2 capacitors as a function of the load capacitance of the crystal is

$$C1 = C2 = 2 \times LC - CP1 = 2 \times LC - CP2$$

In the case of the ADE7912/ADE7913, the typical TC of the XTAL1 and XTAL2 pins is 40 pF (see Table 1). Select a crystal with a load capacitance of

$$LC = \frac{TC}{2} = 20 \text{ pF}$$

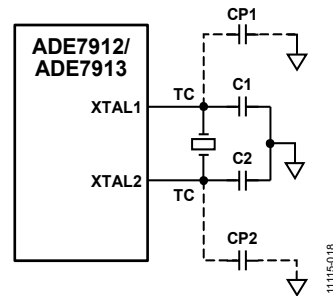Assuming the parasitic capacitances, CP1 and CP2, are equal to 20 pF, select Capacitors C1 and C2 equal to 20 pF.

Figure 39. Crystal Circuitry