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Single Phase, Multifunction Metering IC with Neutral Current Measurement

Data Sheet

ADE7953

FEATURES

Highly accurate; supports EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-21, IEC 62053-22, and IEC 62053-23 standards
Measures active, reactive, and apparent energy; sampled waveform; current and voltage rms
Provides a second current input for neutral current measurement
Less than 0.1% error in active and reactive energy measurements over a dynamic range of 3000:1
Less than 0.2% error in instantaneous IRMS measurement over a dynamic range of 1000:1
Provides apparent energy measurement and instantaneous power readings
1.23 kHz bandwidth operation
Flexible PGA gain stage (up to ×22)
Includes internal integrators for use with Rogowski coil sensors
SPI, I²C, or UART communication

GENERAL DESCRIPTION

The ADE7953 is a high accuracy electrical energy measurement IC intended for single phase applications. It measures line voltage and current and calculates active, reactive, and apparent energy, as well as instantaneous rms voltage and current.

The device incorporates three Σ-Δ ADCs with a high accuracy energy measurement core. The second input channel simultaneously measures neutral current and enables tamper detection and neutral current billing. The additional channel incorporates a complete signal path that allows a full range of measurements. Each input channel supports independent and flexible gain stages, making the device suitable for use with a variety of current sensors such as current transformers (CTs) and low value shunt resistors. Two on-chip integrators facilitate the use of Rogowski coil sensors.

The ADE7953 provides access to on-chip meter registers via a variety of communication interfaces including SPI, I²C, and UART. Two configurable low jitter pulse output pins provide outputs that are proportional to active, reactive, or apparent energy, as well as current and voltage rms. A full range of power quality information such as overcurrent, overvoltage, peak, and sag detection are accessible via the external $\overline{\text{IRQ}}$ pin. Independent active, reactive, and apparent no-load detections are included to prevent "meter creep." Dedicated reverse power ($\overline{\text{REVP}}$), zero-crossing voltage (ZX), and zero-crossing current (ZX_I) pins are also provided. The ADE7953 energy metering IC operates from a 3.3 V supply voltage and is available in a 28-lead LFCSP package.

FUNCTIONAL BLOCK DIAGRAM

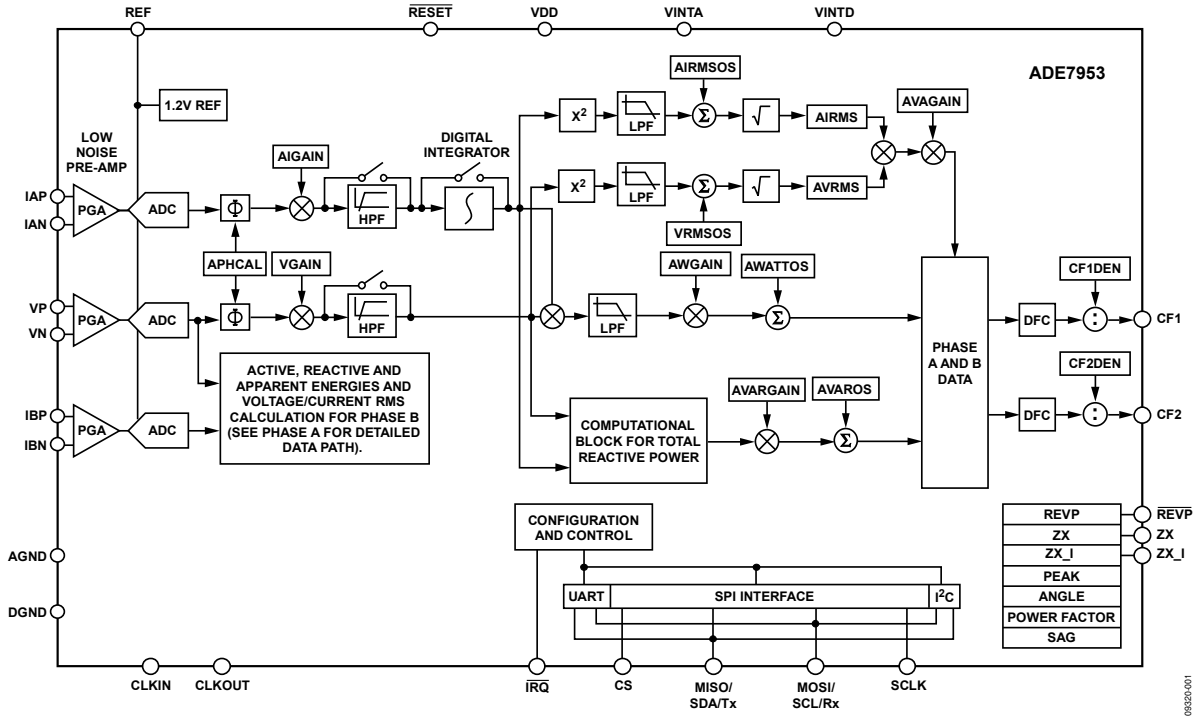

Figure 1.

Rev. C Document Feedback

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ADE7953* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADE7953 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1118: Calibrating a Single-Phase Energy Meter Based on the ADE7953
- AN-1367: I2C Interface Between the ADE7953 and the ADuCM360
- AN-639: Frequently Asked Questions (FAQs) Analog Devices Energy (ADE) Products

Data Sheet

- ADE7953: Single Phase, Multifunction Metering IC with Neutral Current Measurement Data Sheet

Product Highlight

- ADE7953: Single-Phase Multifunction Energy Metering IC with Neutral Current Measurement Overview

User Guides

- UG-194: Evaluation Board for the ADE7953 Single Phase Energy Metering IC

REFERENCE MATERIALS

Informational

- Wireless Sensor Network (WSN) Demo System

DESIGN RESOURCES

- ADE7953 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADE7953 EngineerZone Discussions.

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Changed t_{DAV} from 80 ns (Min) to 80 ns (Max) 6
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2/2011—Revision 0: Initial Version

SPECIFICATIONS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 3.58 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, Register Address 0x120 set to 0x30, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PHASE ERROR BETWEEN CHANNELS					Line frequency = 45 Hz to 65 Hz, HPF on
Power Factor = 0.8 Capacitive			±0.05	Degrees	Phase lead 37°
Power Factor = 0.5 Inductive			±0.05	Degrees	Phase lag 60°
ACTIVE ENERGY MEASUREMENT					
Active Energy Measurement Error (Current Channel A)		0.1		%	Over a dynamic range of 3000:1, PGA = 1, PGA = 22, integrator off
Active Energy Measurement Error (Current Channel B)		0.1		%	Over a dynamic range of 1000:1, PGA = 1, PGA = 16, integrator off
AC Power Supply Rejection					VDD = 3.3 V ± 120 mV rms, 100 Hz
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Output Frequency Variation		0.01		%	
Active Energy Measurement Bandwidth		1.23		kHz	−3 db
REACTIVE ENERGY MEASUREMENT					
Reactive Energy Measurement Error (Current Channel A)		0.1		%	Over a dynamic range of 3000:1, PGA = 1, PGA = 22, integrator off
Reactive Energy Measurement Error (Current Channel B)		0.1		%	Over a dynamic range of 1000:1, PGA = 1, PGA = 16, integrator off
AC Power Supply Rejection					VDD = 3.3 V ± 120 mV rms, 100 Hz
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Output Frequency Variation		0.01		%	
Reactive Energy Measurement Bandwidth		1.23		kHz	−3 db
RMS MEASUREMENT					
IRMS and VRMS Measurement Bandwidth		1.23		kHz	
IRMS (Current Channel A) Measurement Error		0.2		%	Over a dynamic range of 1000:1, PGA = 1, PGA = 22, integrator off
IRMS (Current Channel B) and VRMS Measurement Error		0.2		%	Over a dynamic range of 500:1, PGA = 1, PGA = 16, integrator off
ANALOG INPUTS					
Maximum Signal Levels			±500	mV peak	Differential inputs: IAP to IAN, IBP to IBN
			±500	mV peak	Single-ended input: VP to VN, IBP to IBN
			±250	mV peak	Single-ended input: IAP to IAN
Input Impedance (DC)					
IAP Pin	50			MΩ	
IAN Pin	50			MΩ	
IBP, IBN, VP, VN Pins	540			kΩ	
ADC Offset Error					Uncalibrated error (see the Terminology section)
Current Channel B, Voltage Channel		0	±10	mV	
Current Channel A			−12	mV	PGA = 1
			−1	mV	PGA = 16, PGA = 22
Gain Error					External 1.2 V reference
Current Channel A		±3		%	
Current Channel B		±3		%	
Voltage Channel		±3		%	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG PERFORMANCE					
Signal-to-Noise Ratio					
Current Channel A		74		dB	
Current Channel B		72		dB	
Voltage Channel		70			
Signal-to-Noise-and-Distortion Ratio					
Current Channel A, Current Channel B		68		dB	
Voltage Channel		65		dB	
Bandwidth (−3 dB)		1.23		kHz	
CF1 AND CF2 PULSE OUTPUTS					
Maximum Output Frequency		206.9		kHz	
Duty Cycle		50		%	CF1 or CF2 frequency > 6.25 Hz
Active Low Pulse Width		80		ms	CF1 or CF2 frequency < 6.25 Hz
Jitter		0.04		%	CF1 or CF2 frequency = 1 Hz
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 500 µA at 25°C
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 8 mA at 25°C
REFERENCE					Nominal 1.2 V at REF pin
REF Input Voltage Range	1.19	1.2	1.21	V	T_{MIN} to T_{Max}
Input Capacitance			10	pF	
Reference Error		±0.9		mV	T_A = 25°C
Output Impedance	1.2			kΩ	
Temperature Coefficient		10	50	ppm/°C	
CLKIN/CLKOUT PINS					All specifications CLKIN = 3.58 MHz
Input Clock Frequency	3.54	3.58	3.62	MHz	
Crystal Equivalent Series Resistance	30		200	Ω	
LOGIC INPUTS—$\overline{\text{RESET}}$, CLKIN, CS, SCLK, MOSI/SCL/Rx, MISO/SDA/Tx					
Input High Voltage, V_{INH}	2.4			V	VDD = 3.3 V ± 10%
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V ± 10%
Input Current, I_{IN}					V_{IN} = 0 V
MOSI/SCL/Rx, MISO/SDA/Tx, $\overline{\text{RESET}}$			−10	µA	
CS, SCLK			1	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS—$\overline{\text{IRQ}}$, $\overline{\text{REVP}}$, ZX, ZX_I, CLKOUT, MOSI/SCL/Rx, MISO/SDA/Tx					VDD = 3.3 V ± 10%
Output High Voltage, V_{OH}	3.0			V	I_{SOURCE} = 800 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
POWER SUPPLY					For specified performance
VDD	3.0			V	3.3 V − 10%
			3.6	V	3.3 V + 10%
I_{DD}		7	9	mA	

TIMING CHARACTERISTICS

SPI Interface Timing

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 3.58 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	Description	Min[1]	Max[1]	Unit
t_{CS}	CS to SCLK edge	50		ns
t_{SCLK}	SCLK period	200		ns
t_{SL}	SCLK low pulse width	80		ns
t_{SH}	SCLK high pulse width	80		ns
t_{DAV}	Data output valid after SCLK edge		80	ns
t_{DSU}	Data input setup time before SCLK edge	70		ns
t_{DHD}	Data input hold time after SCLK edge	5		ns
t_{DF}	Data output fall time		20	ns
t_{DR}	Data output rise time		20	ns
t_{SR}	SCLK rise time		20	ns
t_{SF}	SCLK fall time		20	ns
t_{DIS}	MISO disabled after CS rising edge	5	40	ns
t_{SFS}	CS high after SCLK edge	0		ns
t_{SFS_LK}	CS high after SCLK edge (when writing to COMM_LOCK bit)	1200		ns

[1] Min and max values are typical minimum and maximum values.

SPI Interface Timing Diagram

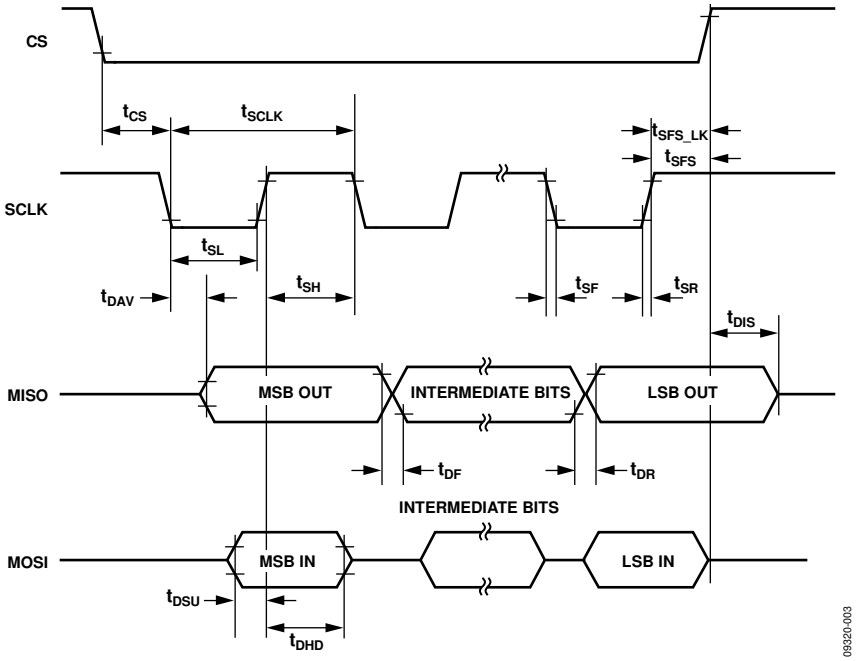

Figure 2. SPI Interface Timing

I²C Interface Timing

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 3.58 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, unless otherwise noted.

Table 3.

		Standard Mode		Fast Mode		
Parameter	**Description**	**Min[1]**	**Max[1]**	**Min[1]**	**Max[1]**	**Unit**
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time for a start or repeated start condition	4.0		0.6		µs
t_{LOW}	Low period of SCL clock	4.7		1.3		µs
t_{HIGH}	High period of SCL clock	4.0		0.6		µs
$t_{SU;STA}$	Setup time for a repeated start condition	4.7		0.6		µs
$t_{HD;DAT}$	Data hold time	0.1	3.45	0.1	0.9	µs
$t_{SU;DAT}$	Data setup time	250		100		ns
t_R	Rise time of SDA and SCL signals		1000	20	300	ns
t_F	Fall time of SDA and SCL signals		300	20	300	ns
$t_{SU;STO}$	Setup time for stop condition	4.0		0.6		µs
t_{BUF}	Bus-free time between a stop and start condition	4.7		1.3		µs
t_{SP}	Pulse width of suppressed spikes	N/A			50	ns

[1] Min and max values are typical minimum and maximum values.

I²C Interface Timing Diagram

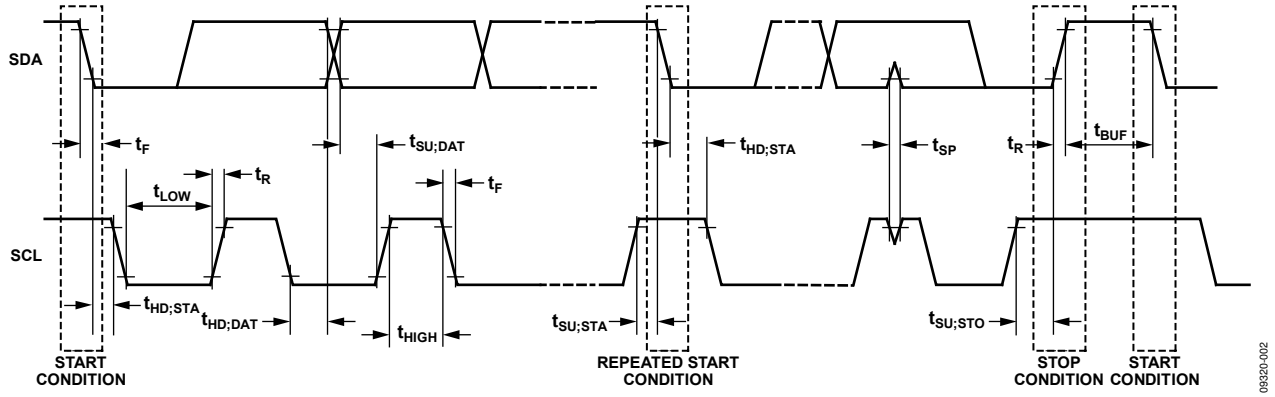

Figure 3. I²C Interface Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
VDD to AGND	−0.3 V to +3.7 V
VDD to DGND	−0.3 V to +3.7 V
Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, VP, VN	−2 V to +2 V
Reference Input Voltage to AGND	−0.3 V to VDD + 0.3 V
Digital Input Voltage to DGND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Note that regarding the temperature profile used in soldering RoHS-compliant parts, Analog Devices, Inc., advises that reflow profiles should conform to J-STD 20 from JEDEC. Refer to the JEDEC website for the latest revision.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

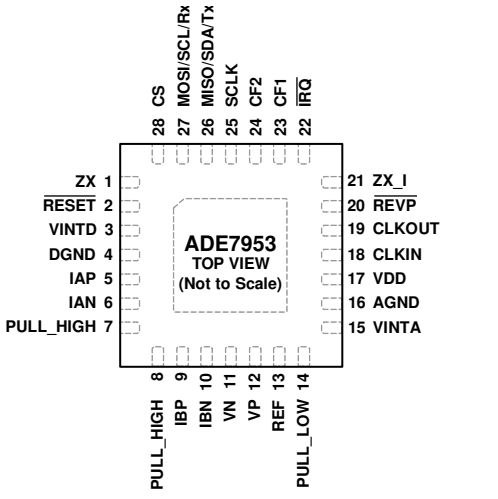

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	ZX	Voltage Channel Zero-Crossing Output Pin. See the Voltage Channel Zero Crossing section. This pin can be configured to output a range of alternative power quality signals (see the Alternative Output Functions section).
2	$\overline{\text{RESET}}$	Active Low Reset Input. To initiate a hardware reset, this pin must be brought low for at minimum of 10 µs.
3	VINTD	This pin provides access to the 2.5 V digital LDO. This pin should be decoupled with a 4.7 µF capacitor in parallel with a 100 nF ceramic capacitor.
4	DGND	Ground Reference for the Digital Circuitry.
5, 6	IAP, IAN	Analog Input for Current Channel A (Phase Current Channel). This differential voltage input has a maximum input range of ±500 mV. The maximum pin voltage for single-ended use is ±250 mV. The PGA associated with this input has a maximum gain stage of 22 (see the Analog Inputs section).
7, 8	PULL_HIGH	These pins should be connected to VDD for proper operation.
9, 10	IBP, IBN	Analog Input for Current Channel B (Neutral Current Channel). This differential voltage input has a maximum input range of ±500 mV. The PGA associated with this input has a maximum gain of 16 (see the Analog Inputs section).
11, 12	VN, VP	Analog Input for Voltage Channel. This differential voltage input has a maximum input range of ±500 mV. The PGA associated with this input has a maximum gain of 16 (see the Analog Inputs section).
13	REF	This pin provides access to the on-chip voltage reference. The internal reference has a nominal voltage of 1.2 V. This pin should be decoupled with a 4.7 µF capacitor in parallel with a 100 nF ceramic capacitor. Alternatively, an external reference voltage of 1.2 V can be applied to this pin (see the Reference Circuit section).
14	PULL_LOW	This pin should be connected to AGND for proper operation.
15	VINTA	This pin provides access to the 2.5 V analog LDO. This pin should be decoupled with a 4.7 µF capacitor in parallel with a 100 nF ceramic capacitor.
16	AGND	Ground Reference for the Analog Circuitry.
17	VDD	Power Supply (3.3 V) for the ADE7953. For specified operation, the input to this pin should be within 3.3 V ± 10%. This pin should be decoupled with a 10 µF capacitor in parallel with a 100 nF ceramic capacitor.
18	CLKIN	Master Clock Input for the ADE7953. An external clock can be provided at this input. Alternatively, a parallel resonant AT crystal can be connected across the CLKIN and CLKOUT pins to provide a clock source for the ADE7953. The clock frequency for specified operation is 3.58 MHz. Ceramic load capacitors of a few tens of picofarads should be used with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for the load capacitance requirements.
19	CLKOUT	A crystal can be connected across this pin and CLKIN to provide a clock source for the ADE7953.

Pin No.	Mnemonic	Description
20	$\overline{\text{REVP}}$	Reverse Power Output Indicator. See the Reverse Power section. This pin can be configured to output a range of alternative power quality signals (see the Alternative Output Functions section).
21	ZX_I	Current Channel Zero-Crossing Output Pin. See the Current Channel Zero Crossing section. This pin can be configured to output a range of alternative power quality signals (see the Alternative Output Functions section).
22	$\overline{\text{IRQ}}$	Interrupt Output. See the ADE7953 Interrupts section.
23	CF1	Calibration Frequency Output 1.
24	CF2	Calibration Frequency Output 2.
25	SCLK	Serial Clock Input for the Serial Peripheral Interface. All serial communications are synchronized to the clock (see the SPI Interface section). If using the I^2C interface, this pin must be pulled high. If using the UART interface, this pin must be pulled to ground.
26	MISO/SDA/Tx	Data Output for SPI Interface/Bidirectional Data Line for I^2C Interface/Transmit Line for UART Interface.
27	MOSI/SCL/Rx	Data Input for SPI Interface/Serial Clock Input for I^2C Interface/Receive Line for UART Interface.
28	CS	Chip Select for SPI Interface. This pin must be pulled high if using the I^2C or UART interface.
	EPAD	Exposed Pad. Create a similar pad on the PCB under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package. Connect the pad to AGND and DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

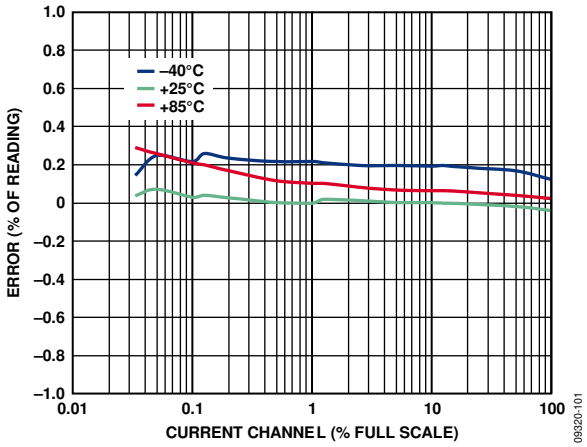

Figure 5. Current Channel A Active Energy Error as a Percentage of Reading (Gain = 1, Power Factor = 1) over Temperature with Internal Reference, Integrator Off

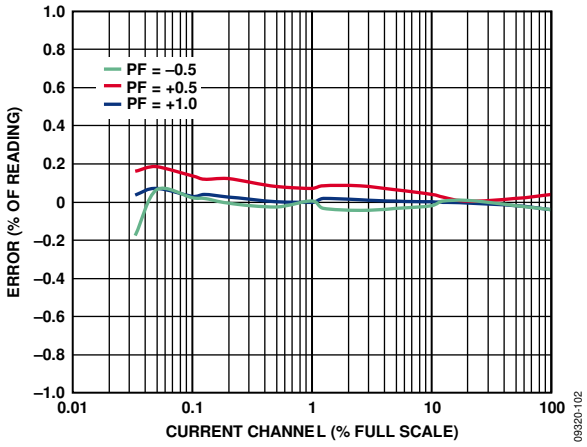

Figure 6. Current Channel A Active Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Power Factor with Internal Reference, Integrator Off

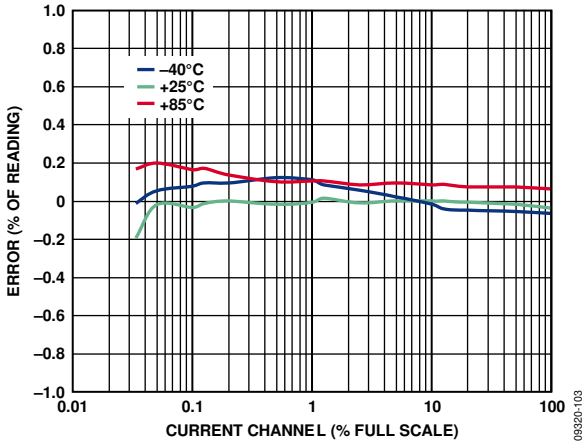

Figure 7. Current Channel A Active Energy Error as a Percentage of Reading (Gain = 22, Power Factor = 1) over Temperature with Internal Reference, Integrator Off

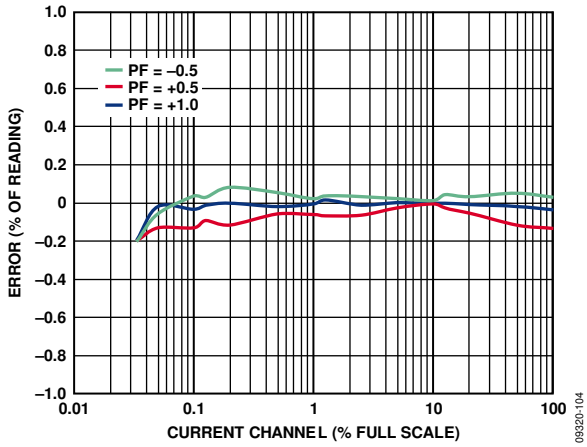

Figure 8. Current Channel A Active Energy Error as a Percentage of Reading (Gain = 22, Temperature = 25°C) over Power Factor with Internal Reference, Integrator Off

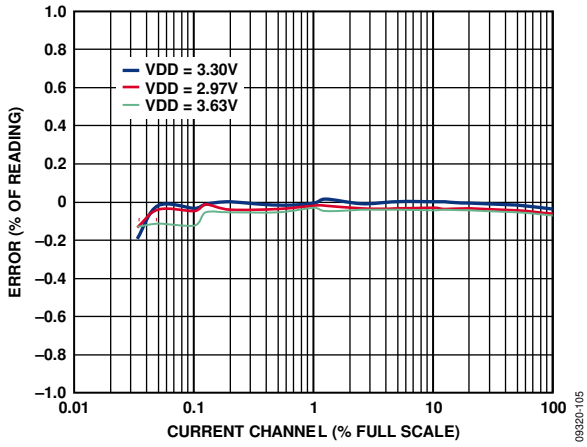

Figure 9. Current Channel A Active Energy Error as a Percentage of Reading (Gain = 22, Temperature = 25°C, Power Factor = 1) over Supply Voltage with Internal Reference, Integrator Off

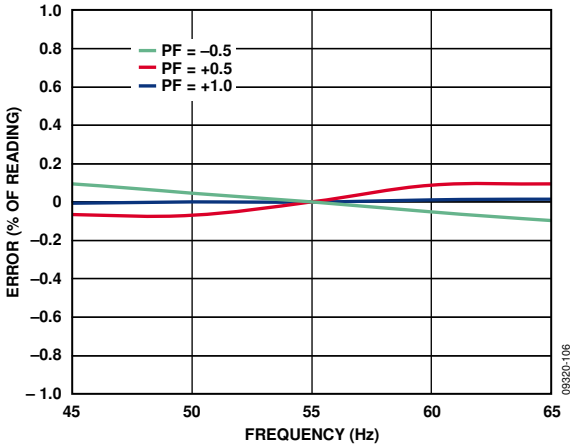

Figure 10. Current Channel A Active Energy Error as a Percentage of Reading (Gain = 22, Temperature = 25°C) over Frequency and Power Factor with Internal Reference, Integrator Off

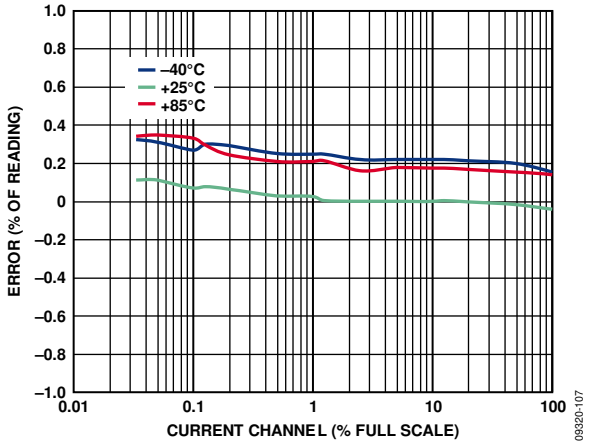

Figure 11. Current Channel A Reactive Energy Error as a Percentage of Reading (Gain = 1, Power Factor = 0) over Temperature with Internal Reference, Integrator Off

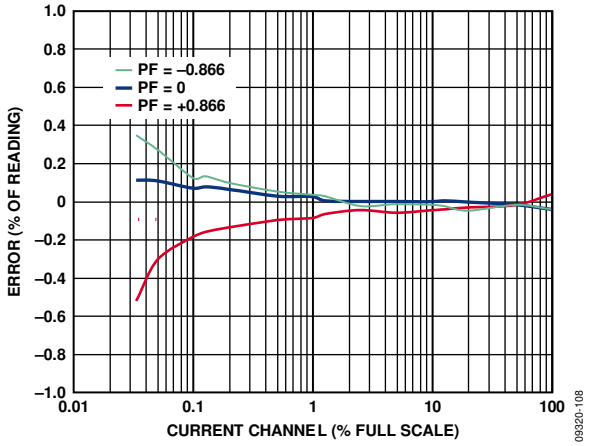

Figure 12. Current Channel A Reactive Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Power Factor with Internal Reference, Integrator Off

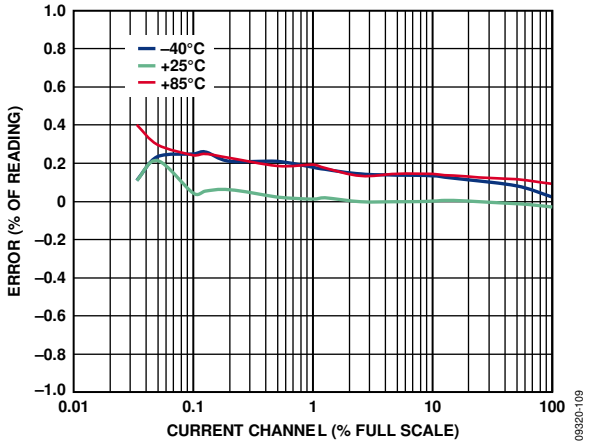

Figure 13. Current Channel A Reactive Energy Error as a Percentage of Reading (Gain = 22, Power Factor = 0) over Temperature with Internal Reference, Integrator Off

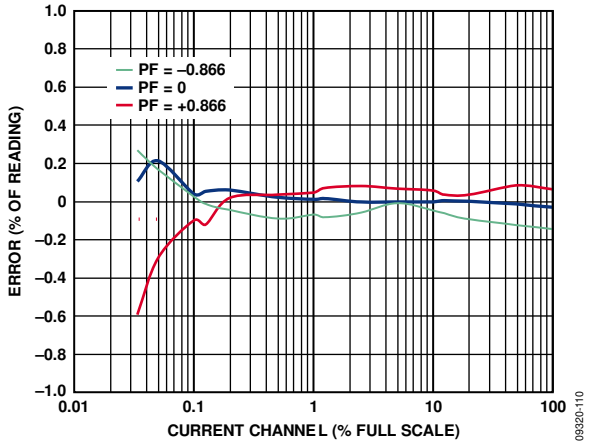

Figure 14. Current Channel A Reactive Energy Error as a Percentage of Reading (Gain = 22, Temperature = 25°C) over Power Factor with Internal Reference, Integrator Off

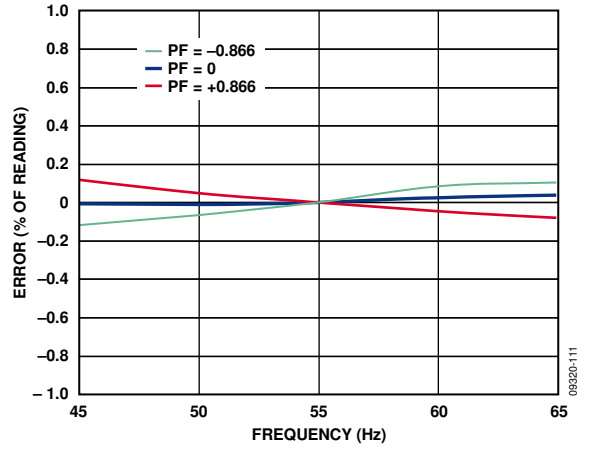

Figure 15. Current Channel A Reactive Energy Error as a Percentage of Reading (Gain = 22, Temperature = 25°C) over Frequency and Power Factor with Internal Reference, Integrator Off

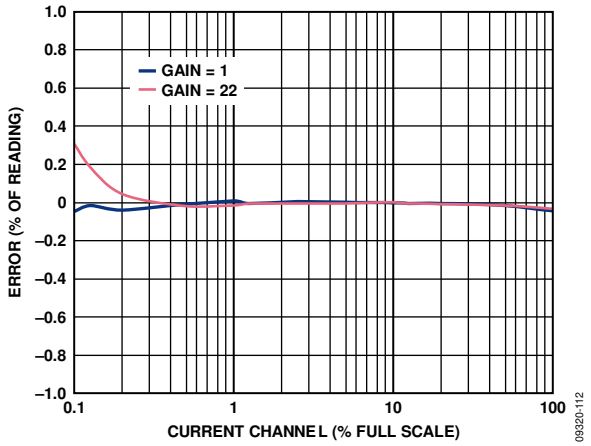

Figure 16. Current Channel A IRMS Error as a Percentage of Reading (Temperature = 25°C, Power Factor = 1) over Gain with Internal Reference, Integrator Off

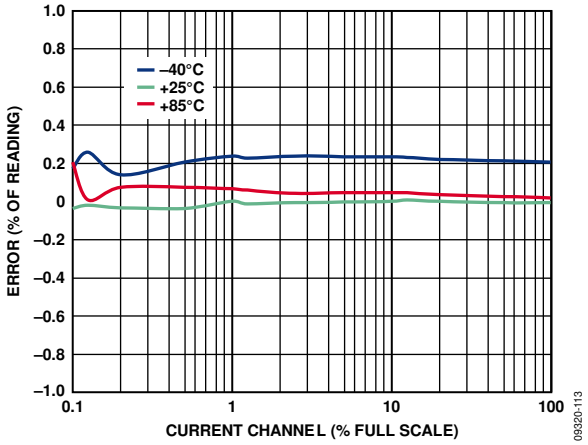

Figure 17. Current Channel B Active Energy Error as a Percentage of Reading (Gain = 1, Power Factor = 1) over Temperature with Internal Reference, Integrator Off

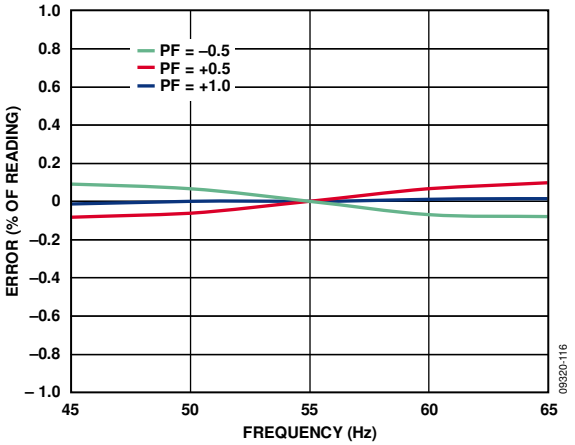

Figure 20. Current Channel B Active Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Frequency and Power Factor with Internal Reference, Integrator Off

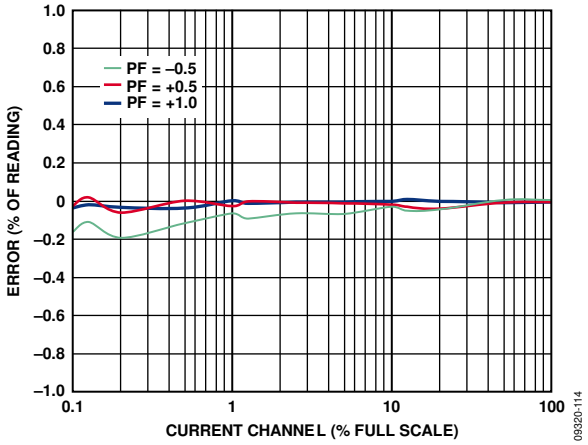

Figure 18. Current Channel B Active Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Power Factor with Internal Reference, Integrator Off

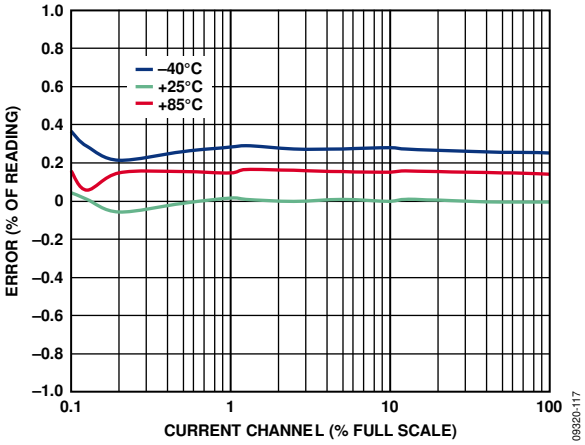

Figure 21. Current Channel B Reactive Energy Error as a Percentage of Reading (Gain = 1, Power Factor = 0) over Temperature with Internal Reference, Integrator Off

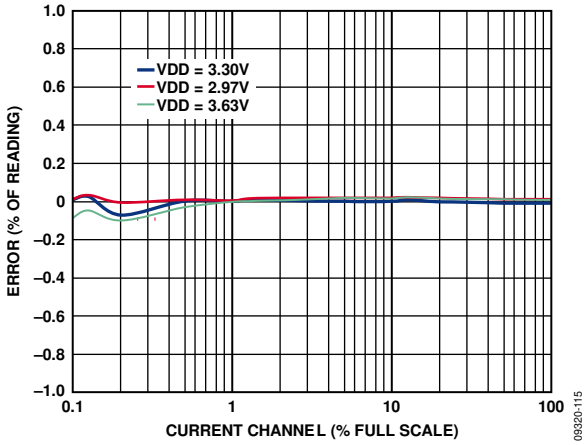

Figure 19. Current Channel B Active Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C, Power Factor = 1) over Supply Voltage with Internal Reference, Integrator Off

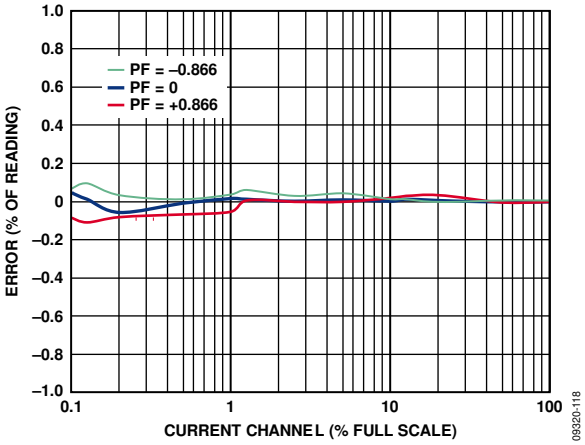

Figure 22. Current Channel B Reactive Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Power Factor with Internal Reference, Integrator Off

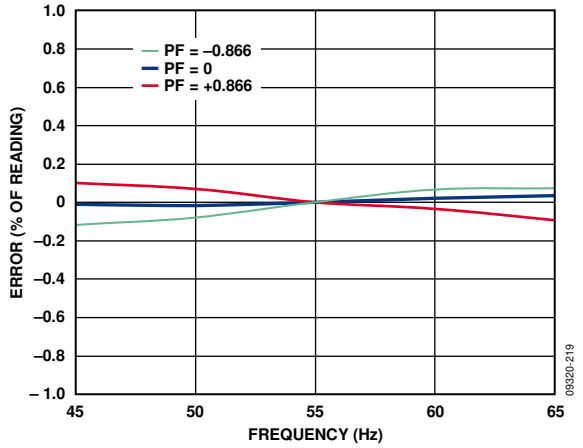

Figure 23. Current Channel B Reactive Energy Error as a Percentage of Reading (Gain = 1, Temperature = 25°C) over Frequency and Power Factor with Internal Reference, Integrator Off

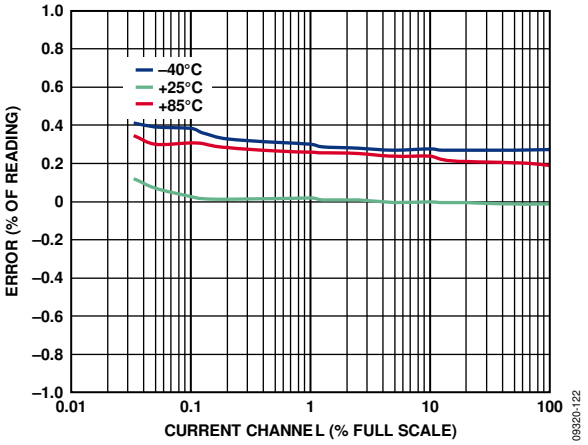

Figure 26. Current Channel A Active Energy Error as a Percentage of Reading (Gain = 16, Power Factor = 1) over Temperature with Internal Reference, Integrator On

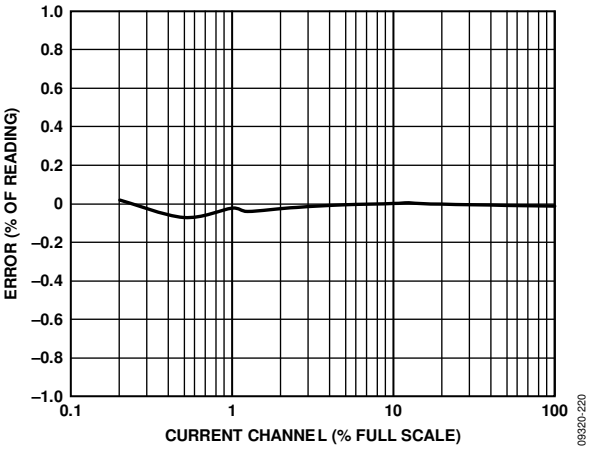

Figure 24. Current Channel B IRMS Error as a Percentage of Reading (Gain = 1, Temperature = 25°C, Power Factor = 1) with Internal Reference, Integrator Off

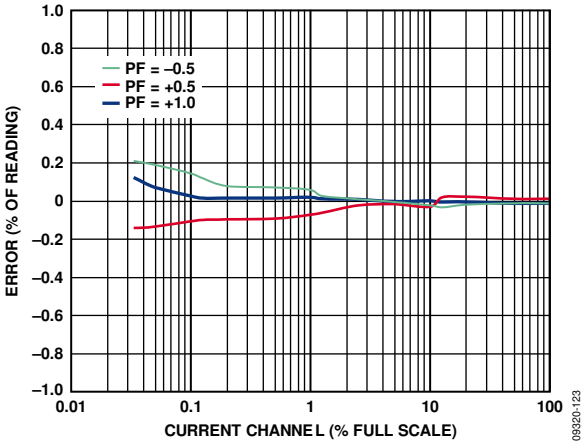

Figure 27. Current Channel A Active Energy Error as a Percentage of Reading (Gain = 16, Temperature = 25°C) over Power Factor with Internal Reference, Integrator On

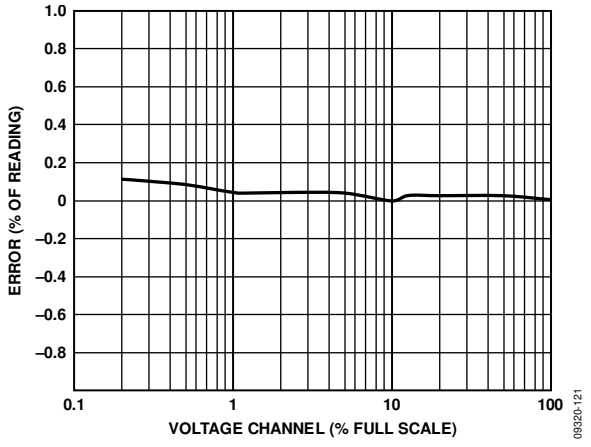

Figure 25. VRMS Error as a Percentage of Reading (Temperature = 25°C, Power Factor = 1) with Internal Reference, Integrator Off

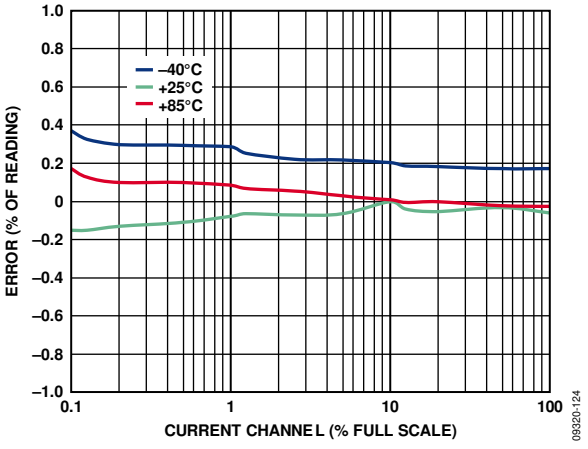

Figure 28. Current Channel B Active Energy Error as a Percentage of Reading (Gain = 16, Power Factor = 1) over Temperature with Internal Reference, Integrator On

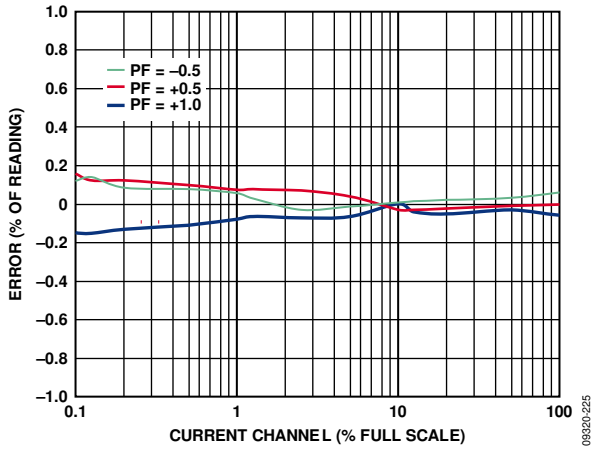

Figure 29. Current Channel B Active Energy Error as a Percentage of Reading (Gain = 16, Temperature = 25°C) over Power Factor with Internal Reference, Integrator On

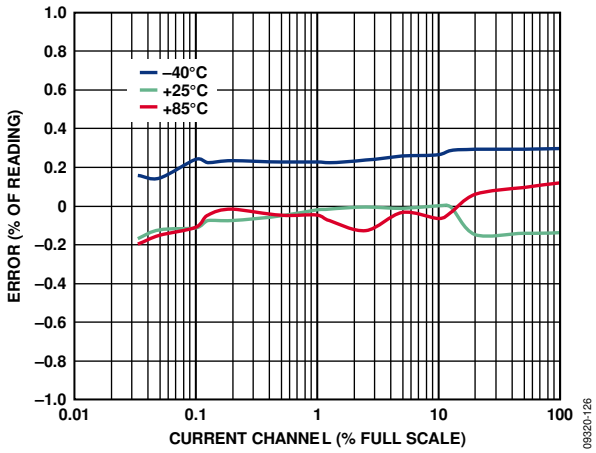

Figure 30. Current Channel A Reactive Energy Error as a Percentage of Reading (Gain = 16, Power Factor = 0) over Temperature with Internal Reference, Integrator On

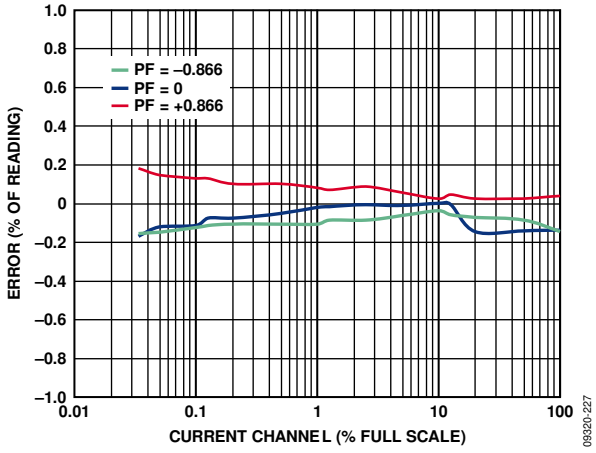

Figure 31. Current Channel A Reactive Energy Error as a Percentage of Reading (Gain = 16, Temperature = 25°C) over Power Factor with Internal Reference, Integrator On

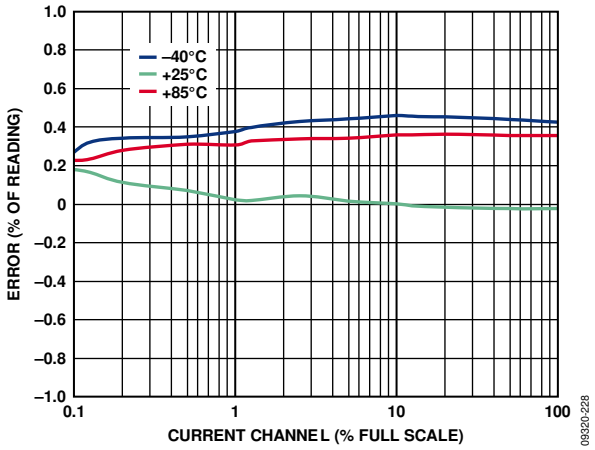

Figure 32. Current Channel B Reactive Energy Error as a Percentage of Reading (Gain = 16, Power Factor = 0) over Temperature with Internal Reference, Integrator On

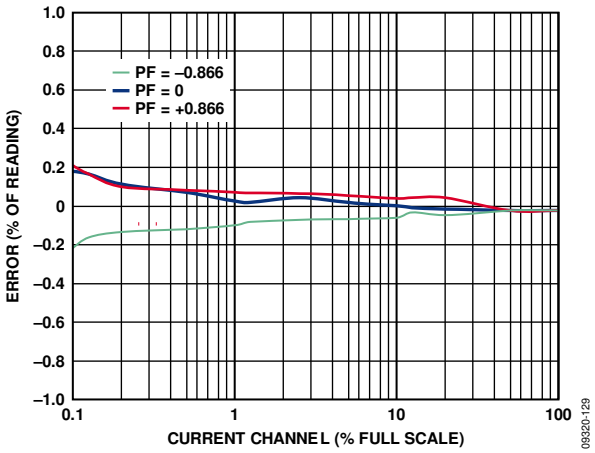

Figure 33. Current Channel B Reactive Energy Error as a Percentage of Reading (Gain = 16, Temperature = 25°C) over Power Factor with Internal Reference, Integrator On

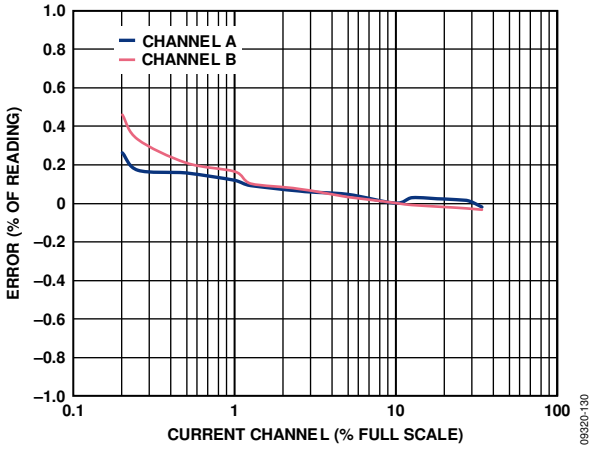

Figure 34. IRMS Error as a Percentage of Reading (Gain = 16, Temperature = 25°C) with Internal Reference, Integrator On

TEST CIRCUIT

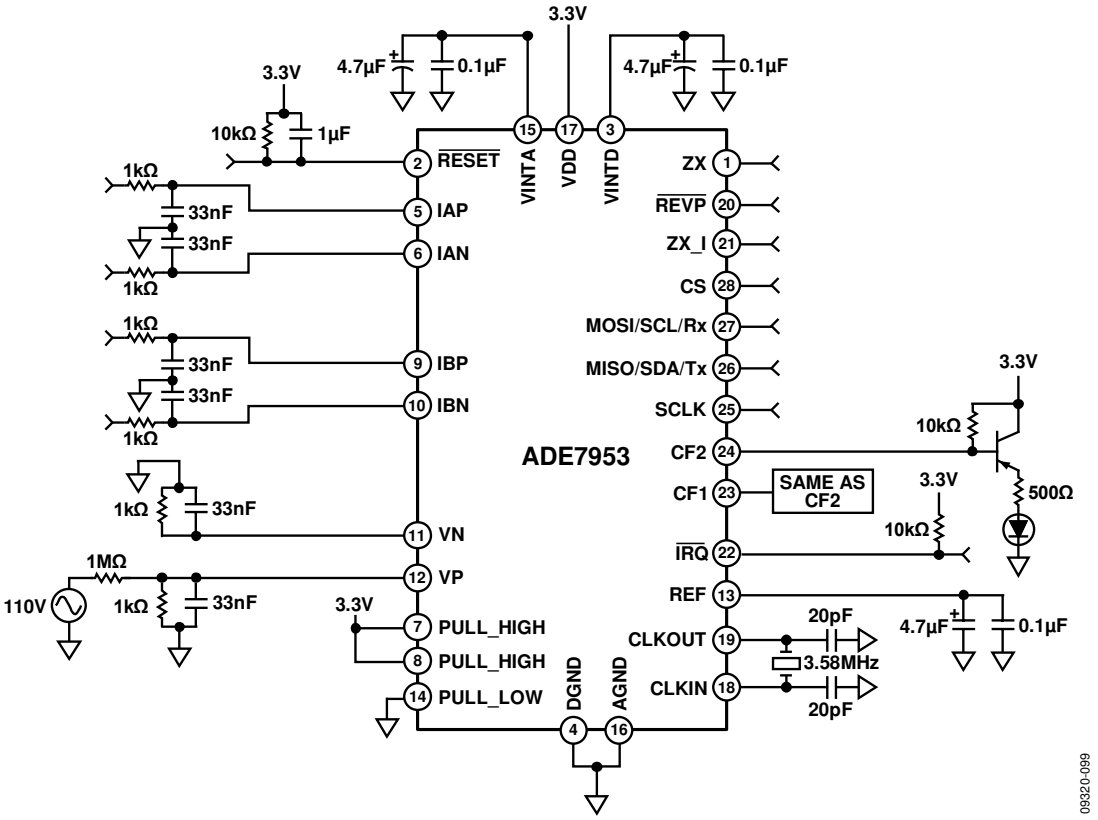

Figure 35. Test Circuit

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7953 is defined by

$$\text{Measurement Error} = \frac{\text{Energy Registered by ADE7953} - \text{True Energy}}{\text{True Energy}} \times 100\% \quad (1)$$

Phase Error Between Channels

The high-pass filter (HPF) and digital integrator introduce a slight phase mismatch between the current channels and the voltage channel. The all-digital design ensures that the phase matching between the current channels and the voltage channel is within ±0.05° over a range of 45 Hz to 65 Hz. This internal phase mismatch can be combined with the external phase error (from current sensor or component tolerance) and calibrated with the phase calibration registers.

Power Supply Rejection (PSR)

PSR quantifies the ADE7953 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms/100 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading (see the Measurement Error definition). For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied by ±10%. Any error introduced is again expressed as a percentage of reading.

ADC Offset Error

The ADC offset error refers to the dc offset associated with the analog inputs to the ADCs. It means that, with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection. However, the offset is removed from the current and voltage channels by a high-pass filter (HPF), and the power calculation is not affected by this offset.

Gain Error

The gain error in the ADCs of the ADE7953 is defined as the per-channel difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADCS section and the Voltage Channel ADC section). The difference is expressed as a percentage of the ideal code.

ADE7953 POWER-UP PROCEDURE

The ADE7953 contains an on-chip power supply monitor that supervises the power supply (VDD). While the voltage applied to the VDD pin is below 2 V ± 10%, the chip is in an inactive state. Once VDD crosses the 2 V ± 10% threshold, the power supply monitor keeps the ADE7953 in an inactive state for an additional 26 ms. This time delay allows VDD to reach the minimum specified operating voltage of 3.3 V – 10%. Once the minimum specified operating voltage is met, the internal circuitry is enabled; this is accomplished in approximately 40 ms.

Once the start-up sequence is complete and the ADE7953 is ready to receive communication from a microcontroller, the reset flag is set in the IRQSTATA register (Address 0x22D and Address 0x32D). An external interrupt is triggered on the IRQ pin. The reset interrupt is enabled by default and cannot be disabled, hence an external interrupt always occurs at the end of a power-up procedure, hardware or software reset.

It is highly recommended that the reset interrupt is used by the microcontroller to gate the first communication with the ADE7953. If the interrupt is not used, a timeout can be implemented; however, as the start-up sequence can vary part-to-part and over temperature, a timeout of a least 100 ms is recommended. The reset interrupt provides the most efficient way of monitoring the completion of the ADE7953 start-up sequence.

Once the start-up sequence is complete, communication with the ADE7953 can begin. See the Communicating with the ADE7953 section for further details.

REQUIRED REGISTER SETTING

For optimum performance, Register Address 0x120 must be configured by the user after powering up the ADE7953. This register ensures that the optimum timing configuration is selected to maximize the accuracy and dynamic range. This register is not set by default and thus must be written by the user each time the ADE7953 is powered up. Register 0x120 is a protected register and thus a key must be written to allow the register to be modified. The following sequence should be followed:

- Write 0xAD to Register Address 0xFE: This unlocks Register 0x120
- Write 0x30 to Register Address 0x120: This configures the optimum settings

The above two instructions must be performed in succession to be successful.

THEORY OF OPERATION

ANALOG INPUTS

The ADE7953 includes three analog inputs that form two current channels and one voltage channel. In a standard configuration, Current Channel A is used to measure the phase current, and Current Channel B is used to measure the neutral current. The voltage channel input measures the difference between the phase voltage and the neutral voltage. The ADE7953 can, however, be used with alternative voltage and current combinations as long as the analog input specifications described in this section are met.

Current Channel A

Current Channel A is a fully differential voltage input that is designed to be used with a current sensor. This input is driven by two pins: IAP (Pin 5) and IAN (Pin 6). The maximum differential voltage that can be applied to IAP and IAN is ±500 mV. A common-mode voltage of less than ±25 mV is recommended. Common-mode voltages in excess of this recommended value may limit the available dynamic range. A programmable gain amplifier (PGA) stage is provided on Current Channel A with gain options of 1, 2, 4, 8, 16, and 22 (see Table 6).

The maximum full-scale input of Current Channel A is ±250 mV when using a single-ended configuration and, therefore, when using a gain setting of 1, the dynamic range is limited. The Current Channel A gain is configured by writing to the PGA_IA register (Address 0x008). By default, the Current Channel A PGA is set to 1. A gain option of 22 is offered exclusively on Current Channel A, allowing high accuracy measurement for signals of very small amplitude. This configuration is particularly useful when using small value shunt resistors or Rogowski coils.

Current Channel B

Current Channel B is a fully differential voltage input that is designed to be used with a current sensor. This input is driven by two pins: IBP (Pin 9) and IBN (Pin 10). The maximum differential voltage that can be applied to IBP and IBN is ±500 mV. A common-mode voltage of less than ±25 mV is recommended. Common-mode voltages in excess of this recommended value may limit the available dynamic range. A PGA gain stage is provided on Current Channel B with gain options of 1, 2, 4, 8, and 16 (see Table 6). The Current Channel B gain is configured by writing to the PGA_IB register (Address 0x009). By default, the Current Channel B PGA is set to 1.

Voltage Channel

The voltage channel input a full differential input driven by two pins: VP (Pin 12) and VN (Pin 11). The voltage channel is typically connected in a single-ended configuration. The maximum single-ended voltage that can be applied to VP is ±500 mV with respect to VN. A common-mode voltage of less than ±25 mV is recommended. Common-mode voltages in excess of this recommended value may limit the dynamic range capabilities of the ADE7953. A PGA gain stage is provided on the voltage channel with gain options of 1, 2, 4, 8, and 16 (see Table 6).

The voltage channel gain is configured by writing to the PGA_V register (Address 0x007). By default, the voltage channel PGA is set to 1.

Table 6. PGA Gain Settings

Gain	Full-Scale Differential Input (mV)	PGA_IA[2:0] (Addr 0x008)	PGA_IB[2:0] (Addr 0x009)	PGA_V[2:0] (Addr 0x007)
1	±500	000[1]	000	000
2	±250	001	001	001
4	±125	010	010	010
8	±62.5	011	011	011
16	±31.25	100	100	100
22	±22.7	101	N/A	N/A

[1] When a gain of 1 is selected on Current Channel A, the maximum pin input is limited to ±250 mV. Therefore, when using a single-ended configuration, the maximum input is ±250 mV with respect to AGND.

ANALOG-TO-DIGITAL CONVERSION

The analog-to-digital conversion in the ADE7953 is performed by three second-order Σ-Δ modulators. For the sake of clarity, the block diagram in Figure 36 shows the operation of a first-order Σ-Δ modulator. The analog-to-digital conversion consists of a Σ-Δ modulator followed by a low-pass filter stage.

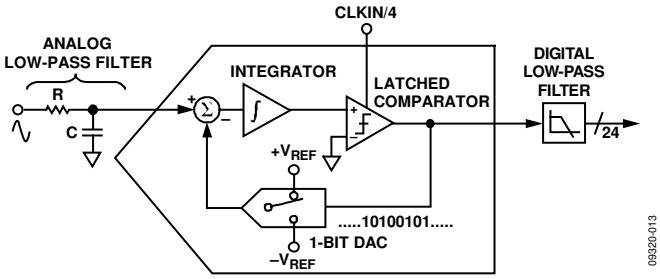

Figure 36. Σ-Δ Conversion

The Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. The ADE7953 sampling clock is equal to 895 kHz (CLKIN/4). The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and, therefore, the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. A meaningful result is obtained only when a large number of samples is averaged. This averaging is carried out in the second part of the ADC, the digital low-pass filter. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level. The Σ-Δ converter uses two techniques—oversampling and noise shaping—to achieve high resolution from what is essentially a 1-bit conversion technique.

Oversampling

Oversampling is the first technique used to achieve high resolution. Oversampling means that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, the sampling rate in the ADE7953 is 895 kHz, and the bandwidth of interest is 40 Hz to 1.23 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered (see Figure 37).

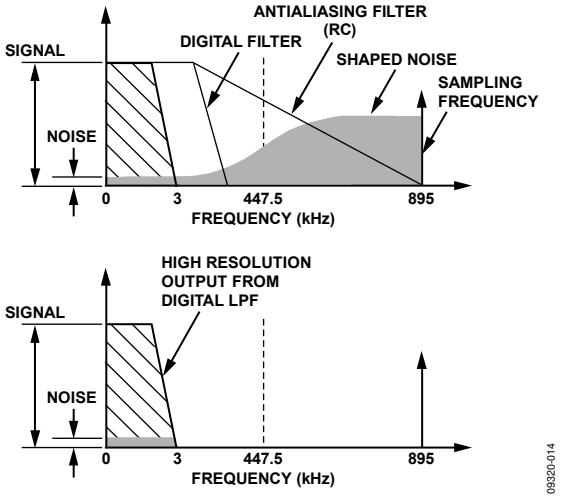

Figure 37. Noise Reduction due to Oversampling and Noise Shaping in the Analog Modulator

However, oversampling alone is not sufficient to improve the signal-to-noise ratio (SNR) in the bandwidth of interest. For example, an oversampling ratio of 4 is required to increase the SNR by only 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies (see the following section.

Noise Shaping

Noise shaping is the second technique used to achieve high resolution. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass-type response for the quantization noise due to feedback. The result is that most of the noise is at the higher frequencies, where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 37.

Antialiasing Filter

As shown in Figure 36, an external low-pass RC filter is required on the input to each modulator. The role of this filter is to prevent aliasing. Aliasing refers to the frequency components in the input signal that are folded back and appear in the sampled signal. This effect occurs with signals that are higher than half the sampling rate of the ADC (also known as the Nyquist frequency) appearing in the sampled signal at a frequency below half the sampling rate. This concept is depicted in Figure 38.

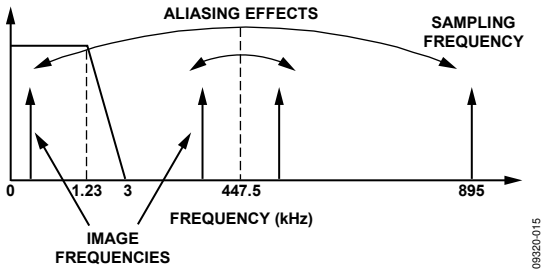

Figure 38. Aliasing Effect

The arrows shown in Figure 38 depict the frequency components above the Nyquist frequency (447.5 kHz in the case of the ADE7953) being folded back down. Aliasing occurs with all ADCs, regardless of the architecture.

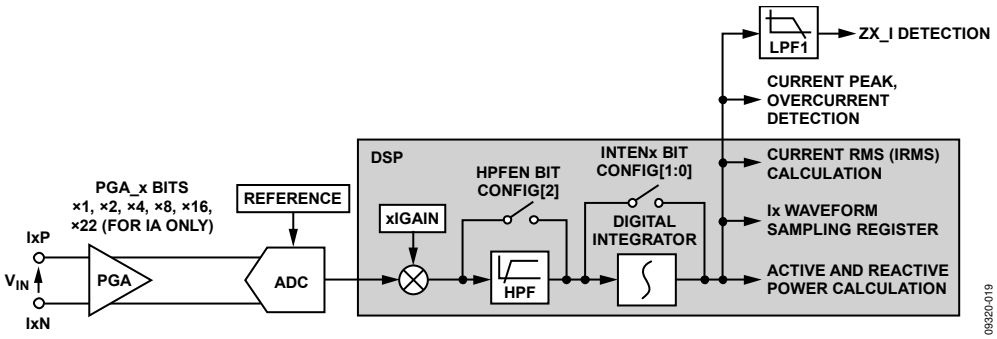

Figure 39. Current Channel ADC and Signal Path

CURRENT CHANNEL ADCS

Figure 39 shows the ADC signal path and signal processing for Current Channel A, which is accessed through the IAP and IAN pins. The signal path for Current Channel B is identical and is accessed through the IBP and IBN pins. The ADC output is a twos complement, 24-bit data-word that is available at a rate of 6.99 kSPS (thousand samples per second). With the specified full-scale analog input of ±250 mV and a PGA_Ix gain setting of 2, the ADC produces its maximum output code. The ADC output swings between −6,500,000 LSBs (decimal) and +6,500,000 LSBs. This output varies from part to part. The signal path includes a xIGAIN register to modify the current gain for Current Channel A or Current Channel B. This register can be used to match Current Channel B to Current Channel A for simple calibration and computation. This gain is performed using the BIGAIN register (Address 0x28C and Address 0x38C). The Current Channel A gain can be modified with the AIGAIN register (Address 0x280 and Address 0x380).

As shown in Figure 39, there is a high-pass filter (HPF) in each current channel signal path. The HPF is enabled by default and removes any dc offset in the ADC output. It is highly recommended that this filter be enabled at all times, but it can be disabled by clearing the HPFEN bit (Bit 2) in the CONFIG register (Address 0x102). Clearing the HPFEN bit disables the filters in both current channels and in the voltage channel.

di/dt Current Sensor and Digital Integrator

As shown in Figure 39, the current channel signal path for both Channel A and Channel B includes an internal digital integrator. This integrator is disabled by default and is required only when interfacing with a di/dt sensor, such as a Rogowski coil. When using either a shunt resistor or a current transformer (CT), this integrator is not required and should remain disabled.

A di/dt sensor detects changes in the magnetic field caused by ac current. Figure 40 shows the principle of a di/dt current sensor.

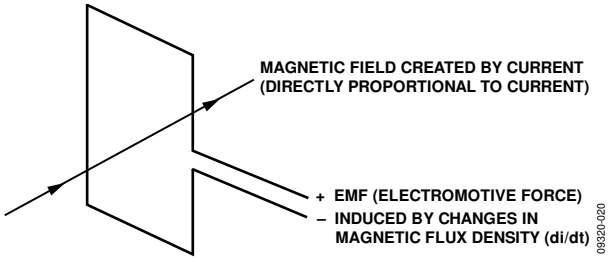

Figure 40. Principle of a di/dt Current Sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. Changes in the magnetic flux density passing through a conductor loop generate an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal that is proportional to the differential of the current over time (di/dt). The voltage output from the di/dt sensor is determined by the mutual inductance between the current-carrying conductor and the di/dt sensor. The current signal must be recovered from the di/dt signal before it can be used. An integrator is therefore necessary to restore the signal to its original form.

The ADE7953 has a built-in digital integrator on each current channel that recovers the current signal from the di/dt sensor. Both digital integrators are disabled by default. The digital integrator on Current Channel A is enabled by setting the INTENA bit (Bit 0) in the CONFIG register (Address 0x102). The digital integrator on Current Channel B is enabled by setting the INTENB bit (Bit 1) in the CONFIG register (Address 0x102).

VOLTAGE CHANNEL ADC

Figure 41 shows the ADC signal path and signal processing for the voltage channel input, which is accessed through the VP and VN pins. The ADC output is a twos complement, 24-bit data-word that is available at a rate of 6.99 kSPS (thousand samples per second). With the specified full-scale analog input of ±500 mV and a PGA_V gain setting of 1, the ADC produces its maximum output code. The ADC output swings between −6,500,000 LSBs (decimal) and +6,500,000 LSBs. Note that this output varies from part to part. The signal path includes a xVGAIN register to modify the voltage gains for the voltage channel. AVGAIN (Address 0x281 and Address 0x381) is the primary voltage gain register used, affecting RMS and Channel A energy register readings. Most frequently, the energy gain registers, not the voltage gain registers, are used in calibration. In the unique case that both the AVGAIN register and Current Channel B are used, set BVGAIN (Address 0x28D and Address 0x38D) to the same AVGAIN value to ensure equal gain in both channels.

As shown in Figure 41, there is a high-pass filter (HPF) in the voltage channel signal path. The HPF is enabled by default and removes any dc offset in the ADC output. It is highly recommended that this filter be enabled at all times, but it can be disabled by clearing the HPFEN bit (Bit 2) in the CONFIG register (Address 0x102). Clearing the HPFEN bit disables the filters in both current channels and in the voltage channel.

REFERENCE CIRCUIT

The ADE7953 has an internal voltage reference of 1.2 V nominal, which appears on the REF pin. This reference voltage is used by the ADCs in the ADE7953. The REF pin can be overdriven by an external source, for example an external 1.2 V reference. The voltage of the ADE7953 internal reference drifts slightly over temperature (see the Specifications section). The value of the temperature drift may vary slightly from part to part. A drift of x% in the reference results in a 2x% deviation in meter accuracy. The reference drift is typically minimal and is usually much smaller than the drift of other components in the meter. By default, the ADE7953 is configured to use the internal reference. If Bit 0 of the EX_REF register (Address 0x800) is set to 1, an external voltage reference can be applied to the REF pin.

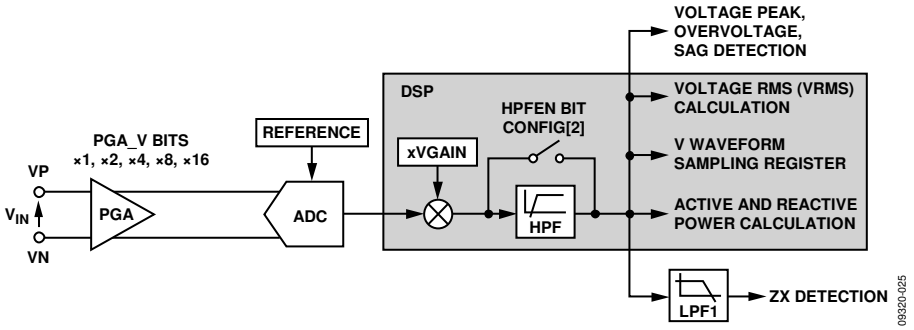

Figure 41. Voltage Channel ADC and Signal Path

ROOT MEAN SQUARE MEASUREMENT

Root mean square (rms) is a measurement of the magnitude of an ac signal. Specifically, the rms of an ac signal is equal to the amount of dc required to produce an equivalent amount of power in the load. The rms is expressed mathematically in Equation 1.

$$RMS = \sqrt{\frac{1}{t}\int_0^t f^2(t)\,dt} \quad (1)$$

For time-sampled signals, rms calculation involves squaring the signal, taking the average, and obtaining the square root.

$$RMS = \sqrt{\frac{1}{N}\sum_{n=1}^{N} f^2[n]} \quad (2)$$

As implied by Equation 2, the rms measurement contains information from the fundamental and all harmonics over a 1.23 kHz measurement bandwidth.

The ADE7953 provide rms measurements for Current Channel A, Current Channel B, and the voltage channel simultaneously. These measurements have a settling time of approximately 200 ms and are updated at a rate of 6.99 kHz.

CURRENT CHANNEL RMS CALCULATION

The ADE7953 provides rms measurements for both Current Channel A and Current Channel B. Figure 42 shows the signal path for this calculation. The signal processing is identical for Current Channel A and Current Channel B.

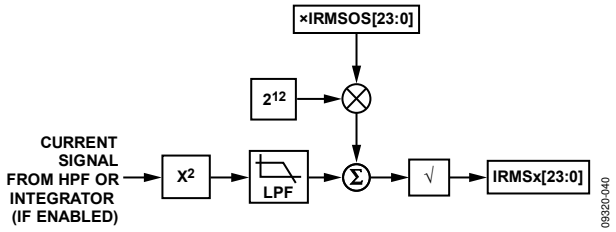

Figure 42. Current Channel RMS Signal Processing

As shown in Figure 42, the current channel ADC output samples are used to continually compute the rms. The rms is achieved by low-pass filtering the square of the output signal and then taking a square root of the result. The 24-bit unsigned rms measurements for Current Channel A and Current Channel B are available in the IRMSA (Address 0x21A and Address 0x31A) and IRMSB (Address 0x21B and Address 0x31B) registers, respectively. Both of these registers are updated at a rate of 6.99 kHz. With full-scale inputs on Current Channel A and Current Channel B, the expected reading on the IRMSA and IRMSB register is 9032007d.

Because the LPF used in the rms signal path is not ideal, it is recommended that the IRMSx registers be read synchronously to the zero-crossing signal (see the Zero-Crossing Detection section). This helps to stabilize reading-to-reading variation by removing the effect of any 2ω ripple present on the rms measurement.

VOLTAGE CHANNEL RMS CALCULATION

The ADE7953 provides an rms measurement on the voltage channel. Figure 43 shows the signal path for this calculation.

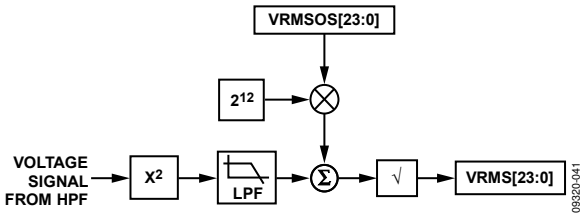

Figure 43. Voltage Channel RMS Signal Processing

As shown in Figure 43, the voltage channel ADC output samples are used to continually compute the rms. The rms is achieved by low-pass filtering the square of the output signal and then taking a square root of the result. The 24-bit unsigned voltage channel rms measurement is available in the VRMS register (Address 0x21C and Address 0x31C). This register is updated at a rate of 6.99 kHz. With full-scale inputs on the voltage channel, a VRMS reading of 9032007d can be expected.

Because the LPF used in the rms signal path is not ideal, it is recommended that the VRMS register be read synchronously to the zero-crossing signal (see the Zero-Crossing Detection section). This helps to stabilize reading-to-reading variation by removing the effect of any 2ω ripple present on the rms measurement.

ACTIVE POWER CALCULATION

Power is defined as the rate of energy flow from the source to the load. It is defined as the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal and is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec.

$$V(t) = \sqrt{2} \times V \times \sin(\omega t) \quad (3)$$

$$I(t) = \sqrt{2} \times I \times \sin(\omega t) \quad (4)$$

where:
V is the rms voltage.
I is the rms current.

$$P(t) = V(t) \times I(t) \quad (5)$$

$$P(t) = VI - VI \times \cos(2\omega t) \quad (6)$$

The average power over an integral number of line cycles (n) is given by the expression in Equation 7.

$$P = \frac{1}{nT} \int_0^{nT} P(t)dt = VI \quad (7)$$

where:
P is the active or real power.
T is the line cycle period.

The active power is equal to the dc component of the instantaneous power signal (P(t) in Equation 5). The active power is therefore equal to VI. This relationship is used to calculate active power in the ADE7953. Figure 44 illustrates this concept.

The signal chain for the active power and energy calculations in the ADE7953 is shown in Figure 45. The instantaneous power signal P(t) is generated by multiplying the current and voltage signals. The dc component of the instantaneous power signal is then extracted by LPF2 (low-pass filter) to obtain the active power information. Because LFP2 does not have an ideal "brick wall" frequency response, the active power signal has some ripple associated with it. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Because the ripple is sinusoidal in nature, it is removed when the active power signal is integrated to compute the active energy (see the Active Energy Calculation section).

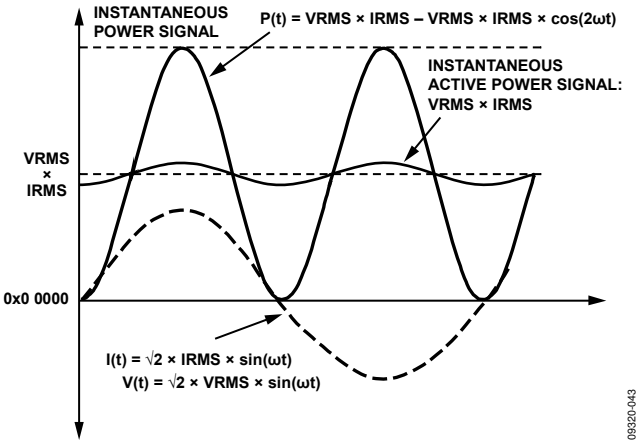

Figure 44. Active Power Calculation

The ADE7953 computes the active power simultaneously on Current Channel A and Current Channel B and stores the resulting measurements in the AWATT (Address 0x212 and Address 0x312) and BWATT (Address 0x213 and Address 0x313) registers, respectively. With full-scale inputs, the expected reading in the AWATT and BWATT registers is approximately 4862401 LSBs (decimal).

The active power measurements are taken over a bandwidth of 1.23 kHz and include the effects of any harmonics within that range. The active power registers are updated at a rate of 6.99 kHz and can be read using the waveform sampling mode (see the Instantaneous Powers and Waveform Sampling section).

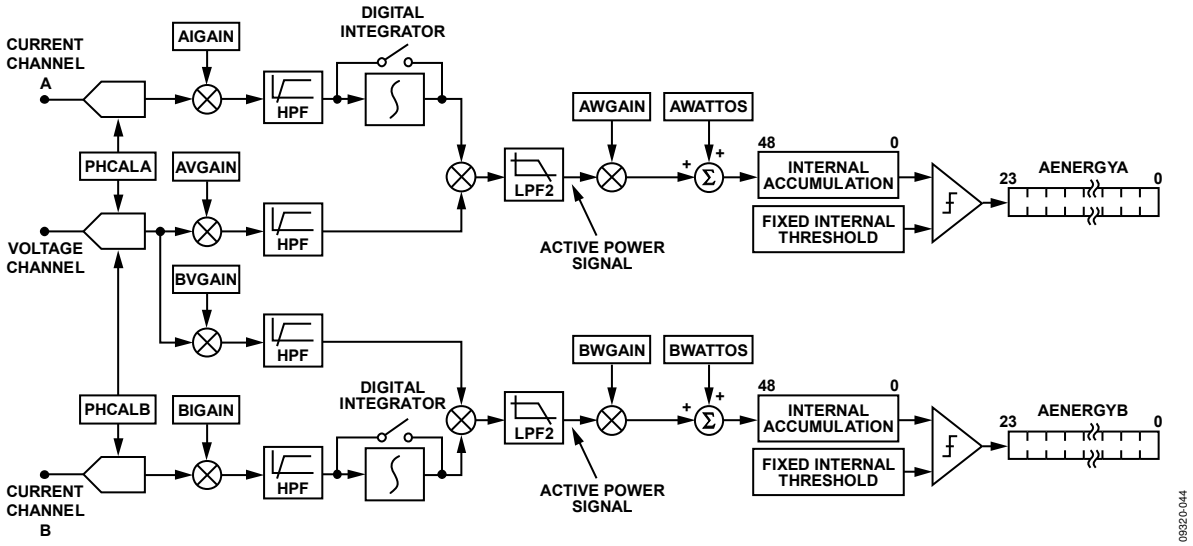

Figure 45. Active Energy Signal Chain