Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Isolated Energy Metering Chipset for Polyphase Shunt Meters

Data Sheet

ADE7978/ADE7933/ADE7932

FEATURES

- Enables shunt current sensors in polyphase energy meters
- Immune to magnetic tampering
- Highly accurate; supports EN 50470-1, EN 50470-3, IEC 62053-21, IEC 62053-22, IEC 62053-23, ANSI C12.20, and IEEE 1459 standards
- Compatible with 3-phase, 3- or 4-wire (delta or wye) meters and other 3-phase services
- Computes active, reactive, and apparent energy on each phase and on the overall system
- Less than 0.2% error in active and reactive energy over a dynamic range of 2000 to 1 at T_A = 25°C
- Less than 0.1% error in voltage rms over a dynamic range of 500 to 1 at T_A = 25°C
- Less than 0.25% error in current rms over a dynamic range of 500 to 1 at T_A = 25°C
- Power quality measurements including THD
- Single 3.3 V supply
- Operating temperature: −40°C to +85°C
- Flexible I^2C, SPI, and HSDC serial interfaces
- Safety and regulatory approvals (pending)
  - UL recognition
    - 5000 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice #5A
    - IEC 61010-1: 400 V rms
  - VDE certificate of conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 846 V peak

APPLICATIONS

- Shunt-based polyphase meters
- Power quality monitoring
- Solar inverters
- Process monitoring
- Protective devices
- Isolated sensor interfaces
- Industrial PLCs

TYPICAL APPLICATION CIRCUIT

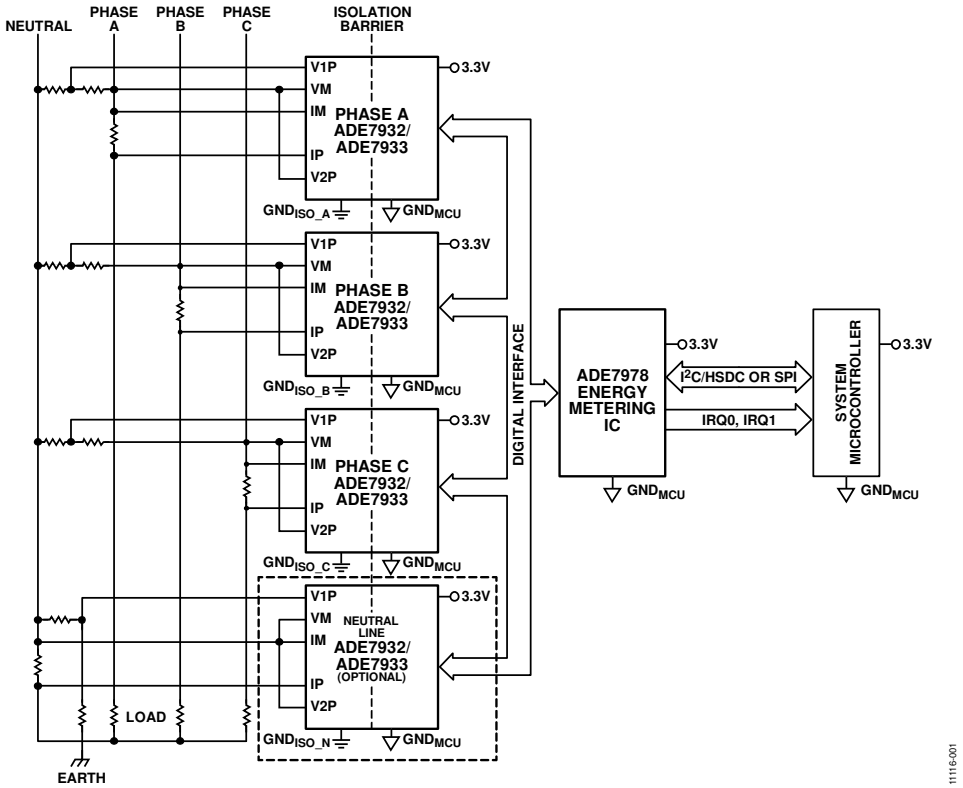

Figure 1. 3-Phase, 4-Wire Meter with Four ADE7933/ADE7932 Devices and One ADE7978

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329; 6,262,600; 7,489,526; and 7,558,080. Other patents are pending.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

11/13—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADE7978 and the ADE7933/ADE7932 form a chipset dedicated to measuring 3-phase electrical energy using shunts as current sensors.

The ADE7933/ADE7932 are isolated, 3-channel sigma-delta analog-to-digital converters (Σ-Δ ADCs) for polyphase energy metering applications that use shunt current sensors. The ADE7932 features two 24-bit ADCs, and the ADE7933 features three 24-bit ADCs. One channel is dedicated to measuring the voltage across the shunt when a shunt is used for current sensing. This channel provides a signal-to-noise ratio (SNR) of 67 dB over a 3.3 kHz signal bandwidth. Up to two additional channels are dedicated to measuring voltages, which are usually sensed using resistor dividers. These channels provide an SNR of 75 dB over a 3.3 kHz signal bandwidth. One voltage channel can be used to measure the temperature of the die via an internal sensor. The ADE7933 includes three channels: one current channel and two voltage channels. The ADE7932 includes one current channel and one voltage channel, but is otherwise identical to the ADE7933.

The ADE7933/ADE7932 include *iso*Power®, an integrated, isolated dc-to-dc converter. Based on the Analog Devices, Inc., *i*Coupler® technology, the dc-to-dc converter provides the regulated power required by the first stage of the ADCs at a 3.3 V input supply. The ADE7933/ADE7932 eliminate the need for an external dc-to-dc isolation block. The *i*Coupler chip scale transformer technology is used to isolate the logic signals between the first and second stages of the ADC. The result is a small form factor, total isolation solution.

The ADE7933/ADE7932 contain a digital interface that is specially designed to interface with the ADE7978. Using this interface, the ADE7978 accesses the ADC outputs and configuration settings of the ADE7933/ADE7932.

The ADE7933/ADE7932 are available in a 20-lead, Pb-free, wide-body SOIC package with increased creepage.

The ADE7978 is a high accuracy, 3-phase electrical energy measurement IC with serial interfaces and three flexible pulse outputs. The ADE7978 can interface with up to four ADE7933/ADE7932 devices. The ADE7978 incorporates all the signal processing required to perform total (fundamental and harmonic) active, reactive, and apparent energy measurement and rms calculations, as well as fundamental-only active and reactive energy measurement and rms calculations. A fixed function digital signal processor (DSP) executes this signal processing.

The ADE7978 measures the active, reactive, and apparent energy in various 3-phase configurations, such as wye or delta services, with both three and four wires. The ADE7978 provides system calibration features for each phase, gain calibration, and optional offset correction. Phase compensation is also available, but it is not necessary because the currents are sensed using shunts. The CF1, CF2, and CF3 logic outputs provide a wide selection of power information: total active, reactive, and apparent powers; the sum of the current rms values; and fundamental active and reactive powers.

The ADE7978 incorporates power quality measurements, such as short duration low or high voltage detection, short duration high current variations, line voltage period measurement, and angles between phase voltages and currents. Two serial interfaces, SPI and I^2C, can be used to communicate with the ADE7978. A dedicated high speed interface—the high speed data capture (HSDC) port—can be used in conjunction with I^2C to provide access to the ADC outputs and real-time power information. The ADE7978 also has two interrupt request pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$, to indicate that an enabled interrupt event has occurred. The ADE7978 is available in a 28-lead, Pb-free LFCSP package.

Note that throughout this data sheet, multifunction pins, such as SCLK/SCL, are referred to by the entire pin name or by a single function of the pin, for example, SCLK, when only that function is relevant.

FUNCTIONAL BLOCK DIAGRAMS

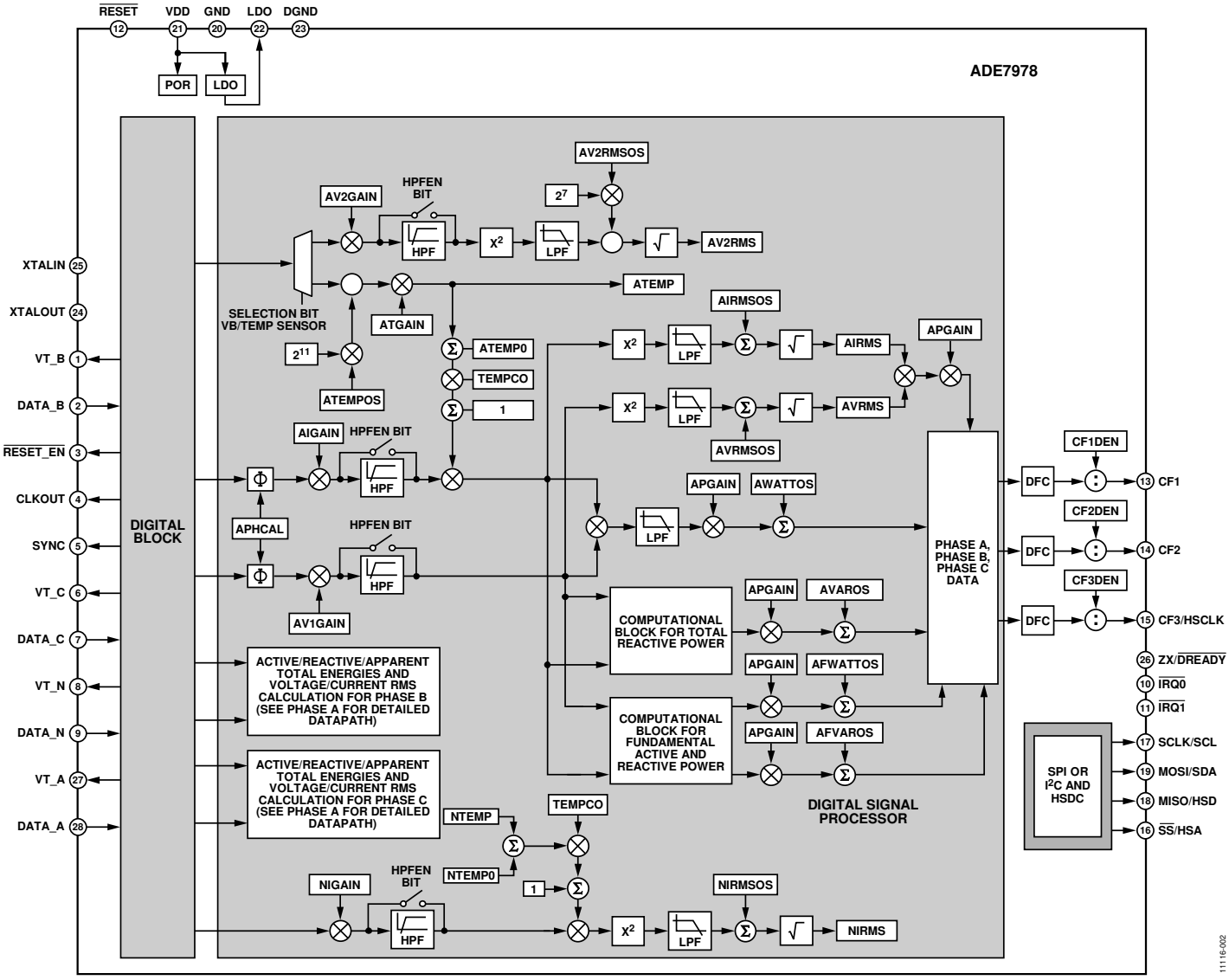

Figure 2. ADE7978 Functional Block Diagram

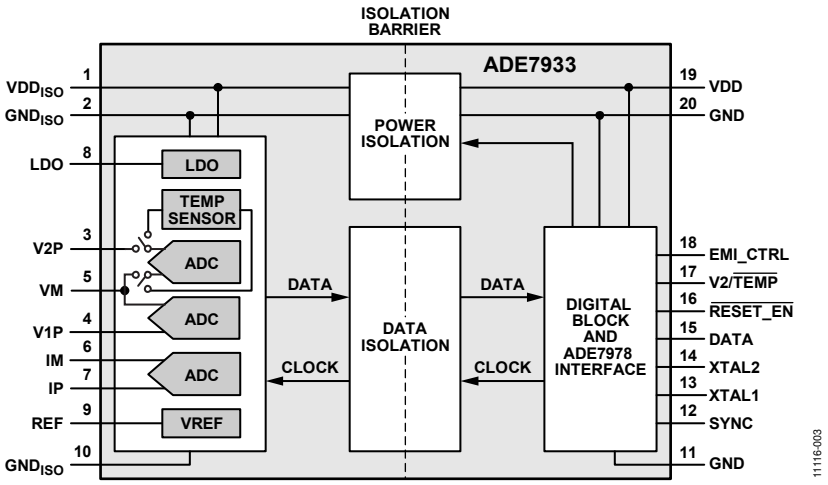

Figure 3. ADE7933 Functional Block Diagram

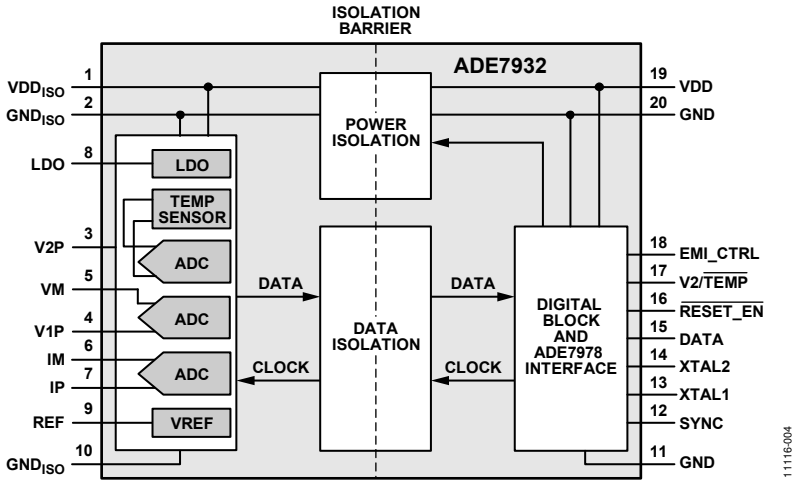

Figure 4. ADE7932 Functional Block Diagram

SPECIFICATIONS

SYSTEM SPECIFICATIONS, ADE7978 AND ADE7933/ADE7932

VDD = 3.3 V ± 10%, GND = DGND = 0 V, ADE7978 XTALIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP} = 25°C.

Table 1.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
ACTIVE ENERGY MEASUREMENT					
Measurement Error (per Phase)					
Total Active Energy		0.1		%	Over a dynamic range of 500 to 1, power factor (PF) = 1, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PF = 1
Fundamental Active Power		0.1		%	Over a dynamic range of 500 to 1, PF = 1, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PF = 1
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms at 50 Hz/100 Hz, IP = 6.25 mV rms, V1P = V2P = 100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc, IP = 6.25 mV rms, V1P = V2P = 100 mV rms
Output Frequency Variation		0.01		%	
Total Active Energy Measurement Bandwidth		3.3		kHz	
REACTIVE ENERGY MEASUREMENT					
Measurement Error (per Phase)					
Total Reactive Power		0.1		%	Over a dynamic range of 500 to 1, PF = 0, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PF = 0
Fundamental Reactive Power		0.1		%	Over a dynamic range of 500 to 1, PF = 0, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PF = 0
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms at 50 Hz/100 Hz, IP = 6.25 mV rms, V1P = V2P = 100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc, IP = 6.25 mV rms, V1P = V2P = 100 mV rms
Output Frequency Variation		0.01		%	
Total Reactive Energy Measurement Bandwidth		3.3		kHz	
RMS MEASUREMENTS					
Measurement Bandwidth		3.3		kHz	I rms and V rms
V rms Measurement Error		0.1		%	Over a dynamic range of 500 to 1
I rms Measurement Error		0.25		%	Over a dynamic range of 500 to 1
Fundamental V rms Measurement Error		0.1		%	Over a dynamic range of 500 to 1
Fundamental I rms Measurement Error		0.25		%	Over a dynamic range of 500 to 1
WAVEFORM SAMPLING					Sampling CLKIN/2048 (16.384 MHz/2048 = 8 kSPS)
Current Channels					See the Waveform Sampling Mode section
Signal-to-Noise Ratio, SNR		67		dB	
Signal-to-Noise-and-Distortion (SINAD) Ratio		67		dB	
Total Harmonic Distortion, THD		−85		dB	
Spurious-Free Dynamic Range, SFDR		88		dBFS	

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
Voltage Channels					
Signal-to-Noise Ratio, SNR		75		dB	
Signal-to-Noise-and-Distortion (SINAD) Ratio		74		dB	
Total Harmonic Distortion, THD		−81		dB	
Spurious-Free Dynamic Range, SFDR		81		dBFS	
Bandwidth (−3 dB)		3.3		kHz	
TIME INTERVAL BETWEEN PHASE SIGNALS					
Measurement Error		0.3		Degrees	Line frequency = 45 Hz to 65 Hz, HPF on
CF1, CF2, CF3 PULSE OUTPUTS					
Maximum Output Frequency		68.8		kHz	WTHR = VARTHR = VATHR = 3, CFxDEN = 1, full scale current and voltage, PF = 1, one phase only
Duty Cycle		50		%	CF1, CF2, or CF3 frequency > 6.25 Hz, CFxDEN is even and > 1
		(1 + 1/CFxDEN) × 50		%	CF1, CF2, or CF3 frequency > 6.25 Hz, CFxDEN is odd and > 1
Active Low Pulse Width		80		ms	CF1, CF2, or CF3 frequency < 6.25 Hz
Jitter		0.04		%	CF1, CF2, or CF3 frequency = 1 Hz, nominal phase currents larger than 10% of full scale

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for definitions of the parameters.

ADE7978 SPECIFICATIONS

VDD = 3.3 V ± 10%, GND = DGND = 0 V, XTALIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP} = 25°C.

Table 2.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
CLOCK INPUT					All specifications for CLKIN = 16.384 MHz
Input Clock Frequency, CLKIN	16.22	16.384	16.55	MHz	Minimum = 16.384 MHz − 1%; maximum = 16.384 MHz + 1%
XTALIN Logic Inputs					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	
XTALIN Total Capacitance[3]		40		pF	
XTALOUT Total Capacitance[3]		40		pF	
CLOCK OUTPUT					
Output Clock Frequency at CLKOUT Pin		4.096		MHz	
Duty Cycle		50		%	
Output High Voltage, V_{OH}	2.4			V	
I_{SOURCE}			4.8	mA	
Output Low Voltage, V_{OL}			0.4	V	
I_{SINK}			4.8	mA	
LOGIC INPUTS—MOSI/SDA, SCLK/SCL, $\overline{SS}$/HSA, DATA_A, DATA_B, DATA_C, DATA_N					
Input High Voltage, V_{INH}	2.4			V	VDD = 3.3 V ± 10%
Input Current, I_{IN}		2	40	nA	Input = VDD = 3.3 V
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V ± 10%
Input Current, I_{IN}		5	180	nA	Input = 0 V, VDD = 3.3 V
Input Capacitance, C_{IN}			10	pF	
LOGIC INPUT—$\overline{RESET}$					
Input High Voltage, V_{INH}	2.4			V	VDD = 3.3 V ± 10%
Input Current, I_{IN}		80	160	nA	Input = VDD = 3.3 V
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V ± 10%
Input Current, I_{IN}		−8	+11	µA	Input = 0 V, VDD = 3.3 V
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS—$\overline{IRQ0}$, $\overline{IRQ1}$, MISO/HSD, CLKOUT, $\overline{SYNC}$, VT_A, VT_B, VT_C, VT_N, ZX/$\overline{DREADY}$, $\overline{RESET\_EN}$					VDD = 3.3 V ± 10%
Output High Voltage, V_{OH}	2.4			V	VDD = 3.3 V
I_{SOURCE}			4.8	mA	
Output Low Voltage, V_{OL}			0.4	V	VDD = 3.3 V ± 10%
I_{SINK}			4.8	mA	
CF1, CF2, CF3/HSCLK					
Output High Voltage, V_{OH}	2.4			V	VDD = 3.3 V ± 10%
I_{SOURCE}			8	mA	
Output Low Voltage, V_{OL}			0.4	V	VDD = 3.3 V ± 10%
I_{SINK}			8.5	mA	
POWER SUPPLY					For specified performance
VDD Pin	2.97		3.63	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
I_{DD}		10.6	15.5	mA	

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for a definition of the parameters.
[3] XTALIN/XTALOUT total capacitances refer to the net capacitances on each pin. Each capacitance is the sum of the parasitic capacitance at the pin and the capacitance of the ceramic capacitor connected between the pin and GND. See the ADE7978 and ADE7933/ADE7932 Clocks section for more information.

I²C Interface Timing Parameters

VDD = 3.3 V ± 10%, GND = DGND = 0 V, XTALIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 3.

		Standard Mode		Fast Mode		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time for Start and Repeated Start Conditions	$t_{HD;STA}$	4.0		0.6		µs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		µs
High Period of SCL Clock	t_{HIGH}	4.0		0.6		µs
Set-Up Time for Repeated Start Condition	$t_{SU;STA}$	4.7		0.6		µs
Data Hold Time	$t_{HD;DAT}$	0	3.45	0	0.9	µs
Data Setup Time	$t_{SU;DAT}$	250		100		ns
Rise Time of SDA and SCL Signals	t_R		1000	20	300	ns
Fall Time of SDA and SCL Signals	t_F		300	20	300	ns
Setup Time for Stop Condition	$t_{SU;STO}$	4.0		0.6		µs
Bus Free Time Between a Stop and Start Condition	t_{BUF}	4.7		1.3		µs
Pulse Width of Suppressed Spikes	t_{SP}	N/A[1]			50	ns

[1] N/A means not applicable.

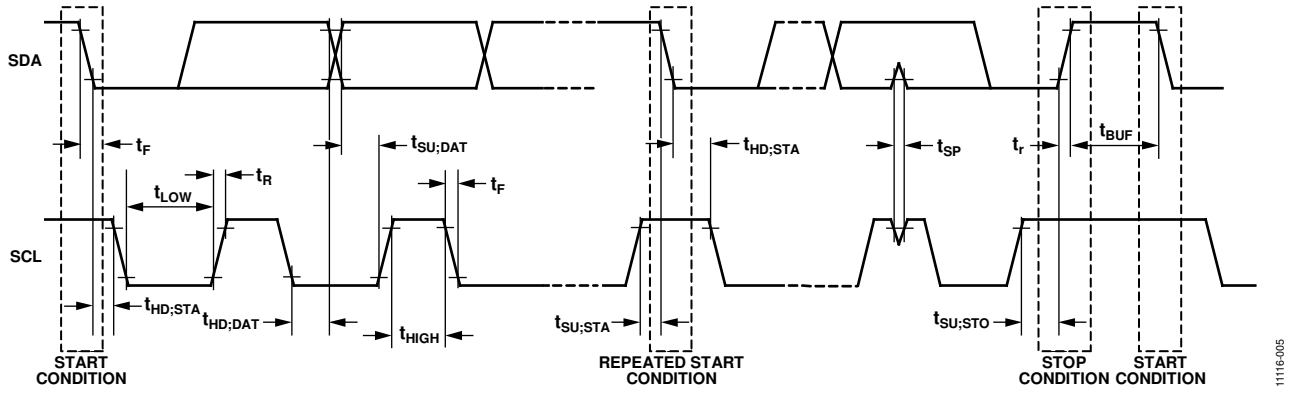

Figure 5. I²C Interface Timing

SPI Interface Timing Parameters

VDD = 3.3 V ± 10%, GND = DGND = 0 V, XTALIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 4.

Parameter	Symbol	Min	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	50		ns
SCLK Period		0.4	4000[1]	µs
SCLK Low Pulse Width	t_{SL}	175		ns
SCLK High Pulse Width	t_{SH}	175		ns
Data Output Valid After SCLK Edge	t_{DAV}		130	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	100		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	50		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}		1	µs
$\overline{SS}$ High After SCLK Edge	t_{SFS}	100		ns

[1] Guaranteed by design.

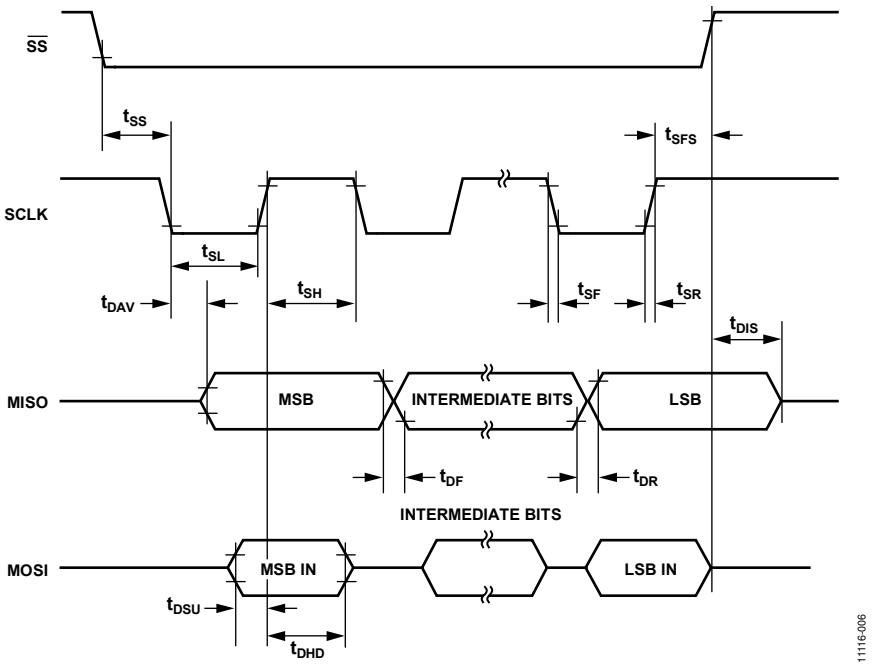

Figure 6. SPI Interface Timing

HSDC Interface Timing Parameters

VDD = 3.3 V ± 10%, GND = DGND = 0 V, XTALIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C.

Table 5.

Parameter	Symbol	Min	Max	Unit
HSA to HSCLK Edge	t_{SS}	0		ns
HSCLK Period		125		ns
HSCLK Low Pulse Width	t_{SL}	50		ns
HSCLK High Pulse Width	t_{SH}	50		ns
Data Output Valid After HSCLK Edge	t_{DAV}		40	ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
HSCLK Rise Time	t_{SR}		10	ns
HSCLK Fall Time	t_{SF}		10	ns
HSD Disable After HSA Rising Edge	t_{DIS}	5		ns
HSA High After HSCLK Edge	t_{SFS}	0		ns

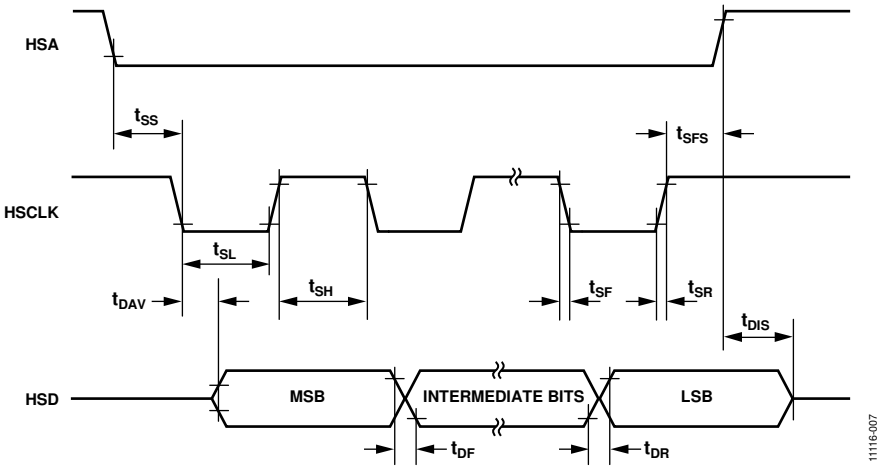

Figure 7. HSDC Interface Timing

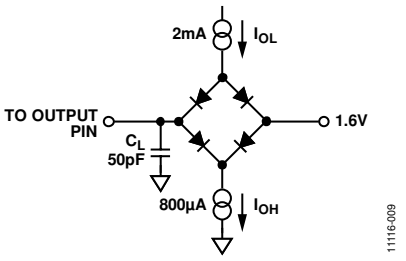

Figure 8. Load Circuit for Timing Specifications

ADE7933/ADE7932 SPECIFICATIONS

V_{DD1} = 3.3 V ± 10%, GND = 0 V, on-chip reference, XTAL1 = 4.096 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP} = 25°C.

Table 6.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
ANALOG INPUTS					
Pseudo Differential Signal Voltage Range					
Between IP and IM Pins	−31.25		+31.25	mV peak	IM pin connected to GND_{ISO}
Between V1P and VM Pins and Between V2P and VM Pins	−500		+500	mV peak	Pseudo differential inputs between V1P and VM pins and between V2P and VM pins, VM pin connected to GND_{ISO}
Maximum VM and IM Voltage	−25		+25	mV	
Crosstalk		−90		dB	IP and IM inputs set to 0 V (GND_{ISO}), V1P and V2P inputs at full scale
		−105		dB	V2P or V1P and VM inputs set to 0 V (GND_{ISO}), IP and V1P or V2P inputs at full scale
Input Impedance to GND_{ISO} (DC)					
IP, IM, V1P, and V2P Pins	480			kΩ	
VM Pin	280			kΩ	
Current Channel ADC Offset Error		−2		mV	
Voltage Channel ADC Offset Error		−35		mV	V2 channel applies to the ADE7933 only
ADC Offset Drift over Temperature	−500		+500	ppm/°C	V1 channel only
Gain Error	−4		+4	%	
Gain Drift over Temperature	−135		+135	ppm/°C	Current channel
	−65		+65	ppm/°C	V1 and V2 channels
AC Power Supply Rejection		−90		dB	VDD = 3.3 V + 120 mV rms at 50 Hz/100 Hz, IP = V1P = V2P = GND_{ISO}
DC Power Supply Rejection		−80		dB	VDD = 3.3 V ± 330 mV dc, IP = 6.25 mV rms, V1P = V2P = 100 mV rms
TEMPERATURE SENSOR					
Accuracy		±5		°C	
CLOCK INPUT					All specifications for XTAL1 = 4.096 MHz
Input Clock Frequency, XTAL1	3.6	4.096	4.21	MHz	Nominal value provided by the ADE7978; min and max values apply if the ADE7933/ADE7932 are used without the ADE7978
XTAL1 Duty Cycle	45	50	55	%	Values apply if the ADE7933/ADE7932 are used without the ADE7978
XTAL1 Logic Inputs					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	
XTAL1 Total Capacitance[2]		40		pF	
XTAL2 Total Capacitance[2]		40		pF	
LOGIC INPUTS—SYNC, V2/$\overline{TEMP}$, $\overline{RESET\_EN}$, EMI_CTRL					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	
Input Current, I_{IN}			15	nA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS—DATA					
Output High Voltage, V_{OH}	2.5			V	I_{SOURCE} = 800 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					For specified performance
VDD Pin	2.97		3.63	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
I_{DD}		12.5	19	mA	
		50		µA	Bit 6 (CLKOUT_DIS) and Bit 7 (ADE7933_SWRST) in the CONFIG3 register set to 1

[1] See the Terminology section for definitions of the parameters.
[2] XTAL1/XTAL2 total capacitances refer to the net capacitances on each pin. Each capacitance is the sum of the parasitic capacitance at the pin and the capacitance of the ceramic capacitor connected between the pin and GND. See the ADE7978 and ADE7933/ADE7932 Clocks section for more information.

Regulatory Approvals (Pending)

The ADE7933/ADE7932 are pending approval by the organizations listed in Table 7. See Table 12 and the Insulation Lifetime section for more information about the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 7.

UL	CSA	VDE
Recognized under UL 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single protection, 5000 V rms isolation voltage	Basic insulation per IEC 61010-1, 400 V rms (564 V peak) maximum working voltage	Reinforced insulation, 846 V peak

[1] In accordance with UL 1577, each ADE7933/ADE7932 is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10 (VDE V 0884-10):2006-12, each ADE7933/ADE7932 is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval.

Insulation and Safety Related Specifications

Table 8. Critical Safety Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		5000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PCB layout
Minimum External Tracking (Creepage)	L(I02)	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	IEC 60112
Isolation Group		II		Material Group DIN VDE 0110, 1/89, Table 1

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 Insulation Characteristics

The ADE7933/ADE7932 are suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by the protective circuits.

Table 9.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	846	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1592	V peak
Input-to-Output Test Voltage, Method A		$V_{pd(m)}$		
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1273	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		1018	V peak
Highest Allowable Overvoltage		V_{IOTM}	6000	V peak
Surge Isolation Voltage	$V_{PEAK} = 10$ kV; 1.2 µs rise time; 50 µs, 50% fall time	V_{IOSM}	6000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 9)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.78	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

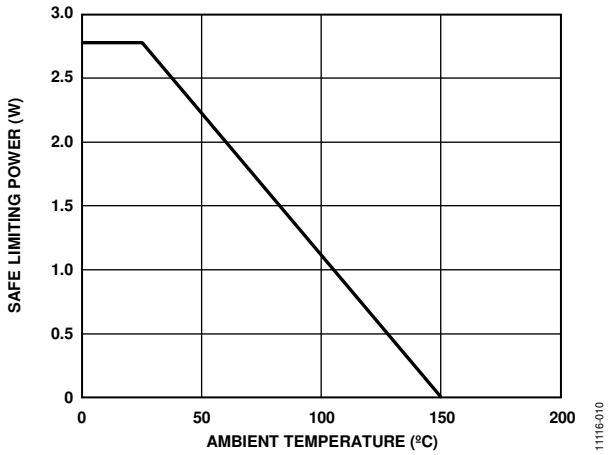

Figure 9. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 10.

Parameter	Rating
ADE7978	
VDD to GND	−0.3 V to +3.7 V
Digital Input Voltage to DGND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VDD + 0.3 V
ADE7933/ADE7932	
VDD to GND	−0.3 V to +3.7 V
Analog Input Voltage to GND_{ISO}, IP, IM, V1P, V2P, VM	−2 V to +2 V
Reference Input Voltage to GND_{ISO}	−0.3 V to VDD + 0.3 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.3 V
Common-Mode Transients[1]	−100 kV/µs to +100 kV/µs
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)[2]	
ADE7978	300°C
ADE7933/ADE7932	260°C

[1] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

[2] Analog Devices recommends that reflow profiles used in soldering RoHS compliant parts conform to JEDEC J-STD 20. For the latest revision of this standard, refer to JEDEC.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} and θ_{JC} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 11. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
28-Lead LFCSP (ADE7978)	29.3	1.8	°C/W
20-Lead SOIC (ADE7933/ADE7932)	48.0	6.2	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 12. ADE7933/ADE7932 Maximum Continuous Working Voltage Supporting a 50-Year Minimum Lifetime[1]

Parameter	Max	Unit	Applicable Certification
AC Voltage, Bipolar Waveform	564	V peak	All certifications, 50-year operation
DC Voltage			
Basic Insulation	600	V peak	

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. For more information, see the Insulation Lifetime section.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

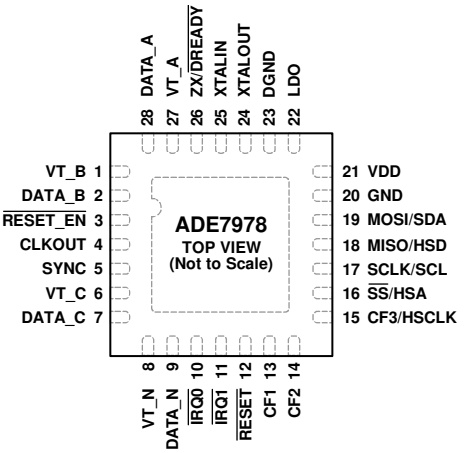

Figure 10. Pin Configuration, ADE7978

Table 13. Pin Function Descriptions, ADE7978

Pin No.	Mnemonic	Description
1	VT_B	Selects the second voltage input (V2P) or the temperature measurement on the Phase B ADE7933/ADE7932. Connect this pin to the V2/TEMP pin of the Phase B ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense Phase B—as in the 3-phase, 3-wire delta configuration—leave this pin unconnected.
2	DATA_B	Receives the bit streams from the Phase B ADE7933/ADE7932. Connect this pin to the DATA pin of the Phase B ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense Phase B—as in the 3-phase, 3-wire delta configuration—connect this pin to VDD.
3	RESET_EN	Reset Output Enable. Connect this pin to the RESET_EN pins of the ADE7933/ADE7932 devices. This pin is used by the ADE7978 to reset the ADE7933/ADE7932 devices (see the Hardware Reset section).
4	CLKOUT	4.096 MHz Output Clock Signal. Connect this pin to the XTAL1 pins of the ADE7933/ADE7932 devices.
5	SYNC	Clock Output (1.024 MHz). This pin is the clock for serial communication with the ADE7933/ADE7932 devices. Connect this pin to the SYNC pins of the ADE7933/ADE7932 devices.
6	VT_C	Selects the second voltage input (V2P) or the temperature measurement on the Phase C ADE7933/ADE7932. Connect this pin to the V2/TEMP pin of the Phase C ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense Phase C, leave this pin unconnected.
7	DATA_C	Receives the bit streams from the Phase C ADE7933/ADE7932. Connect this pin to the DATA pin of the Phase C ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense Phase C, connect this pin to VDD.
8	VT_N	Selects the second voltage input (V2P) or the temperature measurement on the neutral line ADE7933/ADE7932. Connect this pin to the V2/TEMP pin of the neutral line ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense the neutral line, leave this pin unconnected.
9	DATA_N	Receives the bit streams from the neutral line ADE7933/ADE7932. Connect this pin to the DATA pin of the neutral line ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense the neutral line, connect this pin to VDD.
10, 11	IRQ0, IRQ1	Interrupt Request Outputs. These pins are active low logic outputs. For information about the events that can trigger an interrupt, see the Interrupts section.
12	RESET	Reset Input, Active Low. Set this pin low for at least 10 µs to trigger a hardware reset (see the Hardware Reset section).
13, 14, 15	CF1, CF2, CF3/HSCLK	Calibration Frequency (CF) Logic Outputs. These outputs provide power information and are used for operational and calibration purposes. CF3 is multiplexed with the serial clock output of the HSDC port.
16	SS/HSA	Slave Select for the SPI Port/HSDC Port Active.
17	SCLK/SCL	Serial Clock Input for the SPI Port/Serial Clock Input for the I²C Port. This pin has a Schmitt trigger input for use with clock sources that have a slow edge transition time, for example, opto-isolator outputs. The default functionality of this pin is SCL.

Pin No.	Mnemonic	Description
18	MISO/HSD	Data Output for the SPI Port/Data Output for the HSDC Port.
19	MOSI/SDA	Data Input for the SPI Port/Data Output for the I^2C Port. The default functionality of this pin is SDA.
20	GND	Ground Reference for the Input Circuitry.
21	VDD	Supply Voltage. This pin provides the supply voltage. For specified operation, maintain the supply voltage at 3.3 V ± 10%. Decouple this pin to GND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
22	LDO	1.8 V Output of the Digital Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor. Do not connect active external circuitry to this pin.
23	DGND	Ground Reference for the Digital Circuitry.
24	XTALOUT	A crystal with a maximum drive level of 0.5 mW and an equivalent series resistance (ESR) of 20 Ω can be connected across this pin and the XTALIN pin to provide a clock source for the ADE7978.
25	XTALIN	Master Clock. An external clock can be provided at this logic input. Alternatively, a crystal with a maximum drive level of 0.5 mW and an ESR of 20 Ω can be connected across XTALIN and XTALOUT to provide a clock source for the ADE7978. The clock frequency for specified operation is 16.384 MHz. For more information, see the ADE7978 and ADE7933/ADE7932 Clocks section.
26	ZX/$\overline{\text{DREADY}}$	Zero-Crossing (ZX) Output Pin. The ZX pin goes high on the positive-going edge of the selected phase voltage zero crossing; the pin goes low on the negative-going edge of the zero crossing (see the Zero-Crossing Detection section for more information). $\overline{\text{DREADY}}$ is an active low signal that is generated approximately 70 ns after Bit 17 (DREADY) in the STATUS0 register is set to 1. This pin has a frequency of 8 kHz and stays low for 10 µs every period. The default functionality of this pin is $\overline{\text{DREADY}}$.
27	VT_A	Selects the second voltage input (V2P) or the temperature measurement on the Phase A ADE7933/ADE7932. Connect this pin to the V2/$\overline{\text{TEMP}}$ pin of the Phase A ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense Phase A, leave this pin unconnected.
28	DATA_A	Receives the bit streams from the Phase A ADE7933/ADE7932. Connect this pin to the DATA pin of the Phase A ADE7933/ADE7932. If no ADE7933/ADE7932 is used to sense Phase A, connect this pin to VDD.
EP	Exposed Pad	Create a similar pad on the PCB under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package. Connect the pads to DGND and GND.

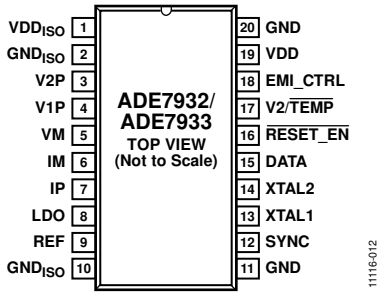

Figure 11. Pin Configuration, ADE7933/ADE7932

Table 14. Pin Function Descriptions, ADE7933/ADE7932

Pin No.	Mnemonic	Description
1	VDD_{ISO}	Isolated Secondary Side Supply Voltage. This pin provides access to the 3.3 V on-chip isolated power supply. Do not connect active external circuitry to this pin. Decouple this pin with a 10 µF capacitor in parallel with a ceramic 0.1 µF capacitor.
2, 10	GND_{ISO}	Ground Reference for the Isolated Secondary Side. This pin provides the ground reference for the analog circuitry. Use this quiet ground reference for all analog circuitry.
3, 4, 5	V2P, V1P, VM	Analog Inputs for the Voltage Channels. These channels are used with voltage transducers and are referred to in this data sheet as the voltage channels. These inputs are pseudo differential voltage inputs with a maximum signal level of ±0.5 V with respect to VM for specified operation. Use these pins with the related input circuitry, as shown in Figure 34. The second voltage channel (V2P) is available on the ADE7933 only. If the V1P or V2P pin is not used on the ADE7933, connect the pin to the VM pin. On the ADE7932, the V2P pin must always be connected to the VM pin.
6, 7	IM, IP	Analog Inputs for the Current Channel. This channel is used with shunts and is referred to in this data sheet as the current channel. These inputs are pseudo differential voltage inputs with a maximum differential level of ±31.25 mV. Use these pins with the related input circuitry, as shown in Figure 34.
8	LDO	2.5 V Output of the Analog Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor using GND_{ISO} (Pin 10). Do not connect active external circuitry to this pin.
9	REF	Voltage Reference. This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. Decouple this pin to GND_{ISO} (Pin 10) with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor.
11, 20	GND	Primary Ground Reference.
12	SYNC	Synchronization Pin. The 4.096 MHz clock signal generated by the ADE7978 is used for serial communication between the ADE7933/ADE7932 and the ADE7978. Connect the ADE7933/ADE7932 SYNC pin to the SYNC pin of the ADE7978.
13	XTAL1	Master Clock. Connect this pin to the ADE7978 CLKOUT pin. The clock frequency for specified operation is 4.096 MHz. When the ADE7933/ADE7932 and the ADE7978 are used as a chipset, the ADE7933/ADE7932 must function synchronously with the ADE7978; therefore, the XTAL1 pin of the ADE7933/ADE7932 must be connected to the CLKOUT pin of the ADE7978. If the ADE7933/ADE7932 are used as standalone chips, a crystal with a maximum drive level of 0.5 mW and an ESR of 20 Ω can be connected across XTAL1 and XTAL2 to provide a clock source for the ADE7933/ADE7932. The clock frequency for specified operation is 4.096 MHz, but lower frequencies down to 3.6 MHz can be used. For more information, see the ADE7978 and ADE7933/ADE7932 Clocks section.
14	XTAL2	Leave this pin open when the ADE7933/ADE7932 are used with the ADE7978. If the ADE7933/ADE7932 are used as standalone chips, a crystal with a maximum drive level of 0.5 mW and an ESR of 20 Ω can be connected across XTAL1 and XTAL2 to provide a clock source for the ADE7933/ADE7932.
15	DATA	Data Output for Communication with the ADE7978. Connect the DATA pin to one of the following pins on the ADE7978: DATA_A, DATA_B, DATA_C, or DATA_N. Connect the DATA pin of the Phase A ADE7933/ADE7932 to the DATA_A pin of the ADE7978, and so on.
16	$\overline{\text{RESET\_EN}}$	Reset Input Enable, Active Low. The ADE7933/ADE7932 is reset by setting the $\overline{\text{RESET\_EN}}$ pin low and toggling the V2/$\overline{\text{TEMP}}$ pin four times with a frequency of 4.096 MHz. The reset ends when this pin and the V2/$\overline{\text{TEMP}}$ pin are set high (see the Hardware Reset section).
17	V2/$\overline{\text{TEMP}}$	This input pin selects the signal that is converted at the second voltage channel of the ADE7933. (In the ADE7932, the temperature sensor is always converted by the second voltage channel.) When this pin is high, the voltage input V2P is sensed; when this pin is low, the temperature sensor is measured. The V2/$\overline{\text{TEMP}}$ pin is also used during the ADE7933/ADE7932 reset procedure. For both the ADE7933 and ADE7932, the V2/$\overline{\text{TEMP}}$ pin must always be connected to one of the following pins on the ADE7978: VT_A, VT_B, VT_C, or VT_N. Connect the V2/$\overline{\text{TEMP}}$ pin of the Phase A ADE7933/ADE7932 to the VT_A pin of the ADE7978, and so on. For more information, see the Second Voltage Channel and Temperature Measurement section.

Pin No.	Mnemonic	Description
18	EMI_CTRL	Emissions Control Pin. This pin manages the emissions of the ADE7933/ADE7932. When the pin is connected to GND, the PWM control block of the dc-to-dc converter generates pulses during Slot 0, Slot 2, Slot 4, and Slot 6. When the pin is connected to VDD, the PWM control block of the dc-to-dc converter generates pulses during Slot 1, Slot 3, Slot 5, and Slot 7. (For more information, see the DC-to-DC Converter section.) Do not leave this pin floating.
19	VDD	Primary Supply Voltage. This pin provides the supply voltage for the ADE7933/ADE7932. For specified operation, maintain the supply voltage at 3.3 V ± 10%. Decouple this pin to GND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

Figure 12 through Figure 17 were generated using the following conditions: sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz; sinusoidal current with variable amplitudes from 100% of full scale down to 0.033% of full scale and with a frequency of 50 Hz; offset compensation executed.

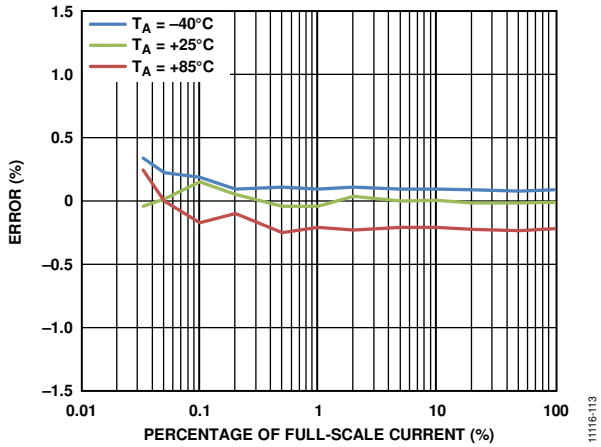

Figure 12. Total Active Energy Error as a Percentage of Reading over Temperature, PF = 1

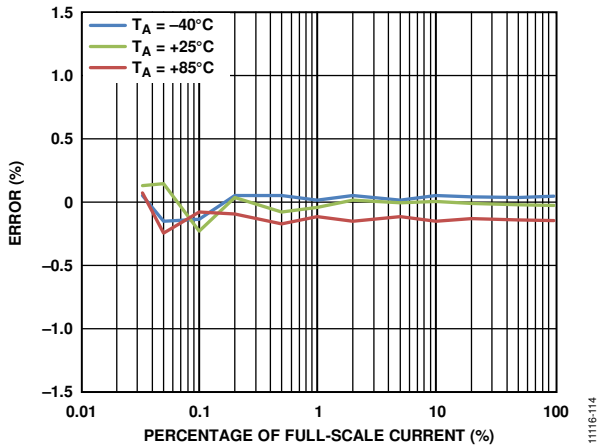

Figure 13. Total Reactive Energy Error as a Percentage of Reading over Temperature, PF = 0

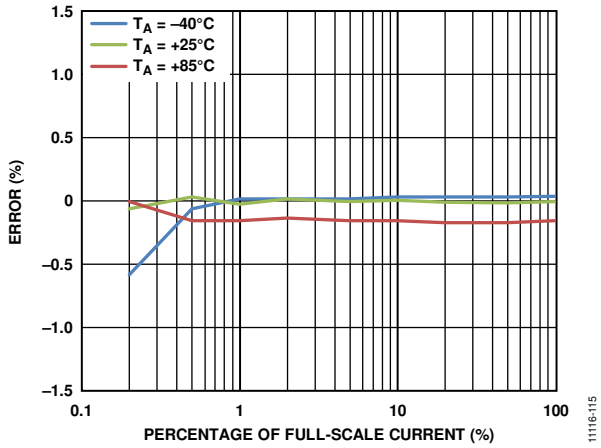

Figure 14. Apparent Energy Error as a Percentage of Reading over Temperature, PF = 1

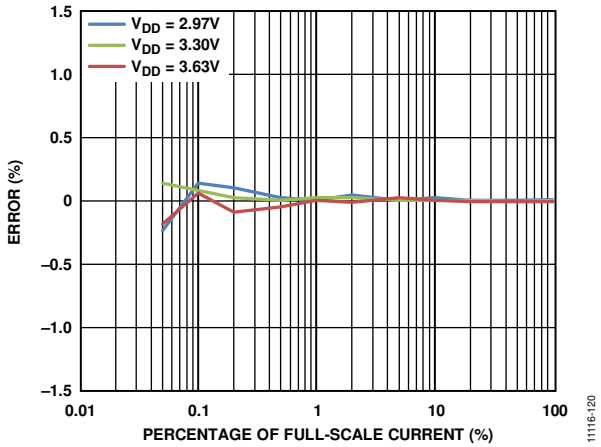

Figure 15. Total Active Energy Error as a Percentage of Reading over Power Supply, PF = 1, T_A = 25°C

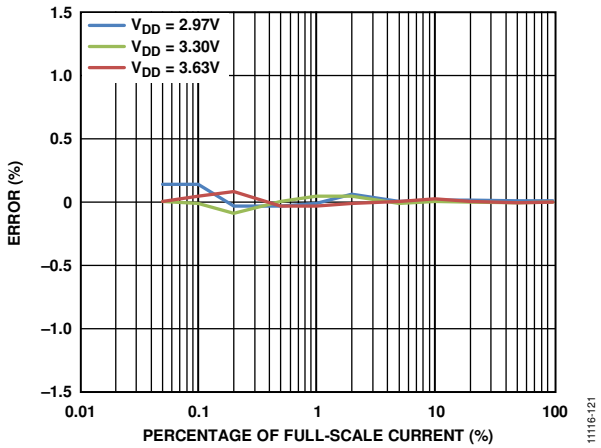

Figure 16. Total Reactive Energy Error as a Percentage of Reading over Power Supply, PF = 0, T_A = 25°C

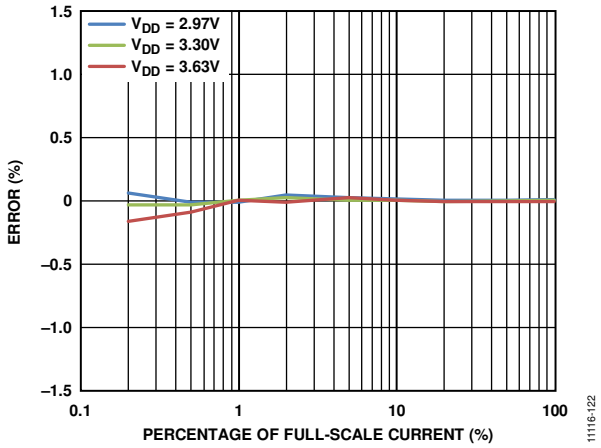

Figure 17. Apparent Energy Error as a Percentage of Reading over Power Supply, PF = 1, T_A = 25°C

Figure 18 through Figure 23 were generated using the following conditions: fundamental voltage component in phase with 5th harmonic; current with a 50 Hz component that has variable amplitudes from 100% of full scale down to 0.033% of full scale and a 5th harmonic with a constant amplitude of 17% of full scale; power factor equal to 1 or 0 on the fundamental and 5th harmonic. Figure 18, Figure 19, Figure 21, and Figure 22 were generated using a voltage with a 50 Hz component that has an amplitude of 50% of full scale and a 5th harmonic with an amplitude of 5% of full scale. Figure 20 and Figure 23 were generated using a voltage with a 50 Hz component that has variable amplitudes from 100% of full scale down to 0.033% of full scale and a 5th harmonic with an amplitude of 5% of full scale.

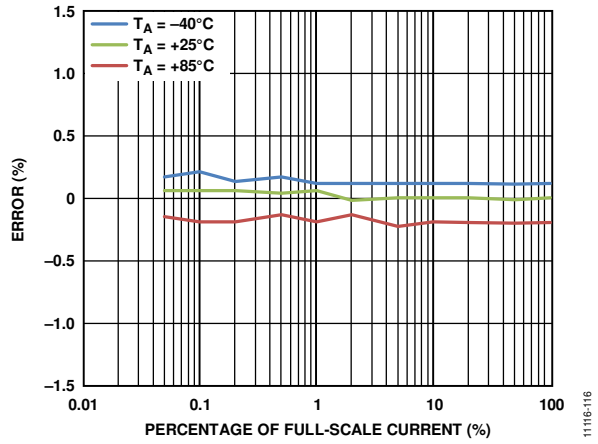

Figure 18. Fundamental Active Energy Error as a Percentage of Reading over Temperature, PF = 1

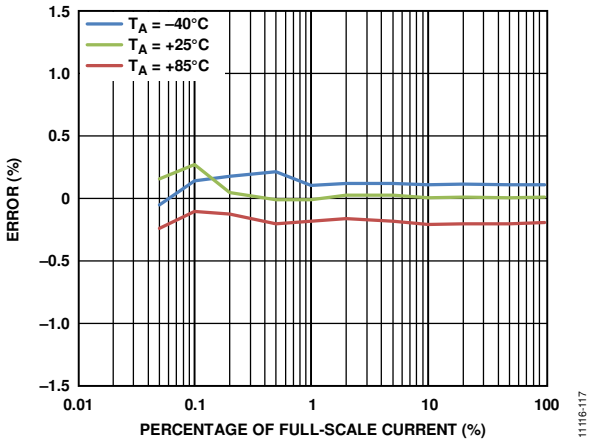

Figure 21. Fundamental Reactive Energy Error as a Percentage of Reading over Temperature, PF = 0

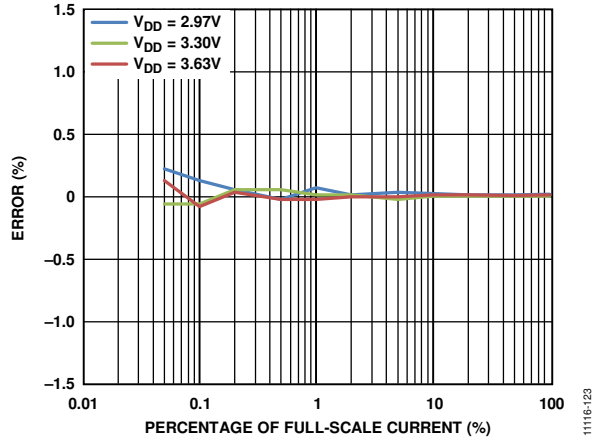

Figure 19. Fundamental Active Energy Error as a Percentage of Reading over Power Supply, PF = 1, T_A = 25°C

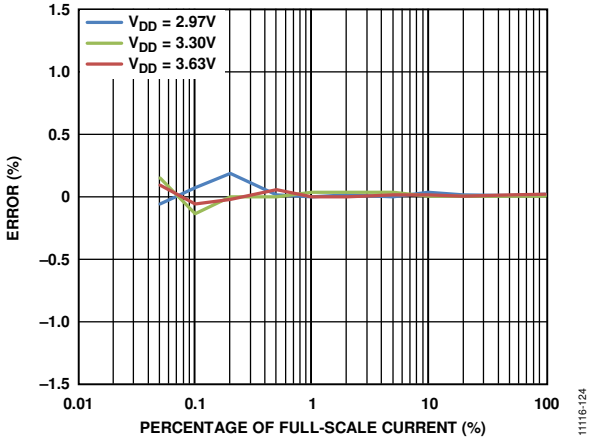

Figure 22. Fundamental Reactive Energy Error as a Percentage of Reading over Power Supply, PF = 0, T_A = 25°C

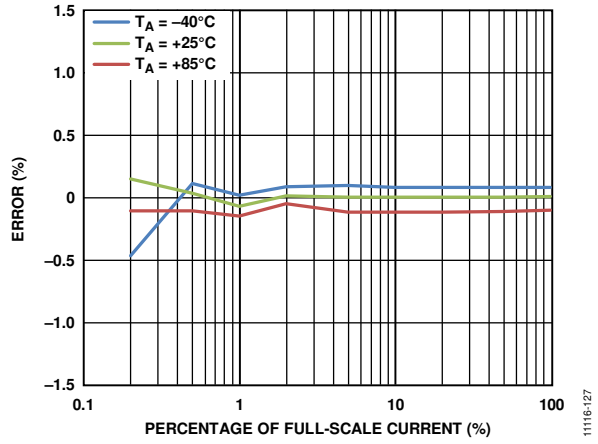

Figure 20. Fundamental Current RMS Error as a Percentage of Reading over Temperature, PF = 1

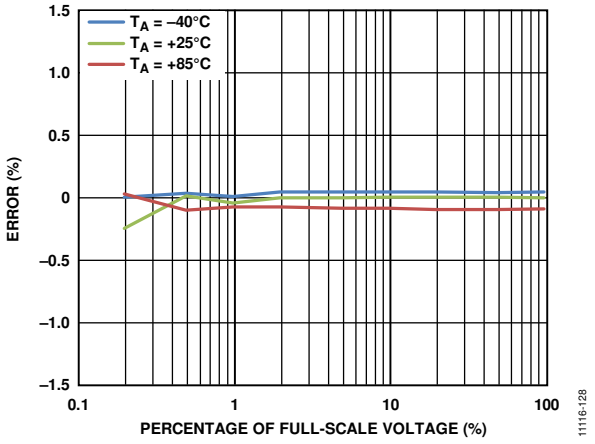

Figure 23. Fundamental Voltage RMS Error as a Percentage of Reading over Temperature, PF = 1

Figure 24 and Figure 25 were generated using the following conditions: sinusoidal voltage with a constant amplitude of 50% of full scale; sinusoidal current with a constant amplitude of 10% of full scale; variable frequency between 45 Hz and 65 Hz.

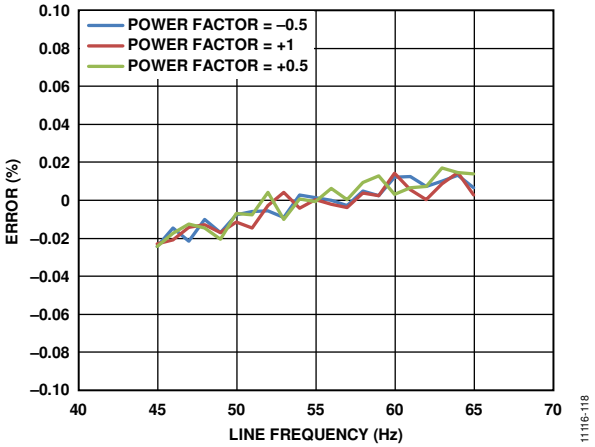

Figure 24. Total Active Energy Error as a Percentage of Reading over Frequency, PF = –0.5, +0.5, and +1

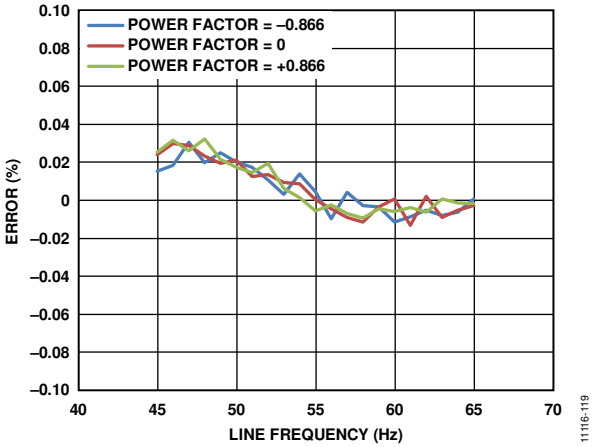

Figure 25. Total Reactive Energy Error as a Percentage of Reading over Frequency, PF = –0.866, 0, and +0.866

Figure 26 through Figure 29 were generated using the following conditions: sinusoidal current and voltage with variable amplitudes from 100% of full scale down to 0.033% of full scale. Figure 26 and Figure 28 were obtained using a frequency of 50 Hz; Figure 27 and Figure 29 were obtained using a variable frequency between 45 Hz and 65 Hz.

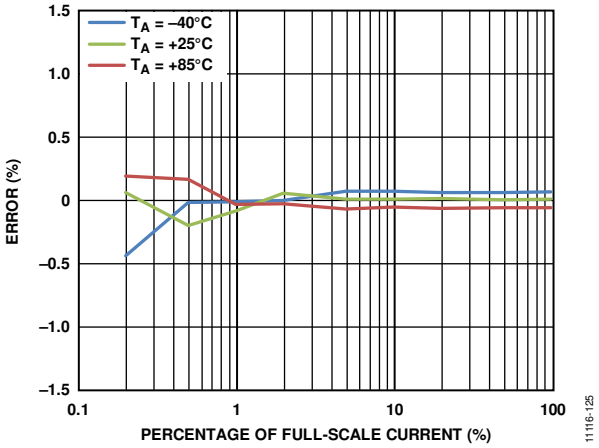

Figure 26. Current RMS Error as a Percentage of Reading over Temperature

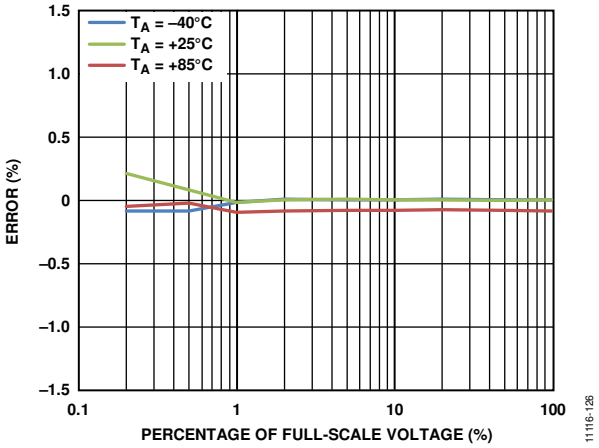

Figure 28. Voltage RMS Error as a Percentage of Reading over Temperature

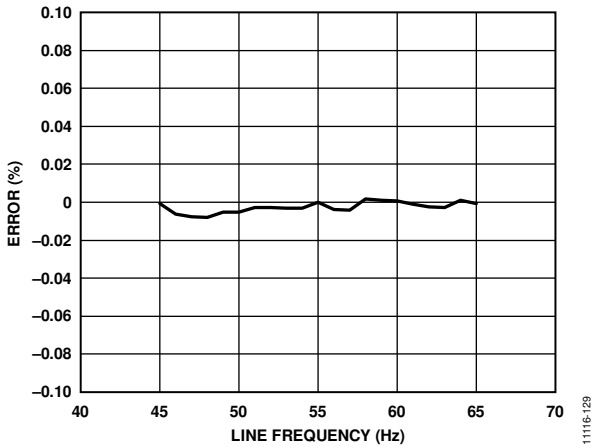

Figure 27. Current RMS Error as a Percentage of Reading over Frequency

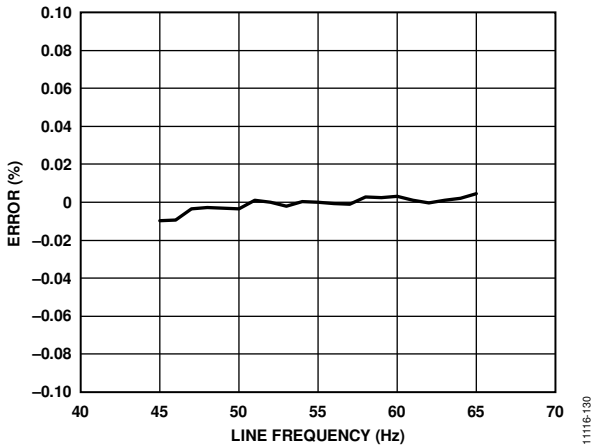

Figure 29. Voltage RMS Error as a Percentage of Reading over Frequency

Figure 30 through Figure 33 were generated using the following conditions: sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz; sinusoidal current with variable amplitudes from 100% of full scale down to 0.033% of full scale and with a frequency of 50 Hz; offset compensation executed. For Figure 31 and Figure 33, besides the fundamental component, the voltage contained a 5th harmonic with a constant amplitude of 5% of full scale, and the current contained a 5th harmonic with a constant amplitude of 17% of full scale. Measurements at 25°C were repeated 30 times, and the standard deviation values were extracted for current levels of 0.2% and 0.05% of full scale.

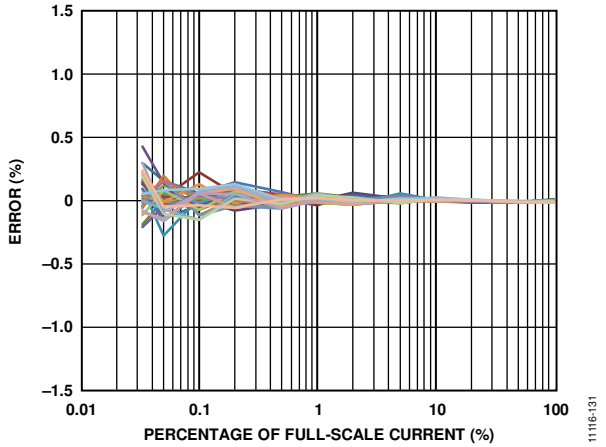

Figure 30. Total Active Energy Error as a Percentage of Reading, PF = 1 (Standard Deviation σ = 0.06% at 0.2% of Full-Scale Current and σ = 0.12% at 0.05% of Full-Scale Current)

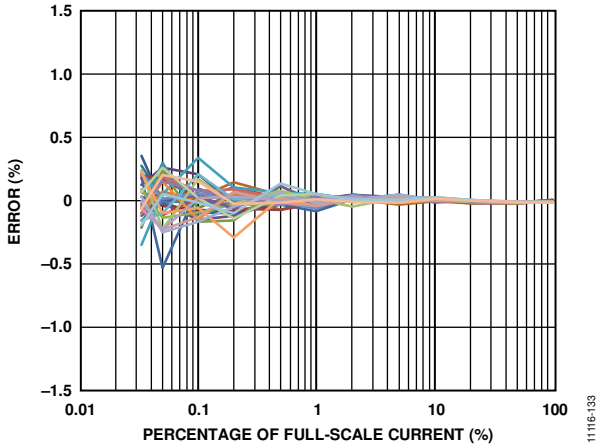

Figure 32. Total Reactive Energy Error as a Percentage of Reading, PF = 0 (Standard Deviation σ = 0.09% at 0.2% of Full-Scale Current and σ = 0.13% at 0.05% of Full-Scale Current)

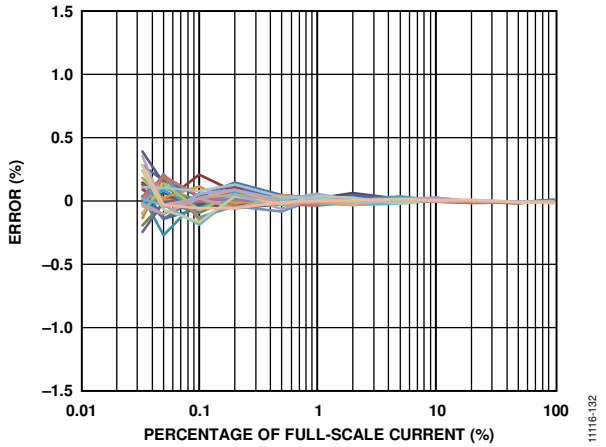

Figure 31. Fundamental Active Energy Error as a Percentage of Reading, PF = 1 (Standard Deviation σ = 0.06% at 0.2% of Full-Scale Current and σ = 0.11% at 0.05% of Full-Scale Current)

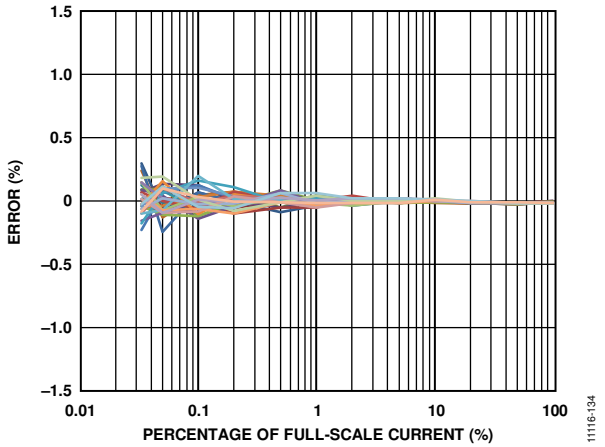

Figure 33. Fundamental Reactive Energy Error as a Percentage of Reading, PF = 0 (Standard Deviation σ = 0.06% at 0.2% of Full-Scale Current and σ = 0.13% at 0.05% of Full-Scale Current)