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High Performance, Multiphase Energy, and Power Quality Monitoring IC

Data Sheet

ADE9000

FEATURES

- 7 high performance ADCs
  - 101 dB SNR
  - Wide input voltage range: ±1 V, 707 mV rms FS at gain = 1
  - Differential inputs
- ±25 ppm/°C maximum channel drift (including ADC, internal VREF, PGA drift) enabling 10000:1 dynamic input range
  - Class 0.2 metrology with standard external components
- Power quality measurements
  - Enables implementation of IEC 61000-4-30 Class S
  - VRMS ½, IRMS ½ rms voltage refreshed each half cycle
  - 10 cycle rms/12 cycle rms
  - Dip and swell monitors
  - Line frequency—one per phase
  - Zero crossing, zero-crossing timeout
  - Phase angle measurements
- Supports CTs and Rogowski coil (di/dt) sensors
  - Multiple range phase/gain compensation for CTs
  - Digital integrator for Rogowski coils
- Flexible waveform buffer
  - Able to resample waveform to ensure 128 points per line cycle for ease of external harmonic analysis
  - Events, such as dip and swell, can trigger waveform storage
  - Simplifies data collection for IEC 61000-4-7 harmonic analysis
- Advanced metrology feature set
  - Total and fundamental active power, volt amperes reactive (VAR), volt amperes (VA), watthour, VAR hour, and VA hour
  - Total and fundamental IRMS, VRMS
  - Total harmonic distortion
  - Power factor
  - Supports active energy standards: IEC 62053-21 and IEC 62053-22; EN50470-3; OIML R46; and ANSI C12.20
  - Supports reactive energy standards: IEC 62053-23, IEC 62053-24
- High speed communication port: 20 MHz serial port interface (SPI)
- Integrated temperature sensor with 12-bit successive approximation register (SAR) ADC
  - ±3°C accuracy from −40°C to +85°C

APPLICATIONS

- Energy and power monitoring
- Power quality monitoring
- Protective devices
- Machine health
- Smart power distribution units
- Polyphase energy meters

GENERAL DESCRIPTION

The ADE9000[1] is a highly accurate, fully integrated, multiphase energy and power quality monitoring device. Superior analog performance and a digital signal processing (DSP) core enable accurate energy monitoring over a wide dynamic range. An integrated high end reference ensures low drift over temperature with a combined drift of less than ±25 ppm/°C maximum for the entire channel including a programmable gain amplifier (PGA) and an analog-to-digital converter (ADC).

The ADE9000 offers complete power monitoring capability by providing total as well as fundamental measurements on rms, active, reactive, and apparent powers and energies. Advanced features such as dip and swell monitoring, frequency, phase angle, voltage total harmonic distortion (VTHD), current total harmonic distortion (ITHD), and power factor measurements enable implementation of power quality measurements. The ½ cycle rms and 10 cycle rms/12 cycle rms, calculated according to IEC 61000-4-30 Class S, provide instantaneous rms measurements for real-time monitoring.

The ADE9000 offers an integrated flexible waveform buffer that stores samples at a fixed data rate of 32 kSPS or 8 kSPS, or a sampling rate that varies based on line frequency to ensure 128 points per line cycle. Resampling simplifies fast Fourier transform (FFT) calculation of at least 50 harmonics in an external processor according to IEC 61000-4-7.

The ADE9000 simplifies the implementation of energy and power quality monitoring systems by providing tight integration of acquisition and calculation engines. The integrated ADCs and DSP engine calculate various parameters and provide data through user accessible registers or indicate events through interrupt pins. With seven dedicated ADC channels, the ADE9000 can be used on a 3-phase system or up to three single-phase systems. It supports current transformers (CTs) or Rogowski coils for current measurements. A digital integrator eliminates a discrete integrator required for Rogowski coils.

The ADE9000 absorbs most complexity in calculations for a power monitoring system. With a simple host microcontroller, the ADE9000 enables the design of standalone monitoring or protection systems, or low cost nodes uploading data into the cloud.

Note that throughout this data sheet, multifunction pins, such as CF4/$\overline{\text{EVENT}}$/DREADY, are referred to either by the entire pin name or by a single function of the pin, for example, $\overline{\text{EVENT}}$, when only that function is relevant.

[1] Protected by U.S. Patents 8,350,558; 8,010,304. Other patents are pending.

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- ADE9000 Evaluation Board

DOCUMENTATION

Data Sheet

- ADE9000: High Performance, Multiphase Energy, and Power Quality Monitoring IC Data Sheet

Product Highlight

- ADE9000 Product Highlight

User Guides

- UG-1082: Evaluating the ADE9000 High Performance, Multiphase Energy, Power Quality Monitoring IC

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADE9000 Software Driver

TOOLS AND SIMULATIONS

- ADE9000 Calibration Tool

REFERENCE MATERIALS

Press

- Highly Integrated AFE for Power Quality Monitoring Saves Significant Design Time and Cost Versus Custom Development

DESIGN RESOURCES

- ADE9000 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

1/2017—Revision 0: Initial Version

TYPICAL APPLICATIONS CIRCUIT

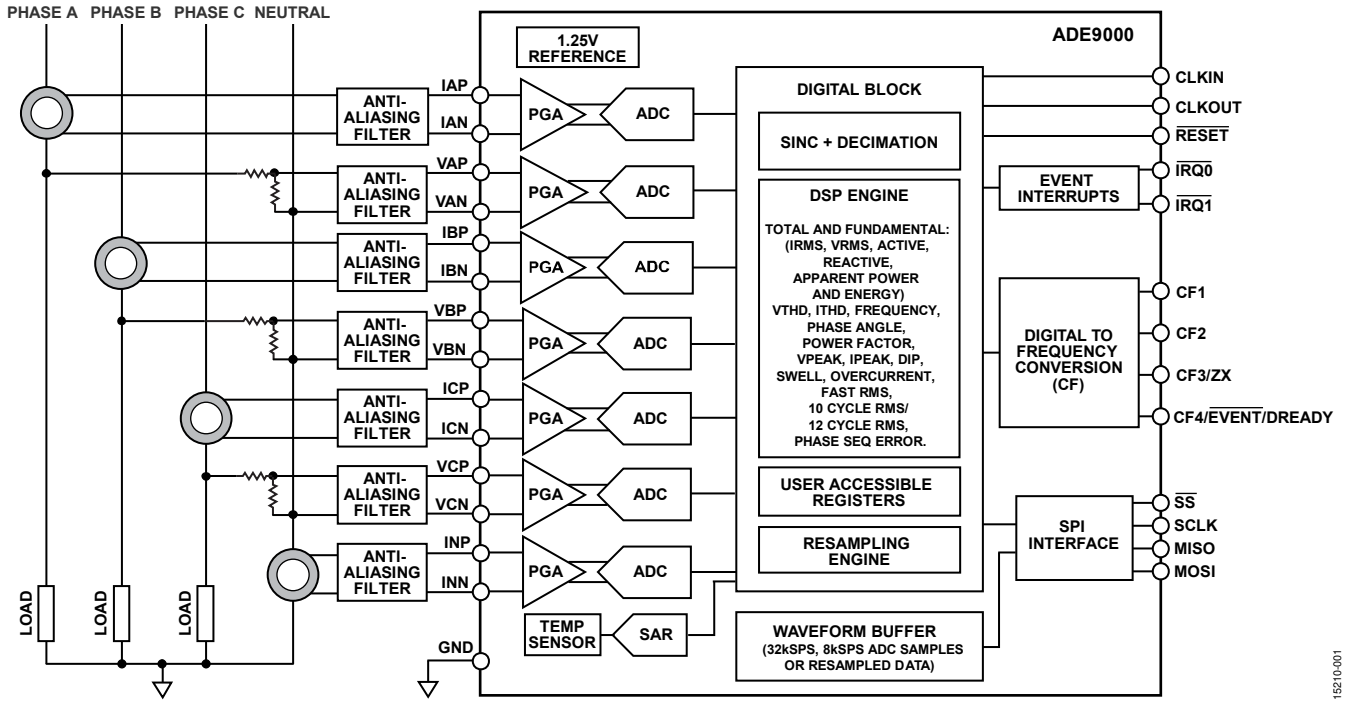

Figure 1.

SPECIFICATIONS

VDD = 2.97 V to 3.63 V, GND = AGND = DGND = 0 V, on-chip reference, CLKIN = 24.576 MHz crystal (XTAL), T_{MIN} to T_{MAX} = −40°C to +85°C, T_A = 25°C (typical), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY (MEASUREMENT ERROR PER PHASE)					
Total Active Energy		0.1		%	Over a dynamic range of 5000 to 1, 10 sec accumulation
		0.2		%	Over a dynamic range of 10,000 to 1, 20 sec accumulation
		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation, PGA = 4, integrator on, high-pass filter (HPF) corner = 4.98 Hz
		0.2		%	Over a dynamic range of 5000 to 1, 10 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
Total Reactive Energy		0.1		%	Over a dynamic range of 5000 to 1, 10 sec accumulation
		0.2		%	Over a dynamic range of 10,000 to 1, 20 sec accumulation
		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.2		%	Over a dynamic range of 5000 to 1, 10 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
Total Apparent Energy		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation
		0.5		%	Over a dynamic range of 5000 to 1, 10 sec accumulation
		0.1		%	Over a dynamic range of 500 to 1, 1 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.5		%	Over a dynamic range of 1000 to 1, 2 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
Fundamental Active Energy		0.1		%	Over a dynamic range of 5000 to 1, 2 sec accumulation
		0.2		%	Over a dynamic range of 10,000 to 1, 10 sec accumulation
		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.2		%	Over a dynamic range of 5000 to 1, 10 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
Fundamental Reactive Energy		0.1		%	Over a dynamic range of 5000 to 1, 2 sec accumulation
		0.2		%	Over a dynamic range of 10,000 to 1, 10 sec accumulation
		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.2		%	Over a dynamic range of 5000 to 1, 10 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Fundamental Apparent Energy		0.1		%	Over a dynamic range of 5000 to 1, 2 sec accumulation
		0.5		%	Over a dynamic range of 10,000 to 1, 10 sec accumulation
		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.5		%	Over a dynamic range of 5000 to 1, 10 sec accumulation, PGA = 4, integrator on, HPF corner = 4.98 Hz
IRMS, VRMS		0.1		%	Over a dynamic range of 1000 to 1
		0.5		%	Over a dynamic range of 5000 to 1
		0.1		%	Over a dynamic range of 500 to 1, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.5		%	Over a dynamic range of 1000 to 1, PGA = 4, integrator on, HPF corner = 4.98 Hz
Fundamental IRMS, VRMS		0.1		%	Over a dynamic range of 1000 to 1
		0.5		%	Over a dynamic range of 5000 to 1
		0.1		%	Over a dynamic range of 500 to 1, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.5		%	Over a dynamic range of 2000 to 1, PGA = 4, integrator on, HPF corner = 4.98 Hz
Active Power, VAR, VA		0.2		%	Over a dynamic range of 1000 to 1
		0.4		%	Over a dynamic range of, 3000 to 1
		0.2		%	Over a dynamic range of 500 to 1, PGA = 4, integrator on, HPF corner = 4.98 Hz
		0.5		%	Over a dynamic range of 1000 to 1, PGA = 4, integrator on, HPF corner = 4.98 Hz
Power Factor (PF) Error		±0.001		%	Over a dynamic range of 5000 to 1
128-Point per Line Cycle Resampled Data		0.1		%	An FFT is performed to receive the magnitude response; this error is the worst case error in the magnitude caused by resampling algorithm distortion; input signal is 50 Hz fundamental and ninth harmonic both at half of full scale (FS)
		−72		dB	Amplitude of highest spur; input signal is 50 Hz fundamental and ninth harmonic both at half of FS
		1.25		%	An FFT is performed to receive the magnitude response; this error is the worst case error in the magnitude caused by resampling algorithm distortion; input signal is 50 Hz fundamental and 31st harmonic, both at half of FS
		−38		dB	Amplitude of highest spur; input signal is 50 Hz fundamental and 31st harmonic, both at half of FS
VRMS½, IRMS½ RMS Voltage Refreshed Each Half-Cycle[1]		0.25		%	Data sourced before HPF, no dc offset at inputs, over a dynamic range of 100 to 1
10 Cycle/12 Cycle IRMS, VRMS[1]		0.2		%	Data sourced before HPF, no dc offset at inputs, over a dynamic range of 100 to 1
Line Period Measurement		0.001		Hz	Resolution at 50 Hz
Current to Current, Voltage to Voltage, and Voltage to Current Angle Measurement		0.018		Degrees	Resolution at 50 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC					
PGA Gain Settings (PGA_GAIN)		1, 2, or 4		V/V	PGA gain setting is referred to as PGA_GAIN
Differential Input Voltage Range (VxP to VxN, IxP to IxN)	−1/Gain		+1/Gain	V	707 mV rms, when V_{REF} = 1.25 V, this voltage corresponds to 53 million codes
Maximum Operating Voltage on Analog Input Pins (VxP, VxN, IxP, and IxN)	−0.6		+0.6	V	Voltage on the pin with respect to ground (GND = AGND = DGND = REFGND)
Signal-to-Noise Ratio (SNR)[2]					
PGA = 1		96		dB	32 kSPS, sinc4 output, V_{IN} = −0.5 dB from FS
		101		dB	8 kSPS, sinc4 + infinite impulse response (IIR), low-pass filter (LPF) output, V_{IN} = −0.5 dB from FS
PGA = 4		93		dB	32 kSPS, sinc4 output
		96		dB	8 kSPS, sinc4 + IIR LPF output
Total Harmonic Distortion (THD)[2]					
PGA = 1		−101	−95	dB	32 kSPS, sinc4 output, V_{IN} = −0.5 dB from FS
		−101	−95	dB	8 kSPS, sinc4 + IIR LPF output, V_{IN} = −0.5 dB from FS
PGA = 4		−107	−99	dB	32 kSPS, sinc4 output
		−107	−99	dB	8 kSPS, sinc4 + IIR LPF output
Signal-to-Noise and Distortion Ratio (SINAD)[2]					
PGA = 1		95		dB	32 kSPS, sinc4 output, V_{IN} = −0.5 dB from FS
		98		dB	8 kSPS, sinc4 + IIR LPF output, V_{IN} = −0.5 dB from FS
PGA = 4		93		dB	32 kSPS, sinc4 output
		96		dB	8 kSPS, sinc4 + IIR LPF output
Spurious-Free Dynamic Range (SFDR)[2]					
PGA = 1		100		dB	32 kSPS, sinc4 output, V_{IN} = −0.5 dB from FS
		100		dB	8 kSPS, sinc4 + IIR LPF output, V_{IN} = −0.5 dB from FS
Output Pass Band (0.1dB)					
Sinc4 Outputs		1.344		kHz	32 kSPS, sinc4 output
Sinc4 + IIR LPF Outputs		1.344		kHz	8 kSPS output
Output Bandwidth (−3 dB) [2]					
Sinc4 Outputs		7.2		kHz	32 kSPS, sinc4 output
Sinc4 + IIR LPF Outputs		3.2		kHz	8 kSPS output
Crosstalk[2]		−120		dB	At 50 Hz or 60 Hz, see the Terminology section
AC Power Supply Rejection Ratio (AC PSRR)[2]		−120		dB	At 50 Hz, see the Terminology section
Common-Mode Rejection Ratio (AC CMRR)[2]		115		dB	At 100 Hz and 120 Hz
Gain Error		±0.3	±1	%typ	See the Terminology section
Gain Drift[2]		±3		ppm/°C	See the Terminology section
Offset		±0.040	±3.8	mV	See the Terminology section
Offset Drift[2]		0	±2	µV/°C	See the Terminology section
Channel Drift (PGA, ADC, Internal Voltage Reference)		±7	±25	ppm/°C	PGA = 1, internal V_{REF}
		±7	±25	ppm/°C	PGA = 2, internal V_{REF}
		±7	±25	ppm/°C	PGA = 4, internal V_{REF}
Differential Input Impedance (DC)	165	185		kΩ	PGA = 1, see the Terminology section
	80	90		kΩ	PGA = 2
	40	45		kΩ	PGA = 4

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
INTERNAL VOLTAGE REFERENCE					Nominal = 1.25 V ± 1 mV
Voltage Reference		1.250		V	T_A = 25°C, REF pin
Temperature Coefficient[2]		±5	±20	ppm/°C	T_A = −40°C to +85°C, tested during device characterization
EXTERNAL VOLTAGE REFERENCE					
Input Voltage (REF)		1.2 or 1.25		V	REFGND must be tied to GND, AGND, and DGND, a 1.25 V external reference is preferred; the FS values mentioned in this data sheet are for a voltage reference of 1.25 V
Input Impedance		7.5		kΩ	
TEMPERATURE SENSOR					
Temperature Accuracy		±2		°C	−10°C to +40°C
		±3		°C	−40°C to +85°C
Temperature Readout Step Size			0.3	°C	
CRYSTAL OSCILLATOR					All specifications use CLKIN = 24.576 MHz ± 30 ppm
Input Clock Frequency	24.33	24.576	24.822	MHz	
Internal Capacitance on CLKIN, CLKOUT		4		pF	
Internal Feedback Resistance Between CLKIN and CLKOUT		2.45		MΩ	
Transconductance (g_m)	5	8		mA/V	
EXTERNAL CLOCK INPUT					
Input Clock Frequency	24.330	24.576	24.822	MHz	±1%
Duty Cycle[2]	45:55	50:50	55:45	%	
CLKIN Logic Input Voltage					3.3 V tolerant
High, V_{INH}	1.2			V	V_{DD} = 2.97 V to 3.63 V
Low, V_{INL}			0.5	V	V_{DD} = 2.97 V to 3.63 V
LOGIC INPUTS (PM0, PM1, $\overline{\text{RESET}}$, MOSI, SCLK, and $\overline{\text{SS}}$)					
Input Voltage					
V_{INH}	2.4			V	
V_{INL}			0.8	V	
Input Current, I_{IN}			15	µA	V_{IN} = 0 V
Internal Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
MISO, $\overline{\text{IRQ0}}$, and $\overline{\text{IRQ1}}$					
Output Voltage					
High, V_{OH}	2.4			V	I_{SOURCE} = 4 mA
Low, V_{OL}			0.8	V	I_{SINK} = 4 mA
Internal Capacitance, C_{IN}			10	pF	
C1, CF2, CF3, and CF4					
Output Voltage					
V_{OH}	2.4			V	I_{SOURCE} = 7 mA
V_{OL}			0.8	V	I_{SINK} = 8 mA
C_{IN}			10	pF	
LOW DROPOUT REGULATORS (LDOs)					
AVDD		1.9		V	
DVDD		1.7		V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					
V_{DD}	2.97	3.3	3.63	V	Power-on reset level is 2.4 V to 2.6 V
Supply Current (V_{DD})					
Power Save Mode 0 (PSM0)		15	17	mA	Normal mode
		14.5	16.5	mA	Normal mode, six ADCs enabled
Power Save Mode 3 (PSM3)		90	300	nA	Idle, V_{DD} = 3.3 V, AV_{DD} = 0 V, DV_{DD} = 0 V

[1] Enables implementation of IEC 61000-4-30 Class S.
[2] Tested during device characterization.

TIMING CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	10			ns
SCLK Frequency	f_{SCLK}			20	MHz
SCLK Low Pulse Width	t_{SL}	20			ns
SCLK High Pulse Width	t_{SH}	20			ns
Data Output Valid After SCLK Edge	t_{DAV}			20	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	10			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	10			ns
Data Output Fall Time	t_{DF}			10	ns
Data Output Rise Time	t_{DR}			10	ns
SCLK Fall Time	t_{SF}			10	ns
SCLK Rise Time	t_{SR}			10	ns
MISO Disable Time After $\overline{SS}$ Rising Edge	t_{DIS}			100	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0			ns

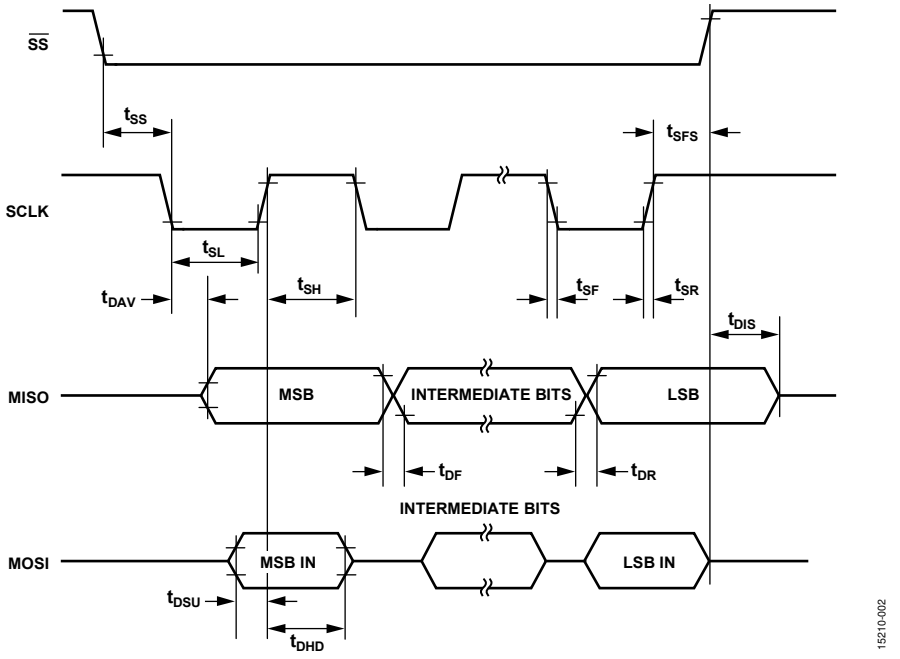

Figure 2. SPI Interface Timing Digram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
VDD to GND	−0.3 V to +3.96 V
Analog Input Voltage to GND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VAN, VBP, VBN, VCP, VCN	−2 V to +2 V
Reference Input Voltage to REFGND	−0.3 V to +2 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)[1]	260°C
ESD	
Human Body Model[2]	4 kV
Machine Model[3]	300 V
Field Induced Charged Device Model (FICDM)[4]	1.25 kV

[1] Analog Devices recommends that reflow profiles used in soldering RoHS compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.
[2] Applicable standard: ANSI/ESDA/JEDEC JS-001-2014.
[3] Applicable standard: JESD22-A115-A (ESD machine model standard of JEDEC).
[4] Applicable standard: JESD22-C101F (ESD FICDM standard of JEDEC).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} and θ_{JC} are specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-40-7[1]	27.14	3.13	°C/W

[1] The junction to air measurement uses a 2S2P JEDEC test board with 4 × 4 standard JEDEC vias. The junction to case measurement uses a 1S0P JEDEC test board with 4 × 4 standard JEDEC vias. See JEDEC standard JESD51-2.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

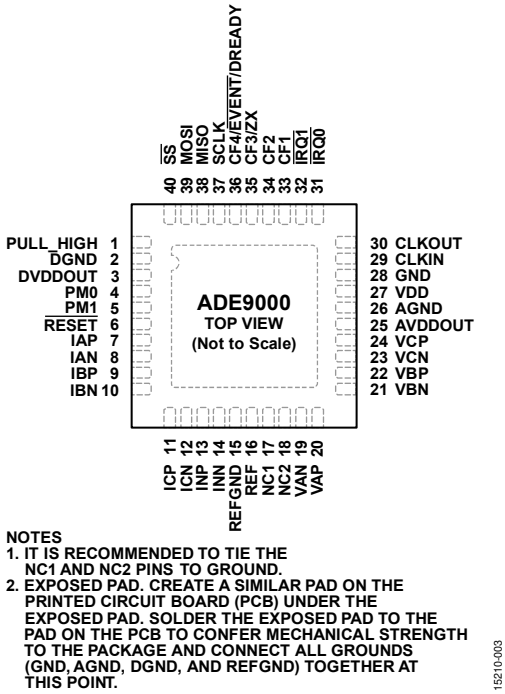

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PULL_HIGH	Pull High. Tie this pin to VDD.
2	DGND	Digital Ground. This pin provides the ground reference for the digital circuitry in the ADE9000. Because the digital return currents in the ADE9000 are small, it is acceptable to connect this pin to the analog ground plane of the whole system. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
3	DVDDOUT	1.8 V Output of the Digital Low Dropout Regulator (LDO). Decouple this pin with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor.
4	PM0	Power Mode Pin 0. PM0, combined with PM1, defines the power mode. For normal operation, ground PM0 and PM1.
5	PM1	Power Mode Pin 1. PM1 combined with PM0, defines the power mode. For normal operation, ground PM0 and PM1.
6	$\overline{\text{RESET}}$	Reset Input, Active Low. This pin must stay low for at least 1 µs to trigger a hardware reset.
7, 8	IAP, IAN	Analog Inputs, Channel IA. The IAP (positive) and IAN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
9, 10	IBP, IBN	Analog Inputs, Channel IB. The IBP (positive) and IBN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
11, 12	ICP, ICN	Analog Inputs, Channel IC. The ICP (positive) and ICN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
13, 14	INP, INN	Analog Inputs, Channel IN. The INP (positive) and INN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
15	REFGND	Ground Reference, Internal Voltage Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
16	REF	Voltage Reference. The REF pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.25 V. An external reference source of 1.2 V to 1.25 V can also be connected at this pin. In either case, decouple REF to REFGND with 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor. After reset, the on-chip reference is enabled. To use the internal voltage reference with external circuits, a buffer is required.
17	NC1	No Connection. It is recommended to tie this pin to ground.
18	NC2	No Connection. It is recommended to tie this pin to ground.

Pin No.	Mnemonic	Description
19, 20	VAN, VAP	Analog Inputs, Channel VA. The VAP (positive) and VAN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
21, 22	VBN, VBP	Analog Inputs, Channel VB. The VBP (positive) and VBN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
23, 24	VCN, VCP	Analog Inputs, Channel VC. The VCP (positive) and VCN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
25	AVDDOUT	1.9 V Output of the Analog Low Dropout Regulator (LDO). Decouple AVDDOUT with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor. Do not connect external active circuitry to this pin.
26	AGND	Analog Ground Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
27	VDD	Supply Voltage. The VDD pin provides the supply voltage. Decouple VDD to GND with a ceramic 0.1 µF capacitor in parallel with a 10 µF ceramic capacitor.
28	GND	Supply Ground Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
29	CLKIN	Crystal/Clock Input. Connect a crystal across CLKIN and CLKOUT to provide a clock source. Alternatively, an external clock can be provided at this logic input.
30	CLKOUT	Crystal Output. Connect a crystal across CLKIN and CLKOUT to provide a clock source. When using CLKOUT to drive external circuits, connect an external buffer.
31	$\overline{\text{IRQ0}}$	Interrupt Request Output. This pin is an active low logic output. See the Interrupts/Events section for information about events that trigger interrupts.
32	$\overline{\text{IRQ1}}$	Interrupt Request Output. This pin is an active low logic output. See the Interrupts/Events section for information about events that trigger interrupts.
33	CF1	Calibration Frequency (CF) Logic Output 1. The CF1, CF2, CF3, and CF4 outputs provide power information based on the CFxSEL bits in the CFMODE register. Use these outputs for operational and calibration purposes. Scale the full-scale output frequency by writing to the CFxDEN registers (see the Digital to Frequency Conversion—CFx Output section).
34	CF2	CF Logic Output 2. This pin indicates CF2.
35	CF3/ZX	CF Logic Output 3/Zero Crossing. This pin indicates CF3 or zero crossing.
36	CF4/$\overline{\text{EVENT}}$/DREADY	CF Logic Output 4/Event Pin/Data Ready. This pin indicates CF4, events, or when new data is ready.
37	SCLK	Serial Clock Input for the SPI Port. All serial data transfers synchronize to this clock (see the Accessing On-Chip Data section). The SCLK pin has a Schmitt trigger input for use with a clock source that has a slow edge transition time, for example, optoisolator outputs.
38	MISO	Data Output for the SPI Port.
39	MOSI	Data Input for the SPI Port.
40	$\overline{\text{SS}}$	Slave Select for the SPI Port.
	EPAD	Exposed Pad. Create a similar pad on the printed circuit board (PCB) under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package and connect all grounds (GND, AGND, DGND, and REFGND) together at this point.

TYPICAL PERFORMANCE CHARACTERISTICS

ENERGY LINEARITY OVER SUPPLY AND TEMPERATURE

Total energies obtained from a sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz, a sinusoidal current with variable amplitudes from 100% of full scale down to 0.01% or 0.02% of full scale, a frequency of 50 Hz, and the integrator off. Fundamental energies obtained with a fundamental voltage component, with an amplitude of 50% of full scale in phase with a fifth harmonic, a current with a 50 Hz component that has variable amplitudes from 100% of full scale down to 0.01% of full scale, a fifth harmonic with a constant amplitude of 40% of fundamental, and the integrator off, unless otherwise noted.

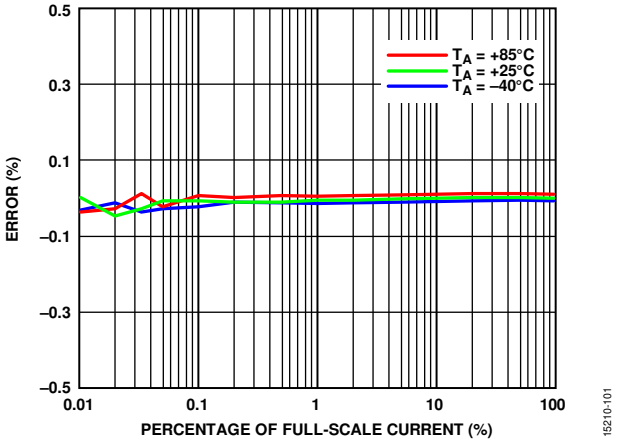

Figure 4. Total Active Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1

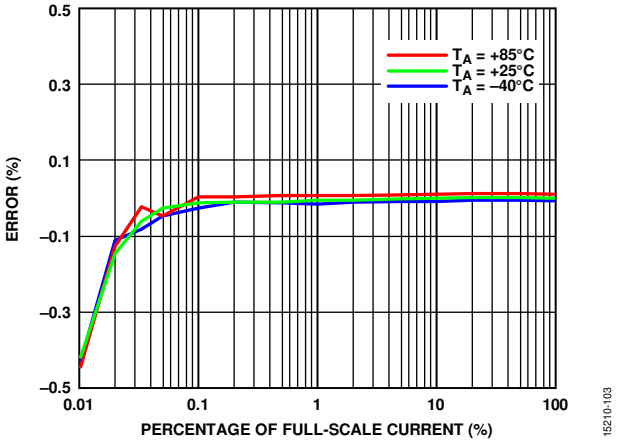

Figure 6. Total Apparent Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1

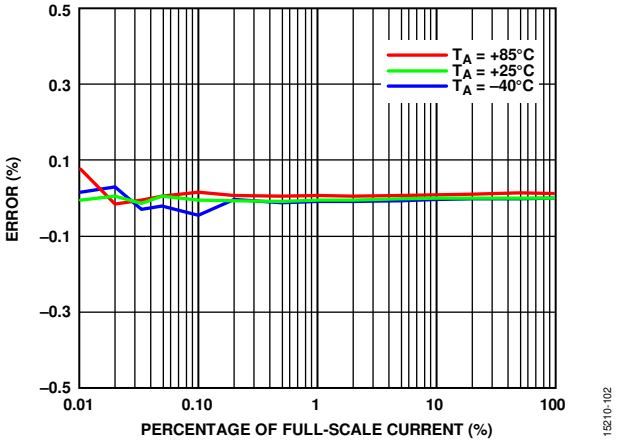

Figure 5. Total Reactive Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 0

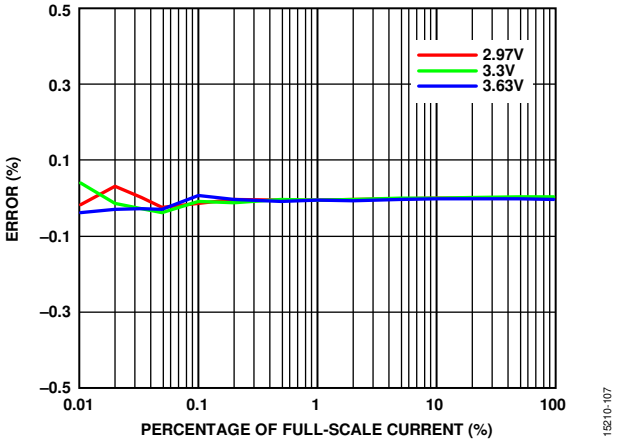

Figure 7. Total Active Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C

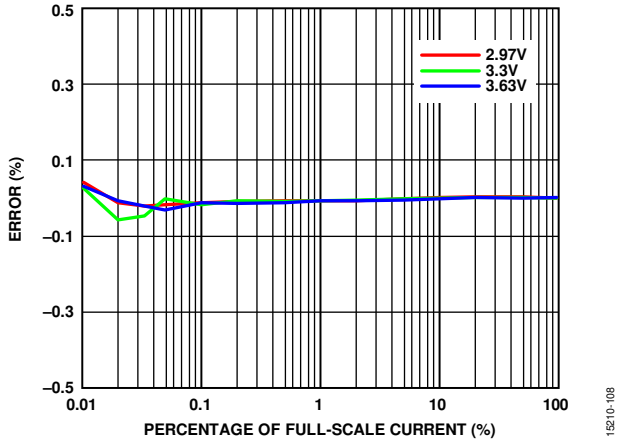

Figure 8. Total Reactive Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 0, T_A = 25°C

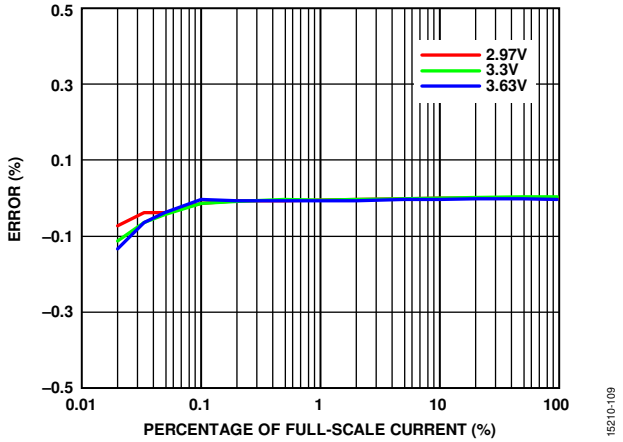

Figure 9. Total Apparent Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C

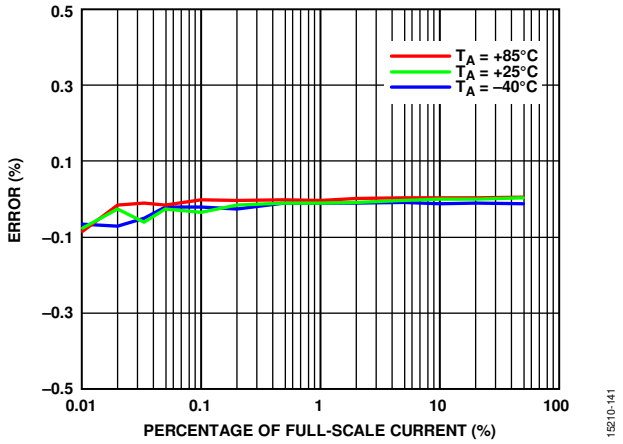

Figure 10. Fundamental Active Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1

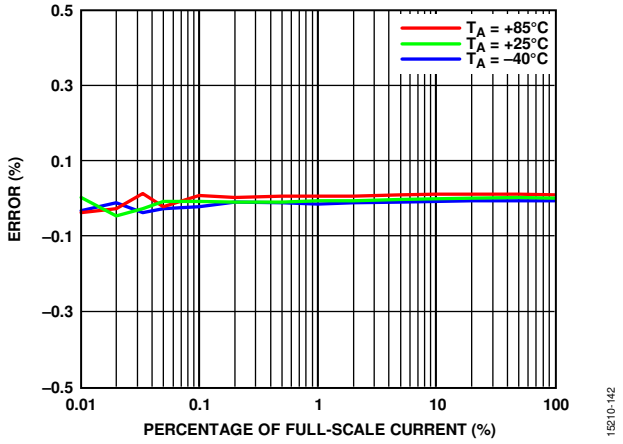

Figure 11. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 0

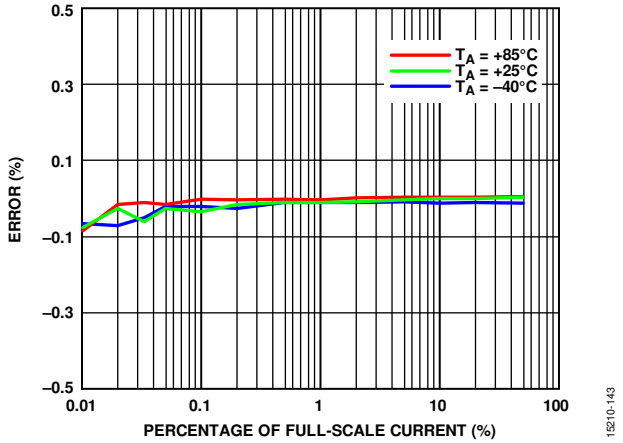

Figure 12. Fundamental Apparent Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1

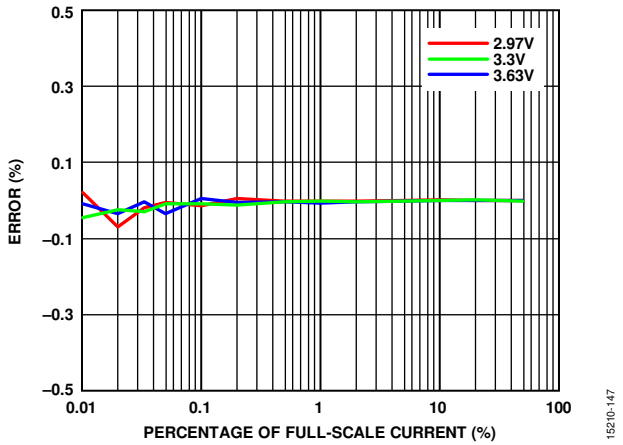

Figure 13. Fundamental Active Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C

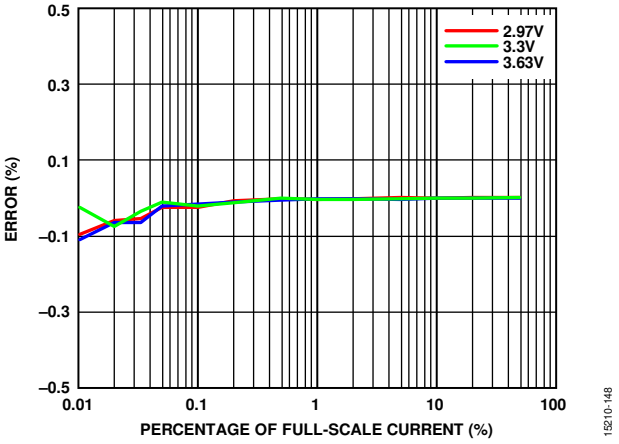

Figure 14. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 0, T_A = 25°C

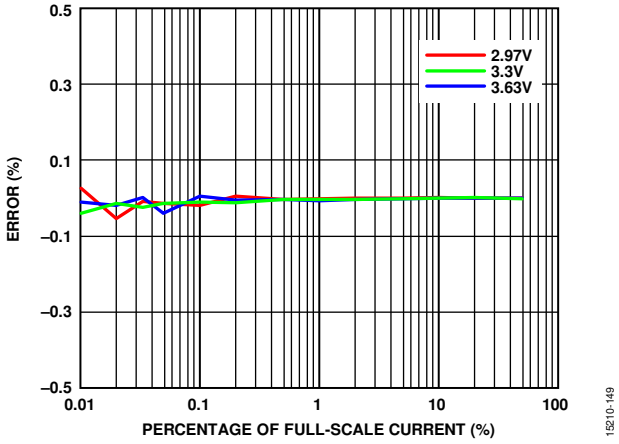

Figure 15. Fundamental Apparent Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C

ENERGY ERROR OVER FREQUENCY AND POWER FACTOR

Total energies obtained from a sinusoidal voltage with an amplitude of 50% of full scale, a sinusoidal current with a constant amplitude of 10% of full scale, a variable frequency between 45 Hz and 65 Hz, and the integrator off. Fundamental energies obtained with a fundamental voltage component, with an amplitude of 50% of full scale in phase with the fifth harmonic, a current with a 50 Hz component that has constant amplitude of 10% of full scale, a fifth harmonic with a constant amplitude of 40% of fundamental, and the integrator off, unless otherwise noted.

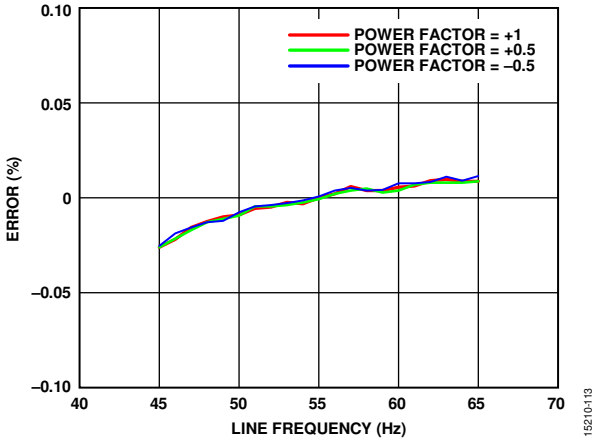

Figure 16. Total Active Energy Error vs. Line Frequency, Power Factor = −0.5, Power Factor = +0.5, and Power Factor = +1

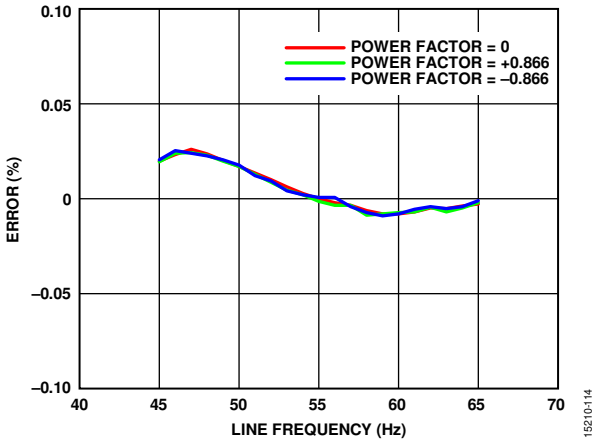

Figure 17. Total Reactive Energy Error vs. Line Frequency, Power Factor = −0.866, Power Factor = 0, and Power Factor = +0.866

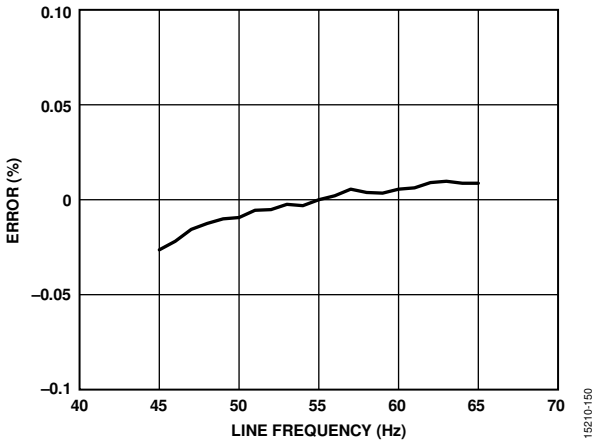

Figure 18. Total Apparent Energy Error vs. Line Frequency

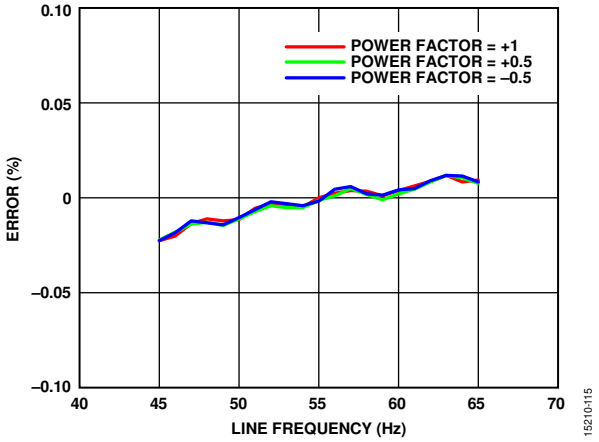

Figure 19. Fundamental Active Energy Error vs. Line Frequency, Power Factor = −0.5, Power Factor = +0.5, and Power Factor = +1

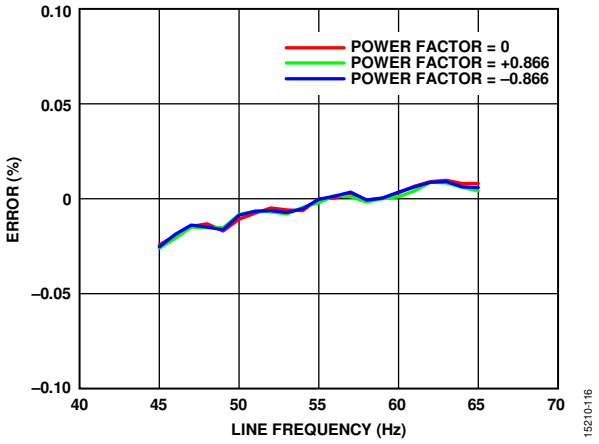

Figure 20. Fundamental Reactive Energy Error vs. Line Frequency, Power Factor = −0.866, Power Factor = 0, and Power Factor = +0.866

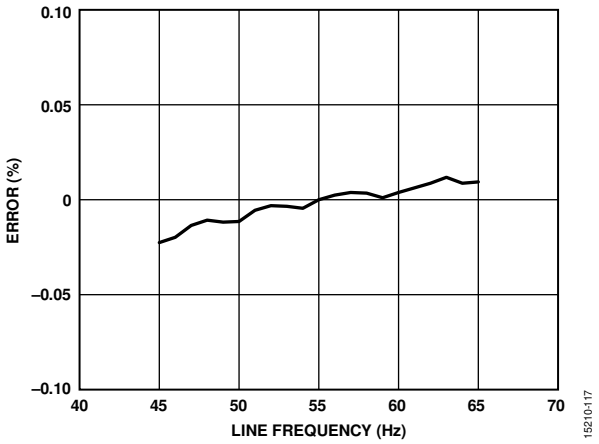

Figure 21. Fundamental Apparent Energy Error vs. Line Frequency

ENERGY LINEARITY REPEATABILITY

Total energies obtained from a sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz, a sinusoidal current with variable amplitudes from 100% of full scale down to 0.01% of full scale, a frequency of 50 Hz, and the integrator off. Fundamental energies obtained with a fundamental voltage component, with an amplitude of 50% of full scale in phase with the fifth harmonic, a current with a 50 Hz component that has variable amplitudes from 100% of full scale down to 0.01% of full scale, and a fifth harmonic with a constant amplitude of 40% of fundamental, and the integrator off. Measurements at 25°C repeated 30 times, unless otherwise noted.

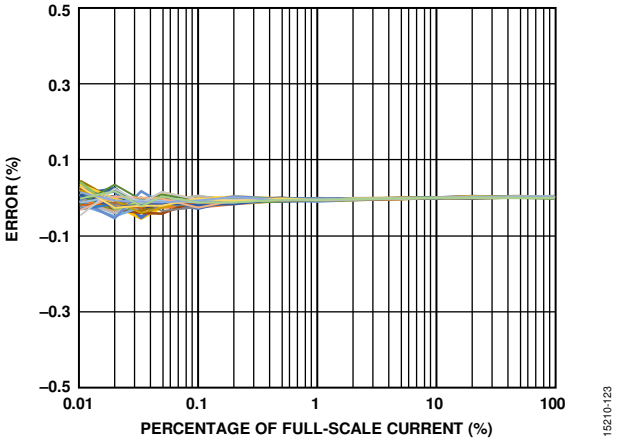

Figure 22. Total Active Energy Error as a Percentage of Full-Scale Current, Power Factor = 1 (Standard Deviation σ = 0.02% at 0.01% of Full-Scale Current)

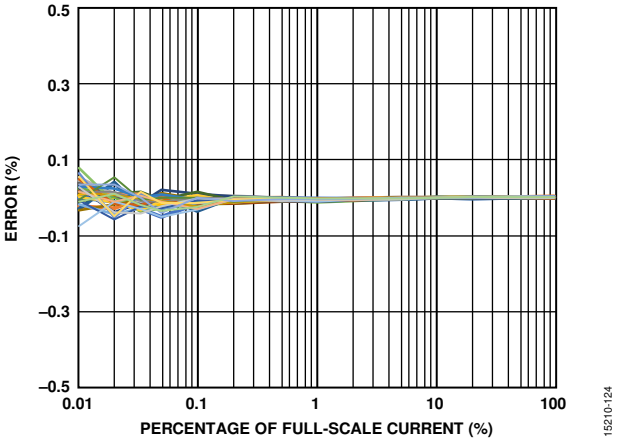

Figure 23. Total Reactive Energy Error as a Percentage of Full-Scale Current, Power Factor = 0 (Standard Deviation σ = 0.03% at 0.01% of Full-Scale Current)

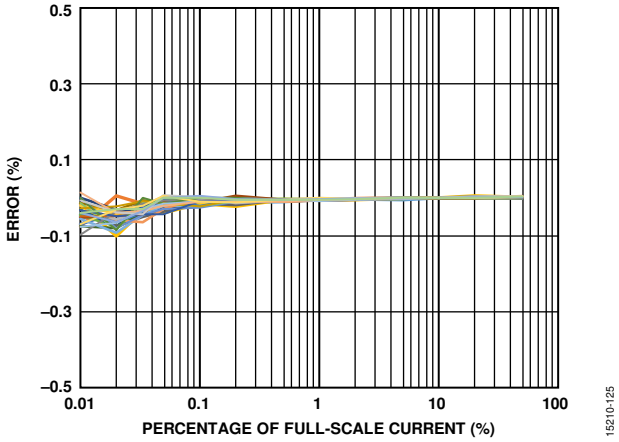

Figure 24. Fundamental Active Energy Error as a Percentage of Full-Scale Current, Power Factor = 1 (Standard Deviation σ = 0.03% at 0.01% of Full-Scale Current)

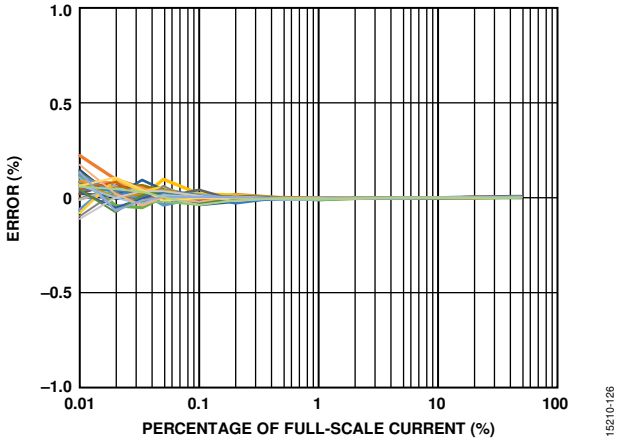

Figure 25. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current, Power Factor = 0 (Standard Deviation σ = 0.04% at 0.01% of Full-Scale Current)

RMS LINEARITY OVER TEMPERATURE AND RMS ERROR OVER FREQUENCY

RMS linearity obtained with a sinusoidal current and voltage with variable amplitudes from 100% of full scale down to 0.01% of full scale using a frequency of 50 Hz, total rms error over frequency obtained with a sinusoidal current amplitude of 10% of full scale and voltage amplitude of 50% of full scale, and the integrator off. Fundamental rms error over frequency obtained with a sinusoidal current amplitude of 10% of full scale, a voltage amplitude of 50% of full scale, a fifth harmonic with a constant amplitude of 40% of fundamental, and the integrator off, unless otherwise noted.

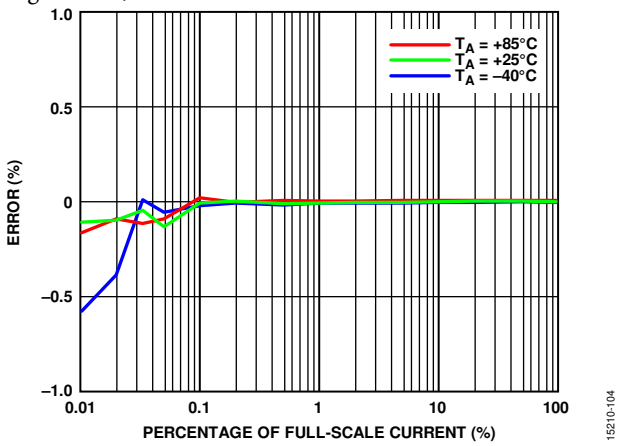

Figure 26. Current RMS Error as a Percentage of Full-Scale Current over Temperature

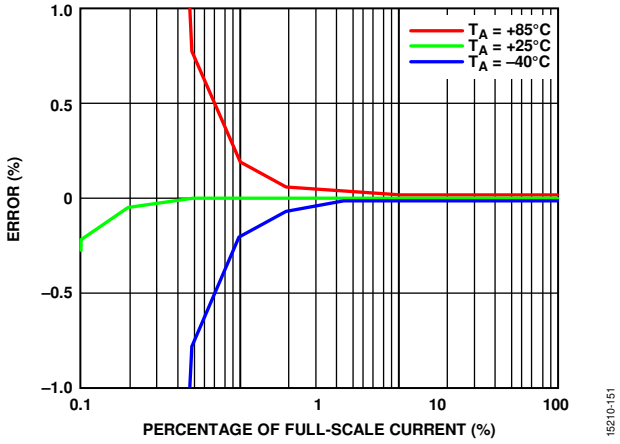

Figure 27. ½ Cycle Current RMS Error as a Percentage of Full-Scale Current over Temperature, Data Sourced Before High-Pass Filter and Calibrated for Offset, Register CONFIG0, Bit RMS_SRC_SEL = 1

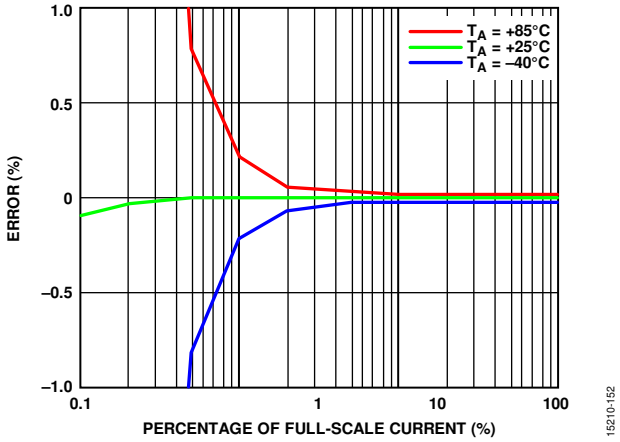

Figure 28. 10 Cycle Current RMS/12 Cycle Current Error as a Percentage of Full-Scale Current over Temperature, Data Sourced Before High-Pass Filter and Calibrated for Offset, Register CONFIG0, Bit RMS_SRC_SEL = 1

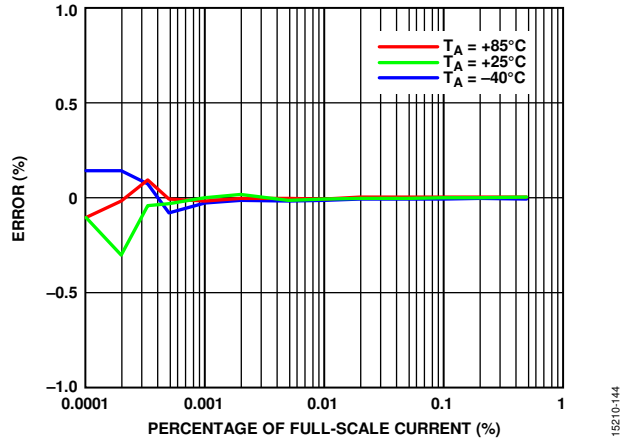

Figure 29. Fundamental Current RMS Error as a Percentage of Full-Scale Current over Temperature

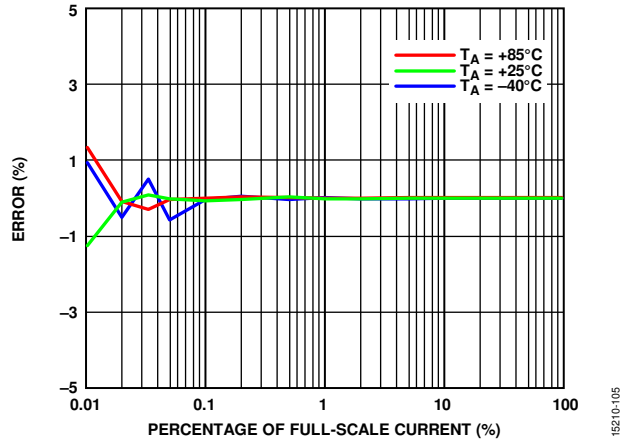

Figure 30. ½ Cycle Current RMS Error as a Percentage of Full-Scale Current over Temperature, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

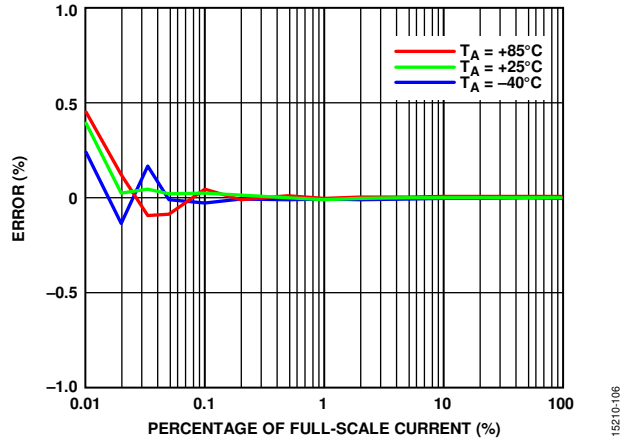

Figure 31. 10 Cycle Current RMS/12 Cycle Current Error as a Percentage of Full-Scale Current over Temperature, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

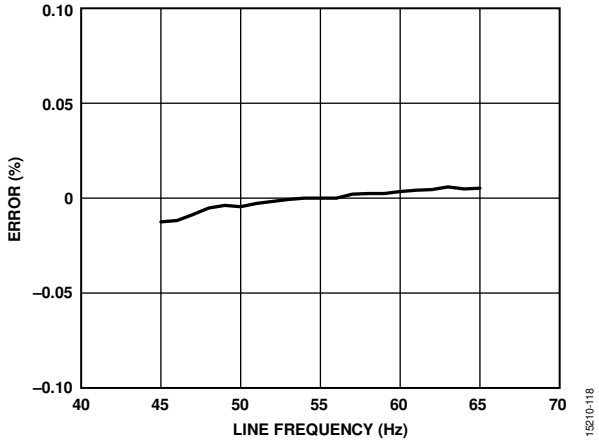

Figure 32. Current RMS Error vs. Line Frequency

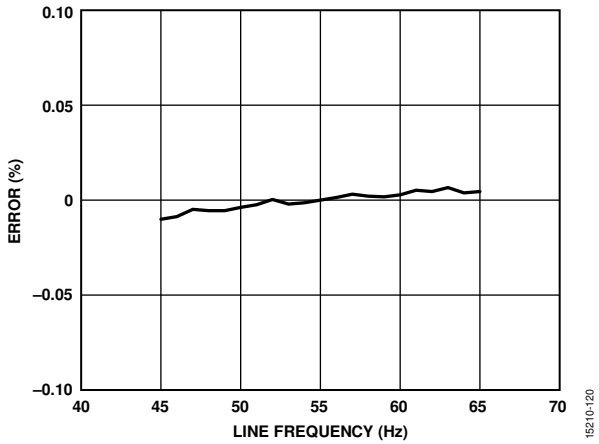

Figure 33. Fundamental Current RMS Error vs. Line Frequency

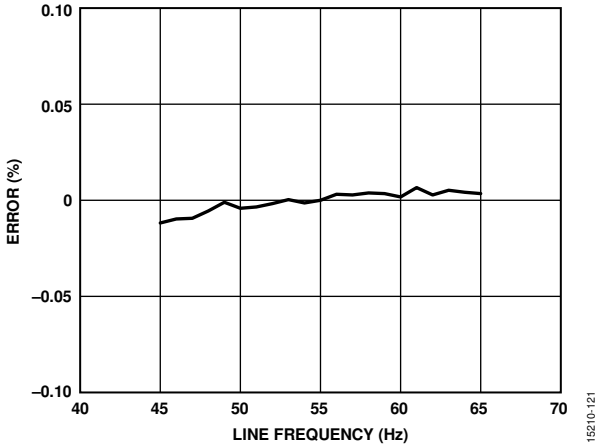

Figure 34. ½ Cycle Current RMS Error vs. Line Frequency, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

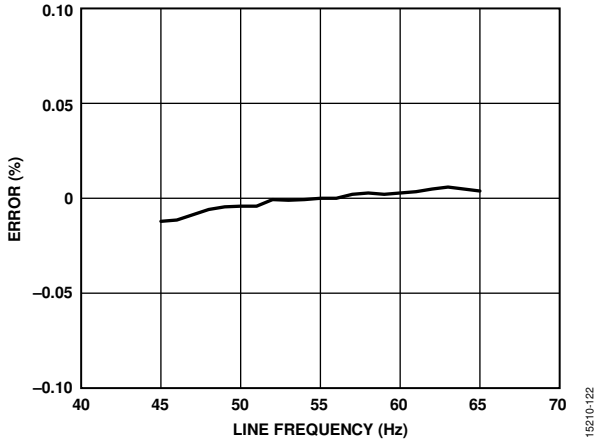

Figure 35. 10 Cycle Current RMS/12 Cycle Current Error vs. Line Frequency, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

ENERGY AND RMS LINEARITY WITH INTEGRATOR ON

The sinusoidal voltage has an amplitude of 50% of full scale and a frequency of 50 Hz, PGA_GAIN is a gain set to 4, the sinusoidal current has variable amplitudes from 100% of full scale down to 0.01% or 0.1% of full scale and a frequency of 50 Hz, full scale at gain of 4 = (full scale at gain of 1)/4, a high-pass corner frequency of 4.97 Hz, and T_A = 25°C, unless otherwise noted.

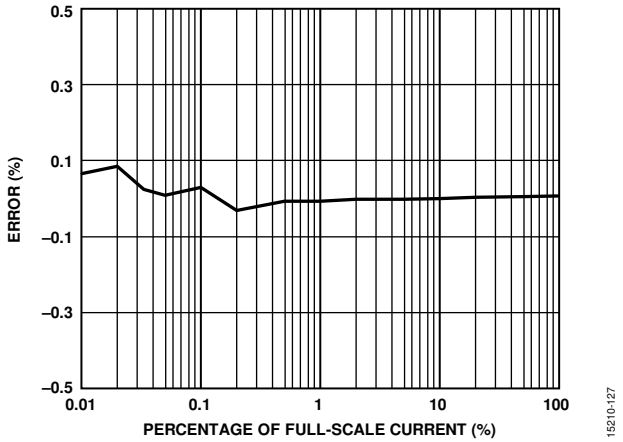

Figure 36. Total Active Energy Error, Gain = 4, Integrator On

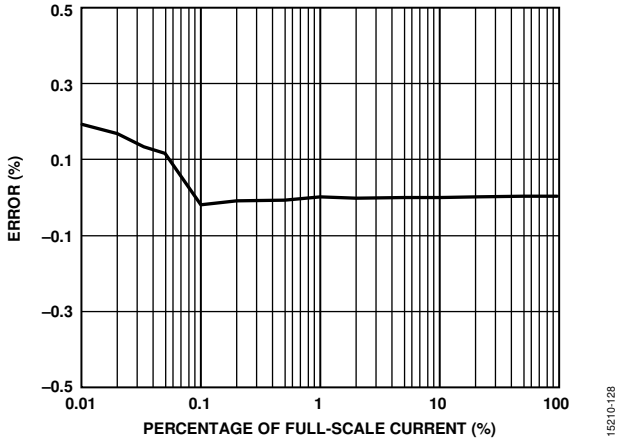

Figure 37. Total Reactive Energy Error, Gain = 4, Integrator On

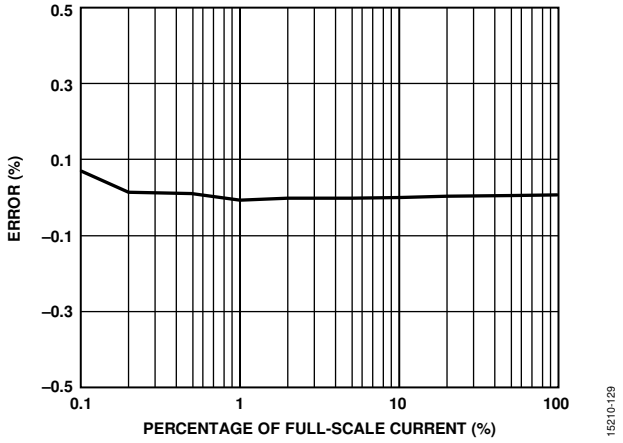

Figure 38. Total Apparent Energy Error, Gain = 4, Integrator On

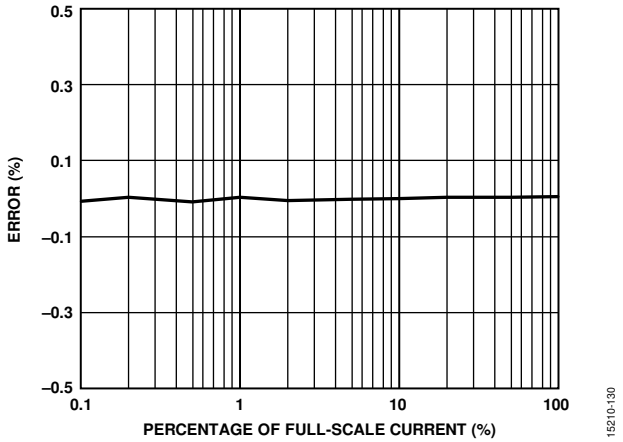

Figure 39. Total Current RMS Error, Gain = 4, Integrator On

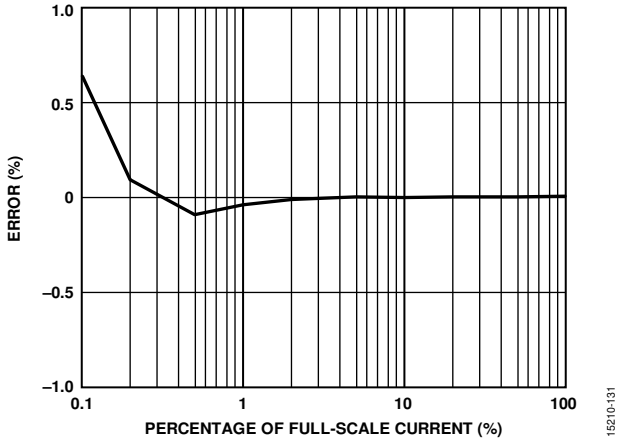

Figure 40. ½ Cycle Current RMS Error, Gain = 4, Integrator On, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

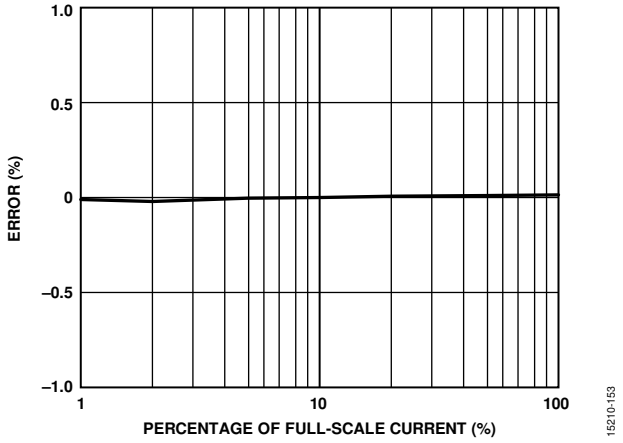

Figure 41. ½ Cycle Current RMS Error, Gain = 4, Integrator On, Data Sourced Before High-Pass Filter and Calibrated for Offset, Register CONFIG0, Bit RMS_SRC_SEL = 1

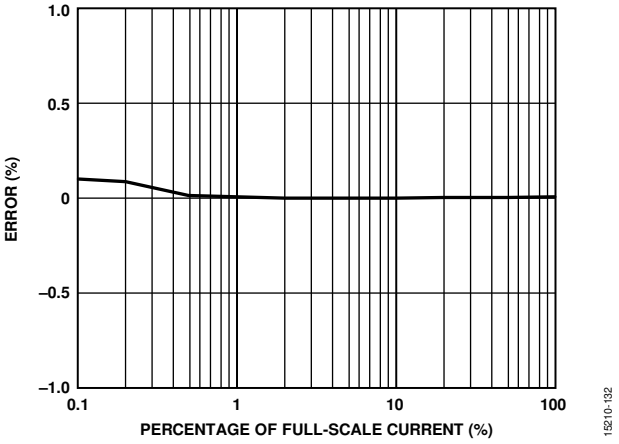

Figure 42. 10 Cycle Current RMS/12 Cycle Current Error, Gain = 4, Integrator On, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

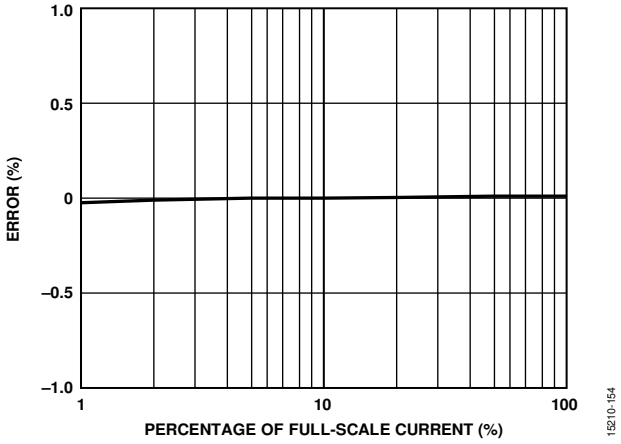

Figure 43. 10 Cycle Current RMS/12 Cycle Current RMS Error, Gain = 4, Integrator On, Data Sourced Before High-Pass Filter and Calibrated for Offset, Register CONFIG0, Bit RMS_SRC_SEL = 1

ENERGY AND RMS ERROR OVER FREQUENCY WITH INTEGRATOR ON

The sinusoidal voltage has a constant amplitude of 50% of full scale, PGA_GAIN is a gain set to 4, the sinusoidal current has a constant amplitude of 10% of full scale, and a variable frequency between 45 Hz and 65 Hz. Fundamental quantities obtained with a fundamental voltage component in phase with a fifth harmonic, a current with a fundamental component of 10% of full scale, a fifth harmonic with an amplitude of 40% of the fundamental, a full scale at gain of 4 = (full scale at gain of 1)/4, a high-pass corner frequency of 4.97 Hz, and T_A = 25°C, unless otherwise noted.

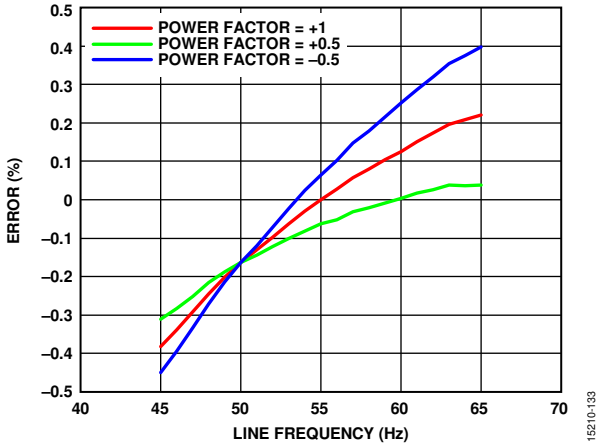

Figure 44. Total Active Energy Error vs. Line Frequency, Gain = 4, Integrator On, Power Factor = –0.5, Power Factor = +0.5, and Power Factor = +1

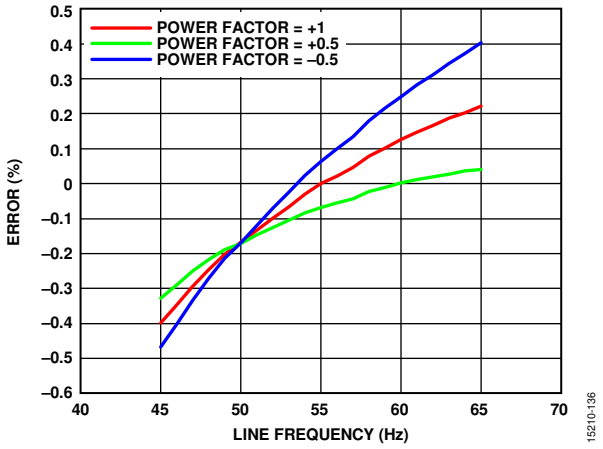

Figure 45. Fundamental Active Energy Error vs. Line Frequency, Gain = 4, Integrator On, Power Factor = –0.5, Power Factor = +0.5, and Power Factor = +1

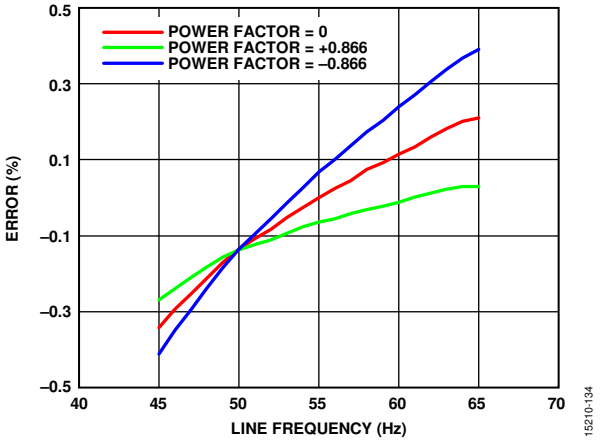

Figure 46. Total Reactive Energy Error vs. Line Frequency, Gain = 4, Integrator On, Power Factor = –0.866, Power Factor = +0.8665, and Power Factor = 0

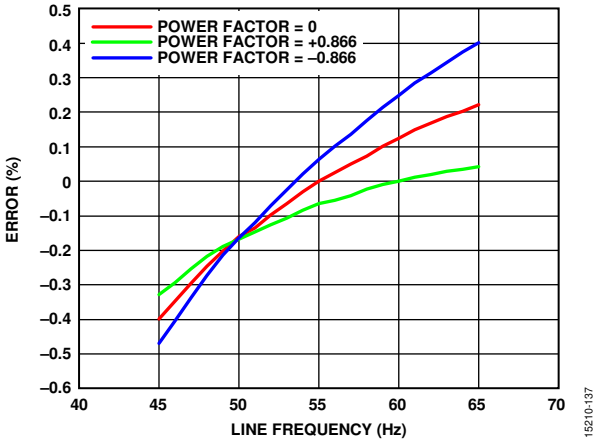

Figure 47. Fundamental Reactive Energy Error vs. Line Frequency, Gain = 4, Integrator On, Power Factor = –0.866, Power Factor = +0.8665, and Power Factor = 0

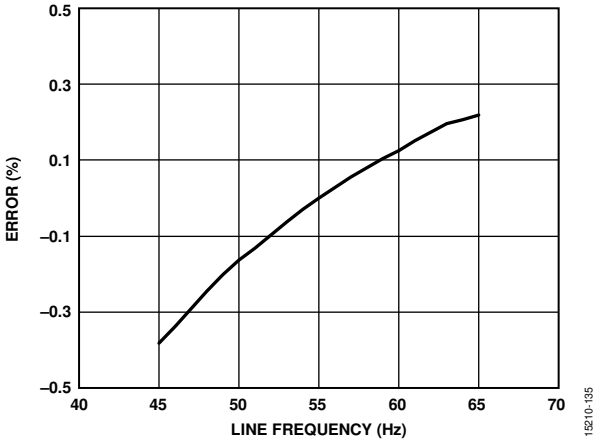

Figure 48. Total Apparent Energy Error vs. Line Frequency, Gain = 4, Integrator On

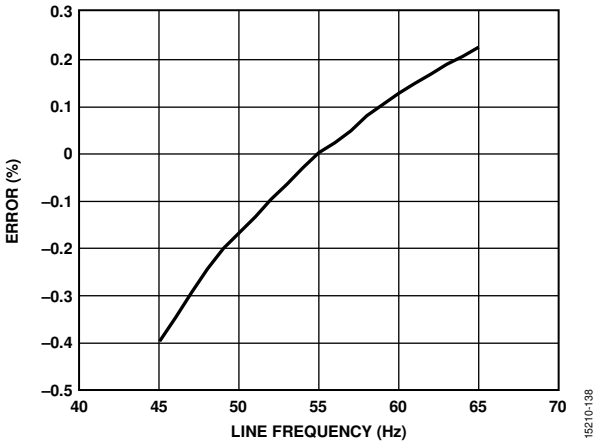

Figure 49. Fundamental Apparent Energy Error vs. Line Frequency, Gain = 4, Integrator On

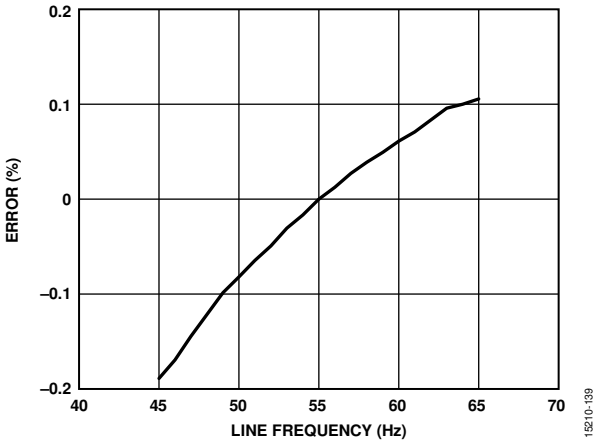

Figure 50. Current RMS Error vs. Line Frequency, Gain = 4, Integrator On

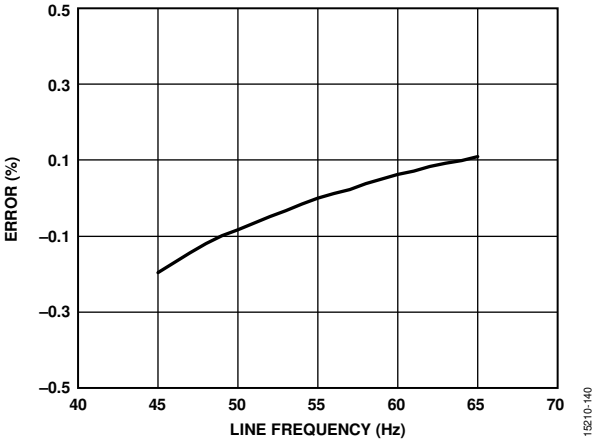

Figure 51. Fundamental Current RMS Error vs. Line Frequency, Gain = 4, Integrator On

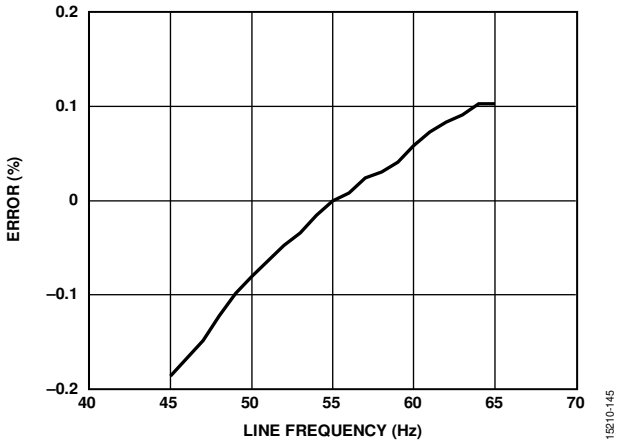

Figure 52. ½ Cycle Current RMS Error, Gain = 4, Integrator On, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

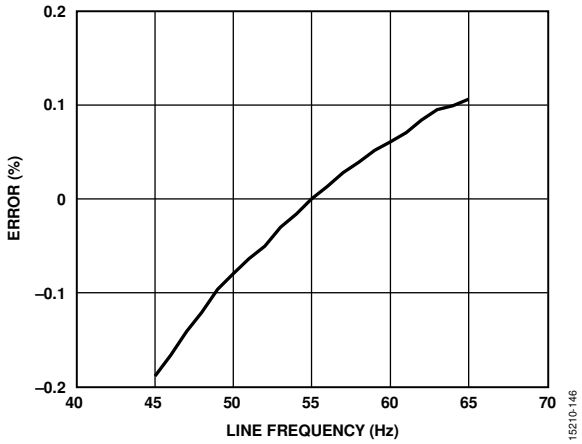

Figure 53. 10 Cycle Current RMS/12 Cycle Current Error, Gain = 4, Integrator On, Data Sourced After High-Pass Filter, Register CONFIG0, Bit RMS_SRC_SEL = 0

SIGNAL-TO-NOISE RATIO PERFORMANCE

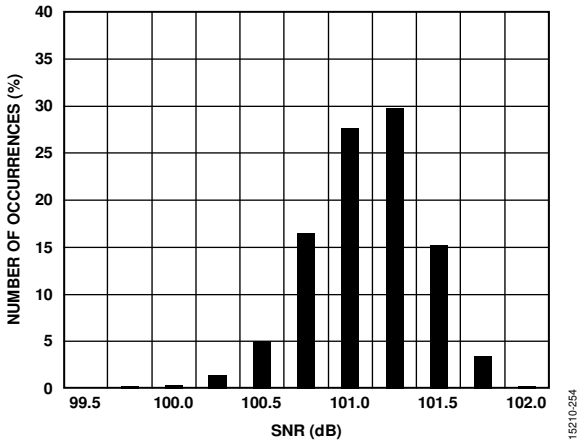

Figure 54. SNR Histogram of ADC SNR for 1000 Devices Tested at T_A = 25°C with PGA_GAIN = 1 and 8 kSPS Data Rate

TEST CIRCUIT

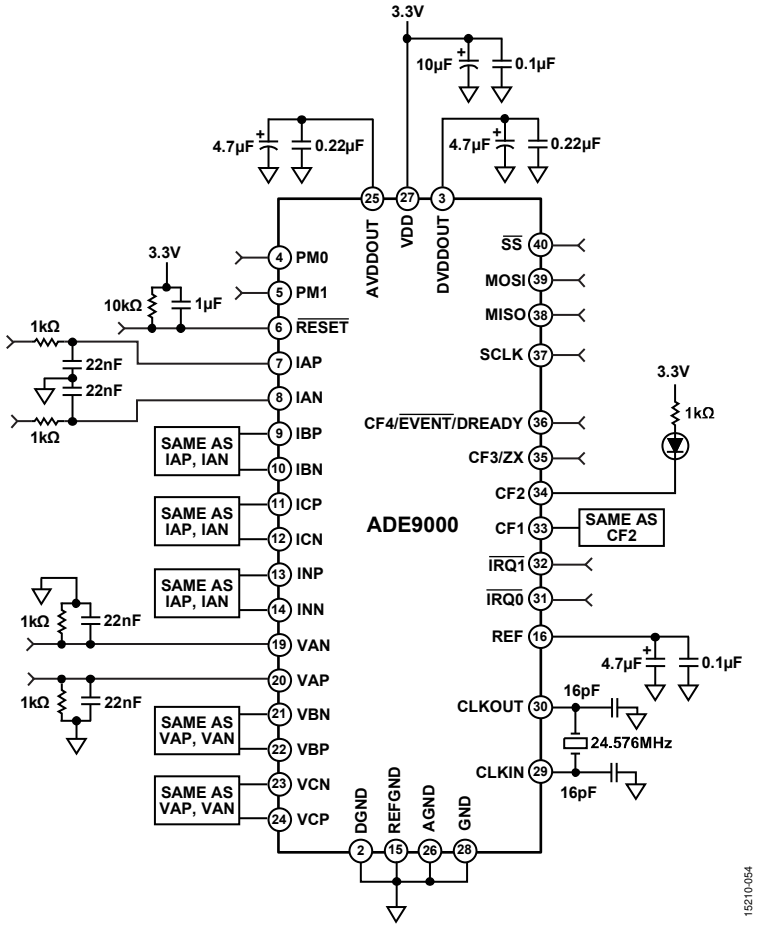

Figure 55. Test Circuit