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High Performance, Polyphase Energy Metering AFE

Data Sheet

ADE9078

FEATURES

- 7 high performance analog-to-digital converters (ADCs)
  - 101 dB signal-to-noise ratio (SNR)
  - 10,000:1 dynamic range
  - Wide input range: ±1 V, 0.707 V rms full scale
  - Differential inputs
- ±25 ppm/°C maximum channel temperature drift (including ADC, internal V_{REF}, and PGA drift) enabling Class 0.2 meters with standard external components
- Power quality measurements
  - Line frequency: 1 measurement per phase
  - Zero crossing detection, zero-crossing timeout
  - Phase angle measurements
- Supports current transformers (CTs) and Rogowski coil (di/dt) sensors
  - Multiple range phase/gain compensation for CTs
  - Digital integrator for Rogowski coils
- Flexible waveform buffer
  - Able to resample waveform to ensure 64 points per line cycle for ease of external harmonic analysis
  - Events can trigger waveform storage
  - Simplifies data collection for IEC 61000-4-7 harmonic analysis
- Advanced metrology feature set
  - Total active power, volt-amperes reactive (VAR), volt-amperes (VA), watthour, VAR-hour, and VA-hour
  - Fundamental VAR and VAR-hour
  - Current and voltage rms per phase (xIRMS, xVRMS)
  - Supports active energy standards: IEC 62053-21, IEC 62053-22; EN50470-3; OIML R46, ANSI C12.20
  - Supports reactive energy standards: IEC 62053-23, IEC 62053-4
- High speed communication port
- 10 MHz serial peripheral interface (SPI)

APPLICATIONS

- Polyphase meters
- Power quality monitoring
- Protective device

GENERAL DESCRIPTION

The ADE9078[1] is a highly accurate, fully integrated energy metering device. Interfacing with both current transformer (CT) and Rogowski coil sensors, the ADE9078 enables users to develop a 3-phase metrology platform, which achieves high performance for Class 1 up to Class 0.2 meters.

FUNCTIONAL BLOCK DIAGRAM

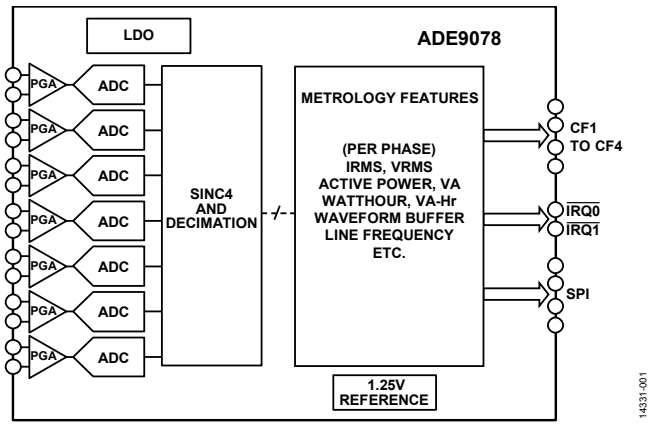

Figure 1.

The ADE9078 integrates seven high performances ADCs and a flexible DSP core. An integrated high end reference ensures low drift over temperature with a combined drift of less than ±25 ppm/°C maximum per channel, each of which includes a programmable gain amplifier (PGA) and ADC.

The ADE9078 offers an integrated flexible waveform buffer that stores samples at a fixed data rate or a sampling rate that varies based on line frequency to ensure 64 points per line cycle. These two options make it easy to implement harmonic analysis in an external processor according to IEC 61000-4-7.

Two power modes are provided to enable detection of meter tampering: PSM2 uses a low power comparator to compare current channels to a threshold and indicates whether it is exceeded on the $\overline{IRQ0}$ and $\overline{IRQ1}$ outputs; PSM1 enables fast measurement of current and voltage rms (xVRMS and xIRMS), active power, and VAR during a tamper.

The ADE9078 allows advanced and highly accurate energy measurements, enabling one platform to cover a wide range of meters, through a combination of various high end metrology features and superior analog performance.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329; 6,262,600; 7,489,526; 7,558,080. Other patents are pending.

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Last Content Update: 02/23/2017

COMPARABLE PARTS

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EVALUATION KITS

- ADE9078 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1415: ADE9078 Low Power Mode for No Voltage Detection

Data Sheet

- ADE9078: High Performance, Polyphase Energy Metering AFE Data Sheet

User Guides

- UG-953: Evaluating the ADE9078 High Performance, Polyphase Energy Metering Analog Front End (AFE)

TOOLS AND SIMULATIONS

- ADE9078 Calibration Tool

DESIGN RESOURCES

- ADE9078 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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TABLE OF CONTENTS

REVISION HISTORY

8/2016—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 2.7 V to 3.63 V, GND = AGND = DGND = 0 V, on-chip reference, CLKIN = 12.288 MHz crystal (XTAL), T_{MIN} to T_{MAX} = −40°C to +85°C for minimum and maximum specifications, T_A = 25°C (typical) for typical specifications.

Table 1.[1]

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					Measurement error per phase
Total Active Energy		0.1		%	Over a dynamic range of 5000 to 1, 10 sec accumulation; gain compensation only
		0.2		%	Over a dynamic range of 10,000 to 1, 20 sec accumulation; gain compensation only
Total Reactive Energy		0.1		%	Over a dynamic range of 5000 to 1, 10 sec accumulation; gain compensation only
		0.2		%	Over a dynamic range of 10,000 to 1, 20 sec accumulation; gain compensation only
Total Apparent Energy		0.1		%	Over a dynamic range of 1000 to 1, 2 sec accumulation
		0.5		%	Over a dynamic range of 5000 to 1, 10 sec accumulation
Fundamental Reactive		0.1		%	Over a dynamic range of 5000 to 1, 2 sec accumulation
		0.2		%	Over a dynamic range of 10,000 to 1, 20 sec accumulation
IRMS, VRMS		0.1		%	Over a dynamic range of 1000 to 1
		0.5		%	Over a dynamic range of 5000 to 1
Active Power, VAR		0.2		%	Over a dynamic range of 5000 to 1, 1 sec accumulation
Power Factor (PF)		±0.001			Over a dynamic range of 5000 to 1
64-Point per Line Cycle Resampled Data		0.1		%	An FFT is performed to receive the magnitude response; this error is the worst case error in the fundamental magnitude caused by resampling algorithm distortion; input signal is 50 Hz fundamental on voltage channel and fundamental with ninth harmonic at half of full scale on current channel
		0.3		%	An FFT is performed to receive the magnitude response; this error is the magnitude error of ninth harmonic caused by the resampling algorithm distortion input signal is 50 Hz fundamental with ninth harmonic at half of full scale on current channel
		−72		dB	Amplitude of highest spur; input signal is 50 Hz fundamental and ninth harmonic at half of full scale on the current channel
		3		%	An FFT is performed to receive the magnitude response; this error is the magnitude error of 31st harmonic caused by resampling algorithm distortion; input signal is 50 Hz fundamental with 31st harmonic at half of full scale on the current channel
		−38		dB	Amplitude of highest spur; input signal is 50 Hz fundamental and 31st harmonic at half of full scale on the current channel
Line Period Measurement		0.001		Hz	Resolution at 50 Hz
Current to Current, Voltage to Voltage, and Voltage to Current Angle Measurement		0.036		Degrees	Resolution at 50 Hz; voltage and current at 1/10th of full scale
PSM1 IRMS		0.2		%	Accuracy achieved 40 ms after entering PSM1 mode at 600:1

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PSM1 Active Power		0.2		%	Accuracy achieved 40 ms after entering PSM1 mode at 600:1
PSM2 Peak Current Detection		5		%	Accuracy of current detection threshold, achieved 120 ms after entering PSM2 mode at 660:1
ADC					See the ADC section
PGA Gain Settings (GAIN)		1, 2, or 4		V/V	PGA gain setting is referred to as GAIN
Differential Input Voltage Range (VxP − VxN, IxP − IxN)	−1/GAIN		+1/GAIN	V	0.707 V rms; when V_{REF} = 1.25 V, this voltage corresponds to 53 million codes
Maximum Operating Voltage on Analog Input Pins (VxP, VxN, IxP, and IxN)	−0.6		0.6	V	Voltage on the pin with respect to ground (GND = AGND = DGND = REFGND), V_{REF} = 1.25 V
Signal-to-Noise Ratio (SNR)[2]					V_{IN} = full scale/gain; see the Terminology section
PGA = 1		101		dB	4 kSPS sinc4 + infinite impulse response (IIR) low-pass filter (LPF) output
		97		dB	16 kSPS sinc4 output
PGA = 4		97		dB	4 kSPS sinc4 + IIR LPF output
		94		dB	16 kSPS sinc4 output
Total Harmonic Distortion (THD)[2]					See the Terminology section
PGA = 1		−106		dB	4 kSPS sinc4 + IIR LPF output
		−106		dB	16 kSPS sinc4 output
PGA = 4		−115		dB	4 kSPS sinc4 + IIR LPF output
		−112		dB	16 kSPS sinc4 output
Signal-to-Noise and Distortion Ratio (SINAD)[2]					See the Terminology section
PGA = 1		100		dB	4 kSPS sinc4 + IIR LPF output
		96		dB	16 kSPS sinc4 output
PGA = 4		96		dB	4 kSPS sinc4 + IIR LPF output
		93		dB	16 kSPS sinc4 output
Spurious-Free Dynamic Range (SFDR)[2]					See the Terminology section
PGA = 1		110		dB	4 kSPS sinc4 + IIR LPF output
Output Pass Band (−0.1 dB)					See the Terminology section
Sinc4 Outputs		0.672		kHz	16 kSPS sinc4 output
Sinc4 + IIR LPF Outputs		0.672		kHz	4 kSPS output
Output Bandwidth (−3 dB)[2]					See the Terminology section
Sinc4 Outputs		3.6325		kHz	16 kSPS sinc4 output
Sinc4 + IIR LPF Outputs		1.6		kHz	4 kSPS output
Crosstalk[2]		−120		dB	See the Terminology section, at 50 Hz and 60 Hz
AC Power Supply Rejection Ratio (AC PSRR)[2]		−120		dB	See the Terminology section, at 50 Hz and 60 Hz
AC Common-Mode Rejection Ratio (AC CMRR)[2]		−115		dB	At 100 Hz and 120 Hz
Gain Error		±0.3	±1	%	See the Terminology section
Gain Drift[2]		±3		ppm/°C	See the Terminology section
Offset		±0.36	±3.8	mV	See the Terminology section
Offset Drift[2]		0	±6	µV/°C	See the Terminology section

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Channel Drift (PGA, ADC, Internal Voltage Reference)		±7	±25	ppm/°C	PGA = 1, internal V_{REF}
		±7	±25	ppm/°C	PGA = 2, internal V_{REF}
		±7	±25	ppm/°C	PGA = 4, internal V_{REF}
Differential Input Impedance (DC)	330	366		kΩ	See the Terminology section, PGA = 1
	160	180		kΩ	PGA = 2
	80	90		kΩ	PGA = 4
INTERNAL VOLTAGE REFERENCE					Nominal 1.25 V ±1 mV
Voltage Reference		1.250		V	T_A = 25°C, REF pin
Temperature Coefficient[2]		±5	±20	ppm/°C	T_A = −40°C to +85°C
EXTERNAL VOLTAGE REFERENCE					
External Voltage Reference Input Voltage (REF)		1.2, 1.25		V	REFGND must be tied to GND, AGND, and DGND; 1.25 V external reference is preferred; the full-scale values mentioned in this data sheet are for a voltage reference of 1.25 V
Average Reference Current		120		µA/V	
CRYSTAL OSCILLATOR					CLKIN = 12.288 MHz ± 30 ppm (see the Crystal Oscillator/External Clock section)
Input Clock Frequency	12.165	12.288	12.411	MHz	
Internal Capacitance on CLKIN and CLKOUT		4		pF	
Internal Feedback Resistance Between CLKIN and CLKOUT		2.5		MΩ	
Transconductance (g_m)		9		mA/V	
EXTERNAL CLOCK INPUT					
Input Clock Frequency	12.165	12.288	12.411	MHz	
Duty Cycle[2]	45:55	50:50	55:45	%	
CLKIN Logic Inputs					3.3 V tolerant
Input Voltage					
High, V_{INH}	1.2			V	V_{DD} = 2.7 V to 3.63 V
Low, V_{INL}			0.5	V	V_{DD} = 2.7 V to 3.63 V
LOGIC INPUTS					
PM0, PM1, $\overline{\text{RESET}}$, MOSI, SCLK, and $\overline{\text{SS}}$					
Input Voltage					
High, V_{INH}	2.4			V	V_{DD} = 2.7 V to 3.63 V
Low, V_{INL}			0.8	V	V_{DD} = 2.7 V to 3.63 V
Input Current, I_{IN}			15	µA	V_{IN} = 0 V
Internal Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
MISO, $\overline{\text{IRQ0}}$, and $\overline{\text{IRQ1}}$					V_{DD} = 2.97 V to 3.63 V
Output Voltage					
High, V_{OH}	2.4			V	I_{SOURCE} = 4 mA
Low, V_{OL}			0.8	V	I_{SINK} = 4 mA
Internal Capacitance, C_{IN}			10	pF	
CF1, CF2, CF3, and CF4					V_{DD} = 2.97 V to 3.63 V
Output Voltage					
High, V_{OH}	2.4			V	I_{SOURCE} = 8 mA
Low, V_{OL}			0.8	V	I_{SINK} = 8 mA
Internal Capacitance, C_{IN}			10	pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC OUTPUTS					
MISO, $\overline{IRQ0}$, and $\overline{IRQ1}$					V_{DD} = 2.7 V
Output Voltage					
High, V_{OH}	2.4			V	I_{SOURCE} = 1 mA
Low, V_{OL}			0.8	V	I_{SINK} = 4 mA
CF1, CF2, CF3, and CF4					V_{DD} = 2.7 V
Output Voltage					
High, V_{OH}	2.4			V	I_{SOURCE} = 3 mA
Low, V_{OL}			0.8	V	I_{SINK} = 8 mA
LOW DROPOUT REGULATORS (LDOs)					
AVDD		1.9		V	See the Power-On Sequence section
DVDD		1.7		V	
POWER SUPPLY					For specified performance
VDD	2.7	3.3	3.63	V	
Supply Current (VDD)					V_{DD} = 3.63 V
Power Save Mode 0 (PSM0)		10	12	mA	Normal mode, seven ADCs enabled
		9.5	11	mA	Normal mode, seven ADCs enabled, total reactive power computation disabled
		10.5	12	mA	Normal mode, seven ADCs enabled, waveform buffer enabled
		10	11.6	mA	Normal mode, six ADCs enabled
Power Save Mode 1 (PSM1)		9	10.6	mA	Fast rms, active power, and total reactive power measurement within 30 ms for tamper detection
Power Save Mode 2 (PSM2)		115	200	µA	Compares current to threshold, AVDD = 0 V, DVDD = 0 V
Power Save Mode 3 (PSM3)		50	200	nA	Idle, AVDD = 0 V, DVDD = 0 V

[1] Throughout this data sheet, multifunction pins, such as CF3/ZX, are referred to either by the entire pin name or by a single function of the pin, for example, CF3, when only that function is relevant.
[2] Tested during device characterization.

TIMING CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	10			ns
SCLK Frequency				10	MHz
SCLK Low Pulse Width	t_{SL}	40			ns
SCLK High Pulse Width	t_{SH}	40			ns
Data Output Valid After SCLK Edge	t_{DAV}			40	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	10			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	10			ns
Data Output Fall Time	t_{DF}			10	ns
Data Output Rise Time	t_{DR}			10	ns
SCLK Fall Time	t_{SF}			10	ns
SCLK Rise Time	t_{SR}			10	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}			100	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0			ns

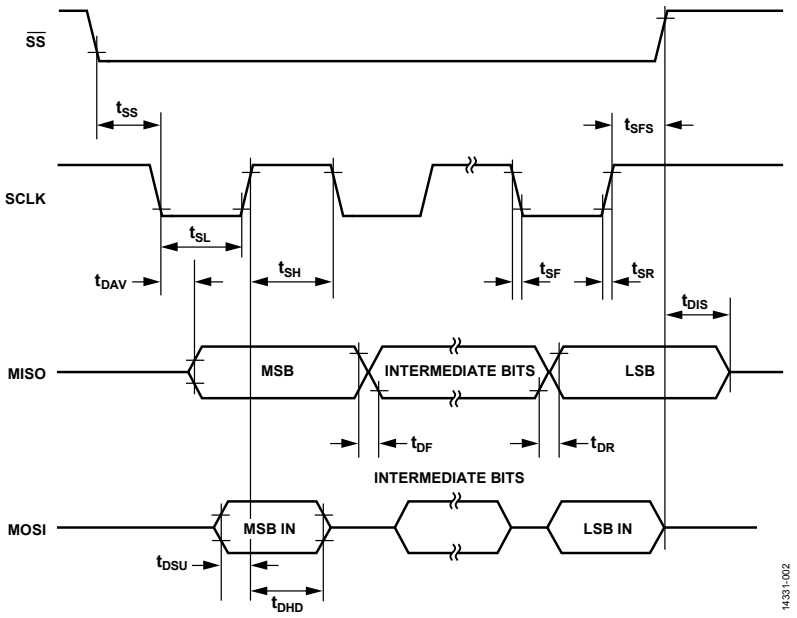

Figure 2. SPI Interface Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
VDD to GND	−0.3 V to +3.96 V
Analog Input Voltage to GND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VAN VBP, VBN, VCP, VCN	−1.9 V to +2 V
Reference Input Voltage to REFGND	−0.3 V to +2 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)[1]	260°C
ESD	
Human Body Model[2]	4 kV
Machine Model[3]	200 V
Field Induced Charged Device Model (FICDM)[4]	1.25 kV

[1] Analog Devices recommends that reflow profiles used in soldering RoHS compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.
[2] Applicable standard: ANSI/ESDA/JEDEC JS-001-2014.
[3] Applicable standard: JESD22-A115-A (ESD machine model standard of JEDEC).
[4] Applicable Standard JESD22-C101F (ESD FICDM standard of JEDEC).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment.

Careful attention to PCB thermal design is required.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-40-7[1]	27.14	3.13	°C/W

[1] Test Condition 1: The junction to air measurement uses a 2S2P JEDEC test board with 4 × 4 standard JEDEC vias. The junction to case measurement uses a 1S0P JEDEC test board with 4 × 4 standard JEDEC vias. See JEDEC standard JESD51-2.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

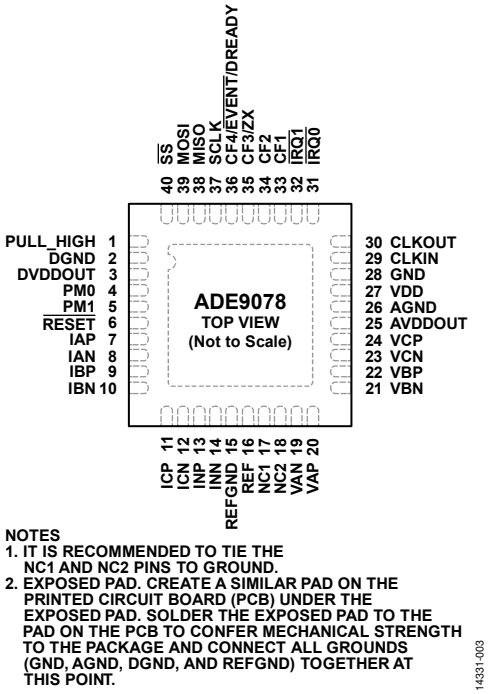

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PULL_HIGH	Pull High. Tie this pin to VDD.
2	DGND	Digital Ground. This pin provides the ground reference for the digital circuitry in the ADE9078. Because the digital return currents in the ADE9078 are small, it is acceptable to connect this pin to the analog ground plane of the whole system. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
3	DVDDOUT	1.8 V Output of the Digital Low Dropout Regulator (LDO). Decouple this pin with a 0.1 µF ceramic capacitor in parallel with a ceramic 4.7 µF capacitor.
4	PM0	Power Mode Pin 0. PM0, combined with PM1, defines the power mode. For normal operation, PM0 and PM1 must be grounded (see the Power Modes section).
5	PM1	Power Mode Pin 1. PM1 combined with PM0, defines the power mode. For normal operation, PM0 and PM1 must be grounded (see the Power Modes section).
6	$\overline{\text{RESET}}$	Reset Input, Active Low. This pin must stay low for at least 1 µs to trigger a hardware reset.
7, 8	IAP, IAN	Analog Inputs, Channel IA. The IAP (positive) and IAN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
9, 10	IBP, IBN	Analog Inputs, Channel IB. The IBP (positive) and IBN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
11, 12	ICP, ICN	Analog Inputs, Channel IC. The ICP (positive) and ICN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
13, 14	INP, INN	Analog Inputs, Channel IN. The INP (positive) and INN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
15	REFGND	Ground Reference, Internal Voltage Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
16	REF	Voltage Reference. The REF pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.25 V. An external reference of 1.2 V to 1.25 V can also be connected at this pin. In either case, decouple REF to REFGND with 0.1 µF ceramic capacitor in parallel with a ceramic 4.7 µF capacitor. After reset, the on-chip reference is enabled. To use the internal voltage reference with external circuits, a buffer is required. The full-scale values mentioned in this data sheet are for a voltage reference of 1.25 V.
17	NC1	No Connection. It is recommended to tie this pin to ground.
18	NC2	No Connection. It is recommended to tie this pin to ground.

Pin No.	Mnemonic	Description
19, 20	VAN, VAP	Analog Inputs, Channel VA. The VAP (positive) and VAN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
21, 22	VBN, VBP	Analog Inputs, Channel VB. The VBP (positive) and VBN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
23, 24	VCN, VCP	Analog Inputs, Channel VC. The VCP (positive) and VCN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1 V. This channel also has an internal PGA of 1, 2, or 4.
25	AVDDOUT	1.9 V Output of the Analog Low Dropout Regulator (LDO). Decouple AVDDOUT with a 0.1 µF ceramic capacitor in parallel with a ceramic 4.7 µF capacitor. Do not connect external active circuitry to this pin.
26	AGND	Analog Ground Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
27	VDD	Supply Voltage. The VDD pin provides the supply voltage. Decouple VDD to GND with a ceramic 0.1 µF capacitor in parallel with a ceramic 10 µF capacitor.
28	GND	Supply Ground Reference. Connect all grounds (GND, AGND, DGND, and REFGND) together at one point.
29	CLKIN	Crystal/Clock Input. Connect a crystal across CLKIN and CLKOUT to provide a clock source. See the Crystal Selection section for details on choosing a suitable crystal. Alternatively, an external clock can be provided at this logic input.
30	CLKOUT	Crystal Output. Connect a crystal across CLKIN and CLKOUT to provide a clock source. When using CLKOUT to drive external circuits, connect an external buffer. When using an external clock on CLKIN, leave CLKOUT unconnected.
31	$\overline{\text{IRQ0}}$	Interrupt Request Output. This pin is an active low logic output. See the Interrupts/Events section for information about events that trigger interrupts.
32	$\overline{\text{IRQ1}}$	Interrupt Request Output. This pin is an active low logic output. See the Interrupts/Events section for information about events that trigger interrupts.
33	CF1	Calibration Frequency (CF) Logic Output 1. The CF1, CF2, CF3, and CF4 outputs provide power information based on the CFxSEL bits in the CFMODE register. Use these outputs for operational and calibration purposes. Scale the full-scale output frequency by writing to the CFxDEN registers (see the Digital to Frequency Conversion—CFx Output section).
34	CF2	CF Logic Output 2. This pin indicates CF2.
35	CF3/ZX	CF Logic Output 3/Zero Crossing. This pin indicates CF3 or zero crossing.
36	CF4/$\overline{\text{EVENT}}$/DREADY	CF Logic Output 4/Event Pin/Data Ready. This pin indicates CF4, events, or when new data is ready.
37	SCLK	Serial Clock Input for the SPI Port. All serial data transfers synchronize to this clock (see the Accessing On-Chip Data section). The SCLK pin has a Schmitt trigger input for use with a clock source that has a slow edge transition time, for example, optoisolator outputs.
38	MISO	Data Output for the SPI Port.
39	MOSI	Data Input for the SPI Port.
40	$\overline{\text{SS}}$	Slave Select for the SPI Port.
	EP	Exposed Pad. Create a similar pad on the printed circuit board (PCB) under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package and connect all grounds (GND, AGND, DGND, and REFGND) together at this point.

TYPICAL PERFORMANCE CHARACTERISTICS

TOTAL ENERGY LINEARITY OVER SUPPLY AND TEMPERATURE

Sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz; sinusoidal current with variable amplitudes from 100% of full scale down to 0.005% or 0.02% of full scale and with a frequency of 50 Hz; integrator off.

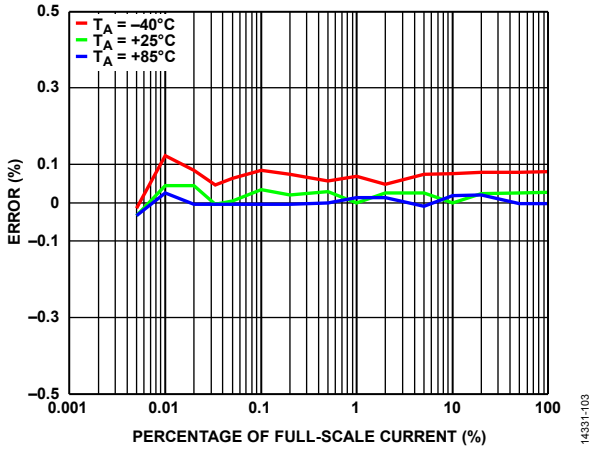

Figure 4. Total Active Energy Error as a Percentage of Reading over Temperature, PF = 1

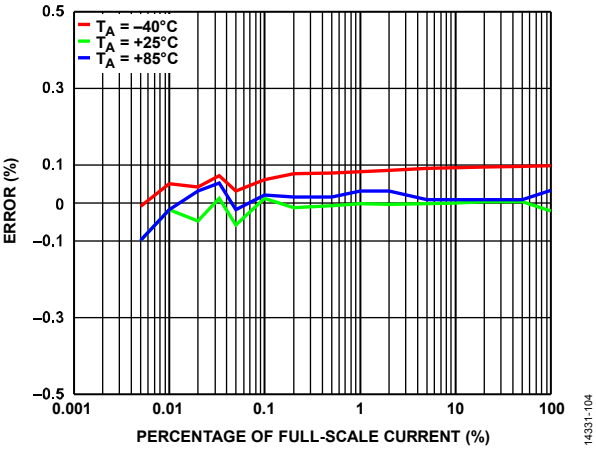

Figure 5. Total Reactive Energy Error as a Percentage of Reading over Temperature, PF = 0

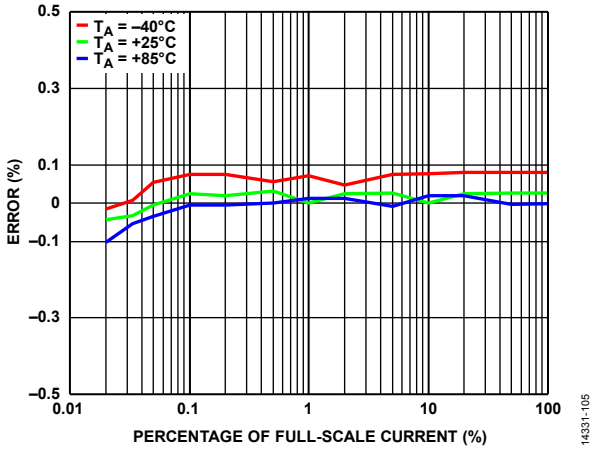

Figure 6. Total Apparent Energy Error as a Percentage of Reading over Temperature, PF = 1

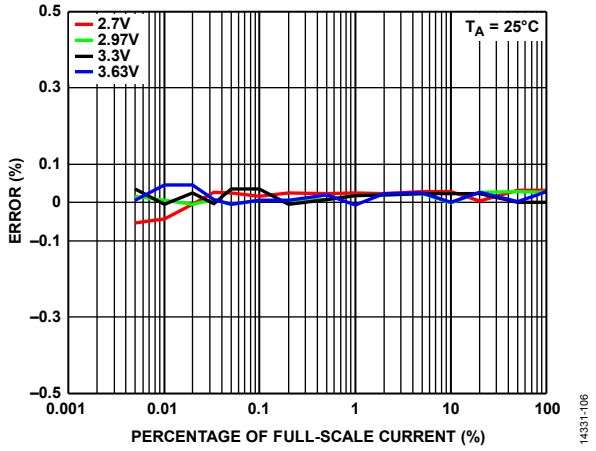

Figure 7. Total Active Energy Error as a Percentage of Reading over Supply Voltage, PF = 1, T_A = 25°C

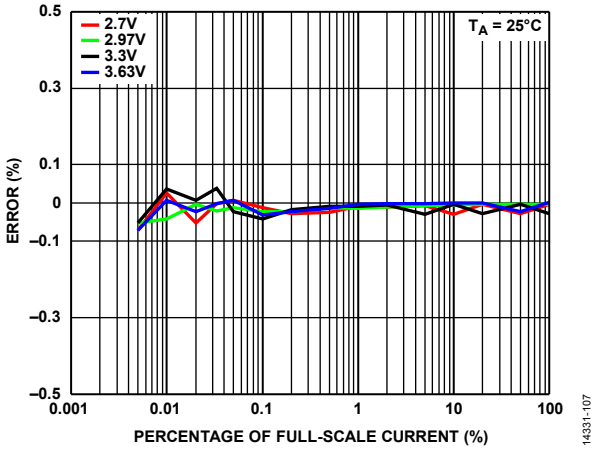

Figure 8. Total Reactive Energy Error as a Percentage of Reading over Supply Voltage, PF = 0, T_A = 25°

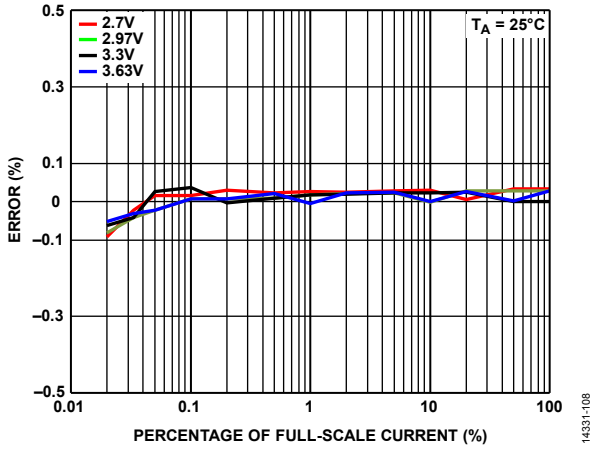

Figure 9. Total Apparent Energy Error as a Percentage of Reading over Supply Voltage, PF = 1, T_A = 25°

FUNDAMENTAL ENERGY LINEARITY WITH FIFTH HARMONIC OVER SUPPLY AND TEMPERATURE

Fundamental voltage component in phase with fifth harmonic; current with a 50 Hz component that has variable amplitudes from 100% of full scale down to 0.005% of full scale and a fifth harmonic with a constant amplitude of 40% of fundamental; integrator off.

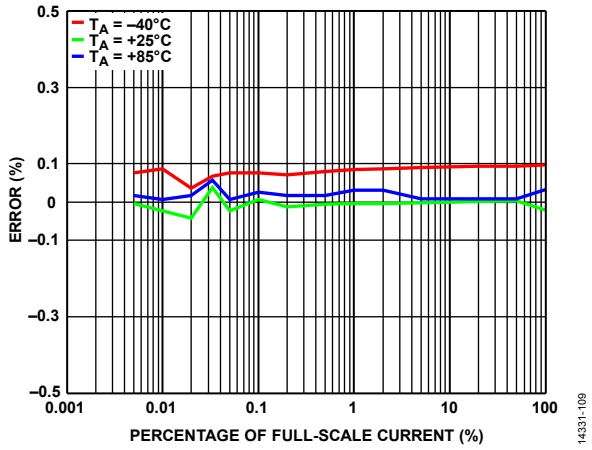

Figure 10. Fundamental Reactive Energy Error as a Percentage of Reading over Temperature, PF = 0

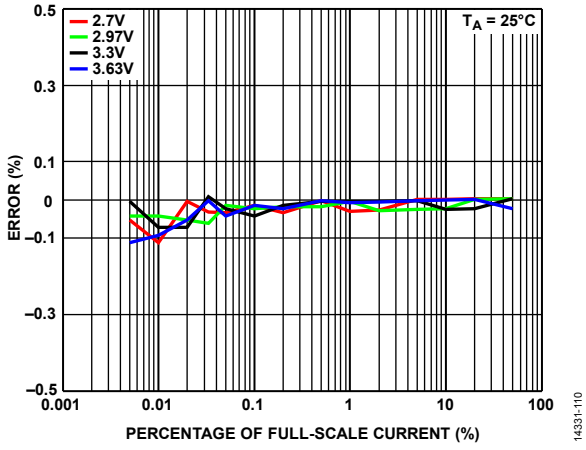

Figure 11. Fundamental Reactive Energy Error as a Percentage of Reading over Supply Voltage, PF = 0, T_A = 25°

TOTAL ENERGY ERROR OVER FREQUENCY

Sinusoidal voltage with a constant amplitude of 50% of full scale; sinusoidal current with a constant amplitude of 10% of full scale; variable frequency between 45 Hz and 65 Hz; integrator off.

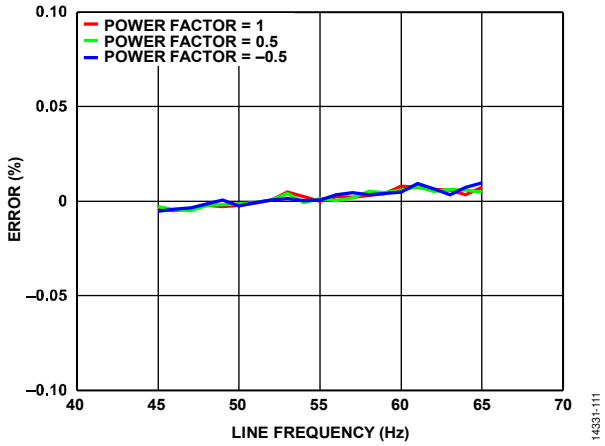

Figure 12. Total Active Energy Error as a Percentage of Reading vs. Line Frequency, PF = –0.5, +0.5, and +1

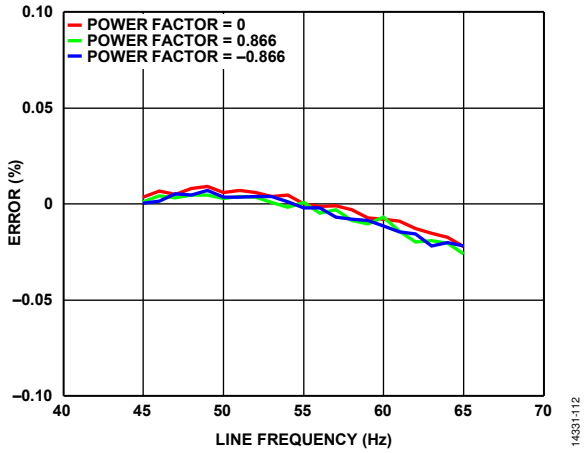

Figure 13. Total Reactive Energy Error as a Percentage of Reading vs. Line Frequency, PF = –0.866, 0, and +0.866

RMS LINEARITY OVER TEMPERATURE AND RMS ERROR OVER FREQUENCY

Sinusoidal current and voltage with variable amplitudes from 100% of full scale down to 0.02% of full scale using a frequency of 50 Hz; variable frequency between 45 Hz and 65 Hz; sinusoidal current amplitude of 10% of full scale and voltage amplitude of 50% of full scale; integrator off.

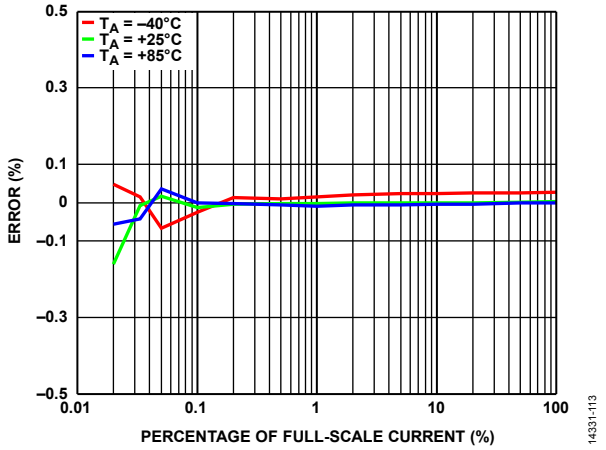

Figure 14. Current RMS Error as a Percentage of Reading over Temperature

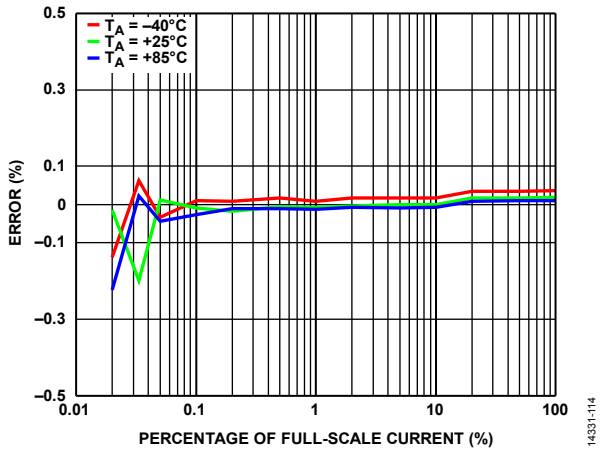

Figure 15. Voltage RMS Error as a Percentage of Reading over Temperature

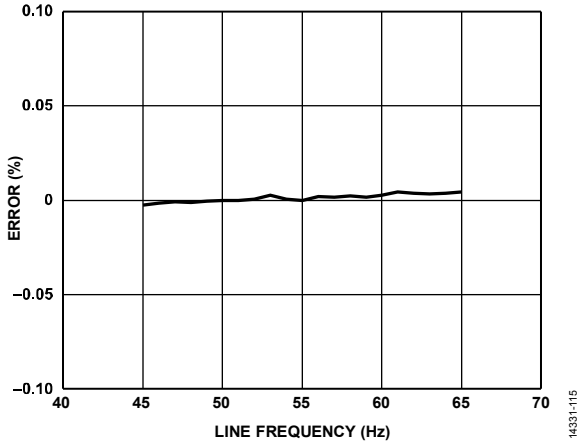

Figure 16. Current RMS Error as a Percentage of Reading vs. Line Frequency

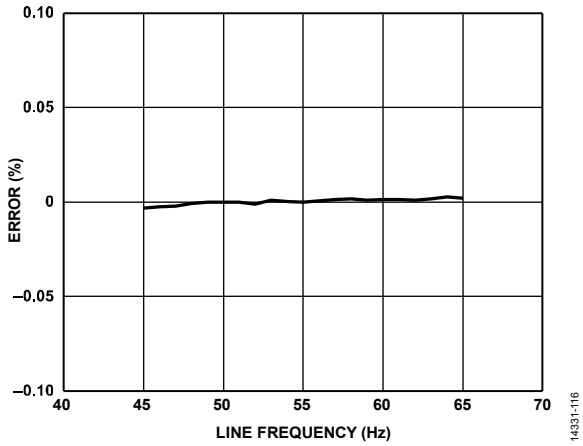

Figure 17. Voltage RMS Error as a Percentage of Reading vs. Line Frequency

ENERGY LINEARITY REPEATABILITY

Sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz; sinusoidal current with variable amplitudes from 100% of full scale down to 0.005% of full scale and with a frequency of 50 Hz. For Figure 20, besides the fundamental component, the voltage contained a fifth harmonic with a constant amplitude of 40% of fundamental, and the current contained a fifth harmonic with a constant amplitude of 40% of fundamental. Integrator off. Measurements at 25°C repeated 30 times.

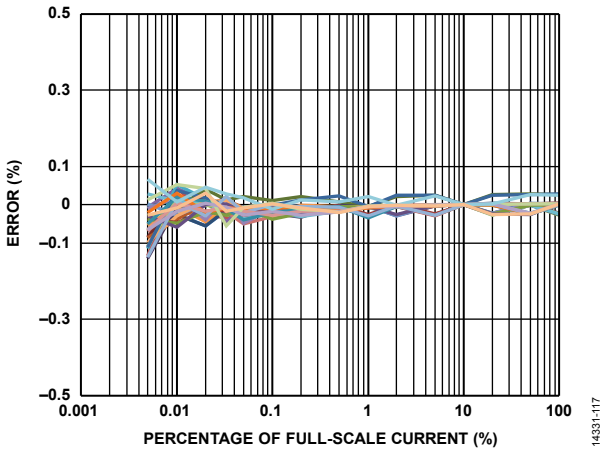

Figure 18. Total Active Energy Error as a Percentage of Reading, PF = 1 (Standard Deviation σ = 0.03% at 0.01% of Full-Scale Current)

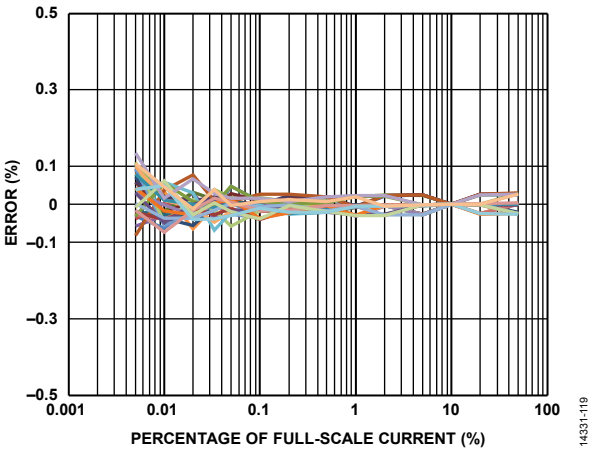

Figure 20. Fundamental Reactive Energy Error as a Percentage of Reading, PF = 0 (Standard Deviation σ = 0.04% at 0.01% of Full-Scale Current)

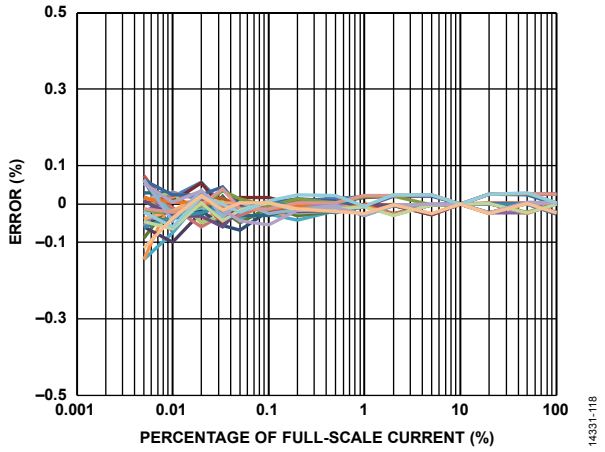

Figure 19. Total Reactive Energy Error as a Percentage of Reading, PF = 0 (Standard Deviation σ = 0.04% at 0.01% of Full-Scale Current)

TOTAL ENERGY AND RMS LINEARITY WITH INTEGRATOR ON

Sinusoidal voltage with an amplitude of 50% of full scale and a frequency of 50 Hz; gain of current channel set to 4; sinusoidal current with variable amplitudes from 100% of full scale down to 0.05% or 0.1% of full scale and with a frequency of 50 Hz; full scale at gain of 4 = (full scale at gain of 1)/4, high-pass corner frequency of 4.97 Hz.

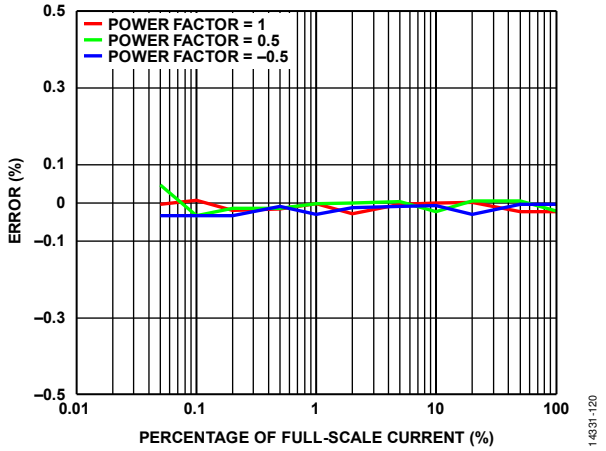

Figure 21. Total Active Energy Error, Gain = 4, Integrator On

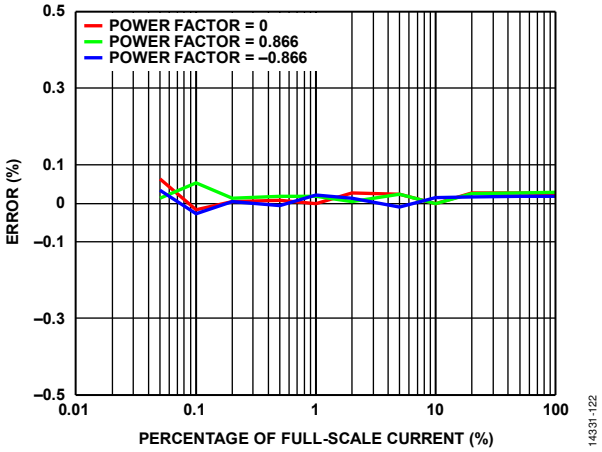

Figure 23. Total Apparent Energy Error, Gain = 4, Integrator On

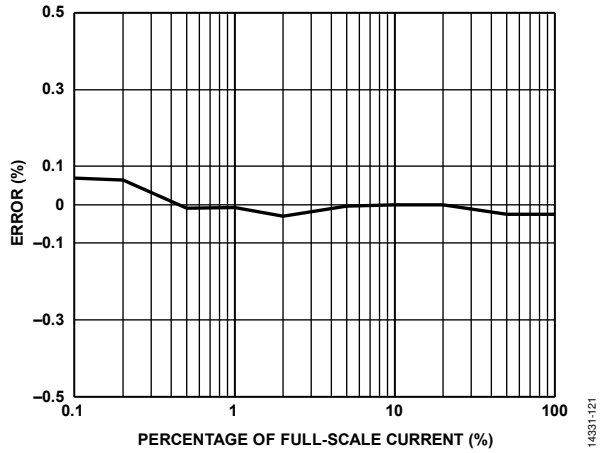

Figure 22. Total Reactive Energy Error, Gain = 4, Integrator On

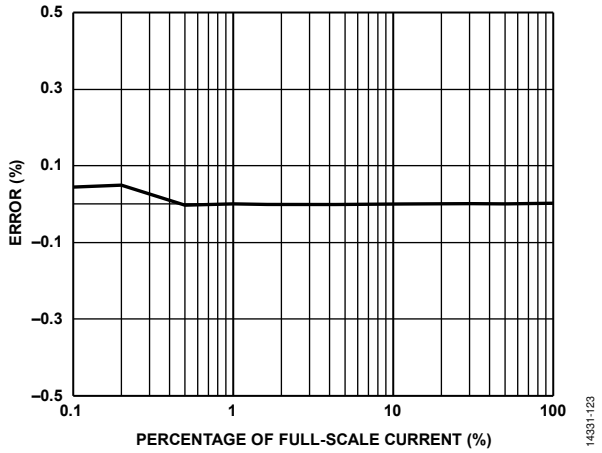

Figure 24. Total RMS Current Error, Gain = 4, Integrator On

TOTAL ENERGY ERROR OVER FREQUENCY WITH INTEGRATOR ON

Sinusoidal voltage with a constant amplitude of 50% of full scale; gain of current channel set to 4; sinusoidal current with a constant amplitude of 10% of full scale; variable frequency between 45 Hz and 65 Hz, gigh-pass corner frequency of 4.97 Hz.

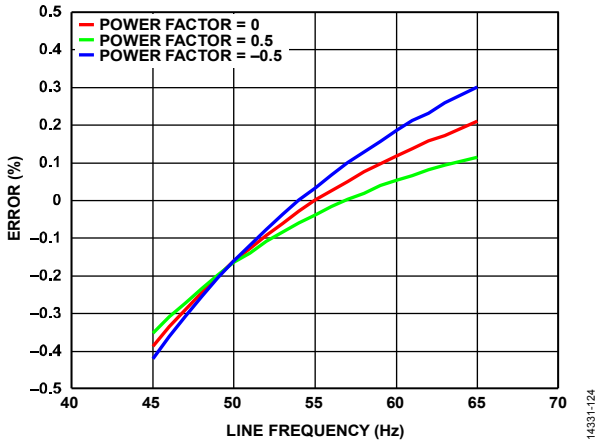

Figure 25. Total Active Energy Error as a Percentage of Reading vs. Line Frequency, Gain = 4, Integrator On

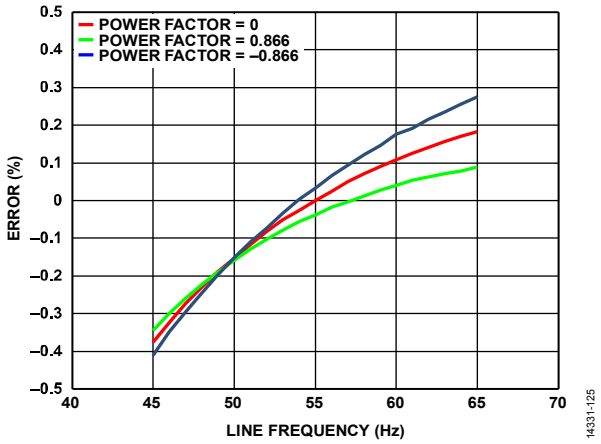

Figure 26. Total Reactive Energy Error as a Percentage of Reading vs. Line Frequency, Gain = 4, Integrator On

TEST CIRCUIT

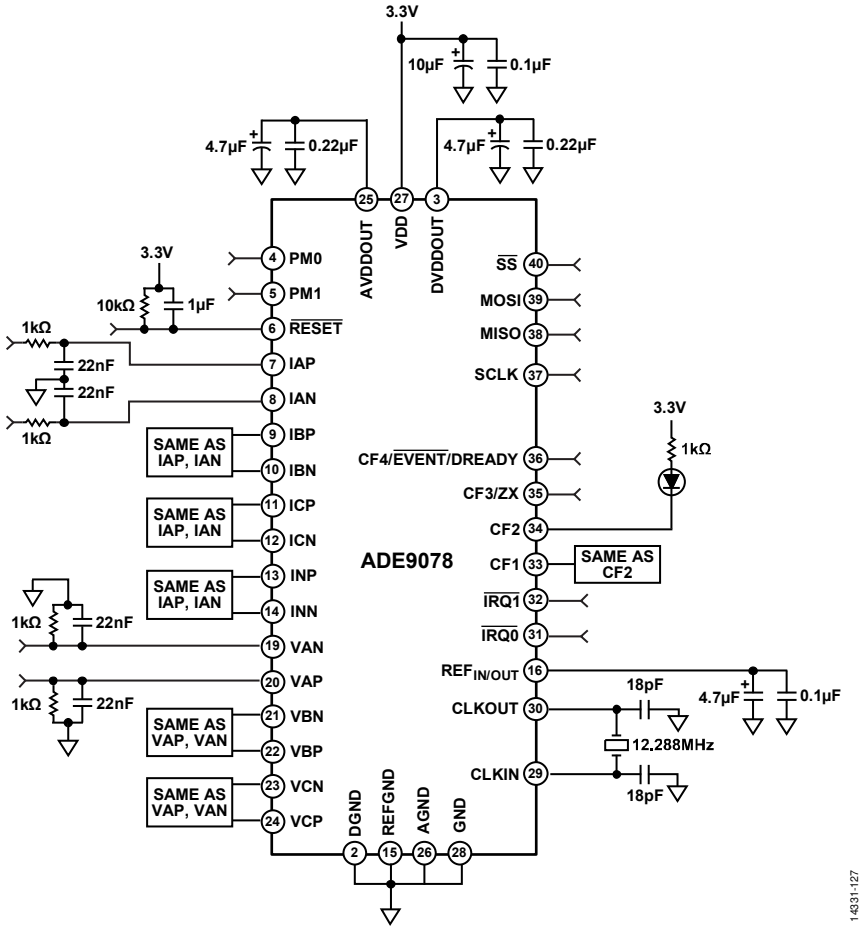

Figure 27. Test Circuit

TERMINOLOGY

Differential Input Voltage Range and Maximum Operating Voltage on VxP, VxN, IxP, and IxN Analog Input Pins

The differential input range describes the maximum difference between the IxP and IxN or VxP and VxN pins. The maximum operating voltage given in Table 1 describes the maximum voltage that can be present on each pin, including any common-mode voltage. Figure 28 illustrates the maximum input between xP and xM, which is seen in the application when a current transformer with center tapped burden resistor is used. Figure 29 illustrates the maximum input voltage range between xP and xN when a pseudo differential input is applied, as is commonly seen when sensing the line voltage.

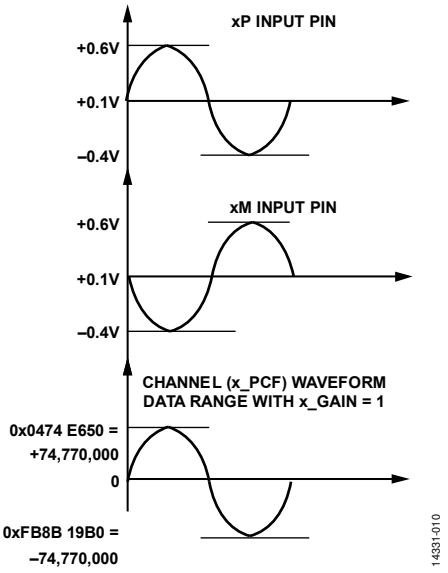

Figure 28. Maximum Input Signal with Differential Antiphase Input with Common-Mode Voltage = 0.1 V Gain = 1

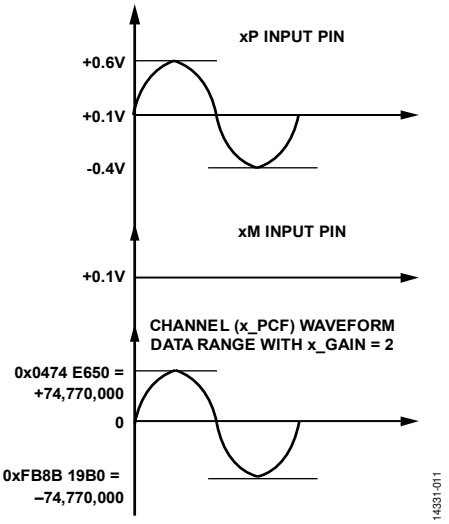

Figure 29. Maximum Input Signal with Pseudo Differential Input with Common-Mode Voltage = 0.1 V, Gain = 2 (x_GAIN = 2)

Crosstalk

Crosstalk is measured by grounding one channel and applying a full-scale 50 Hz or 60 Hz signal on all the other channels. The crosstalk is equal to the ratio between the grounded ADC output value and its ADC full-scale output value. The ADC outputs are acquired for 100 sec. Crosstalk is expressed in decibels.

Differential Input Impedance (DC)

The differential input impedance represents the impedance between the pair IxP and IxN or VxP and VxN. It varies with the PGA gain selection as indicated in Table 1.

ADC Offset

ADC offset is the difference between the average measured ADC output code with both inputs connected to GND and the ideal ADC output code of zero. ADC offset is expressed in microvolts.

ADC Offset Drift over Temperature

The ADC offset drift is the change in offset over temperature. It is measured at −40°C, +25°C, and +85°C. The offset drift over temperature is computed as follows:

$$Drift = \max\left(\left|\frac{Offset(-40^\circ C) - Offset(25^\circ C)}{(-40^\circ C - 25^\circ C)}\right|, \left|\frac{Offset(85^\circ C) - Offset(25^\circ C)}{(85^\circ C - 25^\circ C)}\right|\right)$$

Offset drift is expressed in μV/°C.

Gain Error

The gain error in the ADCs represents the difference between the measured ADC output code (minus the offset) and the ideal output code when an external voltage reference of 1.2 V is used (see the Voltage Reference section). The difference is expressed as a percentage of the ideal code. It represents the overall gain error of one channel.

Gain Drift over Temperature

This temperature coefficient includes the temperature variation of the ADC gain while using an external voltage reference of 1.2 V. It represents the overall temperature coefficient of one current or voltage channel. With an external voltage reference of 1.2 V in use, the ADC gain is measured at −40°C, +25°C, and +85°C. Then the temperature coefficient is computed as follows:

$$Drift = \max\left(\left|\frac{Gain(-40^\circ C) - Gain(25^\circ C)}{Gain(25^\circ C) \times (-40^\circ C - 25^\circ C)}\right|, \left|\frac{Gain(85^\circ C) - Gain(25^\circ C)}{Gain(25^\circ C) \times (85^\circ C - 25^\circ C)}\right|\right)$$

Gain drift is measured in ppm/°C.

AC Power Supply Rejection (PSRR)
AC PSRR quantifies the measurement error as a percentage of reading when the dc power supply is V_{NOM} and modulated with ac and the inputs are grounded. For the ac PSRR measurement, 20 sec of samples is captured with nominal supplies (3.3 V) and a second set are captured with an additional ac signal (330 mV peak at 50 Hz) introduced onto the supplies. Then, the PSRR is expressed as PSRR = 20 $\log_{10}$(V2/V1).

Signal-to-Noise Ratio (SNR)
SNR is calculated by inputting a 50 Hz signal, and samples are acquired for 2 sec. The amplitudes for each frequency up to the bandwidth given in Table 1 as the ADC output bandwidth (−3 dB) are calculated. To determine the SNR, the signal at 50 Hz is compared to the sum of the power from all the other frequencies, removing power from its harmonics. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is calculated by inputting a 50 Hz signal, and samples are acquired for 2 sec. The amplitudes for each frequency up to the bandwidth given in Table 1 as the ADC output bandwidth (−3 dB) are calculated. To determine the SINAD, the signal at 50 Hz is compared to the sum of the power from all the other frequencies. The value for SINAD is expressed in decibels.

Total Harmonic Distortion (THD)
THD is calculated by inputting a 50 Hz signal, and samples are acquired for over 2 sec. The amplitudes for each frequency up to the bandwidth given in Table 1 as the ADC output bandwidth (−3 dB) are calculated. To determine the THD, the amplitudes of the 50 Hz harmonics up to the bandwidth are root sum squared. The value for THD is expressed in decibels.

Spurious-Free Dynamic Range (SFDR)
SFDR is calculated by inputting a 50 Hz signal, and samples are acquired for over 2 sec. The amplitudes for each frequency up to the bandwidth given in Table 1 as the ADC output bandwidth (−3 dB) are calculated. To determine the SFDR, the amplitude of the largest signal that is not a harmonic of 50 Hz is recorded. The value for SFDR is expressed in decibels.

ADC Output Pass Band
The ADC output pass band is the bandwidth within 0.1 dB, resulting from the digital filtering in the sinc4 and sinc4 + IIR LPF.

ADC Output Bandwidth
The ADC output bandwidth is the bandwidth within −3 dB, resulting from the digital filtering in the sinc4 and sinc4 + IIR LPF.

THEORY OF OPERATION

The ADE9078 integrates seven high performance ADCs and a flexible DSP core. An integrated high end reference ensures low drift over temperature with a combined drift of less than ±25 ppm/°C maximum for the whole channel including PGA and ADC.

The ADE9078 is a highly accurate, fully integrated energy metering device. Interfacing with both CT and Rogowski coil sensors, the ADE9078 enables users to develop a 3-phase metrology platform, which achieves high performance for Class 1 through Class 0.2 meters. See the Measurements (Normal Mode) section for more information.

Two power modes are provided to enable detection of meter tampering: PSM2 uses a low power comparator to compare current channels to a threshold and indicates whether it has been exceeded on the $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$ outputs; PSM1 enables fast measurement of current and voltage rms (xVRMS, xIRMS), active power, and VAR during a tamper. See the Measurements (PSM1) section and Measurements (PSM2) section for more information about how to use these modes.

ADC

Overview

The ADE9078 incorporates seven independent, second-order, Σ-Δ ADCs that sample simultaneously. Each ADC is 24 bits and supports fully differential and pseudo differential inputs that can go above and below ground. The ADE9078 includes a low noise, low drift, internal band gap reference. Set the EXT_REF bit in the CONFIG1 register if using an external voltage reference. Each ADC contains a programmable gain amplifier, which allows a gain of 1, 2, or 4. The ADCs incorporate proprietary dither techniques to prevent idle tones at low input levels, extending the accuracy range.

Analog Input Configuration

There is no internal buffering on the device. The impedance of the ADE9078 depends on the programmable gain selected (see the Specifications table).

Fully Differential Inputs

The input signals on the IAP, IAN, IBP, IBN, ICP, ICN, VAP, VAN, VBP, VBN, VCP, and VCN pins must not exceed 0.6 V relative to AGND, the analog ground reference. The differential full-scale input range of the ADCs is ±1 V peak (0.707 V rms), and the maximum allowed common-mode voltage at the ADC pins must not exceed ±0.1 V.

Figure 30 and Figure 31 show two common types of input signals for an energy metering application. Figure 30 shows the maximum input allowed with differential antiphase signals. A current transformer with center tapped burden resistor generates differential antiphase signals. Figure 31 shows the maximum input signal with pseudo differential signals, similar to those obtained when sensing the mains voltage signal through a resistive divider or using a Rogowski coil current sensor.

The following conditions must be met for the input signals with gain = 1:

- |IAP, IAN, IBP, IBN, ICP, ICN, VAP, VAN, VBP, VBN, VCP, and VCN| ≤ 0.6 V peak relative to AGND
- |IxP − IxN| ≤ 1 V peak, |VxP − VxN| ≤ 1 V peak

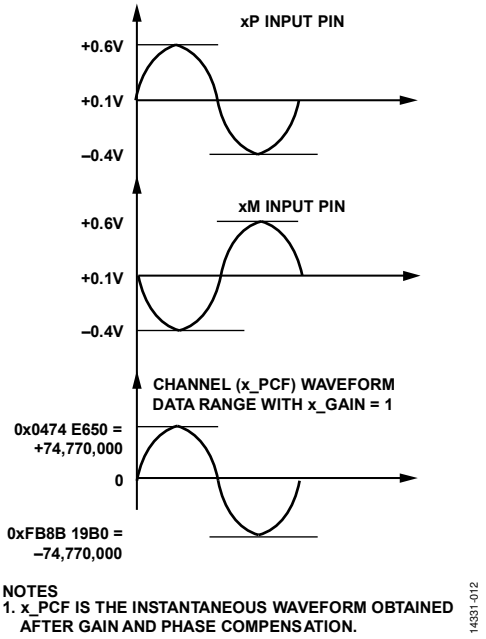

Figure 30. Maximum Input Signal with Differential Antiphase Input with Common-Mode Voltage = 0.1 V, Gain = 1

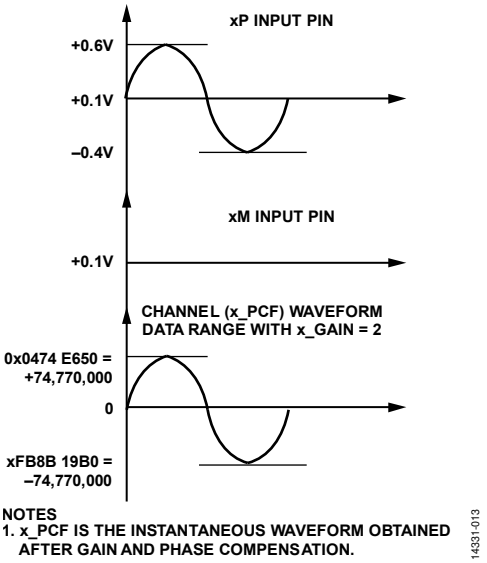

Figure 31. Maximum Input Signal with Pseudo Differential Input with Common-Mode Voltage = 0.1 V, Gain = 2

Each ADC contains a programmable gain amplifier that allows a gain of 1, 2, or 4. The ADC produces full-scale output codes with an input of ±1 V. With a gain of 1, this full-scale input corresponds to a differential antiphase input of 0.707 V rms, as shown in Figure 30. At a gain of 2, full-scale output codes are produced with an input of 0.353 V rms, as shown in Figure 31. At a gain

of 4, full-scale output codes are generated with a 0.1765 V rms input signal. Note that the voltages on the xP and xN pins must be within ±0.6 V as described in this section and Table 1.

Write the x_GAIN bits in the PGA_GAIN register to configure the gain for each channel.

Interfacing to Current and Voltage Sensors

Figure 32 and Figure 34 show the typical circuits to connect to current transformer and Rogowski coil current sensors. Figure 33 shows the typical interface circuit to measure the mains voltage.

The antialiasing filter corner is chosen to be around 7 kHz to provide sufficient attenuation of out of band signals near the modulator clock frequency. The same RC filter corner is used on voltage channels, as well, to avoid phase errors between current and voltage signals. Note that the Rogowski coil (that is, a di/dt sensor) input network has a second-order antialiasing filter. The integrator used in conjunction to the Rogowski coil has a −20 dB/dec attenuation and an approximately −90° phase shift. When combined with a di/dt sensor, the resulting magnitude and phase response is a flat gain over the frequency band of interest. However, the di/dt sensor has a 20 dB/dec gain associated with it, and it generates significant high frequency noise. An antialiasing filter of at least the second order is required to avoid noise aliasing back in the band of interest when the ADC is sampling. See Figure 34 for the recommended antialiasing filter.

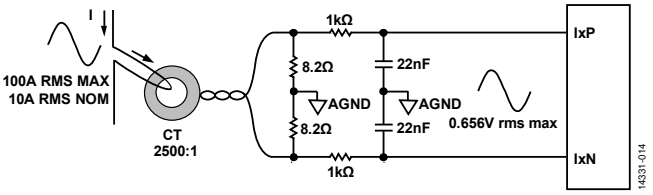

Figure 32. Application Circuit with a Current Transformer Current Sensor

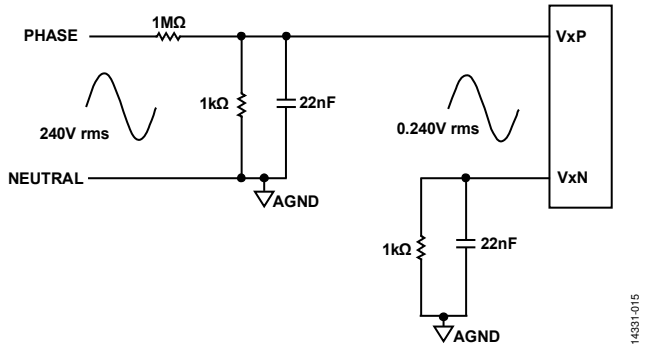

Figure 33. Application Circuit with Voltage Sensed Through Resistor Divider

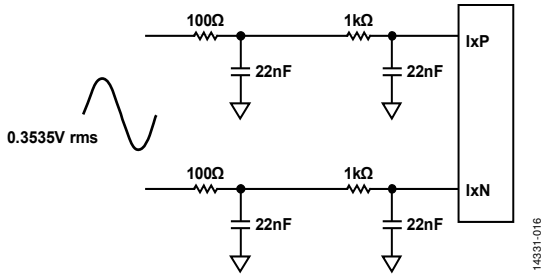

Figure 34. Application Circuit with Rogowski Coil Current Sensor

Internal RF Immunity Filter

Energy metering applications require the meter to be immune to external radio frequency fields of 30 V/m, from 80 MHz to 10 GHz, according to IEC 61000-4-3. The ADE9078 has internal antialiasing filters to improve performance in testing because it is difficult to filter these signals externally. The second-order, internal low-pass filter has a corner frequency of 10 MHz. Note that external antialias filters are required to attenuate frequencies above 7 kHz, as shown in the Interfacing to Current and Voltage Sensors section.

Modes of Operation

Each ADC has two modes of operation: normal mode and disabled mode.

In the normal mode, the ADCs turn on and sample continuously. Use the CHNL_DIS register to disable the ADCs individually.

Four different power modes are available in the ADE9078 (see the Power Modes section). All ADCs turn on during the PSM0 power mode. In the PSM1 power mode, all of the ADCs except for the neutral current ADC are turned on. In PSM2 mode and PSM3 mode, all ADCs are disabled and cannot be turned on.

Table 6. ADC Operation in PSMx Power Modes

PSMx Power Mode	ADC Mode of Operation
PSM0	Normal (on)
PSM1	IA, IB, IC, VA, VB, VC: normal (on) IN: disabled (always off)
PSM2	Disabled (always off)
PSM3	Disabled (always off)

Output Data Rates and Format

When a conversion is complete, the DREADY bit of the STATUS0 register is set to 1. If the CF4_CFG bits in the CONFIG1 register are equal to 11, the CF4/$\overline{\text{EVENT}}$/DREADY pin corresponds to DREADY and pulses high to indicate when seven new ADC results are ready. Note that the DREADY update rate depends on the data selected in the WF_SRC bits in the WFB_CFG register.

For the ADE9078, the modulator sampling rate (MODCLK) is fixed at 1.024 MHz (CLKIN/12 = 12.288 MHz/12). The output data rate of the sinc4 filter is 16 kHz (SINC_ODR = MODCLK/64), whereas the low-pass filter/decimator stage yields an output rate four times slower than the sinc4 filter output rate (SINC_ODR). Figure 35 shows the digital filtering, which takes the 1.024 MHz ADC samples and creates waveform information at a decimated rate of 16 kHz or 4 kHz.

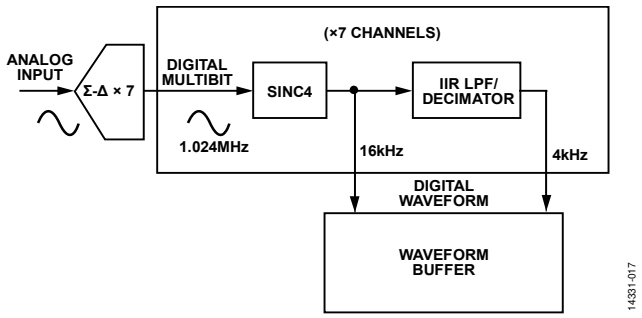

Figure 35. Datapath Following ADC Stage

The output data rates are summarized in Table 7.

Table 7. Output Data Rates

Parameter	Data Rate
CLKIN Frequency	12.288 MHz
ADC Modulator Clock, MODCLK	1.024 MHz
Sinc4, SINC_ODR	16 kHz
Low-Pass Filter	4 kHz
Bandwidth (Pass Band)	0.672 kHz

The ADC data in the waveform buffer is stored as 32-bit data by shifting left by 4 bits and sign extending, as shown in Figure 36.

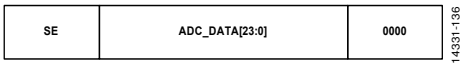

Figure 36. Format for the ADC Data Stored in the Waveform Buffer, x_SINC_DAT and x_LPF_DAT Registers

The expected output code from the sinc4 filter when input is at 1 V peak is 4,190,000 decimal (d), which corresponds to a value of 67,110,000d in the waveform buffer. The expected output code from the decimator filter when input is at 1 V peak is 4,660,000d, which corresponds to a value of 74,520,000d in the waveform buffer (see the Waveform Buffer section for more information).

Voltage Reference

The ADE9078 supports a 1.25 V internal reference. The temperature drift of the reference voltage is ±5 ppm/°C typical, ±20 ppm/°C maximum. An external reference can be connected between the REF and REFGND pins. Set the EXT_REF bit of the CONFIG1 register when using an external voltage reference, which disables the internal reference buffer.

CRYSTAL OSCILLATOR/EXTERNAL CLOCK

The ADE9078 contains a crystal oscillator. Alternatively, a digital clock signal can be applied at the CLKIN pin of the ADE9078.

When a crystal is used as the clock source for the ADE9078, attach the crystal and the ceramic capacitors, with capacitances of C_{L1} and C_{L2}, as shown in Figure 37. It is not recommended to attach an external feedback resistor in parallel to the crystal.

When a digital clock signal is applied at the CLKIN pin, the inverted output is available at the CLKOUT pin. This output is not buffered internally and cannot drive any other external devices directly. Note that CLKOUT is available in the PSM0 and PSM1 operating modes only.

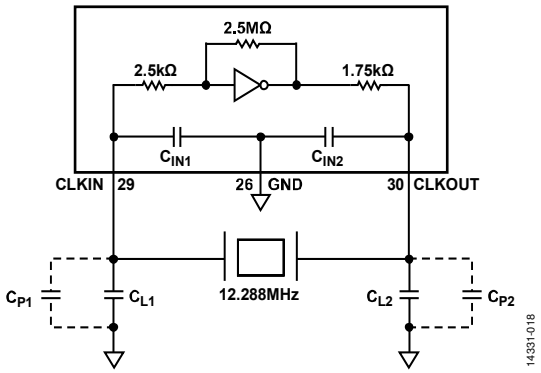

Figure 37. Crystal Application Circuit

Crystal Selection

The transconductance of the crystal oscillator circuit in the ADE9078, g_m, is provided in Table 1. It is recommended to have three to five times more g_m than the calculated $g_{mCRITICAL}$ for the crystal.

The following equation shows how to calculate the $g_{mCRITICAL}$ for the crystal from information given in the crystal data sheet:

$$g_{mCRITICAL} = 4 \times ESR_{MAX} \times 1000 \times (2\pi \times f_{CLK\,(Hz)})^2 \times (C0 + C_L)^2$$

where:

$g_{mCRITICAL}$ is the minimum gain required to start the crystal in mA/V.
ESR_{MAX} is the maximum electrical series resistance (ESR), expressed in Ω.
$f_{CLK\,(Hz)}$ is 12.288 MHz, expressed in Hz as 12.288×10^6.
$C0$ is the maximum shunt capacitance, expressed in farads.
C_L is the total load capacitance, expressed in farads.

Crystals with low ESR and smaller load capacitance have a lower $g_{mCRITICAL}$ and are easier to drive.

The evaluation board of the ADE9078 uses a crystal manufactured by Abracon (ABLS-12.288MHZ-L4Q-T), which has a maximum ESR of 50 Ω, a load capacitance of 18 pF, and a maximum shunt capacitance of 7 pF, which results in a $g_{mCRITICAL}$ of 0.75 mA/V, as follows:

$$g_{mCRITICAL} = 4 \times ESR_{MAX} \times 1000 \times (2\pi \times f_{CLK\,(Hz)})^2 \times (C0 + C_L)^2$$

$$g_{mCRITICAL} = 4 \times 50 \times 1000 \times (2\pi \times 12.288 \times 10^6)^2 \times (7 \times 10^{-120} + 18 \times 10^{-12})^2 = 0.75 \text{ mA/V}$$

The gain of the crystal oscillator circuit in the ADE9078, the g_m, provided in Table 1 is more than $5 \times g_{mCRITICAL}$; thus, there is sufficient margin to start up this crystal.

Load Capacitor Calculation

Crystal manufacturers specify the combined load capacitance across the crystal, C_L. The capacitances in Figure 37 can be described as follows:

- C_{P1} and C_{P2} are the parasitic capacitances on the clock pins formed due to PCB traces.
- C_{IN1} and C_{IN2} are the internal capacitances of the CLKIN and CLKOUT pins, respectively.
- C_{L1} and C_{L2} are the selected load capacitors to reach the correct combined C_L for the crystal.

The internal pin capacitances, C_{IN1} and C_{IN2}, are 4 pF each, as given in Table 1. To find the values of C_{P1} and C_{P2}, measure the capacitance on each of the clock pins of the PCB, CLKIN, and CLKOUT, respectively, with respect to the AGND pin. If the measurement is performed after soldering the IC to the PCB, subtract the 4 pF internal capacitance of the clock pins to determine the actual value of parasitic capacitance on each of the crystal pins.