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Energy Metering IC with Autocalibration

Data Sheet

ADE9153A

FEATURES

- ***m*Sure autocalibration**
  - **Automatic calibration based on a direct measurement of the full signal path**
  - **Calibration procedure not requiring a reference meter**
  - ***m*Sure autocalibration Class 1 meter guaranteed**
- **3 high performance ADCs**
  - **88 dB SNR**
  - **High gain current channel: ±26.04 mV peak, 18.4 mV rms input at highest gain setting**
- **Advanced metrology feature set**
  - **WATT, VAR, VA, Wh, VARh, and VAh**
  - **Supports active energy standards: IEC 62053-21; IEC 62053-22; EN50470-3; OIML R46; and ANSI C12.20**
  - **Supports reactive energy standards: IEC 62053-23 and IEC 62053-24**
  - **Current and voltage rms measurement**
  - **Power quality measurements**
- **Operating temperature, industrial range: −40°C to +85°C**

APPLICATIONS

- **Single-phase energy meters**
- **Energy and power measurement**
- **Street lighting**
- **Smart power distribution system**
- **Machine health**

GENERAL DESCRIPTION

The ADE9153A[1] is a highly accurate, single-phase, energy metering IC with autocalibration. The *m*Sure® autocalibration feature allows a meter to automatically calibrate the current and voltage channels without using an accurate source or an accurate reference meter when a shunt resistor is used as a current sensor. Class 1 and Class 2 meters are supported by *m*Sure autocalibration.

The ADE9153A incorporates three high performance analog-to-digital converters (ADCs), providing an 88 dB signal-to-noise ratio (SNR). The ADE9153A offers an advanced metrology feature set of measurements like line voltage and current, active energy, fundamental reactive energy, and apparent energy calculations, and current and voltage rms calculations. ADE9153A includes power quality measurements such as zero crossing detection, line period calculation, angle measurement, dip and swell, peak and overcurrent detection, and power factor measurements. Each input channel supports independent and flexible gain stages. Current Channel A is ideal for shunts, having a flexible gain stage and providing full-scale input ranges from 62.5 mV peak down to 26.04 mV peak. Current Channel B has gain stages of 1×, 2×, and 4× for use with current transformers (CTs). A high speed, 10 MHz, serial peripheral interface (SPI) port allows access to the ADE9153A registers.

Note that throughout this data sheet, multifunction pins, such as ZX/DREADY/CF2, are referred to either by the entire pin name or by a single function of the pin, for example, CF2, when only that function is relevant.

The ADE9153A operates from a 3.3 V supply and is available in a 32-lead LFCSP package.

TYPICAL APPLICATIONS CIRCUIT

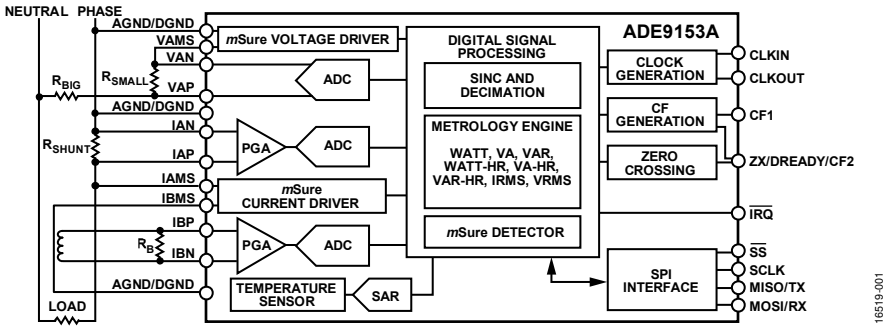

Figure 1.

[1] Protected by U.S. Patents 8,350,558; 8,010,304; WO2013038176 A3; 0113507 A1; 0253102 A1; 0354266 A1; and 0154029 A1.

Rev. 0 **Document Feedback**

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REVISION HISTORY

2/2018—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.97 V to 3.63 V, AGND = DGND = 0 V, on-chip reference, CLKIN = 12.288 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, and T_A = 25°C (typical), unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY (MEASUREMENT ERROR PER PHASE)					Percentage of the typical value derived from comparing the actual value with the typical-based expected values when a 10:1 signal is applied
Total Active Energy		0.1		%	Over a dynamic range of 3000 to 1, 10 sec accumulation programmable gain amplifier (PGA), AI_PGAGAIN = 16×
		0.2		%	AI_PGAGAIN = 38.4×
		0.25		%	Over a dynamic range of 10,000 to 1, 30 sec accumulation; AI_PGAGAIN = 16×
		0.5		%	AI_PGAGAIN = 38.4×
Fundamental Reactive Energy		0.1		%	Over a dynamic range of 3000 to 1, 10 sec accumulation; AI_PGAGAIN = 16×
		0.2		%	AI_PGAGAIN = 38.4×
		0.25		%	Over a dynamic range of 10,000 to 1, 30 sec accumulation AI_PGAGAIN = 16×
		0.5		%	AI_PGAGAIN = 38.4×
Total Apparent Energy		0.1		%	Over a dynamic range of 1000 to 1, 1 sec accumulation; AI_PGAGAIN = 16×
		0.2		%	AI_PGAGAIN = 38.4×
		0.25		%	Over a dynamic range of 3000 to 1, 10 sec accumulation AI_PGAGAIN = 16×
		0.5		%	AI_PGAGAIN = 38.4×
RMS Current (I_{RMS}) and Apparent Power (VA)		0.1		%	Over a dynamic range of 1000 to 1, 1 sec (averaging) AI_PGAGAIN = 16×, BI_PGAGAIN = 1×
		0.2		%	Over a dynamic range of 1000 to 1, 1 sec (averaging), AI_PGAGAIN = 38.4×
		0.3		%	Over a dynamic range of 3000 to 1, 1 sec (averaging), AI_PGAGAIN = 16×, BI_PGAGAIN = 1×
		0.6		%	Over a dynamic range of 3000 to 1, 1 sec (averaging), AI_PGAGAIN = 38.4×
RMS Voltage (V_{RMS})		0.2		%	Over a dynamic range of 1000 to 1, 1 sec (averaging)
Active Power (WATT), Fundamental Reactive Power (VAR)		0.25		%	Over a dynamic range of 3000 to 1, 1 sec, AI_PGAGAIN = 16×
		0.5		%	Over a dynamic range of 3000 to 1, 1 sec, AI_PGAGAIN = 38.4×
One Cycle RMS Current and Voltage Refreshed Each Half Cycle		0.5		%	Over a dynamic range of 500 to 1 on current and 250 to 1 on voltage
		1		%	Over a dynamic range of 1000 to 1 on current and 500 to 1 on voltage
Line Period Measurement		0.001		Hz	Resolution at 50 Hz
Voltage to Current Angle Measurement		0.036		Degrees	Resolution at 50 Hz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC					
PGA Gain Settings (xI_PGAGAIN)					
Current Channel A (Phase Shunt)		16, 24, 32, 38.4		V/V	PGA gain setting is referred to as gain
Current Channel B (Neutral CT)		1, 2, 4		V/V	PGA gain setting is referred to as gain
Pseudo Differential Input Voltage Range					
(IAP − IAN)	−1/gain		+1/gain	V	44.19 mV rms on Current Channel A, AI_PGAGAIN = 16×
(VAP − VAN)	−0.5		+0.5	V	353.6 mV rms on voltage channel
Differential Input Voltage Range					
(IBP − IBN)	−1/gain		+1/gain	V	707 mV rms on Current Channel B
Maximum Operating Voltage on the Analog Input Pins					
VAP	0		1.35	V	Voltage on the pin with respect to ground
IAP, IAN	−0.1125		+0.1125	V	Voltage on the IAx pin with respect to ground
IBP, IBN	0.35		1.45	V	Voltage on the IBx pin with respect to ground; internal common-mode voltage at IBx pin = 0.9 V
SNR					
Current Channel A					
AI_PGAGAIN = 16×		90		dB	V_{IN} is a full-scale signal
AI_PGAGAIN = 38.4×		88		dB	V_{IN} is a full-scale signal
Current Channel B					
BI_PGAGAIN = 1x		90		dB	V_{IN} is a full-scale signal
BI_PGAGAIN = 4x		78		dB	V_{IN} is a full-scale signal
Voltage Channel		87		dB	V_{IN} is a full-scale signal
ADC Output Pass Band (0.1 dB)		0.672		kHz	
ADC Output Bandwidth (−3 dB)		1.6		kHz	
Crosstalk		−120		dB	At 50 Hz or 60 Hz; see the Terminology section
AC Power Supply Rejection Ratio (AC PSRR)					At 50 Hz; see the Terminology section
Current Channel A		−115		dB	
Current Channel B		−100		dB	
Voltage Channel		−100		dB	
AC Common-Mode Rejection Ratio (AC CMRR)		−120		dB	At 50 Hz
ADC Gain Error					Percentage of error from the ideal value; see the Terminology section
Current Channel A		±0.2	±1.5	%	
Current Channel B		−2.0	±3.5	%	
Voltage Channel		−0.8	±3.0	%	
ADC Offset					
Current Channel A					See the Terminology section
AI_PGAGAIN = 16×		+0.04	±0.1	mV	
AI_PGAGAIN = 38.4×		−0.02	±0.05	mV	
Current Channel B		−0.26	±0.37	mV	
Voltage Channel		+0.35	±0.75	mV	
ADC Offset Drift		±0.5	±5	µV/°C	See the Terminology section

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Channel Drift (PGA, ADC, Internal Voltage Reference)					See the Terminology section
Current Channel A		±5	±30	ppm/°C	
Current Channel B		±20	±50	ppm/°C	
Voltage Channel		±20	±50	ppm/°C	
Differential Input Impedance (DC)					See the Terminology section
Current Channel A	5000	7800		kΩ	
Current Channel B	100	113		kΩ	
Voltage Channel	240	256		kΩ	
INTERNAL VOLTAGE REFERENCE					Nominal = 1.25 V ± 1 mV
Voltage Reference		1.25		V	T_A = 25°C at REFIN
Temperature Coefficient		±5	±30	ppm/°C	T_A = −40°C to +85°C; tested during device characterization
TEMPERATURE SENSOR					
Temperature Accuracy		±5		°C	−40°C to +85°C
Temperature Readout Step Size			0.3	°C	
CRYSTAL OSCILLATOR					All specifications at CLKIN = 12.288 MHz; the crystal oscillator is designed to interface with 100 µW crystals
Input Clock Frequency	12.287	12.288	12.289	MHz	±100 ppm
Internal Capacitance on CLKIN, CLKOUT		4		pF	
Internal Feedback Resistance Between CLKIN and CLKOUT		2.58		MΩ	
Transconductance (g_m)	5	8.7		mA/V	
EXTERNAL CLOCK INPUT					
Input Clock Frequency, CLKIN	12.287	12.288	12.289	MHz	±100 ppm
Duty Cycle	45:55	50:50	55:45		
CLKIN Logic Input Voltage					3.3 V tolerant
High, V_{INH}	1.2			V	
Low, V_{INL}			0.5	V	
LOGIC INPUTS—MOSI/RX, SCLK					
Input Voltage					
High, V_{INH}	2.4			V	
Low, V_{INL}			0.8	V	
Input Current, I_{IN}			11	µA	V_{IN} = 0 V
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
MISO/TX, $\overline{IRQ}$					
Output Voltage					
High, V_{OH}	2.5			V	I_{SOURCE} = 4 mA
Low, V_{OL}			0.4	V	I_{SINK} = 3 mA
Internal Capacitance, C_{IN}			10	pF	
CF1, CF2					
Output Voltage					
High, V_{OH}	2.4			V	I_{SOURCE} = 6 mA
Low, V_{OL}			0.8	V	I_{SINK} = 6 mA
Internal Capacitance, C_{IN}			10	pF	
LOW DROPOUT REGULATORS (LDOs)					
AVDD		1.9		V	
DVDD		1.7		V	
VDD2P5		2.5		V	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY					For specified performance
VDD Pin	2.97		3.63	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
VDD Pin Current, I_{DD}		9.3	12	mA	Consumption in operation, without *m*Sure running
		8.5		µA	When the ADE9153A is held in reset

AUTOCALIBRATION

VDD = 3.3 V, AGND = DGND = 0 V, on-chip reference, CLKIN = 12.288 MHz, T_A = 25°C (typical), I_{MAX} = 60 A rms, V_{NOM} = 230 V, R_{SHUNT_PHASE} = 200 µΩ, turns ratio on $CT_{NEUTRAL}$ = 2500:1, burden on $CT_{NEUTRAL}$ = 16.4 Ω, and $CT_{NEUTRAL}$ voltage potential divider of 1000:1 (990 kΩ and 1 kΩ resistors), unless otherwise noted. The values in Table 2 are specified for the system described; if the shunt or voltage potential divider is changed, the values in Table 2 change as well. For example, increasing the shunt value decreases the calibration time required for the phase current channel; conversely, decreasing the shunt value increases the calibration time.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
AUTOCALIBRATION					T_A = 25°C ±5 °C
Current Channel A (Phase Shunt)					
Calibration Time					
Turbo Mode					For more information on the power modes and calibration times, see the *m*Sure Autocalibration Feature section
0.353% Accuracy Target		16		sec	
0.25% Accuracy Target		45		sec	
Normal Mode					
0.353% Accuracy Target		40		sec	
0.25% Accuracy Target		115		sec	
Current Consumption					Additional consumption from 3.3 V supply
Turbo Mode		16		mA rms	With peak consumption of 33 mA
Normal Mode		9.3		mA rms	With peak consumption of 19 mA
Current Channel (Neutral CT)					
Calibration Time					For more information, see the *m*Sure Autocalibration Feature section
0.5 % Accuracy Target,					
Turbo Mode		12		sec	
Normal Mode		20		sec	
Current Consumption					Additional consumption from 3.3 V supply
Turbo Mode		16		mA rms	With peak consumption of 33 mA
Normal Mode		9.3		mA rms	With peak consumption of 19 mA
Voltage Channel					
Calibration Time					For more information, see the *m*Sure Autocalibration Feature section
0.353% Accuracy Target		25		sec	
0.25% Accuracy Target		85		sec	
Current Consumption		<1		mA rms	Additional consumption from 3.3 V supply

SPI TIMING CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	10			ns
SCLK Frequency	f_{SCLK}			10	MHz
SCLK Low Pulse Width	t_{SL}	40			ns
SCLK High Pulse Width	t_{SH}	40			ns
Data Output Valid After SCLK Edge	t_{DAV}			40	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	10			ns
Data Input Hold Time After SCLK Edge	t_{DHD}	10			ns
Data Output Fall Time	t_{DF}			10	ns
Data Output Rise Time	t_{DR}			10	ns
SCLK Fall Time	t_{SF}			10	ns
SCLK Rise Time	t_{SR}			10	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}			100	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0			ns

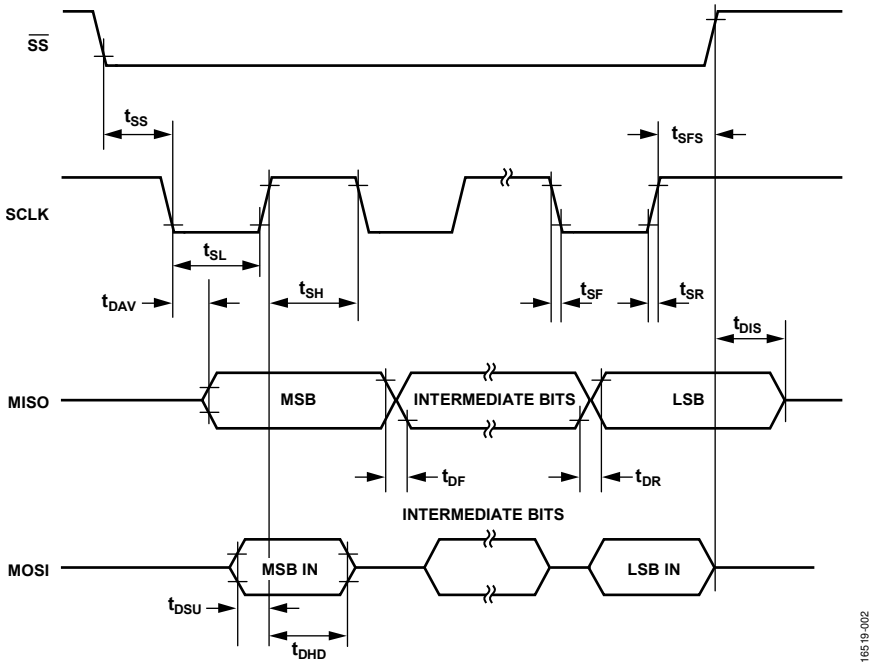

Figure 2. SPI Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
VDD to AGND/DGND	−0.3 V to +3.96 V
Analog Input Voltage to AGND/DGND, IAP, IAN, IBP, IBN, VP, VN[1]	−0.75 V to +2.2 V
Reference Input Voltage to AGND/DGND	−0.3 V to +2.2 V
Digital Input Voltage to AGND/DGND	−0.3 V to +3.96 V
Digital Output Voltage to AGND/DGND	−0.3 V to +3.96 V
Operating Temperature	
Industrial Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)[2]	260°C
Electrostatic Discharge (ESD)	
Human Body Model (HBM)	4 kV
Machine Model (MM)	200 V
Field Induced Charged Device Model (FICDM)	1.25 kV

[1] The rating of −0.75 V on the analog input pins is limited by protection diodes inside the ADE9153A. These pins were tested with 7.5 mA going to the pin to simulate a 30× overcurrent condition on the channel, based on the test circuit antialiasing resistor of 150 Ω.
[2] Analog Devices, Inc., recommends that reflow profiles used in soldering RoHS-compliant devices conform to J-STD-020D.1 from JEDEC. Refer to JEDEC for the latest revision of this standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} and θ_{JC} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-32-12[3]	27.83	2.10	°C/W

[1] The θ_{JA} measurement uses a 2S2P JEDEC test board.
[2] The θ_{JC} measurement uses a 1S0P JEDEC test board.
[3] All thermal measurements comply with JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

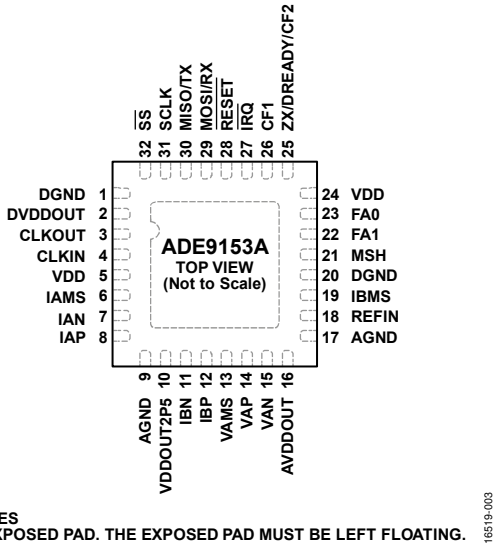

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 20	DGND	Digital Ground. These pins provide the ground reference for the digital circuitry in the ADE9153A and form the return path for the Current Channel A and Current Channel B *m*Sure currents.
2	DVDDOUT	1.7 V Output of the Digital LDO Regulator. Decouple this pin with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor to Pin 1 (DGND). Do not connect external load circuitry to this pin.
3	CLKOUT	Clock Output. Connect a crystal across CLKIN and CLKOUT to provide a clock source. An external buffer is required to drive other circuits from CLKOUT.
4	CLKIN	Master Clock Input. Connect a crystal across CLKIN and CLKOUT to provide a clock source. See the ADE9153A Technical Reference Manual for details on choosing a suitable crystal. Alternatively, an external clock can be provided at the logic input.
5, 24	VDD	Supply Voltage. These pins provide the supply voltage for the ADE9153A. Maintain the supply voltage at 3.3 V ± 10% for specified operation. Decouple these pins to AGND or DGND with a 4.7 µF capacitor in parallel with a ceramic 0.1 µF capacitor.
6	IAMS	Output for the *m*Sure Current Driver on Current Channel A (Phase Current Channel). IAMS is connected to the positive end of the shunt on the phase (to the side of the shunt closest to the load, on the same side as IAP).
7, 8	IAN, IAP	Analog Inputs for Current Channel A (Phase Current Channel). The IAP and IAN current channel is ideal for use with shunts. The IAP (positive) and IAN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±125 mV. These channels have an internal PGA gain of 16, 24, 32, and 38.4. Use these pins with the related input circuitry, as shown in Figure 37.
9, 17	AGND	Ground Reference for the Analog Circuitry. See Figure 37 for information on how to connect these ground pins.
10	VDDOUT2P5	2.5 V Output of the Analog LDO Regulator. Decouple this pin with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor to Pin 9 (AGND). Do not connect external load circuitry to this pin.
11, 12	IBN, IBP	Analog Inputs for Current Channel B (Neutral Current Channel). The IBP and IBN current channel is ideal for use with CTs. The IBP (positive) and IBN (negative) inputs are fully differential voltage inputs with a maximum differential level of ±1000 mV. These channels have an internal PGA gain of 1, 2, or 4. Use these pins with the related input circuitry, as shown in Figure 37.
13	VAMS	Path for *m*Sure on the Voltage Channel. VAMS is connected to the bottom end of the resistor divider, which is typically connected to the phase, as shown in Figure 1.
14, 15	VAP, VAN	Analog Inputs for the Voltage Channels. The VAP (positive) and VAN (negative) inputs are fully differential with an input level of 0.1 V to 1.7 V. Use these pins with the related input circuitry, as shown in Figure 37.
16	AVDDOUT	1.9 V Output of the Analog LDO Regulator. Decouple this pin with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor to Pin 17 (AGND). Do not connect external load circuitry to this pin.

Pin No.	Mnemonic	Description
18	REFIN	Voltage Reference. This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.25 V. Decouple this pin to Pin 17 (AGND) with a 0.1 µF ceramic capacitor in parallel with a 4.7 µF ceramic capacitor. After reset, the on-chip reference is enabled. An external reference source with 1.25 V ± 0.01% can also be connected at this pin.
19	IBMS	Output for the *m*Sure Current Driver on Current Channel B (Neutral Current Channel). IBMS is connected to a wire leading through the primary winding of the CT and back to Pin 20 (DGND).
21	MSH	External Capacitor Pin for the *m*Sure Current Driver. Connect an external 0.47 µF ceramic capacitor between the MSH pin and Pin 20 (DGND).
22	FA1	*m*Sure Capacitor, Positive Terminal. Connect an external capacitor of value 0.47 µF between FA0 and FA1.
23	FA0	*m*Sure Capacitor, Negative Terminal. Connect an external capacitor of value 0.47 µF between FA0 and FA1.
25	ZX/DREADY/CF2	Voltage Channel Zero-Crossing Output Pin. See the Voltage Channel section. This pin can be configured to output CF2 if necessary. See the description for CF1.
26	CF1	Calibration Frequency (CF) Logic Outputs. The CF1 and CF2 outputs provide proportional power information based on the CFxSEL bits in the CFMODE register. Use these outputs for operational and calibration purposes. Scale the full-scale output frequency by writing to the CFxDEN registers, respectively.
27	$\overline{\text{IRQ}}$	Interrupt Request Output. This pin is an active low logic output. See the Interrupts/Events section for information about events that trigger interrupts.
28	$\overline{\text{RESET}}$	Active Low Reset Input. To initiate a hardware reset, this pin must be brought low for a minimum of 10 µs.
29	MOSI/RX	Data Input for the SPI Port (MOSI) and Receive Pin for the UART (RX).
30	MISO/TX	Data Output for the SPI Port (MISO) and Transmit Pin for the UART (TX).
31	SCLK	Serial Clock Input for the SPI Port. All serial data transfers are synchronized to this clock. The SCLK pin has a Schmitt trigger input for use with a clock source that has a slow edge transition time (for example, transitioning to opto-isolator outputs).
32	$\overline{\text{SS}}$	Slave Select for the SPI Port.
	EPAD	Exposed Pad. The exposed pad must be left floating.

TYPICAL PERFORMANCE CHARACTERISTICS

ENERGY LINEARITY OVER SUPPLY AND TEMPERATURE

Energy characteristics obtained from a 50% of full scale, sinusoidal, 50 Hz voltage signal; the sinusoidal, 50 Hz, swept amplitude current signal is from 100% of full scale to 0.01% of full scale.

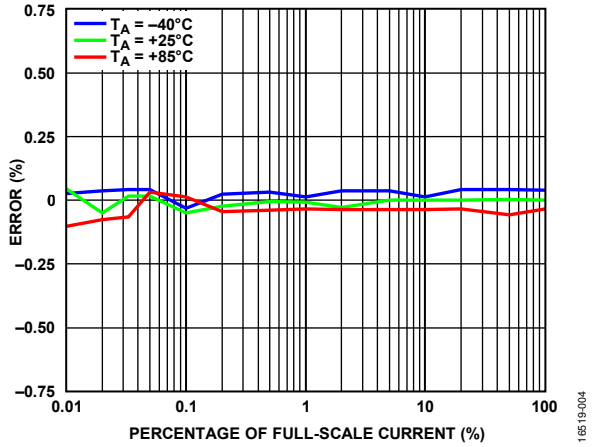

Figure 4. Total Active Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1, Current Channel A (AI) PGA Gain = 16×

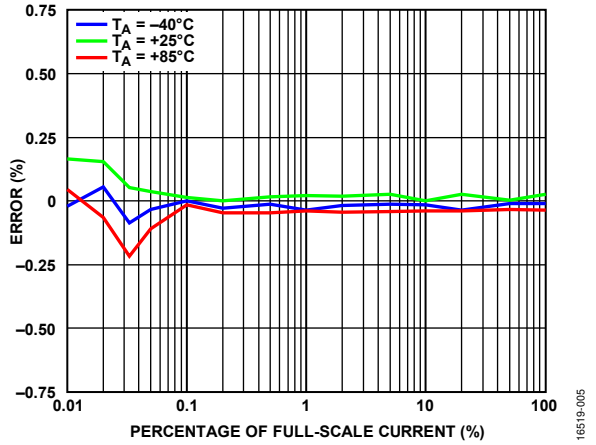

Figure 5. Total Active Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1, AI PGA Gain = 38.4×

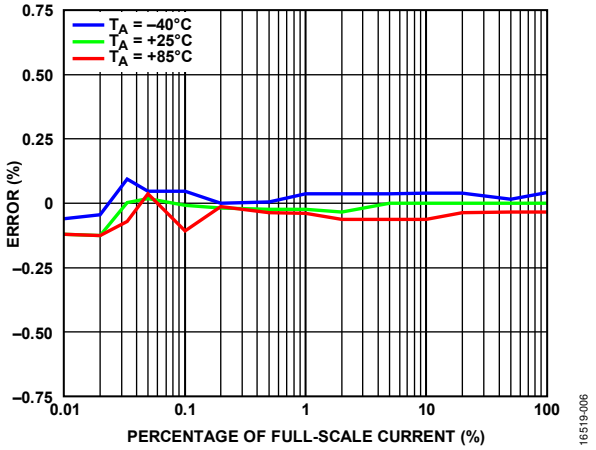

Figure 6. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 0, AI PGA Gain = 16×

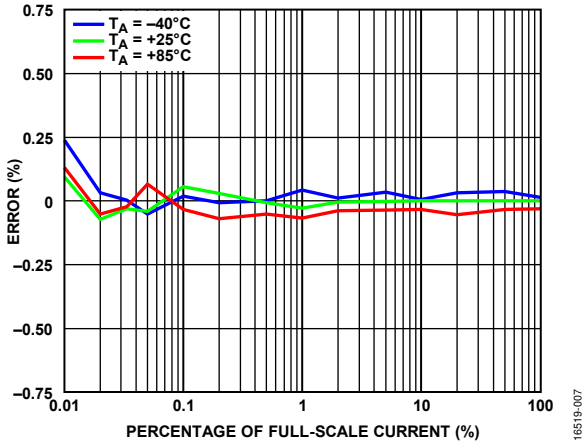

Figure 7. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 0, AI PGA Gain = 38.4×

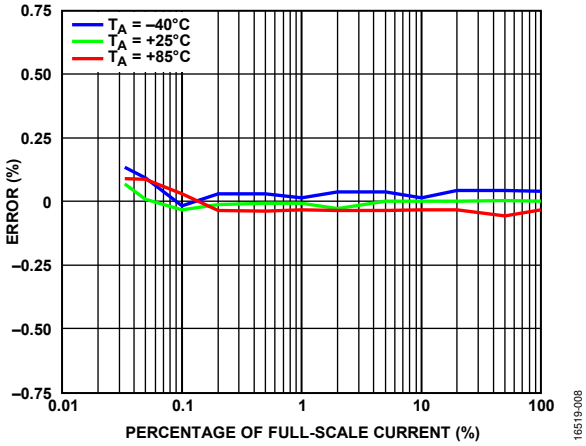

Figure 8. Total Apparent Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1, AI PGA Gain = 16×

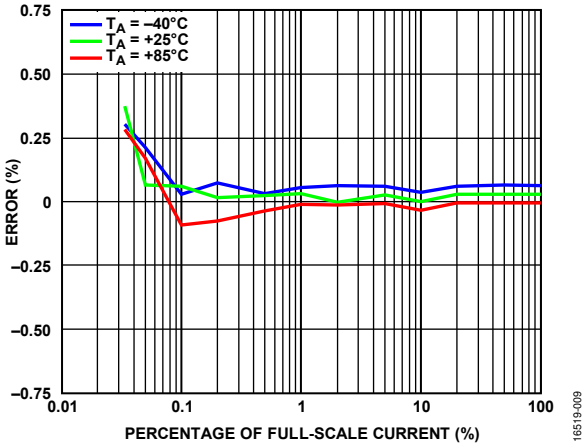

Figure 9. Total Apparent Energy Error as a Percentage of Full-Scale Current over Temperature, Power Factor = 1, AI PGA Gain = 38.4×

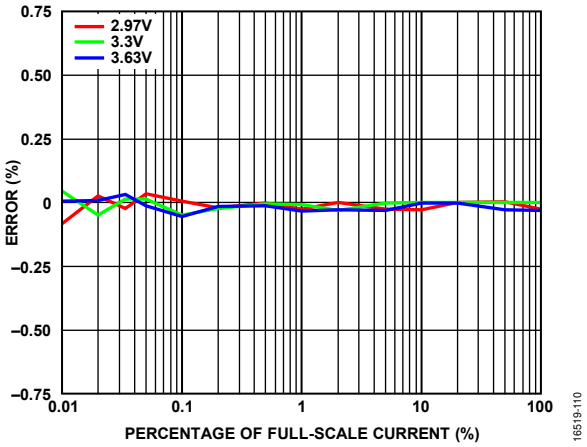

Figure 10. Total Active Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C, AI PGA Gain = 16×

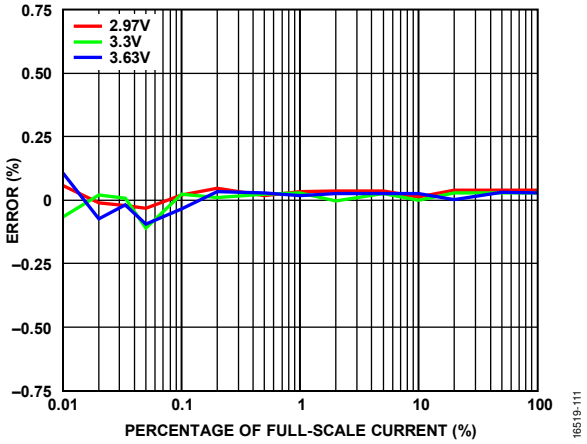

Figure 11. Total Active Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C, AI PGA Gain = 38.4×

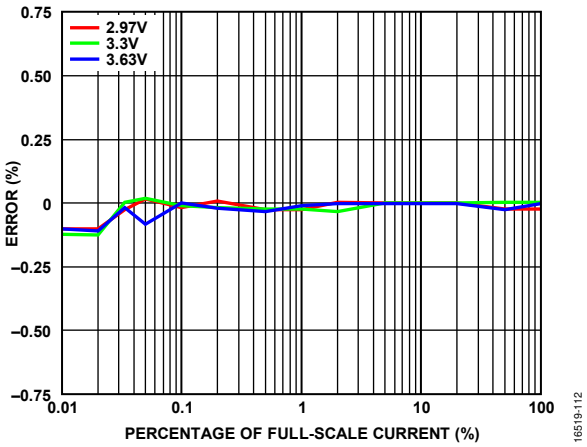

Figure 12. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 0, T_A = 25°C, AI PGA Gain = 16×

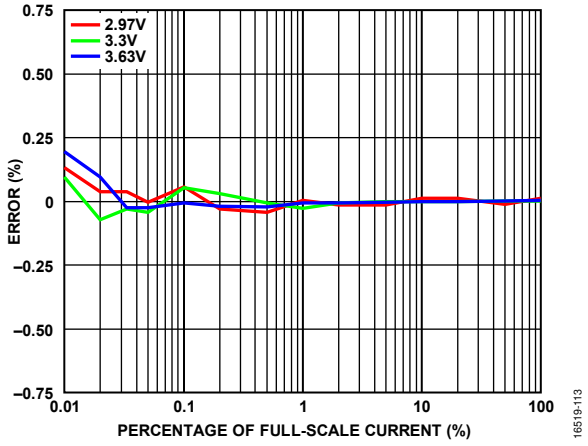

Figure 13. Fundamental Reactive Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 0, T_A = 25°C, AI PGA Gain = 38.4×

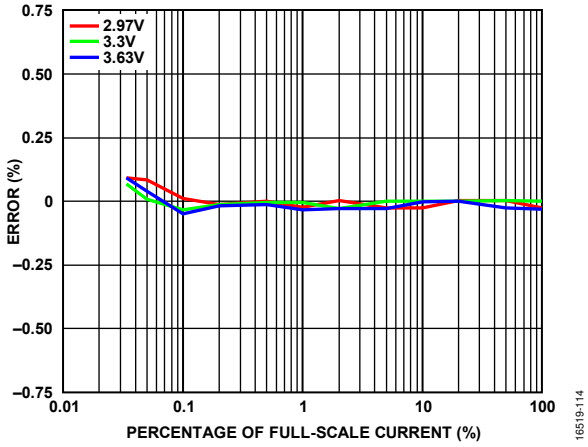

Figure 14. Total Apparent Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C, AI PGA Gain = 16×

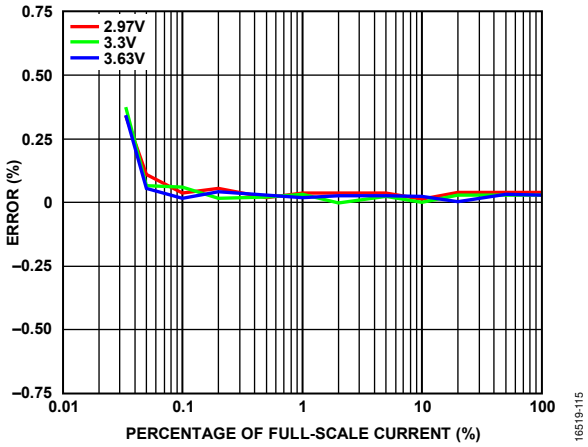

Figure 15. Total Apparent Energy Error as a Percentage of Full-Scale Current over Supply Voltage, Power Factor = 1, T_A = 25°C, AI PGA Gain = 38.4×

ENERGY ERROR OVER FREQUENCY AND POWER FACTOR

Energy characteristics obtained from a 50% of full scale, sinusoidal, 50 Hz voltage signal and a 10% of full scale, sinusoidal, 50 Hz, current signal over a variable frequency between 45 Hz and 65 Hz.

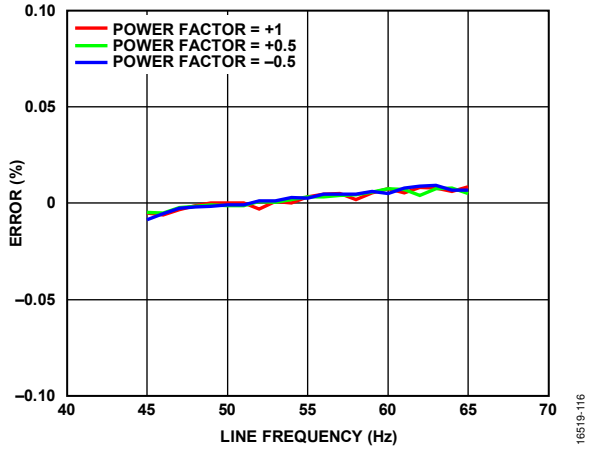

Figure 16. Total Active Energy Error vs. Line Frequency, Power Factor = −0.5, +0.5, and +1, AI PGA Gain = 38.4×

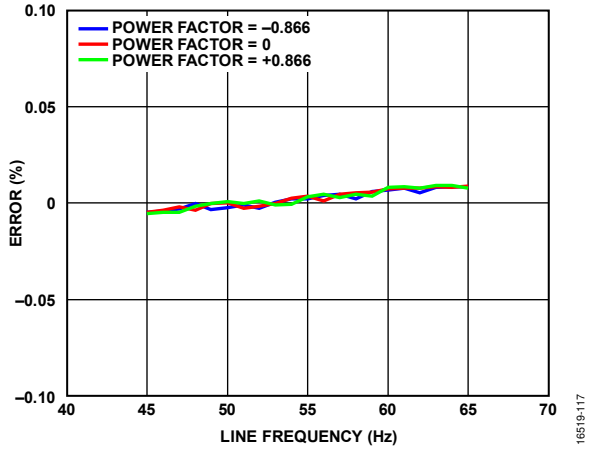

Figure 17. Fundamental Reactive Energy Error vs. Line Frequency, Power Factor = −0.866, +0.866, and 0, AI PGA Gain = 38.4×

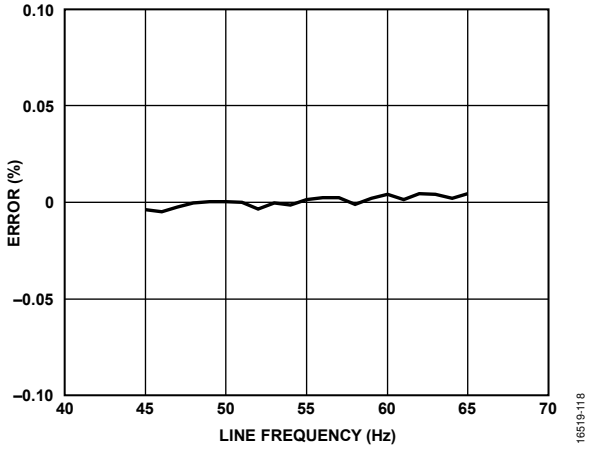

Figure 18. Total Apparent Energy Error vs. Line Frequency, AI PGA Gain = 38.4×

RMS LINEARITY OVER TEMPERATURE AND RMS ERROR OVER FREQUENCY

RMS linearity obtained with a sinusoidal, 50 Hz current and voltage signals with a swept amplitude from 100% of full scale to 0.033% of full scale.

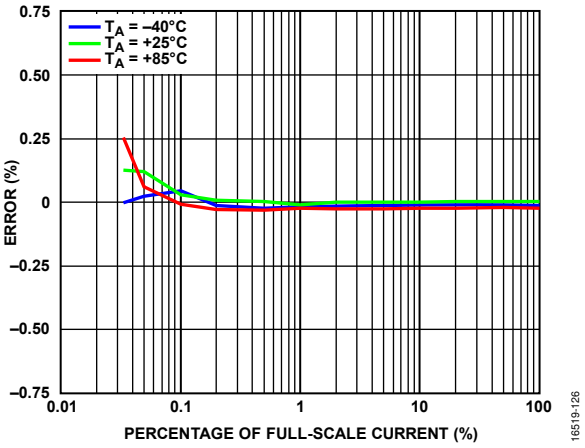

Figure 19. Current Channel A RMS Error as a Percentage of Full-Scale Current over Temperature, AI PGA Gain = 16×

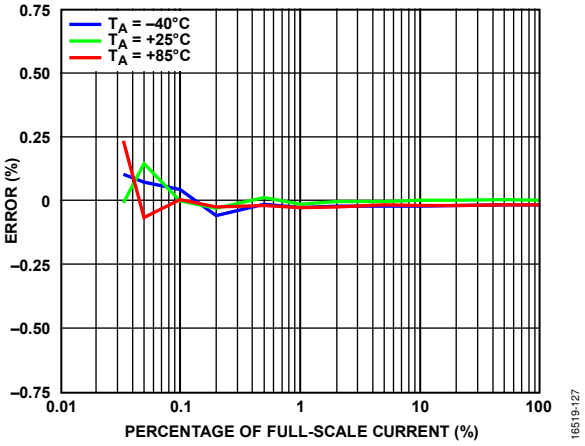

Figure 20. Current Channel A RMS Error as a Percentage of Full-Scale Current over Temperature, AI PGA Gain = 38.4×

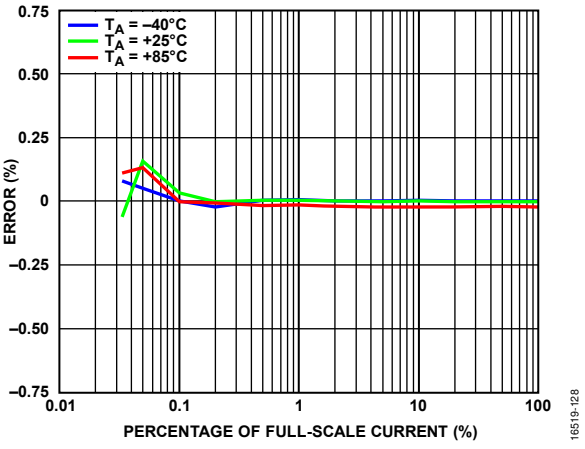

Figure 21. Current Channel B RMS Error as a Percentage of Full-Scale Current over Temperature

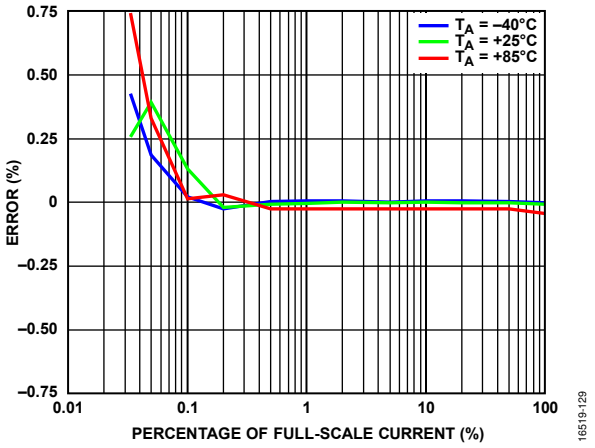

Figure 22. Voltage Channel RMS Error as a Percentage of Full-Scale Current over Temperature

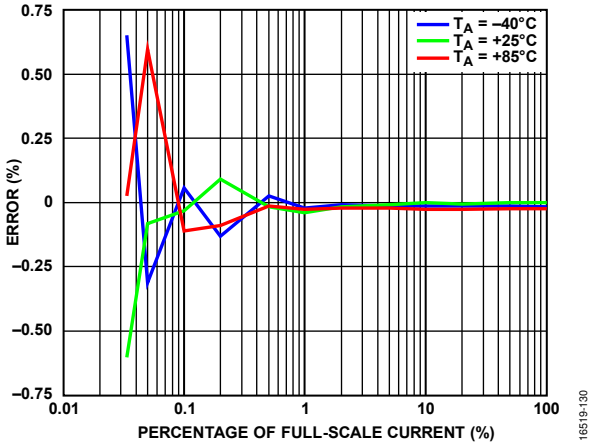

Figure 23. Current Channel A RMS Offset Error as a Percentage of Full-Scale Current over Temperature, AI PGA Gain = 16×

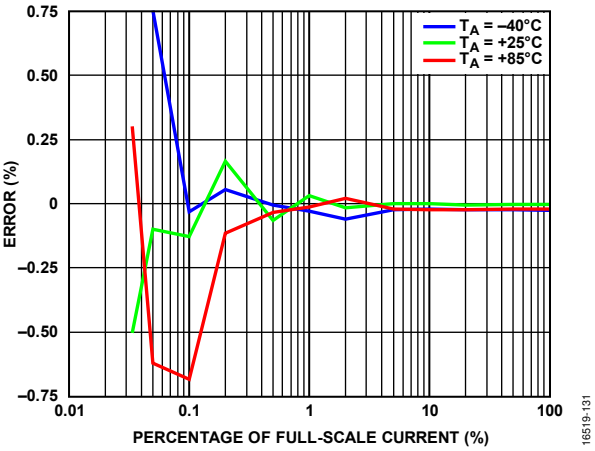

Figure 24. Current Channel A RMS Offset Error as a Percentage of Full-Scale Current over Temperature, AI PGA Gain = 38.4×

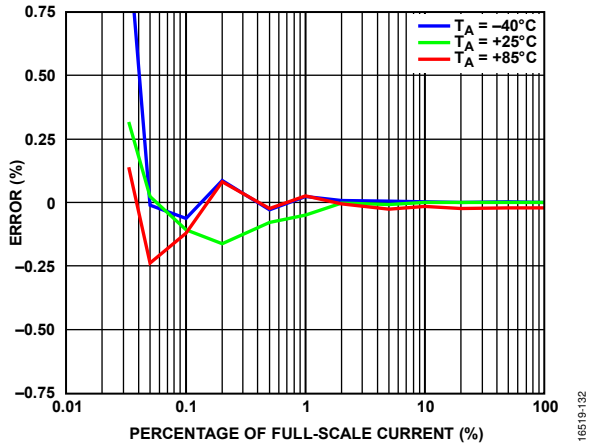

Figure 25. Current Channel B RMS Offset Error as a Percentage of Full-Scale Current over Temperature

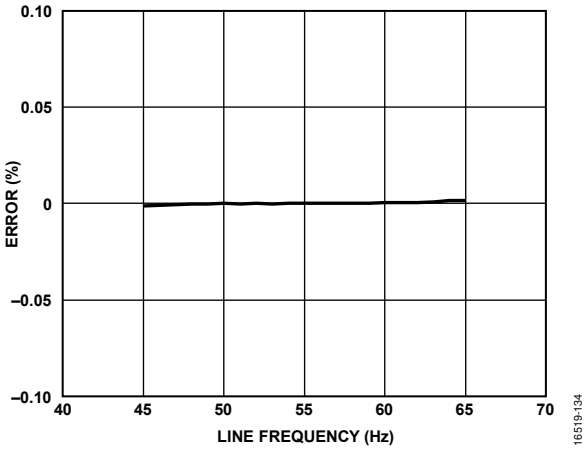

Figure 27. Current Channel A RMS Error vs. Line Frequency

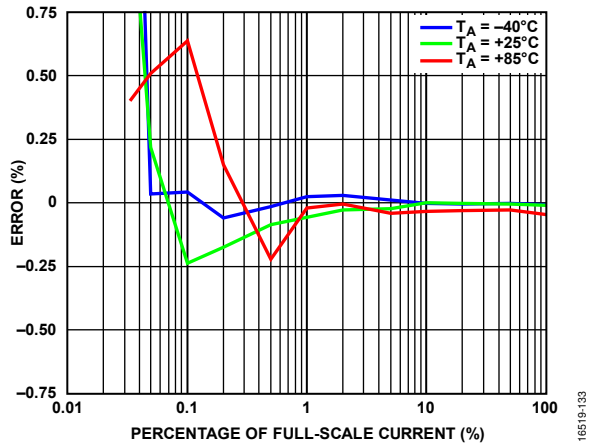

Figure 26. Voltage Channel RMS Offset Error as a Percentage of Full-Scale Current over Temperature

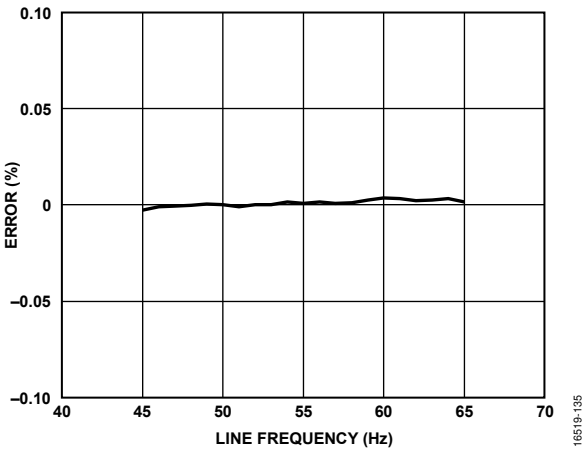

Figure 28. Current Channel B RMS Error vs. Line Frequency

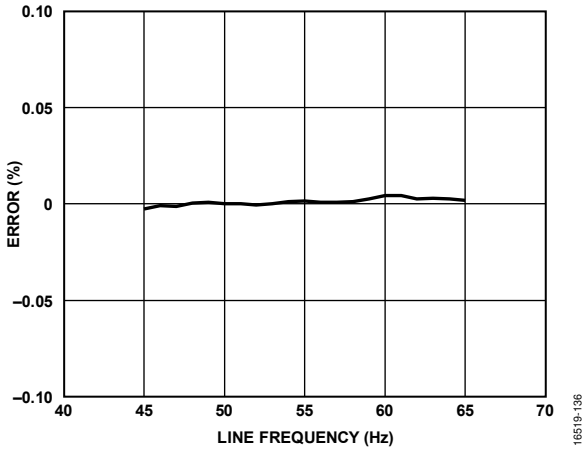

Figure 29. Voltage Channel RMS Error vs. Line Frequency

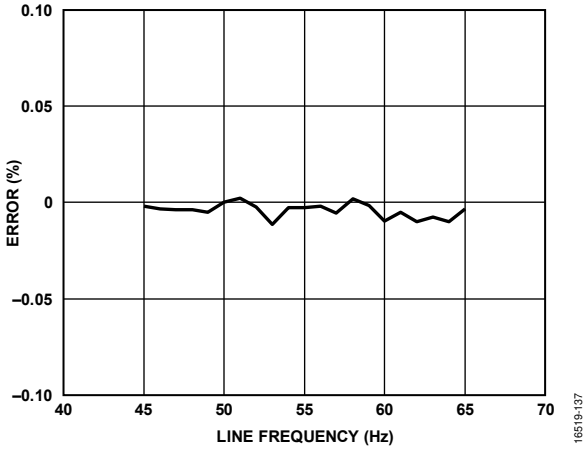

Figure 30. Current Channel A RMS Overcurrent Error vs. Line Frequency

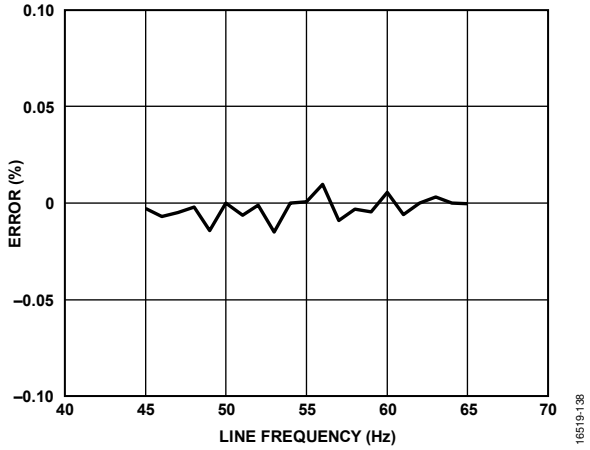

Figure 31. Current Channel B RMS Overcurrent Error vs. Line Frequency

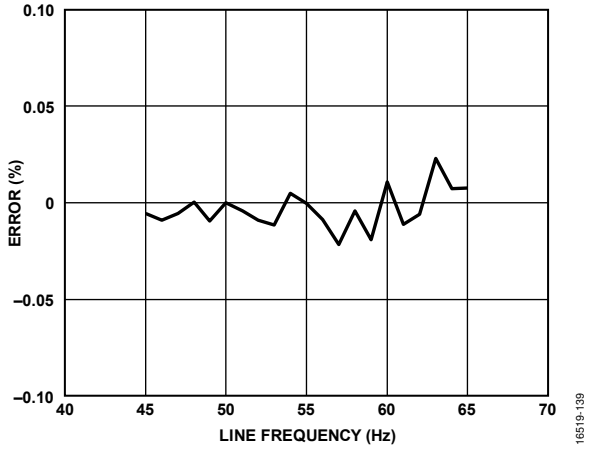

Figure 32. Voltage Channel RMS Overcurrent Error vs. Line Frequency

SIGNAL-TO-NOISE RATIO (SNR) PERFORMANCE OVER DYNAMIC RANGE

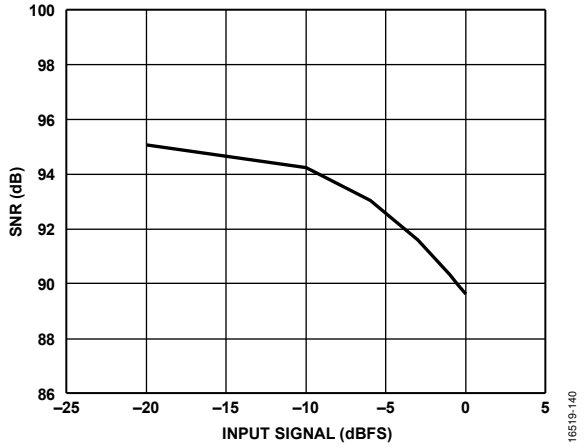

Figure 33. Current Channel A SNR with Respect to Full Scale, AI PGA Gain = 16×

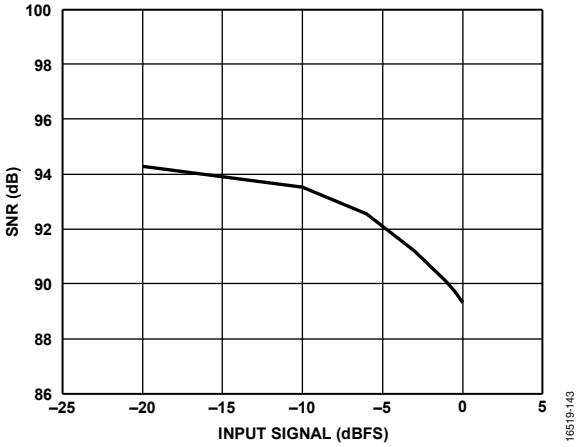

Figure 35. Current Channel B SNR with Respect to Full Scale

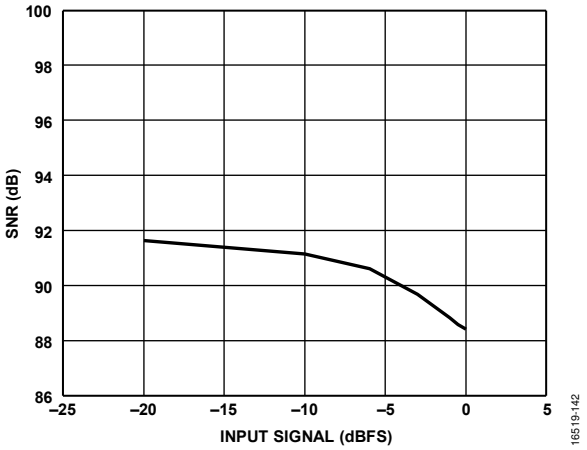

Figure 34. Current Channel A SNR with Respect to Full Scale, AI PGA Gain = 38.4×

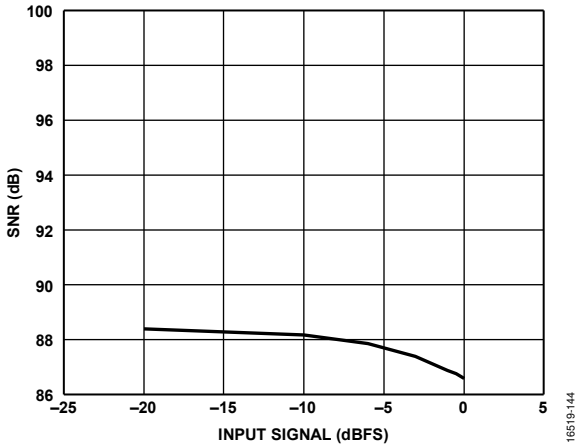

Figure 36. Voltage Channel SNR with Respect to Full Scale

TEST CIRCUIT

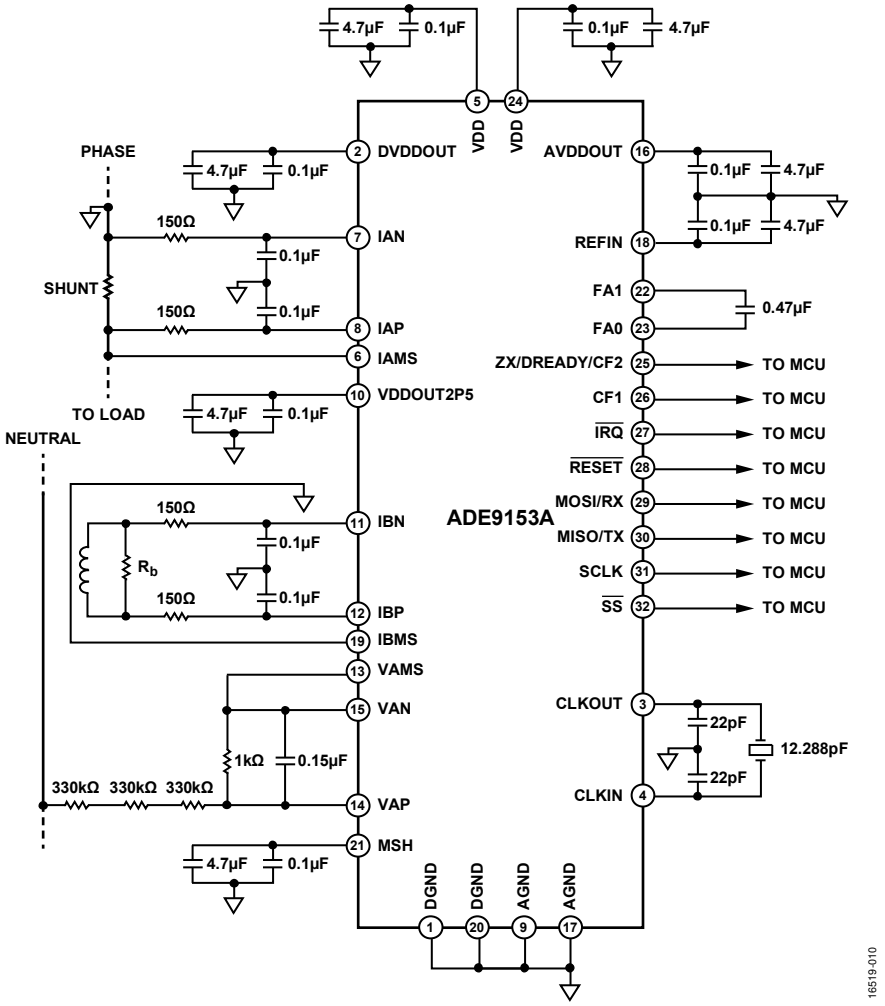

Figure 37. Test Circuit

TERMINOLOGY

Crosstalk
Crosstalk is measured by grounding one channel and applying a full-scale 50 Hz or 70 Hz signal on all the other channels. The crosstalk is equal to the ratio between the grounded ADC output value and its ADC full-scale output value. The ADC outputs are acquired for 200 sec. Crosstalk is expressed in decibels.

Differential Input Impedance (DC)
The differential input impedance represents the impedance between the IAP and IAN pair, the IBP and IBN pair, or the VAP and VAN pair.

ADC Offset
ADC offset is the difference between the average measured ADC output code with both inputs connected to ground and the ideal ADC output code of zero. ADC offset is expressed in mV.

ADC Offset Drift over Temperature
The ADC offset drift is the change in offset over temperature. It is measured at −40°C, +25°C, and +85°C. Calculate the offset drift over temperature as follows:

$$Drift = \max\left(\left|\frac{Offset(-40°C) - Offset(+25°C)}{(-40°C - (+25°C))}\right|, \left|\frac{Offset(+85°C) - Offset(+25°C)}{(+85°C - (+25°C))}\right|\right)$$

Offset drift is expressed in µV/°C.

Channel Drift over Temperature
The channel drift over temperature coefficient includes the temperature variation of the PGA and ADC gain when using the internal voltage reference. This coefficient represents the overall temperature coefficient of one channel. With the internal voltage reference, the ADC gain is measured at −40°C, +25°C, and +85°C. Then, the temperature coefficient is calculated as follows:

$$Drift = \max\left(\left|\frac{Gain(-40°C) - Gain(+25°C)}{Gain(+25°C) \times (-40°C - +25°C)}\right|, \left|\frac{Gain(+85°C) - Gain(+25°C)}{Gain(+25°C) \times (+85°C - +25°C)}\right|\right)$$

Gain drift is measured in ppm/°C.

ADC Gain Error
The gain error in the ADCs represents the difference between the measured ADC output code (minus the offset) and the ideal output code when an external voltage reference of 1.25 V is used. The difference is expressed as a percentage of the ideal code and represents the overall gain error of one channel.

AC Power Supply Rejection (AC PSRR)
AC PSRR quantifies the measurement error as a percentage of reading when the dc power supply is V_{NOM} and modulated with ac and the inputs are grounded. For the ac PSRR measurement, 100 sec of samples are captured with nominal supplies (3.3 V) and a second set is captured with an additional ac signal (233 mV rms at 100 Hz) introduced onto the supplies. Then, the PSRR is expressed as PSRR = $20 \log_{10}(V_{RIPPLE}/V_{NOMINAL})$.

Signal-to-Noise Ratio (SNR)
SNR is calculated by inputting a 50 Hz signal, and acquiring samples over 10 sec. The amplitudes for each frequency, up to the bandwidth given in Table 1 as the ADC output bandwidth (−3 dB), are calculated. To determine the SNR, the signal at 50 Hz is compared to the sum of the power from all the other frequencies, removing power from its harmonics. The value for SNR is expressed in decibels.

ADC Output Pass Band
The ADC output pass band is the bandwidth within 0.1 dB, resulting from the digital filtering in the sinc4 filter and sinc4 filter + infinite impulse response (IIR), low-pass filter (LPF).

ADC Output Bandwidth
The ADC output bandwidth is the bandwidth within −3 dB, resulting from the digital filtering in the sinc4 and sinc4 + IIR LPF.

Speed of Convergence
The speed of convergence is the time it takes for *m*Sure to reach a certain level of accuracy. This speed, or time required, is logarithmically proportional to the required accuracy. In other words, if a greater accuracy is required in *m*Sure autocalibration, the time required increases logarithmically.

Similarly, the speed is related to the power mode in which *m*Sure is being run: the lower the power mode, the slower the speed of convergence. This relationship is shown in Table 2 for the specified system. The speed of convergence determines the time it takes to complete the autocalibration process and to reach a certain specified accuracy.

Absolute Accuracy
Absolute accuracy takes into account the accuracy of the *m*Sure reference. The speed of convergence to reach this accuracy depends on the time of an *m*Sure autocalibration run. The longer the time of an *m*Sure autocalibration run, the greater the accuracy.

Certainty of Estimation
The certainty of the *m*Sure estimation, which is also referred to as simply certainty (CERT), is a metric of the precision of the *m*Sure measurement. This certainty is displayed as a percentage; the lower the value, the more confidence there is in the estimation value.

Conversion Constant
In this data sheet, the conversion constant (CC) is the value that *m*Sure returns when estimating the transfer function of the sensor and front end. This value is in units of A/code or V/code, depending on which channel the estimation occurs.

THEORY OF OPERATION

*m*SURE AUTOCALIBRATION FEATURE

The ADE9153A offers *m*Sure autocalibration technology, enabling the automatic calibration of the current and voltage channel accurate, automatic calibration. Autocalibration features have two main components: absolute accuracy and the speed of convergence (see the Terminology section for more details).

When performing autocalibration, the current channels, AI and BI, can be run in two power modes: turbo mode and normal mode. The power mode is a trade-off between the speed of convergence and current consumption. In turbo mode, the speed of convergence is 4× faster and the current consumption is only 2× higher when compared to normal mode, which means that the average consumption over a full run is less than in low power mode, but the instantaneous consumption is higher, as shown in Figure 38.

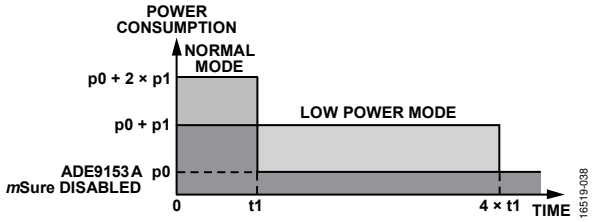

Figure 38. mSure Autocalibration Power Modes to Same Certainty

The ADE9153A can perform the autocalibration of a meter without requiring an accurate source or reference meter. By powering up the meter, the CC of each channel can be measured, and that requirement alone is enough to perform the autocalibration.

After the meter is powered, the autocalibration feature can be run on each channel, one at a time, by using the MS_ACAL_CFG register. Each channel has a set amount of run time. After each channel finishes a run, the certainty of the measurements are confirmed with the MS_ACAL_xCERT registers. Then, the MS_ACAL_xCC register can be used to calculate a gain value that calibrates the meter.

*m*Sure System Warning Interrupts

A set of interrupts in the ADE9153A are dedicated to alerting the user regarding any issues during an *m*Sure autocalibration. These alerts are all indicated as a bit in the MS_STATUS_IRQ register, which is a Tier 2 status register as described in the Interrupts/Events section.

The MS_CONFERR bit is set if a run of *m*Sure is incorrectly set up with the MS_ACAL_CFG register. Clear these registers to 0 and check the settings being written before starting another run.

The MS_ABSENT bit is set if the *m*Sure signal is not detected. If this bit is triggered, wiring in the meter may be incorrect or broken.

The MS_TIMEOUT bit is set if autocalibration is left to run for more than the 600 sec limit of the system. If this interrupt is triggered, ensure that the runs of *m*Sure are being correctly handled in terms of enabling and disabling *m*Sure when appropriate.

The MS_SHIFT bit is set when there is a shift in the CC value that occurs in the middle of a run. This setting means that an event at the meter level changed the CC before the run finished and another run must be performed to achieve a more accurate value. The certainty in this case is high, >50,000 ppm.

Figure 39 to Figure 41 show the speed of convergence of the *m*Sure result (the CC value). As the value of the shunt increases, or as the gain of the PGA increases, the speed of convergence also increases due to the signal size being larger. These are both parameters that must be set based on the overall system, taking into account factors such as the maximum current being measured. Figure 39 to Figure 41 show how the speed of convergence is influenced from factors in a system.

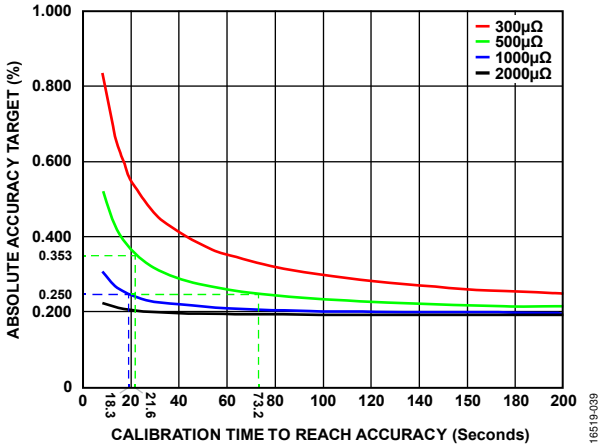

Figure 39. Speed of Convergence for Autocalibration (Shunt Channel, Normal Mode) Based on Shunt Value

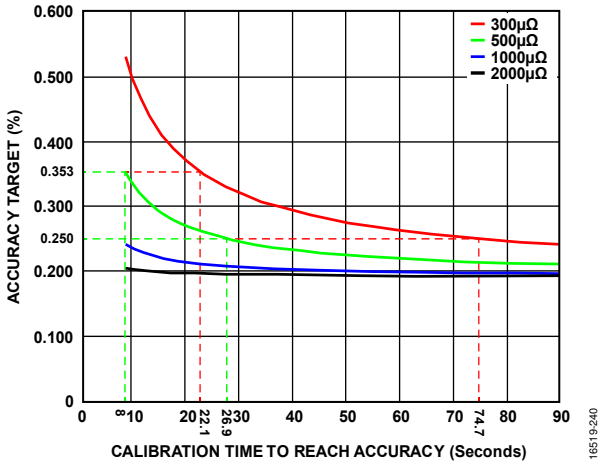

Figure 40. Speed of Convergence for Autocalibration (Shunt Channel, Turbo Mode) Based on Shunt Value

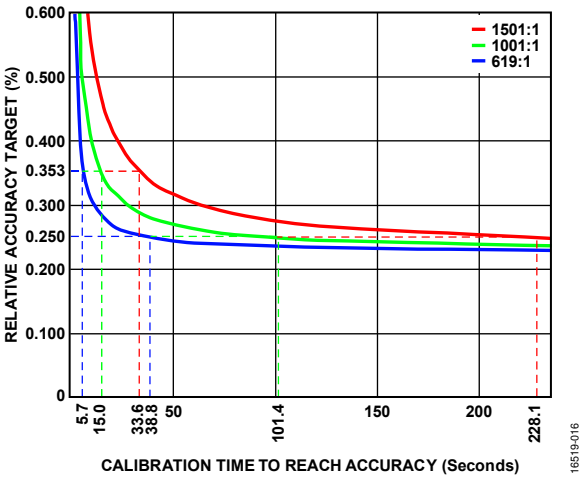

Figure 41. Speed of Convergence for Autocalibration (Voltage Channel) Based on the Potential Divider Ratio

MEASUREMENTS

Current Channel

The ADE9153A has two current channels. Channel A is optimized for use with a shunt, and Channel B is for use with a current transformer. The current channel datapaths for Channel A and Channel B are shown in Figure 42 and Figure 43, respectively.

Current Channel Gain, xIGAIN

The ADE9153A provides current gain calibration registers, AIGAIN and BIGAIN, with one register for each channel.

The current channel gain varies with xIGAIN, as shown in the following equation:

$$Current\ Channel\ Gain = \left(1 + \frac{xIGAIN}{2^{27}}\right)$$

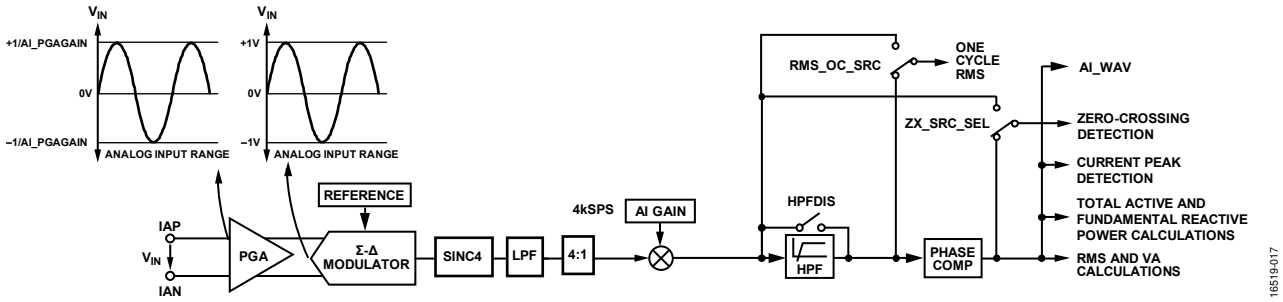

Figure 42. ADE9153A Current Channel A Datapath

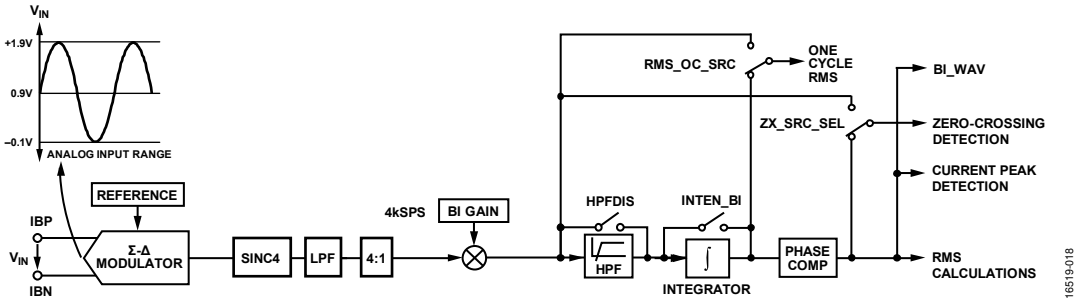

Figure 43. ADE9153A Current Channel B Datapath

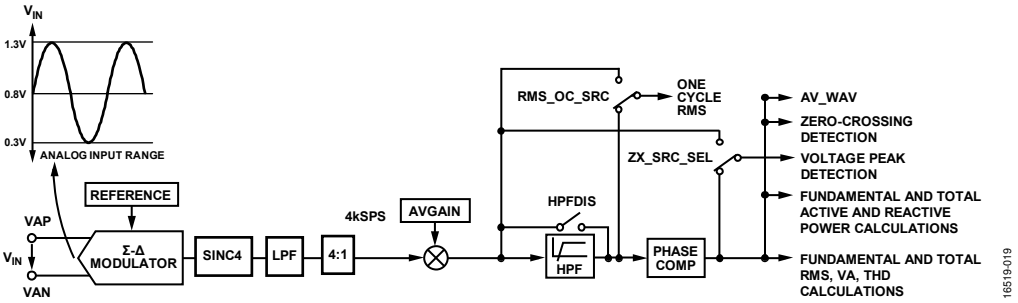

Figure 44. ADE9153A Voltage Channel Datapath

High-Pass Filter

A high-pass filter removes dc offsets for accurate rms and energy measurements. This filter is enabled by default and features a corner frequency of 1.25 Hz.

To disable the high-pass filter on all current and voltage channels, set the HPFDIS bit in the CONFIG0 register. The corner frequency is configured with the HPF_CRN bits in the CONFIG2 register.

Digital Integrator

A digital integrator is included on Current Channel B for the possibility of interfacing with a di/dt current sensor, also known as Rogowski coils. It is important to take note that the integrator cannot be used with any of the *m*Sure functions. To configure the digital integrator, use the INTEN_BI bits in the CONFIG0 register. The digital integrator is disabled by default.

Phase Compensation

The ADE9153A provides a phase compensation register for each current channel: APHASECAL and BPHASECAL. The phase calibration range is −15° to +2.25° at 50 Hz and −15° to +2.7° at 60 Hz.

Use the following equation to calculate the xPHASECAL value for a given phase correction (φ)° angle. Phase correction (φ)° is positive to correct a current that lags the voltage, and negative to correct a current that leads the voltage, as seen in a current transformer.

$$xPHASECAL = \left(\frac{\sin((\varphi - \omega) + \sin\omega}{\sin(2\omega - \varphi)} \right) \times 2^{27}$$

$$\omega = 2\pi \times f_{LINE}/f_{DSP}$$

where:
f_{LINE} is the line frequency.
f_{DSP} = 4 kHz.

Voltage Channel

The ADE9153A has a single voltage channel with the datapath shown in Figure 44. The AVGAIN register calibrates the voltage channel and has the same scaling as the xIGAIN registers.

RMS and Power Measurements

The ADE9153A calculates total values of rms current, rms voltage, active power, fundamental reactive power, and apparent power. The algorithm for computing the fundamental reactive power requires initialization of the network frequency using the SELFREQ bit in the ACCMODE register and the nominal voltage in the VLEVEL register.

Calculate the VLEVEL value according to the following equation:

$$VLEVEL = x \times 1{,}444{,}084$$

where x is the dynamic range of the nominal voltage input signal with respect to full scale.

For example, if the signal is at ½ of full scale, x = 2. Therefore,

$$VLEVEL = 2 \times 1{,}444{,}084$$

Total RMS

The ADE9153A offers total current and voltage rms measurements on all channels. Figure 45 shows the datapath of the rms measurements.

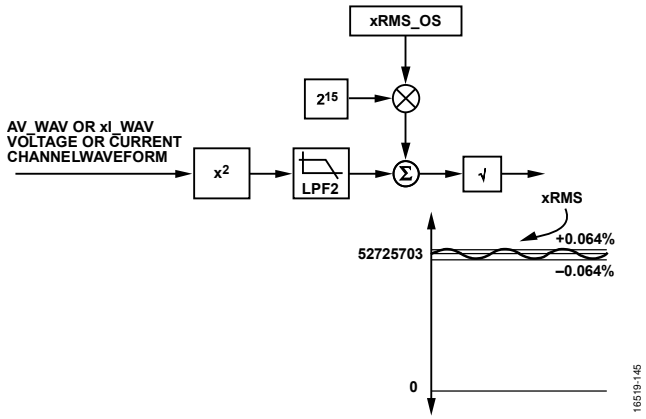

Figure 45. Filter-Based Total RMS Datapath

The total rms calculations, one for each channel (AIRMS, BIRMS, and AVRMS), are updated every 4 kSPS. The xIRMS value at full scale is 52,725,703 codes. The xVRMS value at full scale is 26,362,852 codes. The total rms measurements can be calibrated for gain and offset. Perform gain calibration on the respective Current A voltage channel datapath with the xGAIN registers. The following equation indicates how the offset calibration registers modify the result in the corresponding rms registers:

$$xRMS = \sqrt{xRMS_0^2 + 2^{15} \times xRMOS\_OS}$$

where $xRMS_0$ is the initial xRMS register value before offset calibration.

Total Active Power

The ADE9153A offers a total active power measurement. The datapath for the total active power measurement is shown in Figure 46.

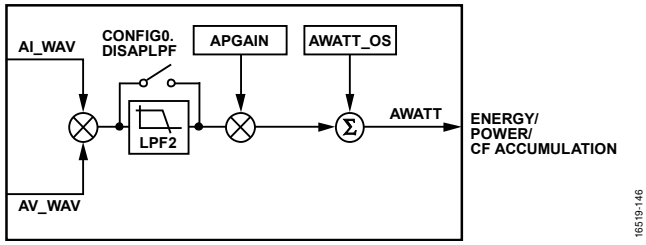

Figure 46. Total Active Power (AWATT) Datapath

The total active power calculation, AWATT, is updated every 4 kSPS. With full-scale inputs, the AWATT value is 10,356,306 codes.

The low-pass filter, LPF2, is enabled by default (DISAPLPF = 0) and must be set to this default value for typical operation. Disable LPF2 by setting the DISAPLPF bit in the CONFIG0 register.

The following equation indicates how the gain and offset calibration registers modify the results in the power register:

$$AWATT = \left(1 + \frac{APGAIN}{2^{27}}\right) AWATT_0 + AWATT\_OS$$

APGAIN is a common gain for all power measurements: active, reactive, and apparent power measurements.

Fundamental Reactive Power

The ADE9153A offers a fundamental reactive power measurement. Figure 47 shows the datapath for the fundamental reactive power calculation.

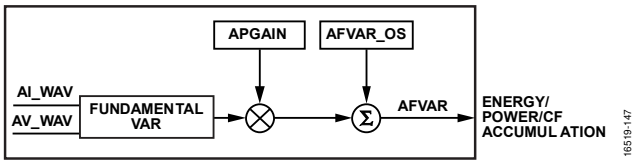

Figure 47. Fundamental Reactive Power (AFVAR) Datapath

The fundamental reactive power calculation, AFVAR, is updated every 4 kSPS. With full-scale inputs, the AFVAR value is 10,356,306 codes.

LPF2 is enabled by default (DISRPLPF = 0) and must be set to this default value for typical operation. Disable LPF2 by setting the DISRPLPF bit in the CONFIG0 register.

The following equation indicates how the gain and offset calibration registers modify the results in the power register:

$$AFVAR = \left(1 + \frac{APGAIN}{2^{27}}\right) AFVAR_0 + AFVAR\_OS$$

Total Apparent Power

The ADE9153A offers a total apparent power measurement. The datapath for the total apparent power calculation is shown in Figure 48.

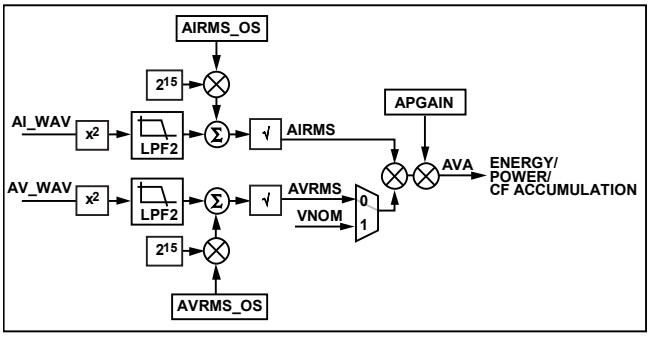

Figure 48. Total Apparent Power (AVA) Datapath

The total apparent power calculation, AVA, is updated every 4 kSPS. With full-scale inputs, the AVA value is 10,356,306 codes.

LPF2 is enabled by default (DISRPLPF = 0) and must be set to this default value for typical operation. Disable LPF2 by setting the DISRPLPF bit in the CONFIG0 register.

The ADE9153A offers a register, VNOM, to calculate the total apparent power when the voltage is missing. This register is set to correspond to a desired voltage rms value. If the VNOMA_EN bit in the CONFIG0 register is set, the VNOM value is used instead of AVRMS.

Energy Accumulation, Power Accumulation, and No Load Detection Features

The ADE9153A calculates total active, fundamental reactive, and total apparent energy. By default, the accumulation mode is signed accumulation but can be changed to absolute, positive only, or negative only for active and reactive energies using the WATTACC and VARACC bits in the ACCMODE register.

Energy Accumulation

The energy is accumulated into a 42-bit signed internal energy accumulator at 4 kSPS. The user readable energy register is signed and 45 bits wide, split between two 32-bit registers as shown in Figure 49. With full-scale inputs, the user energy register overflows in 106.3 sec.

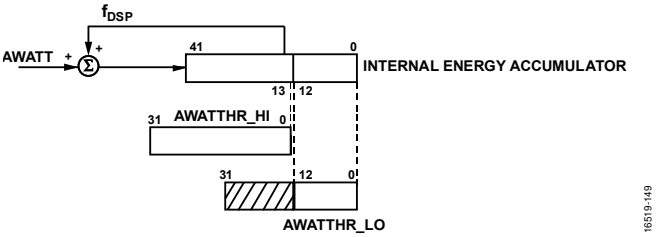

Figure 49. Internal Energy Accumulator to AWATTHR_HI and AWATTHR_LO

Energy Accumulation Modes

The energy registers can accumulate a user defined number of samples or half line cycles configured by the EGY_TMR_MODE bit in the EP_CFG register. Half line cycle accumulation uses the voltage channel zero crossings. The number of samples or half line cycles is set in the EGY_TIME register. The maximum value of EGY_TIME is 8191 decimal. With full-scale inputs, the internal register overflows in 13.3 sec. For a 50 Hz signal, EGY_TIME must be lower than 1329 decimal to prevent overflow during half line cycle accumulation.

After EGY_TIME + 1 samples or half line cycles, the EGYRDY bit is set in the status register and the energy register is updated. The data from the internal energy register is added or latched to the user energy register, depending on the EGY_LD_ACCUM bit setting in the EP_CFG register.

Reset Energy Register on Read

The user can reset the energy register on a read using the RD_RST_EN bit in the EP_CFG register. In this way, the value in the user energy register is reset when it is read.

Power Accumulation

The ADE9153A accumulates the total active, fundamental reactive, and total apparent powers into the AWATT_ACC, AFVAR_ACC, and AVA_ACC 32-bit signed registers, respectively. This accumulation can be used as an averaged power reading.

The number of samples accumulated is set using the PWR_TIME register. The PWRRDY bit in the status register is set after PWR_TIME + 1 samples accumulate at 4 kSPS. The maximum value of the PWR_TIME register is 8191 decimal, and the maximum power accumulation time is 1.024 sec.

The CFxSIGN, AVARSIGN, and AWSIGN bits in the PHSIGN register indicate the sign of accumulated powers over the PWR_TIME interval. When the sign of the accumulated power changes, the corresponding REVx bits in the status register are set and $\overline{\text{IRQ}}$ generates an interrupt.

The ADE9153A allows the user to accumulate total active power and fundamental reactive power into separate positive and negative accumulation registers: PWATT_ACC, NWATT_ACC, PFVAR_ACC, and NFVAR_ACC. A new accumulation from zero begins when the power update interval set in PWR_TIME elapses.

No Load Detection Feature

The ADE9153A features no load detection for each energy to prevent energy accumulation due to noise. If the accumulated energy over the user defined time period is below the user defined threshold, zero energy is accumulated into the energy register. The NOLOAD_TMR bits in the EP_CFG register determine the no load time period, and the ACT_NL_LVL, REACT_NL_LVL, and APP_NL_LVL registers contain the user defined no load threshold. The no load status is available in the PHNOLOAD register and the status register, which can be driven to the $\overline{\text{IRQ}}$ interrupt pin.

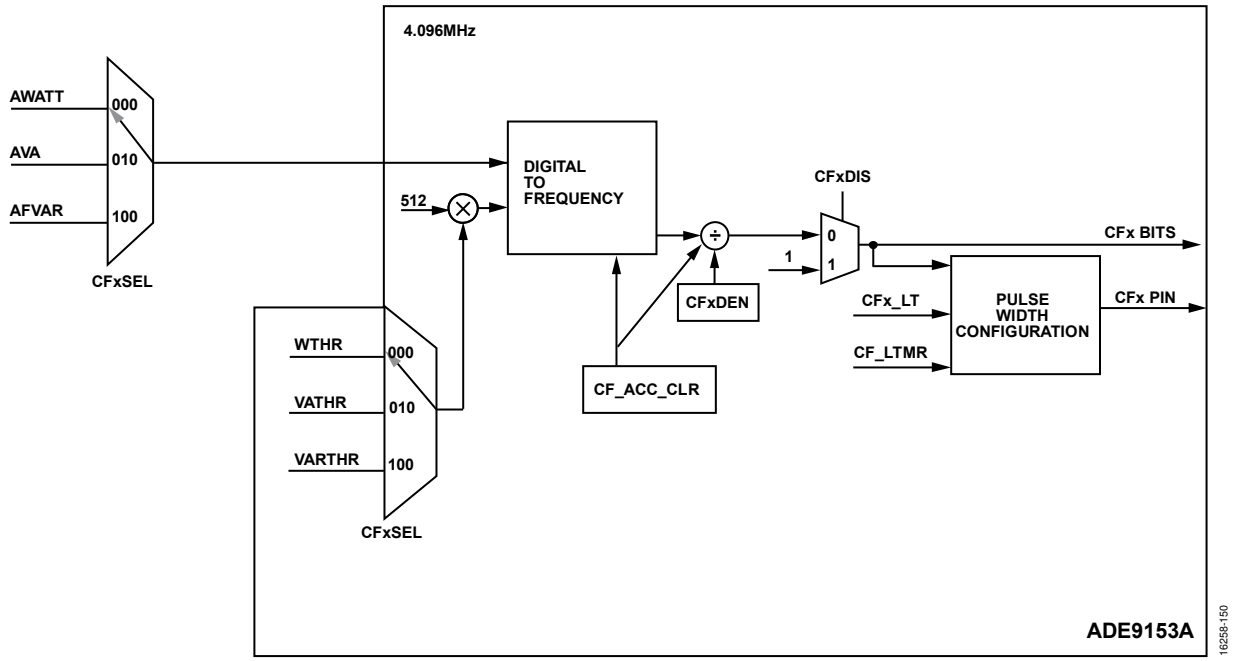

Figure 50. Digital to Frequency Conversion for CFx