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### FEATURES

- RF bandwidth to 4 GHz
- 2.7 V to 3.3 V power supply
- Separate  $V_P$  allows extended tuning voltage
- Programmable dual-modulus prescaler 4/5, 8/9
- Programmable charge pump currents
- 3-wire serial interface
- Digital lock detect
- Power-down mode
- Pin compatible with the [ADF4110/ADF4111/ADF4112/ADF4113](#), [ADF4106](#), [ADF4153](#)
- Programmable modulus on fractional-N synthesizer
- Trade-off noise vs. spurious performance
- Fast-lock mode with built-in timer
- Loop filter design possible with ADIsimPLL™

### APPLICATIONS

- Base stations for mobile radio (WiMAX, PHS, GSM, PCS, DCS, CDMA, PMR, W-CDMA, supercell 3G)
- Wireless handsets (PMR, GSM, PCS, DCS, CDMA, WCDMA)
- CATV equipment
- Wireless LANs
- Communications test equipment

### GENERAL DESCRIPTION

The ADF4154 is a fractional-N frequency synthesizer that implements local oscillators in the up conversion and down conversion sections of wireless receivers and transmitters. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, and a programmable reference divider. There is a  $\Sigma$ - $\Delta$  based fractional interpolator to allow programmable fractional-N division. The INT, FRAC, and MOD registers define an overall N-divider ( $N = (INT + (FRAC/MOD))$ ). In addition, the 4-bit reference counter (R-counter) allows selectable  $REF_{IN}$  frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and a voltage-controlled oscillator (VCO).

A key feature of the ADF4154 is the fast-lock mode with a built-in timer. The user can program a predetermined countdown time value so that the PLL remains in wide bandwidth mode, instead of the user having to control this time externally.

Control of all on-chip registers is via a simple 3-wire interface. The device operates with a power supply ranging from 2.7 V to 3.3 V and can be powered down when not in use.

### FUNCTIONAL BLOCK DIAGRAM

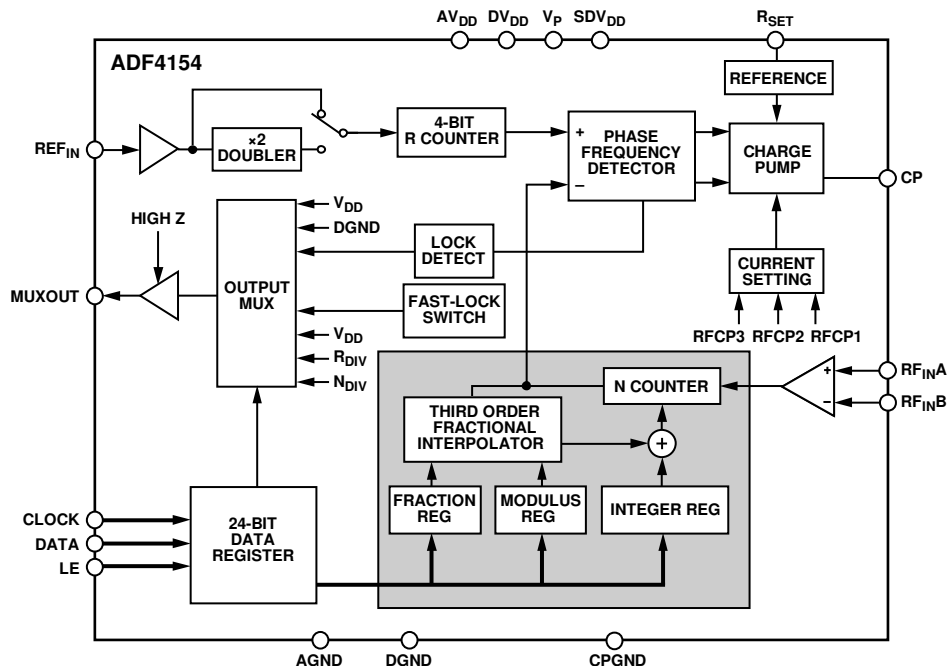


Figure 1.

#### Rev. C

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# ADF4154\* PRODUCT PAGE QUICK LINKS

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- ADF4154 Evaluation Board

## DOCUMENTATION

### Application Notes

- AN-30: Ask the Applications Engineer - PLL Synthesizers
- AN-873: Lock Detect on the ADF4xxx Family of PLL Synthesizers

### Data Sheet

- ADF4154:Fractional-N Frequency Synthesizer Data Sheet

### User Guides

- UG-161: PLL Frequency Synthesizer Evaluation Board
- UG-476: PLL Software Installation Guide

## SOFTWARE AND SYSTEMS REQUIREMENTS

- Fractional-N Software

## TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF
- dt\_ADF4x5x\_Register\_Configuration

## REFERENCE MATERIALS

### Product Selection Guide

- RF Source Booklet

### Technical Articles

- Phase Locked Loops for High-Frequency Receivers and Transmitters – Part 1
- Phase Locked Loops for High-Frequency Receivers and Transmitters – Part 3
- Phase-Locked Loops for High-Frequency Receivers and Transmitters - Part 2

## DESIGN RESOURCES

- ADF4154 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all ADF4154 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

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### 5/04—Revision 0: Initial Version

## SPECIFICATIONS

$AV_{DD} = DV_{DD} = SDV_{DD} = 2.7\text{ V to }3.3\text{ V}$ ;  $V_P = AV_{DD}$  to  $5.5\text{ V}$ ;  $AGND = DGND = 0\text{ V}$ ;  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted; dBm referred to  $50\ \Omega$ . The operating temperature for the B version is  $-40^\circ\text{C}$  to  $+80^\circ\text{C}$ .

Table 1.

Parameter	B Version	Unit	Test Conditions/Comments
<b>RF CHARACTERISTICS (3 V)</b>			
RF Input Frequency (RF <sub>IN</sub> ) <sup>1</sup>	0.5/4.0 1.0/4.0	GHz min/max GHz min/max	See Figure 15 for the input circuit. –8 dBm/0 dBm min/max. For lower frequencies, ensure slew rate > 400 V/μs. –10 dBm/0 dBm min/max.
<b>REFERENCE CHARACTERISTICS</b>			
REF <sub>IN</sub> Input Frequency <sup>1</sup>	10/250	MHz min/max	See Figure 14 for input circuit. For $f < 10\text{ MHz}$ , use a dc-coupled, CMOS-compatible square wave, slew rate > 25 V/μs.
REF <sub>IN</sub> Input Sensitivity	0.7/AV <sub>DD</sub>	V p-p min/max	Biased at AV <sub>DD</sub> /2. <sup>2</sup>
REF <sub>IN</sub> Input Capacitance	10	pF max	
REF <sub>IN</sub> Input Current	±100	μA max	
<b>PHASE DETECTOR</b>			
Phase Detector Frequency <sup>3</sup>	32	MHz max	
<b>CHARGE PUMP</b>			
I <sub>CP</sub> Sink/Source			Programmable. See Table 5.
High Value	5	mA typ	With R <sub>SET</sub> = 5.1 kΩ.
Low Value	312.5	μA typ	
Absolute Accuracy	2.5	% typ	With R <sub>SET</sub> = 5.1 kΩ.
R <sub>SET</sub> Range	2.7/10	kΩ min/max	
I <sub>CP</sub> Three-State Leakage Current	1	nA typ	Sink and source current.
Matching	2	% typ	0.5 V < V <sub>CP</sub> < V <sub>P</sub> – 0.5 V.
I <sub>CP</sub> vs. V <sub>CP</sub>	2	% typ	0.5 V < V <sub>CP</sub> < V <sub>P</sub> – 0.5 V.
I <sub>CP</sub> vs. Temperature	2	% typ	V <sub>CP</sub> = V <sub>P</sub> /2.
<b>LOGIC INPUTS</b>			
V <sub>INH</sub> , Input High Voltage	1.4	V min	
V <sub>INL</sub> , Input Low Voltage	0.6	V max	
I <sub>INH</sub> /I <sub>INL</sub> , Input Current	±1	μA max	
C <sub>IN</sub> , Input Capacitance	10	pF max	
<b>LOGIC OUTPUTS</b>			
V <sub>OH</sub> , Output High Voltage	1.4	V min	Open-drain 1 kΩ pull-up to 1.8 V.
V <sub>OL</sub> , Output Low Voltage	0.4	V max	I <sub>OL</sub> = 500 μA.
<b>POWER SUPPLIES</b>			
AV <sub>DD</sub>	2.7/3.3	V min/V max	
DV <sub>DD</sub> , SDV <sub>DD</sub>	AV <sub>DD</sub>		
V <sub>P</sub>	AV <sub>DD</sub> /5.5	V min/V max	
I <sub>DD</sub>	24	mA max	20 mA typical.
Low Power Sleep Mode	1	μA typ	
<b>NOISE CHARACTERISTICS</b>			
Normalized Phase Noise Floor (PN <sub>SYNTH</sub> ) <sup>4</sup>	–220	dBc/Hz typ	PLL loop BW = 500 kHz. Measured at 100 kHz offset.
Normalized 1/f Noise (PN <sub>1/f</sub> ) <sup>5</sup>	–114	dBc/Hz typ	10 kHz offset; normalized to 1 GHz.
Phase Noise Performance <sup>6</sup> 1750 MHz Output <sup>7</sup>	–102	dBc/Hz typ	@ VCO output. @ 1 kHz offset, 26 MHz PFD frequency.

<sup>1</sup> Use a square wave for frequencies below  $f_{MIN}$ .

<sup>2</sup> AC coupling ensures AV<sub>DD</sub>/2 bias. See Figure 14 for a typical circuit.

<sup>3</sup> Guaranteed by design. Sample tested to ensure compliance.

<sup>4</sup> The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting  $20\log(N)$  (where N is the N divider value) and  $10\log(F_{PFD})$ .  $PN_{SYNTH} = PN_{TOT} - 10\log(F_{PFD}) - 20\log(N)$ .

<sup>5</sup> The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency,  $F_{RF}$ , and at a frequency offset f is given by  $PN = PN_{1/f} + 10\log(10\text{ kHz}/f) + 20\log(F_{RF}/1\text{ GHz})$ . Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.

<sup>6</sup> The phase noise is measured with the EVAL-ADF4154EB1 and the HP8562E spectrum analyzer.

<sup>7</sup>  $f_{REFIN} = 26\text{ MHz}$ ,  $f_{PFD} = 26\text{ MHz}$ , offset frequency = 1 kHz,  $R_{FOUT} = 1750\text{ MHz}$ , loop B/W = 20 kHz, lowest noise mode.

**TIMING CHARACTERISTICS**

$AV_{DD} = DV_{DD} = SDV_{DD} = 2.7\text{ V to }3.3\text{ V}$ ;  $V_P = AV_{DD}\text{ to }5.5\text{ V}$ ;  $AGND = DGND = 0\text{ V}$ ;  $T_A = T_{MIN}\text{ to }T_{MAX}$ , unless otherwise noted; dBm referred to  $50\ \Omega$ .

Table 2.

Parameter <sup>1</sup>	Limit at $T_{MIN}\text{ to }T_{MAX}$ (B Version)	Unit	Test Conditions/Comments
$t_1$	20	ns min	LE setup time
$t_2$	10	ns min	DATA to CLOCK setup time
$t_3$	10	ns min	DATA to CLOCK hold time
$t_4$	25	ns min	CLOCK high duration
$t_5$	25	ns min	CLOCK low duration
$t_6$	10	ns min	CLOCK to LE setup time
$t_7$	20	ns min	LE pulse width

<sup>1</sup> Guaranteed by design, but not production tested.

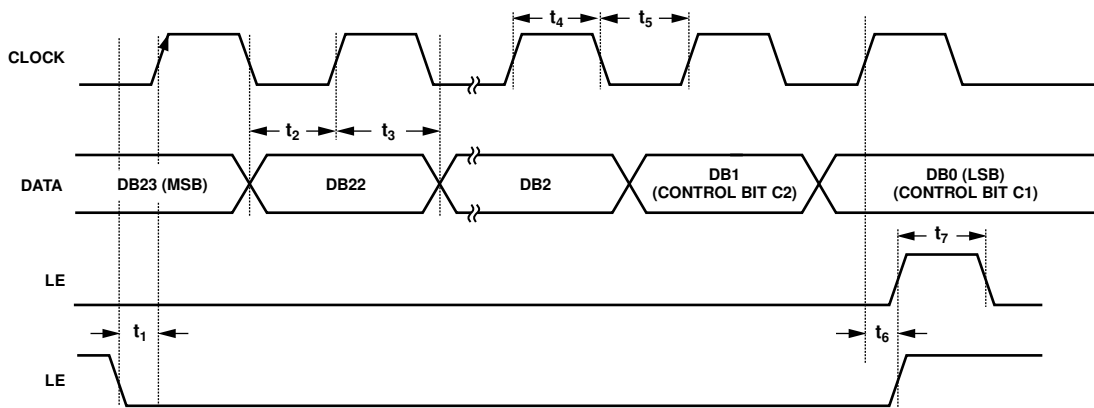


Figure 2. Timing Diagram

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## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter <sup>1, 2, 3</sup>	Rating
$V_{DD}$ to GND	-0.3 V to +4 V
$V_{DD}$ to $V_{DD}$	-0.3 V to +0.3 V
$V_P$ to GND	-0.3 V to +5.8 V
$V_P$ to $V_{DD}$	-0.3 V to +5.8 V
Digital I/O Voltage to GND	-0.3 V to $V_{DD} + 0.3$ V
Analog I/O Voltage to GND	-0.3 V to $V_{DD} + 0.3$ V
$REF_{IN}$ , $RF_{IN}$ to GND	-0.3 V to $V_{DD} + 0.3$ V
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP $\theta_{JA}$ Thermal Impedance	112°C/W
LFCSP $\theta_{JA}$ Thermal Impedance (Paddle Soldered)	30.4°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

<sup>1</sup> This device is a high performance RF-integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken when handling and assembling the device.

<sup>2</sup> GND =  $A_{GND} = D_{GND} = 0$  V.

<sup>3</sup>  $V_{DD} = AV_{DD} = DV_{DD} = SDV_{DD}$ .

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

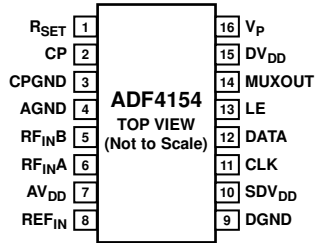
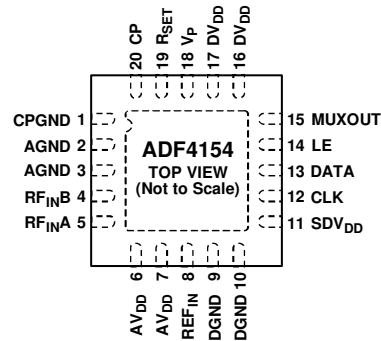


Figure 3. TSSOP Pin Configuration



NOTES  
1. THE EXPOSED PAD MUST BE CONNECTED TO AGND.

Figure 4. LFCSP Pin Configuration

Table 4. Pin Function Descriptions

TSSOP	LFCSP	Mnemonic	Description
1	19	R <sub>SET</sub>	Set Resistor. Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I <sub>CPmax</sub> and R <sub>SET</sub> is $I_{CPmax} = \frac{25.5}{R_{SET}}$ where R <sub>SET</sub> = 5.1 kΩ and I <sub>CPmax</sub> = 5 mA.
2	20	CP	Charge Pump Output. When enabled, this pin provides ±I <sub>CP</sub> to the external loop filter, which in turn drives the external VCO.
3	1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
4	2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
5	4	RF <sub>INB</sub>	Complementary Input to the RF Prescaler. This point should be decoupled to the ground plane with a small bypass capacitor, typically 100 pF (see Figure 15).
6	5	RF <sub>INA</sub>	Input to the RF Prescaler. This small-signal input is normally ac-coupled from the VCO.
7	6, 7	AV <sub>DD</sub>	Positive Power Supply for the RF Section. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. AV <sub>DD</sub> has a value of 3 V ± 10%. AV <sub>DD</sub> must have the same voltage as DV <sub>DD</sub> .
8	8	REF <sub>IN</sub>	Reference Input. This CMOS input has a nominal threshold of V <sub>DD</sub> /2 and an equivalent input resistance of 100 kΩ (see Figure 14). This input can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
9	9, 10	DGND	Digital Ground.
10	11	SDV <sub>DD</sub>	Σ-Δ Power. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. SDV <sub>DD</sub> has a value of 3 V ± 10%. SDV <sub>DD</sub> must have the same voltage as DV <sub>DD</sub> .
11	12	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the shift register on the CLK rising edge. This input is a high impedance CMOS input.
12	13	DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs as the control bits. This input is a high impedance CMOS input.
13	14	LE	Load Enable, CMOS Input. When LE is high, the data stored in the shift registers is loaded into one of the four latches, which is selected by the user via the control bits.
14	15	MUXOUT	Multiplexer Output. This pin allows either the RF lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
15	16, 17	DV <sub>DD</sub>	Positive Power Supply for the Digital Section. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV <sub>DD</sub> has a value of 3 V ± 10%. DV <sub>DD</sub> must have the same voltage as AV <sub>DD</sub> .
16	18	V <sub>P</sub>	Charge Pump Power Supply. This should be greater than or equal to V <sub>DD</sub> . In systems where V <sub>DD</sub> is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5.5 V.
N/A	EP	EPAD	Exposed Pad. The exposed pad must be connected to AGND.



# TYPICAL PERFORMANCE CHARACTERISTICS

Loop bandwidth = 20 kHz; reference = 250 MHz; VCO = Vari-L Company, Inc., VCO190-1750T; evaluation board = EVAL-ADF4154EB1; measurements taken with the Agilent E5500 phase noise measurement system.

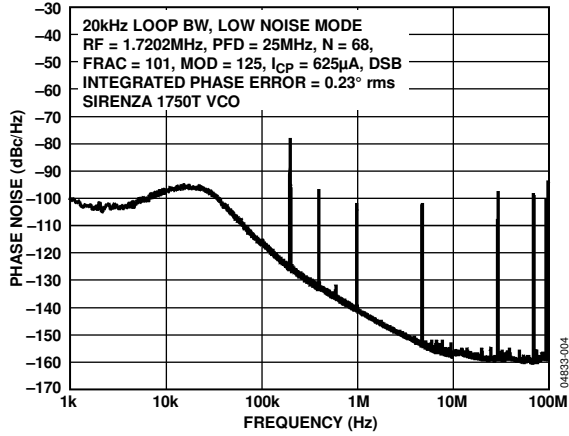


Figure 5. Single-Sideband Phase Noise Plot (Lowest Noise Mode)

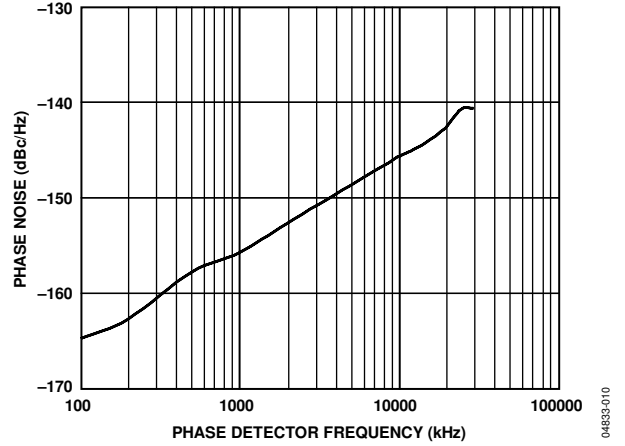


Figure 8. PFD Noise Floor vs. PFD Frequency (Lowest Noise Mode)

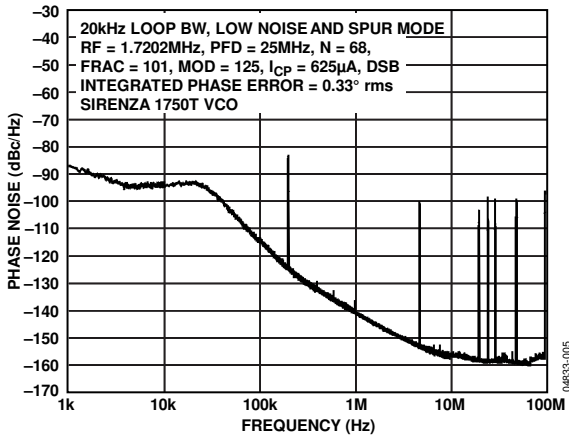


Figure 6. Single-Sideband Phase Noise Plot (Low Noise Mode and Spur Mode)

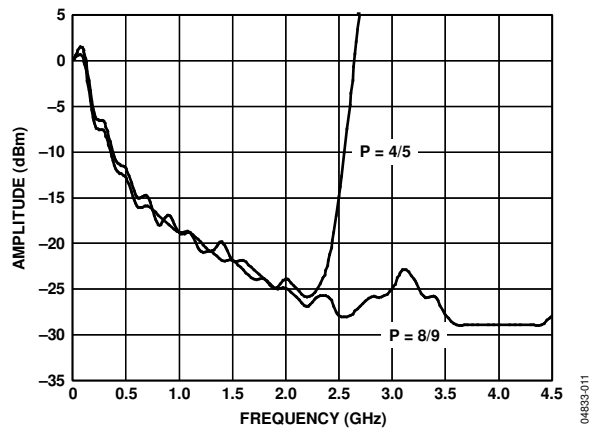


Figure 9. RF Input Sensitivity

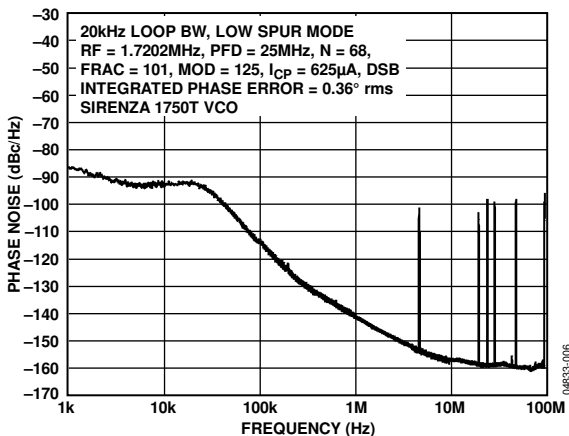


Figure 7. Single-Sideband Phase Noise Plot (Lowest Spur Mode)

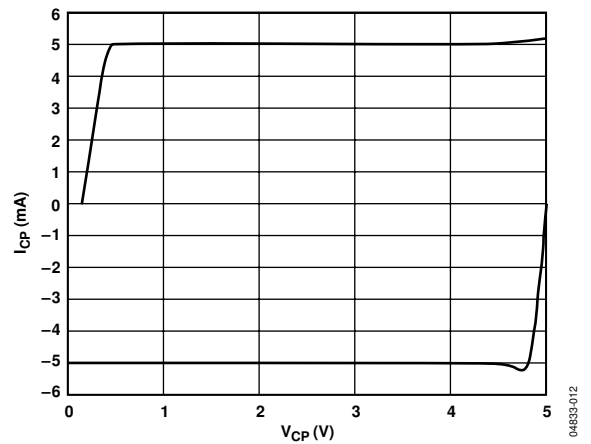


Figure 10. Charge Pump Output Characteristics

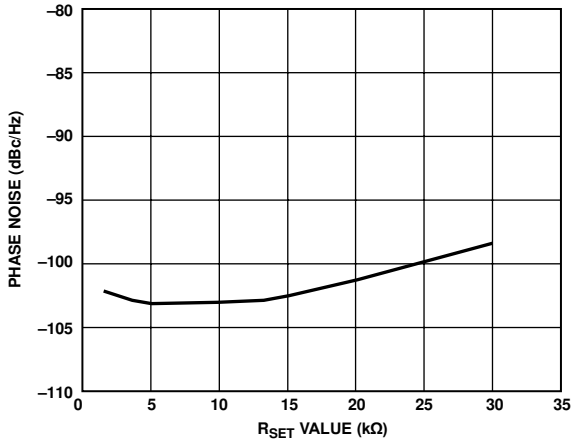


Figure 11. Phase Noise vs. RSET

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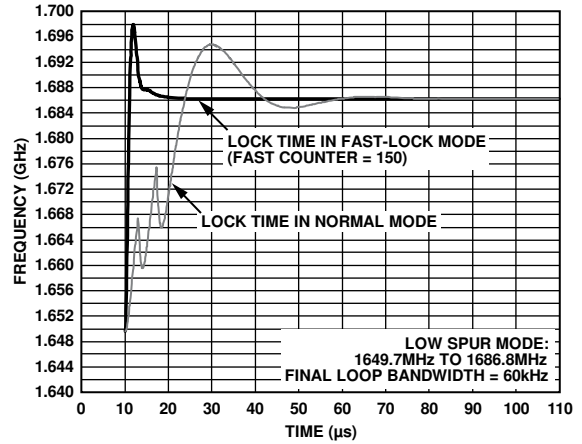


Figure 13. Frequency vs. Lock Time

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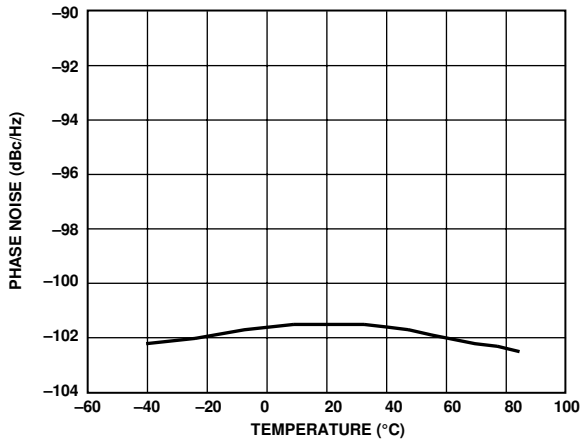


Figure 12. Phase Noise vs. Temperature

04833-014

# CIRCUIT DESCRIPTION

## REFERENCE INPUT SECTION

The reference input stage is shown in Figure 14. While the device is operating, usually SW1 and SW2 are closed switches and SW3 is open. When a power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that the REF<sub>IN</sub> pin is not loaded while the device is powered down.

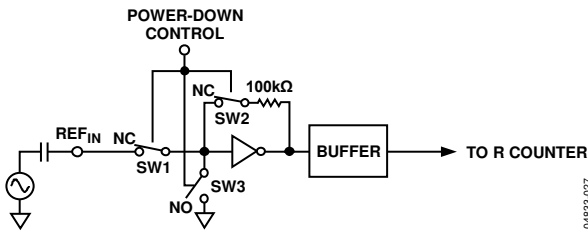


Figure 14. Reference Input Stage

## RF INPUT STAGE

The RF input stage is shown in Figure 15. It is followed by a two-stage limiting amplifier to generate the current mode logic (CML) clock levels needed for the prescaler.

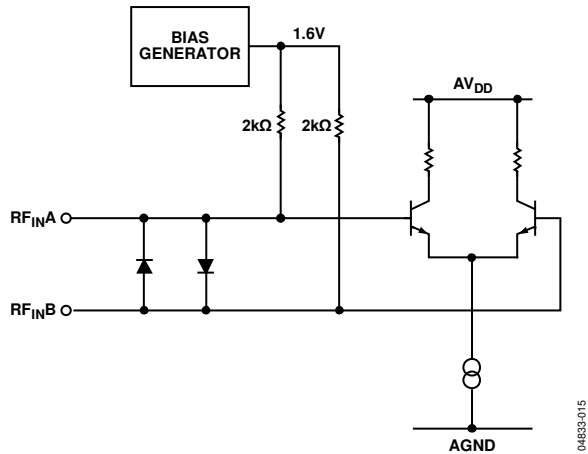


Figure 15. RF Input Stage

## RF INT DIVIDER

The RF INT CMOS counter allows a division ratio in the PLL feedback counter. Division ratios from 31 to 511 are allowed.

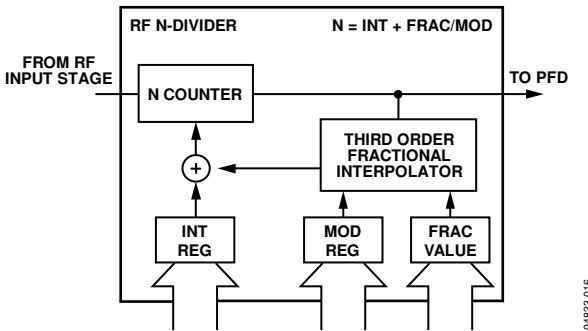


Figure 16. A and B Counters

## INT, FRAC, MOD, AND R RELATIONSHIP

The INT, FRAC, and MOD values, in conjunction with the R-counter, enable generating output frequencies that are spaced by fractions of the PFD. See the RF Synthesizer: A Worked Example section for more information. The RF VCO frequency (RF<sub>OUT</sub>) equation is

$$RF_{OUT} = F_{PFD} \times (INT + (FRAC/MOD)) \tag{1}$$

where RF<sub>OUT</sub> is the output frequency of the external voltage-controlled oscillator (VCO).

$$F_{PFD} = REF_{IN} \times (1 + D)/R \tag{2}$$

where:

REF<sub>IN</sub> is the reference input frequency.

D is the REF<sub>IN</sub> doubler bit.

R is the preset divide ratio of binary 4-bit programmable reference counter (1 to 15).

INT is the preset divide ratio of binary 9-bit counter (31 to 511).

MOD is the preset modulus ratio of binary 12-bit programmable FRAC counter (2 to 4095).

FRAC is the preset fractional ratio of binary 12-bit programmable FRAC counter (0 to MOD-1).

## R-COUNTER

The 4-bit R-counter allows the input reference frequency (REF<sub>IN</sub>) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 15 are allowed.

## PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R-counter and N-counter and produces an output proportional to the phase and frequency difference between them. Figure 17 is a simplified schematic. The PFD includes a fixed delay element that sets the width of the antibacklash pulse, which is typically 3 ns. This pulse ensures that there is no dead zone in the PFD transfer function and gives a consistent reference spur level.

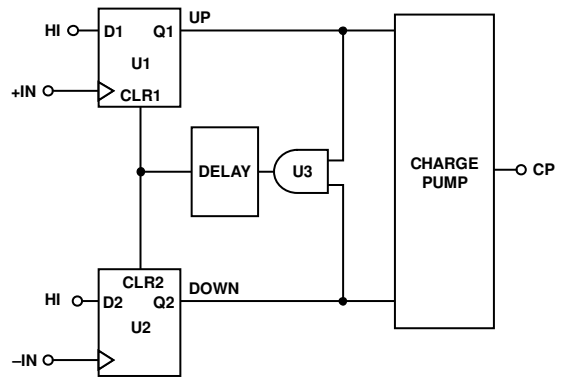


Figure 17. PFD Simplified Schematic

**MUXOUT AND LOCK DETECT**

The output multiplexer on the ADF4154 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 (see Table 8). Figure 18 shows the MUXOUT section in block diagram form.

The N-channel, open-drain, analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, the lock detect is high with narrow low-going pulses.

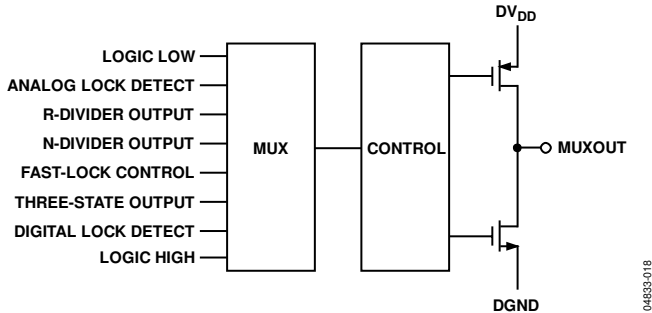


Figure 18. MUXOUT Schematic

**INPUT SHIFT REGISTERS**

The ADF4154 digital section includes a 4-bit R value, a 9-bit RF N value, a 12-bit RF FRAC value, and a 12-bit interpolator modulus value/fast-lock timer. Data is clocked MSB first into the 24-bit shift register on each rising edge of CLK.

Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2 and C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in Figure 2. The truth table for these bits is shown in Table 5. Table 6 shows a summary of how the latches are programmed.

**PROGRAM MODES**

Table 5 through Table 9 show how to set up the program modes in the ADF4154.

The ADF4154 programmable modulus is double buffered, meaning that two events must occur before the part can use a new modulus value. The first event is that the new modulus value must be latched into the device by writing to the R-divider register, and the second event is that a new write must be performed on the N-divider register. Therefore, whenever the modulus value is updated, the N-divider register must be written to so that the modulus value is loaded correctly.

Table 5. C2 and C1 Truth Table

Control Bits		Data Latch
C2	C1	
0	0	N-divider register
0	1	R-divider register
1	0	Control register
1	1	Noise and spur register

# REGISTERS

Table 6. Register Summary

N-DIVIDER REG																							
FAST-LOCK	9-BIT RF N VALUE									12-BIT RF FRAC VALUE										CONTROL BITS			
	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1
FL1	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C2 (0)	C1 (0)

R-DIVIDER REG																							
LOAD CONTROL	MUXOUT			RESERVED	PRESCALER	4-BIT R VALUE				12-BIT INTERPOLATOR MODULUS VALUE/ FAST-LOCK TIMER										CONTROL BITS			
	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1
P3	M3	M2	M1	P2	P1	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C2 (0)	C1 (1)

CONTROL REG															
RESERVED				REF <sub>N</sub> DOUBLER	CP/2	CHARGE PUMP CURRENT SETTING			PHASE DETECTOR POLARITY	LOCK DETECT PRECISION	RF POWER-DOWN	RF CHARGE PUMP THREE-STATE	RF COUNTER RESET	CONTROL BITS	
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	U6	CP3	CP2	CP1	CP0	U5	U4	U3	U2	U1	C2 (1)	C1 (0)

NOISE AND SPUR REG										
RESERVED	NOISE AND SPUR MODE				RESERVED			NOISE AND SPUR MODE	CONTROL BITS	
DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
T9	T8	T7	T6	T5	T4	T3	T2	T1	C2 (1)	C1 (1)

04833-019

**Table 7. N-Divider Register Map**

FAST-LOCK	9-BIT RF N VALUE (INT)										12-BIT FRAC VALUE (FRAC)										CONTROL BITS			
	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
	FL1	N9	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C2 (0)	C1 (0)

F12	F11	F10	.....	F3	F2	F1	FRACTIONAL VALUE (FRAC)
0	0	0	.....	0	0	0	0
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

N9	N8	N7	N6	N5	N4	N3	N2	N1	INTEGER VALUE (INT)
0	0	0	0	1	1	1	1	1	31
0	0	0	1	0	0	0	0	0	32
0	0	0	1	0	0	0	0	1	33
0	0	0	1	0	0	0	1	0	34
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	0	1	509
1	1	1	1	1	1	1	1	0	510
1	1	1	1	1	1	1	1	1	511

FL1	FAST-LOCK
0	NORMAL OPERATION
1	FAST-LOCK ENABLED



Table 8. R-Divider Register Map

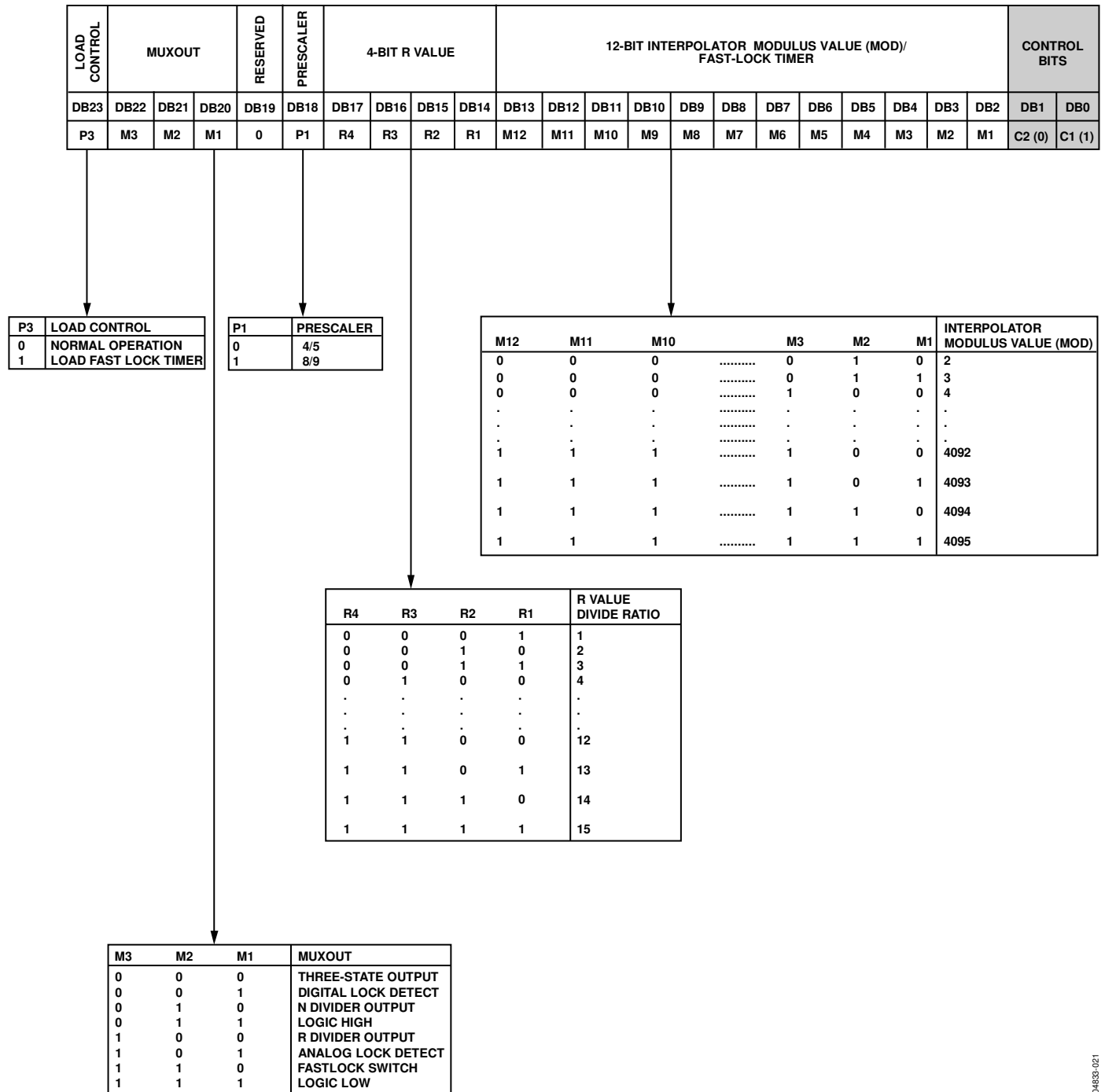
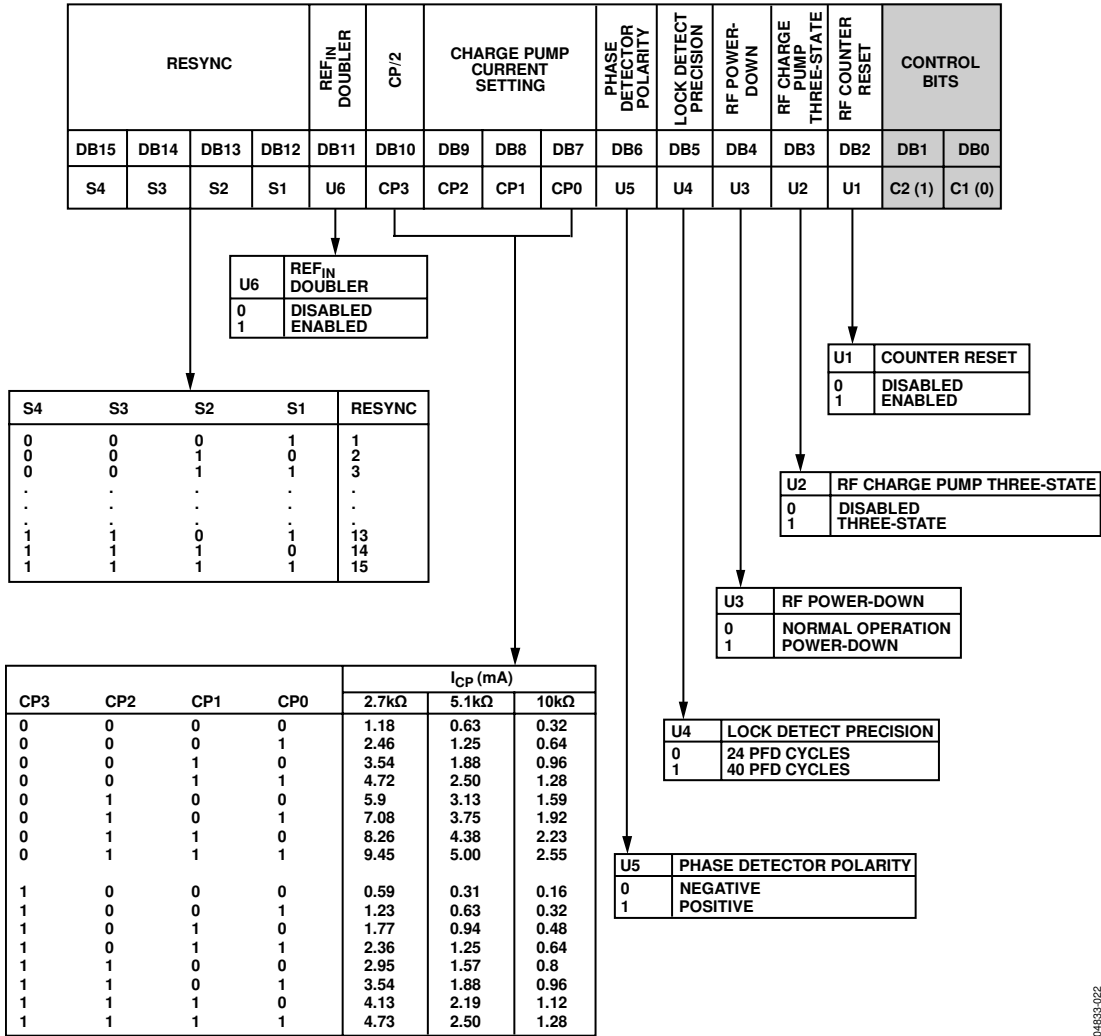
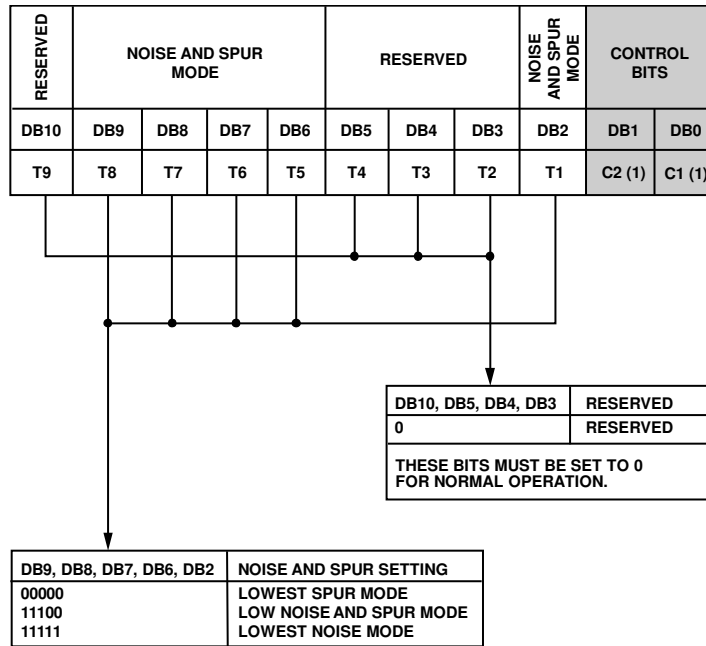


Table 9. Control Register Map



04853-022

Table 10. Noise and Spur Register



04833-023

## REGISTER DEFINITIONS

### **N-Divider Register, R0**

The on-chip N-divider register is programmed by setting R0 [1, 0] to [0, 0]. Table 7 shows the input data format for programming this register.

#### **9-Bit RF N Value (INT)**

These nine bits control what is loaded as the INT value. This is used to determine the overall feedback division factor (see Equation 1).

#### **12-Bit RF FRAC Value**

These 12 bits control what is loaded as the FRAC value into the fractional interpolator. This value helps determine the overall feedback division factor (see Equation 1). The FRAC value must be less than the value loaded into the MOD register.

#### **Fast Lock**

Setting the part to logic high enables fast-lock mode. To use fast lock, the required time value for wide bandwidth mode must be loaded into the R-divider register.

The charge pump current increases from 16× the minimum current and reverts back to 1× the minimum current after the time value loaded expires.

See the Fast-Lock Timer and Register Sequences section for more information.

### **R-DIVIDER REGISTER, R1**

The on-chip R-divider register is programmed by setting R1 [1, 0] to [0, 1]. Table 8 shows the input data format for programming this register.

#### **Load Control**

When this bit is set to logic high, the value being programmed in the modulus is not loaded into the modulus. Instead, it sets the fast-lock timer. The value of the fast-lock timer divided by  $f_{\text{PFD}}$  is the amount of time the PLL stays in wide bandwidth mode.

#### **MUXOUT**

The on-chip multiplexer is controlled by R1 [22 ... 20] on the ADF4154. Table 8 shows the truth table.

#### **Digital Lock Detect**

The digital lock detect output goes high if there are 40 successive PFD cycles with an input error of less than 15 ns. It stays high until a new channel is programmed or until the error at the PFD input exceeds 30 ns for one or more cycles. If the loop bandwidth is narrow compared with the PFD frequency, the error at the PFD inputs may drop below 15 ns for 40 cycles around a cycle slip. Therefore, the digital lock detect may briefly, and falsely, go high until the error exceeds 30 ns. In this case, the digital lock detect is reliable only as a loss-of-lock detector.

### **Prescaler (P/P + 1)**

The dual-modulus prescaler ( $P/P + 1$ ), along with the INT, FRAC, and MOD counters, determines the overall division ratio from the  $\text{RF}_{\text{IN}}$  to the PFD input. Operating at CML levels, the prescaler uses the clock from the RF input stage and divides it down for the counters. The prescaler is based on a synchronous 4/5 core. When it is set to 4/5, the maximum RF frequency allowed is 2 GHz. Therefore, when operating the ADF4154 with frequencies greater than 2 GHz, the prescaler must be set to 8/9. The prescaler limits the INT value as follows:

$$\text{With } P = 4/5, N_{\text{MIN}} = 31$$

$$\text{With } P = 8/9, N_{\text{MIN}} = 91$$

The prescaler can also influence the phase noise performance. If  $\text{INT} < 91$ , a prescaler of 4/5 should be used. For applications where  $\text{INT} > 91$ , a prescaler of 8/9 should be used for optimum noise performance (see Table 8).

#### **4-Bit R Value**

The 4-bit R value allows the input reference frequency ( $\text{REF}_{\text{IN}}$ ) to be divided down to produce the reference clock for the PFD. Division ratios from 1 to 15 are allowed.

#### **12-Bit Interpolator Modulus Value/Fast-Lock Timer**

Depending on the value of the load control bit, Bits DB13:DB2 can either be used to set the modulus or the fast-lock timer value.

When the load control bit (DB23) is set to 0, the required modulus can be programmed in the R-divider register (DB13:DB2).

When the load control bit (DB23) is set to 1, the required fast-lock timer value can be programmed in the R-divider register (DB13:DB2).

This programmable register sets the fractional modulus, which is the ratio of the PFD frequency to the channel step resolution on the RF output. Refer to the RF Synthesizer: A Worked Example section for more information.

The ADF4154 programmable modulus is double buffered, meaning that two events must occur before the part can use a new modulus value. The first event is that the new modulus value must be latched into the device by writing to the R-divider register, and the second event is that a new write must be performed on the N-divider register. Therefore, whenever the modulus value is updated, the N-divider register must be written to so that the modulus value is loaded correctly.

### **CONTROL REGISTER, R2**

The on-chip control register is programmed by setting R2 [1, 0] to [0, 1]. Table 9 shows the input data format for programming this register.

#### **RF Counter Reset**

DB2 is the RF counter reset bit for the ADF4154. When this bit is set to 1, the RF synthesizer counters are held in reset. For normal operation, this bit should be set to 0.

**RF Charge Pump Three-State**

This bit (DB3) puts the charge pump into three-state mode when it is programmed to 1. For normal operation, it should be set to 0.

**RF Power-Down**

DB4 on the ADF4154 provides the programmable power-down mode. Setting Bit DB4 to 1 powers down the device. Setting Bit DB4 to 0 returns the synthesizer to normal operation. While in software power-down mode, the part retains all information in its registers. Only when supplies are removed are the register contents lost.

When a power-down is activated, the following events occur:

1. All active dc current paths are removed.
2. The synthesizer counters are forced to their load state conditions.
3. The charge pump is forced into three-state mode.
4. The digital lock detect circuitry is reset.
5. The RF<sub>IN</sub> input is debiased.
6. The input register remains active and capable of loading and latching data.

**Lock Detect Precision (LDP)**

When the LDP bit (DB5) is programmed to 0, 24 consecutive reference cycles of 15 ns must occur before the digital lock detect is set. When this bit is programmed to 1, 40 consecutive reference cycles of 15 ns must occur before digital lock detect is set.

**Phase Detector Polarity**

DB6 sets the phase detector polarity. When the VCO characteristics are positive, this bit should be set to 1. When they are negative, this bit should be set to 0.

**Charge Pump (CP) Current Setting and CP/2**

DB7, DB8, DB9, and DB10 set the charge pump current, which should be set according to the loop filter design (see Table 9).

**REF<sub>IN</sub> Doubler**

Setting the REF<sub>IN</sub> doubler bit (DB11) to 0 feeds the REF<sub>IN</sub> signal directly to the 4-bit R-counter, which disables the doubler.

Setting the REF<sub>IN</sub> doubler bit to 1 multiplies the REF<sub>IN</sub> frequency by a factor of 2 before feeding into the 4-bit R-counter. When the doubler is disabled, the REF<sub>IN</sub> falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of REF<sub>IN</sub> become active edges at the PFD input.

When the doubler is enabled and the lowest spur mode is chosen, the in-band phase noise performance is sensitive to the REF<sub>IN</sub> duty cycle. The phase noise degradation can be as much as 5 dB for the REF<sub>IN</sub> duty cycles outside a 45% to 55% range. The phase noise is insensitive to the REF<sub>IN</sub> duty cycle in the lowest noise mode and in the lowest noise and spur mode. The phase noise is insensitive to the REF<sub>IN</sub> duty cycle when the doubler is disabled.

The maximum allowed REF<sub>IN</sub> frequency when the doubler is enabled is 30 MHz.

**NOISE AND SPUR REGISTER, R3**

The on-chip noise and spur register is programmed by setting R3 [1, 0] to [1, 1].

Table 10 shows the input data format for programming this register.

**Noise and Spur Mode**

Noise and spur mode allows the user to optimize a design either for improved spurious performance or for improved phase noise performance. When the lowest spur setting is chosen, dither is enabled. This randomizes the fractional quantization noise so that it looks more like white noise than spurious noise, meaning that the part is optimized for improved spurious performance. This operation is typically used when the PLL closed-loop bandwidth is wide for fast-locking applications. A wide-loop bandwidth is defined as a loop bandwidth greater than 1/10 of the RF<sub>OUT</sub> channel step resolution ( $f_{RES}$ ). A wide-loop filter does not attenuate the spurs to a level that a narrow-loop bandwidth would. When the low noise and spur setting is enabled, dither is disabled.

This optimizes the synthesizer to operate with improved noise performance. However, the spurious performance is degraded in this mode compared with the lowest spur setting. To further improve noise performance, the lowest noise setting option can be used, which reduces the phase noise. As well as disabling the dither, it ensures that the charge pump operates in an optimum region for noise performance. This setting is extremely useful if a narrow-loop filter bandwidth is used. The synthesizer ensures extremely low noise, and the filter attenuates the spurs. The typical performance characteristics show the trade-offs in a typical WCDMA setup for different noise and spur settings.

**RESERVED BITS**

These bits should be set to 0 for normal operation.

## INITIALIZATION SEQUENCE

The following initialization sequence should be followed after powering up the part:

1. Clear all test modes by writing all 0s to the noise and spur register.
2. Select the noise and spur mode required for the application by writing to the noise and spur register. For example, writing Hex 0003C7 to the part selects low noise mode.
3. Enable the counter reset in the control register by writing a 1 to DB2 and selecting the required settings in the control register.
4. Load the R-divider register (with the load control bit [DB23] set to 0).
5. Load the N-divider register.
6. Disable the counter reset by writing a 0 to DB2 in the control register.

The part should now lock to the set frequency.

## RF SYNTHESIZER: A WORKED EXAMPLE

This equation governs how the synthesizer should be programmed.

$$RF_{OUT} = [INT + (FRAC/MOD)] \times [f_{PFD}] \quad (3)$$

where:

$RF_{OUT}$  is the RF frequency output.

$INT$  is the integer division factor.

$FRAC$  is the fractionality.

$MOD$  is the modulus.

The PFD frequency can be calculated as follows:

$$f_{PFD} = [REF_{IN} \times (1 - D)/R] \quad (4)$$

where:

$REF_{IN}$  is the reference frequency input.

$D$  is the value of the RF  $REF_{IN}$  doubler bit.

$R$  is the RF reference division factor.

For example, in a GSM 1800 system, where a 1.8 GHz RF frequency output ( $RF_{OUT}$ ) is required, a 13 MHz reference frequency input ( $REF_{IN}$ ) is available and a 200 kHz channel resolution ( $f_{RES}$ ) is required on the RF output.

$$MOD = REF_{IN} / f_{RES}$$

$$MOD = 13 \text{ MHz} / 200 \text{ kHz} = 65$$

From Equation 4,

$$f_{PFD} = [13 \text{ MHz} \times (1 + 0)/1] = 13 \text{ MHz} \quad (5)$$

$$1.8 \text{ GHz} = 13 \text{ MHz} \times (INT + FRAC/65) \quad (6)$$

where:

$INT$  is 138.

$FRAC$  is 30.

## MODULUS

The choice of modulus ( $MOD$ ) depends on the reference signal ( $REF_{IN}$ ) available and the channel resolution ( $f_{RES}$ ) required at

the RF output. For example, a GSM 1800 system using a 13 MHz  $REF_{IN}$  sets the modulus to 65, resulting in meeting the required RF output resolution ( $f_{RES}$ ) of 200 kHz (13 MHz/65).

## REFERENCE DOUBLER AND REFERENCE DIVIDER

The on-chip reference doubler allows the input reference signal to be doubled. This is useful for increasing the PFD comparison frequency, which in turn improves the noise performance of the system. For example, doubling the PFD frequency usually results in an improvement in noise performance of 3 dB. It is important to note that the PFD cannot operate with frequencies greater than 32 MHz due to a limitation in the speed of the  $\Sigma$ - $\Delta$  circuit of the N-divider.

## 12-BIT PROGRAMMABLE MODULUS

Unlike most fractional-N PLLs, the ADF4154 allows the user to program the modulus over a 12-bit range. Therefore, several configurations of the ADF4154 are possible for an application by varying the modulus value, the reference doubler, and the 4-bit R-counter.

For example, consider an application that requires a 1.75 GHz RF and a 200 kHz channel step resolution. The system has a 13 MHz reference signal.

One possible setup is feeding the 13 MHz  $REF_{IN}$  directly into the PFD and programming the modulus to divide by 65, which results in the required 200 kHz resolution.

Another possible setup is using the reference doubler to create a 26 MHz input frequency from the 13 MHz  $REF_{IN}$  signal. The 26 MHz signal is then fed into the PFD, which programs the modulus to divide by 130. This setup also results in 200 kHz resolution, plus it offers superior phase noise performance compared with the previous setup.

The programmable modulus is also very useful for multi-standard applications. If a dual-mode phone requires PDC and GSM 1800 standards, the programmable modulus is a huge benefit. The PDC requires a 25 kHz channel step resolution, whereas the GSM 1800 requires a 200 kHz channel step resolution. A 13 MHz reference signal could be fed directly to the PFD. The modulus would be programmed to 520 when in PDC mode (13 MHz/520 = 25 kHz). The modulus would be reprogrammed to 65 for GSM 1800 operation (13 MHz/65 = 200 kHz). It is important that the PFD frequency remains constant (13 MHz). By keeping the PFD constant, the user can design a one-loop filter that can be used in both setups without running into stability issues. The ratio of the RF frequency to the PFD frequency affects the loop design. By keeping this relationship constant, the same loop filter can be used in both applications.

## SPURIOUS OPTIMIZATION AND FAST LOCK

The ADF4154 can be optimized for low spurious signals by using the noise and spur register. However, to achieve fast-lock time, a wider loop bandwidth is needed. Note that a wider loop



bandwidth can lead to notable spurious signals, which cannot be reduced significantly by the loop filter.

Using the fast-lock feature can achieve the same fast-lock time as the noise and spur register, but with the advantage of lower spurious signals because the final loop bandwidth is reduced by a quarter.

**FAST-LOCK TIMER AND REGISTER SEQUENCES**

If the fast-lock mode is used, a timer value needs to be loaded into the PLL to determine the time spent in wide bandwidth mode.

When the load control bit is set to 1, the timer value is loaded via the 12-bit modulus value. To use fast lock, the PLL must be written to in the following sequence:

1. Load the R-divider register with DB23 = 1 and the chosen fast-lock timer value (DB13 to DB2) instead of the modulus. Note that the duration that the PLL remains in wide bandwidth is equal to the fast-lock timer/ $f_{PFD}$ .
2. Load the noise and spur register.
3. Load the control register.
4. Load the R-divider register with DB23 = 0 and MUXOUT = 110 (DB22 to DB20). This sets the fast-lock switch to appear at the MUXOUT pin. All the other needed parameters, including the modulus, also need to be loaded.
5. Load the N-divider register, including fast lock = 1 (DB23), to activate fast-lock mode.

After this procedure is complete, the user need only repeat Step 5 to invoke fast lock for subsequent frequency jumps.

**FAST LOCK: AN EXAMPLE**

If a PLL has reference frequencies of 13 MHz and  $f_{PFD} = 13$  MHz and a required lock time of 50  $\mu$ s, the PLL is set to wide bandwidth for 40  $\mu$ s.

If the time period set for the wide bandwidth is 40  $\mu$ s, then

$$\text{Fast-Lock Timer Value} = \text{Time in Wide Bandwidth} \times f_{PFD}$$

$$\text{Fast-Lock Timer Value} = 40 \mu\text{s} \times 13 \text{ MHz} = 520$$

Therefore, 520 must be loaded into the R-divider register in Step 1 of the sequence described in the Fast-Lock Timer and Register Sequences section.

**FAST LOCK: LOOP FILTER TOPOLOGY**

To use fast-lock mode, an extra connection from the PLL to the loop filter is needed. The damping resistor in the loop filter must be reduced to  $\frac{1}{4}$  of its value while in wide bandwidth mode. This is required because the charge pump current is increased by 16 while in wide bandwidth mode, and stability must be ensured. During fast lock, the MUXOUT pin is shorted to ground (the fast-lock switch must be programmed to appear at the MUXOUT pin). The following two topologies can be used:

- Divide the damping resistor (R1) into two values (R1 and R1A) that have a ratio of 1:3 (see Figure 19).

- Connect an extra resistor (R1A) directly from MUXOUT, as shown in Figure 19. The extra resistor must be chosen such that the parallel combination of an extra resistor and the damping resistor (R1) is reduced to  $\frac{1}{4}$  of the original value of R1 (see Figure 20).

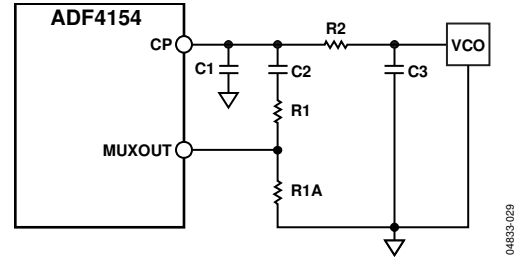


Figure 19. Fast-Lock Loop Filter Topology—Topology 1

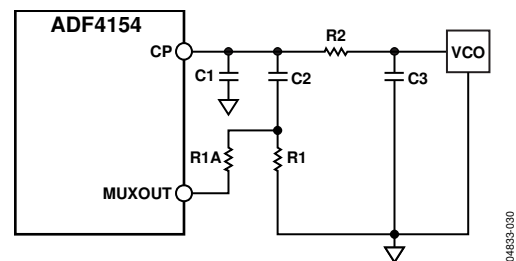


Figure 20. Fast-Lock Loop Filter Topology—Topology 2

**SPUR MECHANISMS**

The following section describes three spur mechanisms that can arise when using a fractional-N synthesizer and how to minimize them in the ADF4154.

**Fractional Spurs**

The fractional interpolator in the ADF4154 is a third-order  $\Sigma$ - $\Delta$  modulator (SDM) with a modulus MOD that is programmable to an integer value between 2 and 4095. In low spur mode (dither enabled), the minimum allowed value of MOD is 50. The SDM is clocked at the PFD reference rate ( $f_{PFD}$ ) that allows PLL output frequencies to be synthesized at a channel step resolution of  $f_{PFD}/\text{MOD}$ .

In low noise mode and low noise and spur mode (dither off), the quantization noise from the  $\Sigma$ - $\Delta$  modulator appears as fractional spurs. The interval between spurs is  $f_{PFD}/L$ , where L is the repeat length of the code sequence in the digital  $\Sigma$ - $\Delta$  modulator. For the third-order modulator used in the ADF4154, the repeat length depends on the value of MOD, as shown in Table 11.

**Table 11. Fractional Spurs with Dither Off**

Condition (Dither Off)	Repeat Length	Spur Interval
If MOD is divisible by 2, but not 3	$2 \times \text{MOD}$	Channel step/2
If MOD is divisible by 3, but not 2	$3 \times \text{MOD}$	Channel step/3
If MOD is divisible by 6	$6 \times \text{MOD}$	Channel step/6
Otherwise	MOD	Channel step

In low spur mode (dither enabled), the repeat length is extended to  $2^{21}$  cycles, regardless of the value of MOD, which makes the quantization error spectrum appear as broadband noise. This can degrade the in-band phase noise at the PLL output by as much as 10 dB. Therefore, for lowest noise, dither off is a better choice, particularly when the final loop BW is low enough to attenuate even the lowest frequency fractional spur.

### Integer Boundary Spurs

Another mechanism for fractional spur creation are interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related (as is the case with fractional-N synthesizers), spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or the difference in frequency between an integer multiple of the reference and the VCO frequency.

These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference, where the difference frequency can be inside the loop bandwidth, thus the name integer boundary spurs.

### Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers because the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. One such mechanism is feedthrough of low levels of on-chip reference switching noise through the RF<sub>IN</sub> pin back to the VCO, resulting in reference spur levels as high as -90 dBc. Care should be taken in the PCB layout to ensure that the VCO is well separated from the input reference to avoid a possible feed-through path on the board.

### SPUR CONSISTENCY

When jumping from Frequency A to Frequency B and then back again using fractional-N synthesizers, the spur levels often differ each time Frequency A is programmed. However, in the ADF4154, the spur levels on any particular channel are always consistent.

### FILTER DESIGN—ADIsimPLL

A filter design and analysis program is available to help the user implement the PLL design. Visit [www.analog.com/pll](http://www.analog.com/pll) for a free download of the ADIsimPLL software. The software designs, simulates, and analyzes the entire PLL frequency and time domain response. Various passive and active filter architectures are allowed.

### INTERFACING

The ADF4154 has a simple, SPI®-compatible serial interface for writing to the device. SCLK, SDATA, and LE control the data transfer. When LE (latch enable) is high, the 22 bits that have been clocked into the input register on each rising edge of SCLK are transferred to the appropriate latch. See Figure 2 for the timing diagram and Table 5 for the latch truth table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 909 kHz or one update every 1.1  $\mu$ s.

### ADuC812 Interface

Figure 21 shows the interface between the ADF4154 and the ADuC812 MicroConverter®. Because the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA set to 0. To initiate the operation, bring the I/O port driving LE low. Each latch of the ADF4154 requires a 24-bit word, which is accomplished by writing three 8-bit bytes from the MicroConverter to the device. After the third byte is written, the LE input should be brought high to complete the transfer.

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed is 180 kHz.

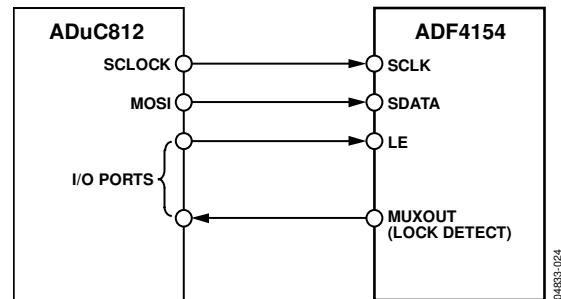


Figure 21. ADuC812-to-ADF4154 Interface

### ADSP-21xx Interface

Figure 22 shows the interface between the ADF4154 and the ADSP-21xx digital signal processor. As discussed previously, the ADF4154 requires a 24-bit serial word for each latch write. The easiest way to accomplish this using a device in the ADSP-21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for eight bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store each of the three 8-bit bytes, enable the autobuffered mode, and write to the transmit register of the DSP. This last operation initiates the autobuffered transfer.

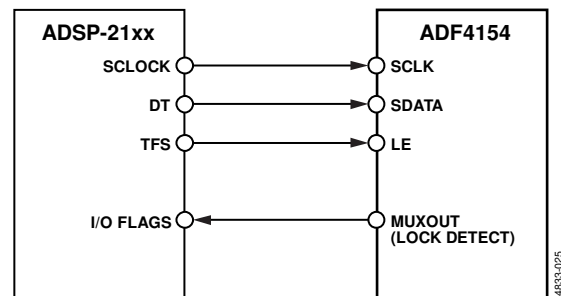


Figure 22. ADSP-21xx-to-ADF4154 Interface

**PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE**

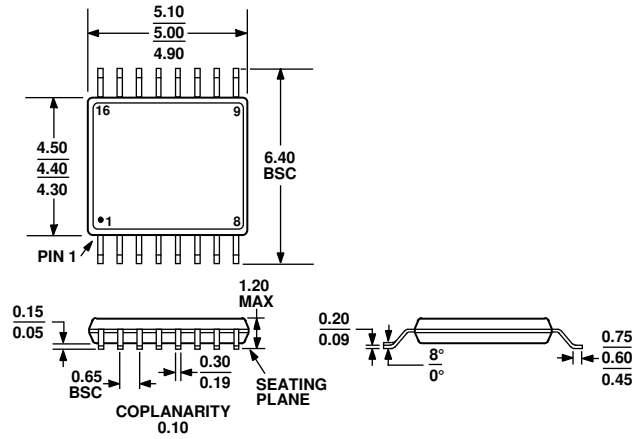
The lands on the chip scale package (CP-20-1) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. The land should be centered on the pad. This ensures that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edges of the pad pattern to avoid shorting.

Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated into the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz of copper to plug the via.

The user should connect the printed circuit board thermal pad to AGND.

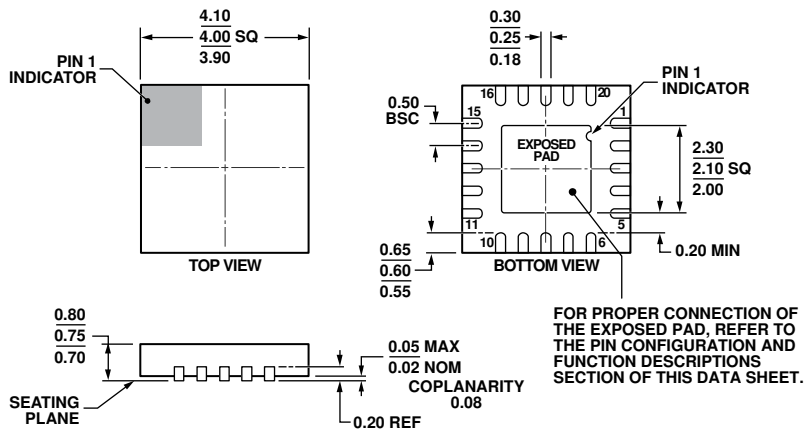
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 23. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-1.

Figure 24. 20-Lead Lead Frame Chip Scale Package [LFCSP\_WQ] 4 mm x 4 mm Very Very Thin Quad, (CP-20-6)

Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Description	Package Option
ADF4154BRU	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4154BRU-REEL	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4154BRU-REEL7	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4154BRUZ	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4154BRUZ-RL	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4154BRUZ-RL7	-40°C to +85°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADF4154BCPZ	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4154BCPZ-RL	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
ADF4154BCPZ-RL7	-40°C to +85°C	20-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-20-6
EVAL-ADF4154EBZ1		Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**NOTES**

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).