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Direct Modulation/Waveform Generating, 6.1 GHz Fractional-N Frequency Synthesizer

Data Sheet **ADF4158**

FEATURES

Radio frequency (RF) bandwidth to 6.1 GHz
25-bit fixed modulus allows subhertz frequency resolution
Frequency and phase modulation capability
Sawtooth and triangular waveforms in the frequency domain
Parabolic ramp
Ramp superimposed with FSK
Ramp with 2 different sweep rates
Ramp delay
Ramp frequency readback
Ramp interruption
2.7 V to 3.3 V power supply
Separate V_P allows extended tuning voltage
Programmable charge pump currents
3-wire serial interface
Digital lock detect
Power-down mode
Cycle slip reduction for faster lock times
Switched bandwidth fast-lock mode
Qualified for automotive applications

APPLICATIONS

Frequency modulated continuous wave (FMCW) radar
Communications test equipment

GENERAL DESCRIPTION

The ADF4158 is a 6.1 GHz fractional-N frequency synthesizer with direct modulation and waveform generation capability. It contains a 25-bit fixed modulus, allowing subhertz resolution at 6.1 GHz. It consists of a low noise digital phase frequency detector (PFD), a precision charge pump, and a programmable reference divider. There is a sigma-delta (Σ-Δ) based fractional interpolator to allow programmable fractional-N division. The INT and FRAC registers define an overall N-divider as $N = INT + (FRAC/2^{25})$.

The ADF4158 can be used to implement frequency shift keying (FSK) and phase shift keying (PSK) modulation. There are also a number of frequency sweep modes available that generate various waveforms in the frequency domain, for example, sawtooth and triangular waveforms. The ADF4158 features cycle slip reduction circuitry, which leads to faster lock times, without the need for modifications to the loop filter.

Control of all on-chip registers is via a simple 3-wire interface. The device operates with a power supply ranging from 2.7 V to 3.3 V and can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

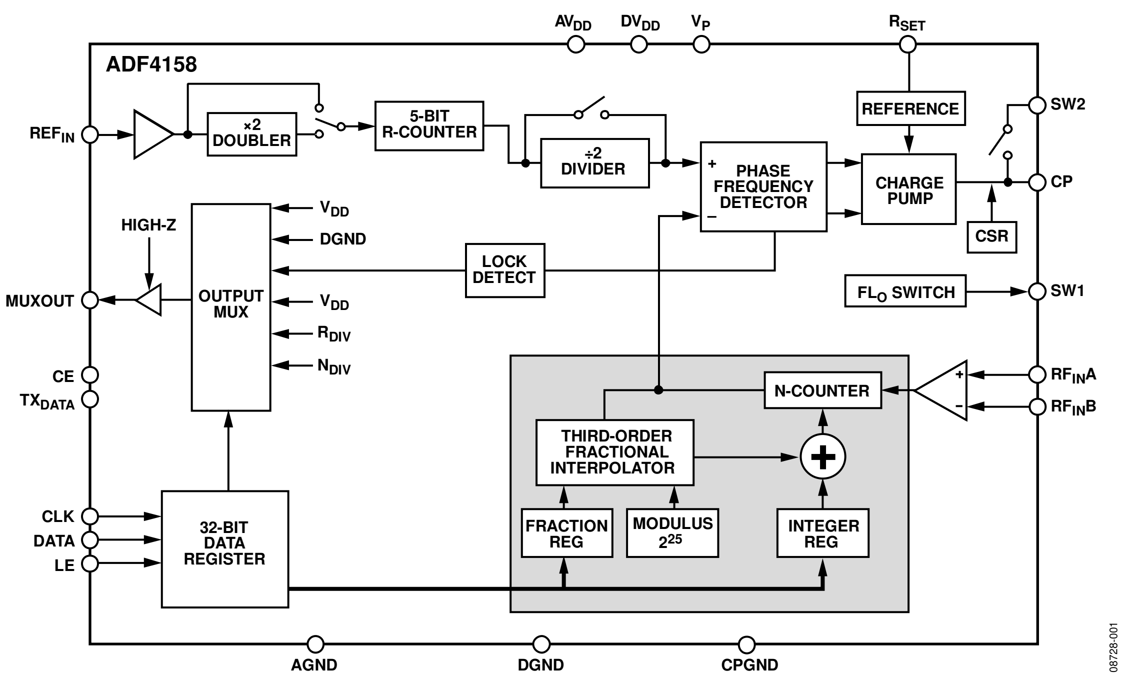

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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EVALUATION KITS

- ADF4158 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1154: Optimizing Phase Noise and Spur Performance of the ADF4157 and ADF4158 PLLs Using Constant Negative Bleed

Data Sheet

- ADF4158: Direct Modulation/Waveform Generating, 6.1 GHz Fractional-N Frequency Synthesizer Data Sheet

User Guides

- UG-123: Evaluation Board for ADF4158 Fractional-N PLL Frequency Synthesizer
- UG-476: PLL Software Installation Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADF4158 and ADF4159 Evaluation Board Software

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF
- ADF4158CCPZ IBIS Model

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- ADF4158 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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3/14—Rev. F to Rev. G

2/14—Rev. E to Rev. F

3/13—Rev. D to Rev. E

6/12—Rev. C to Rev. D

12/11—Rev. B to Rev. C

9/11—Rev. A to Rev. B

7/11—Rev. 0 to Rev. A

4/10—Revision 0: Initial Version

SPECIFICATIONS

$AV_{DD} = DV_{DD}$ = 2.7 V to 3.3 V, $V_P = AV_{DD}$ to 5.5 V, AGND = DGND = 0 V, $T_A = T_{MIN}$ to T_{MAX}, dBm referred to 50 Ω, unless otherwise noted.

Table 1.

	C Version[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
RF CHARACTERISTICS					
RF Input Frequency (RF_{IN})	0.5		6.1	GHz	−10 dBm minimum to 0 dBm maximum; for lower frequencies, ensure slew rate (SR) > 400 V/µs
					−15 dBm minimum to 0 dBm maximum for 2 GHz to 4 GHz RF input frequency
REFERENCE CHARACTERISTICS					
REF_{IN} Input Frequency	10		260	MHz	For f < 10 MHz, use a dc-coupled CMOS-compatible square wave, slew rate > 25 V/µs
			16	MHz	If an internal reference doubler is enabled
REF_{IN} Input Sensitivity	0.4		AV_{DD}	V p-p	Biased at $AV_{DD}/2$[2]
REF_{IN} Input Capacitance			10	pF	
REF_{IN} Input Current			±100	µA	
PHASE DETECTOR					
Phase Detector Frequency[3]			32	MHz	
CHARGE PUMP					
I_{CP} Sink/Source					Programmable
High Value		5		mA	With R_{SET} = 5.1 kΩ
Low Value		312.5		µA	
Absolute Accuracy		2.5		%	With R_{SET} = 5.1 kΩ
R_{SET} Range	2.7		10	kΩ	
I_{CP} Three-State Leakage Current		1		nA	Sink and source current
Matching		2		%	$0.5 V < V_{CP} < V_P - 0.5 V$
I_{CP} vs. V_{CP}		2		%	$0.5 V < V_{CP} < V_P - 0.5 V$
I_{CP} vs. Temperature		2		%	$V_{CP} = V_P/2$
LOGIC INPUTS					
V_{INH}, Input High Voltage	1.4			V	
V_{INL}, Input Low Voltage			0.6	V	
I_{INH}/I_{INL}, Input Current			±1	µA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUTS					
V_{OH}, Output High Voltage	1.4			V	Open-drain output chosen; 1 kΩ pull-up to 1.8 V
V_{OH}, Output High Voltage	V_{DD} − 0.4			V	CMOS output chosen
I_{OH}, Output High Current			100	µA	
V_{OL}, Output Low Voltage			0.4	V	I_{OL} = 500 µA
POWER SUPPLIES					
AV_{DD}	2.7		3.3	V	
DV_{DD}		AV_{DD}			
V_P	AV_{DD}		5.5	V	
I_{DD}		23	32	mA	

Parameter	C Version[1]			Unit	Test Conditions/Comments
	Min	Typ	Max		
NOISE CHARACTERISTICS					
Normalized Phase Noise Floor (PN_{SYNTH})[4]		−216		dBc/Hz	PLL loop bandwidth = 500 kHz; measured at 100 kHz offset
Normalized 1/f Noise (PN_{1_f})[5]		−110		dBc/Hz	100 kHz offset; normalized to 1 GHz
Phase Noise Performance[6]					At VCO output
5805 MHz Output[7]		−93		dBc/Hz	At 5 kHz offset, 32 MHz PFD frequency

[1] Operating temperature for C version: −40°C to +125°C.
[2] AC coupling ensures $AV_{DD}/2$ bias.
[3] Guaranteed by design. Sample tested to ensure compliance.
[4] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log(N) (where N is the N divider value) and 10 log(f_{PFD}). $PN_{SYNTH} = PN_{TOT} - 10\log(f_{PFD}) - 20\log(N)$.
[5] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF}, and at a frequency offset f is given by $PN = PN_{1\_f} + 10\log(10\text{ kHz}/f) + 20\log(f_{RF}/1\text{ GHz})$. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL™.
[6] The phase noise is measured with the EVAL-ADF4158EB1Z and the Agilent E5052A phase noise system.
[7] f_{REFIN} = 128 MHz; f_{PFD} = 32 MHz; offset frequency = 5 kHz; RF_{OUT} = 5805 MHz; INT = 181; FRAC = 13631488; loop bandwidth = 100 kHz.

TIMING SPECIFICATIONS

$AV_{DD} = DV_{DD} = SDV_{DD}$ = 2.7 V to 3.3 V; $V_P = AV_{DD}$ to 5.5 V; AGND = DGND = SDGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, dBm referred to 50 Ω, unless otherwise noted.

Table 2. Write Timing

Parameter	Limit at T_{MIN} to T_{MAX} (C Version)	Unit	Test Conditions/Comments
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

Write Timing Diagram

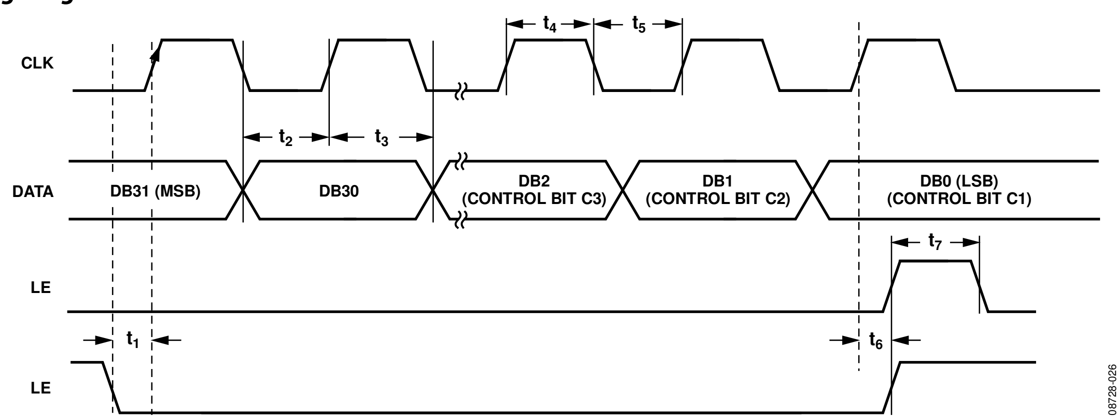


Figure 2. Write Timing Diagram

Table 3. Read Timing

Parameter	Limit at T_{MIN} to T_{MAX} (C Version)	Unit	Test Conditions/Comments
t_1	20	ns min	TX_{DATA} setup time
t_2	20	ns min	CLK setup time to DATA (on MUXOUT)
t_3	25	ns min	CLK high duration
t_4	25	ns min	CLK low duration
t_5	10	ns min	CLK to LE setup time

Read Timing Diagram

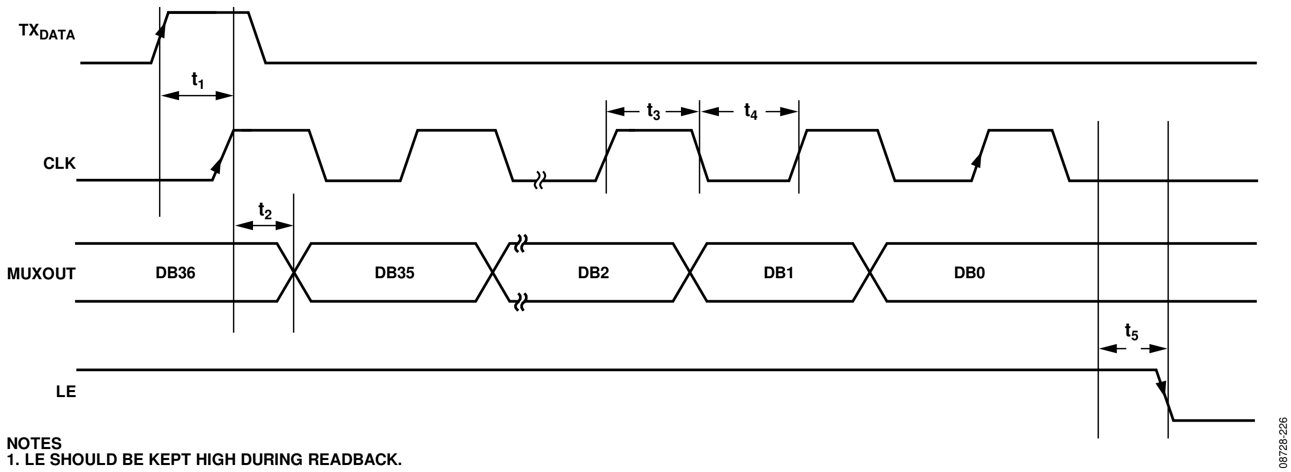


Figure 3. Read Timing Diagram

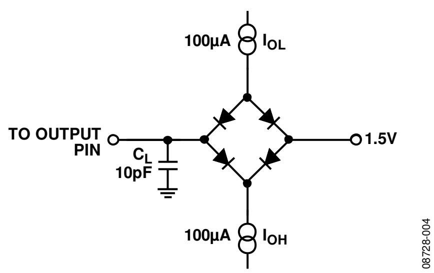


Figure 4. Load Circuit for MUXOUT Timing, C_L = 10 pF

ABSOLUTE MAXIMUM RATINGS

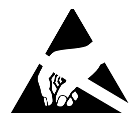
T_A = 25°C, GND = AGND = DGND = SDGND = 0 V, V_{DD} = AV_{DD} = DV_{DD} = SDV_{DD}, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +4 V
DV_{DD} to AV_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +5.8 V
V_P to V_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
REF_{IN}, RF_{IN} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (C Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance (Paddle Soldered)	30.4°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND PIN FUNCTION DESCRIPTIONS

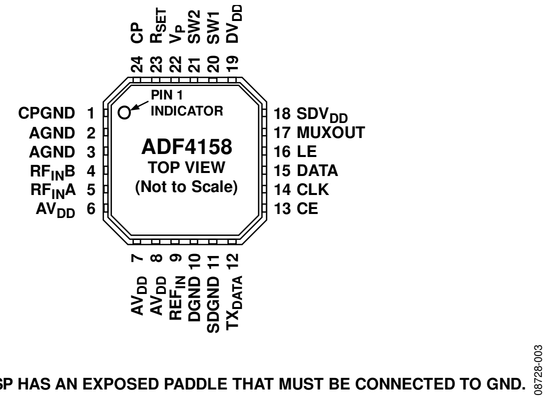


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
2, 3	AGND	Analog Ground. This is the ground return path of the prescaler.
4	$RF_{IN}B$	Complementary Input to the RF Prescaler. Decouple this point to the ground plane with a small bypass capacitor, typically 100 pF.
5	$RF_{IN}A$	Input to the RF Prescaler. This small signal input is normally ac-coupled from the VCO.
6, 7, 8	AV_{DD}	Positive Power Supply for the RF Section. Place decoupling capacitors to the digital ground plane as close as possible to this pin. AV_{DD} must have the same voltage as DV_{DD}.
9	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and an equivalent input resistance of 100 kΩ. It can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
10	DGND	Digital Ground.
11	SDGND	Digital Σ-Δ Modulator Ground. Ground return path for the Σ-Δ modulator.
12	TX_{DATA}	Tx Data Pin. Provide data to be transmitted in FSK or PSK mode on this pin.
13	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode.
14	CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the shift register on the CLK rising edge. This input is a high impedance CMOS input.
15	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs being the control bits. This input is a high impedance CMOS input.
16	LE	Load Enable, CMOS Input. When LE is high, the data stored in the shift registers is loaded into one of the eight latches, with the latch being selected using the control bits.
17	MUXOUT	Multiplexer Output. This pin allows either the RF lock detect, the scaled RF, or the scaled reference frequency to be accessed externally.
18	SDV_{DD}	Power Supply Pin for the Digital Σ-Δ Modulator. This pin should be the same voltage as AV_{DD}. Place decoupling capacitors to the ground plane as close as possible to this pin.
19	DV_{DD}	Positive Power Supply for the Digital Section. Place decoupling capacitors to the digital ground plane as close as possible to this pin. DV_{DD} must have the same voltage as AV_{DD}.
20 , 21	SW1, SW2	Switches for Fast Lock.
22	V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5.5 V and used to drive a VCO with a tuning range of up to 5.5 V.
23	R_{SET}	Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I_{CP} and R_{SET} is $$I_{CPmax} = \frac{25.5}{R_{SET}}$$ where: I_{CPmax} = 5 mA. R_{SET} = 5.1 kΩ.
24	CP	Charge Pump Output. When enabled, this provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.
25	EPAD	Exposed Paddle. The LFCSP has an exposed paddle that must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

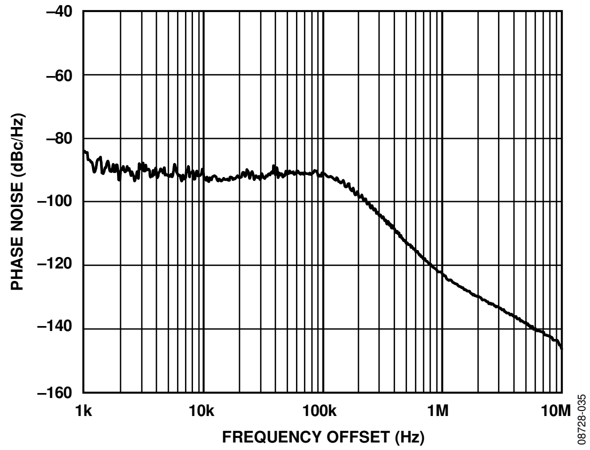


Figure 6. Phase Noise at 5805 MHz, PFD = 32 MHz, Loop Bandwidth = 100 kHz

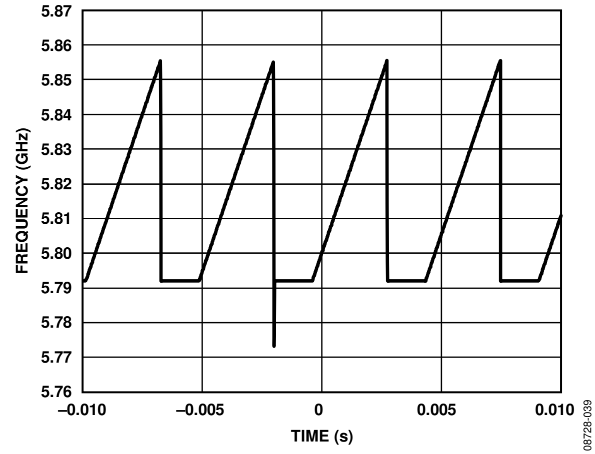


Figure 9. Delay Between Ramps for Sawtooth Waveform, PFD = 32 MHz, INT = 181, FRAC = 0, DEV Offset = 4, DEV Word = 20972, Step Word = 200, CLK_2 Divider = 10, CLK_1 Divider = 125, DEL Start Word = 1025

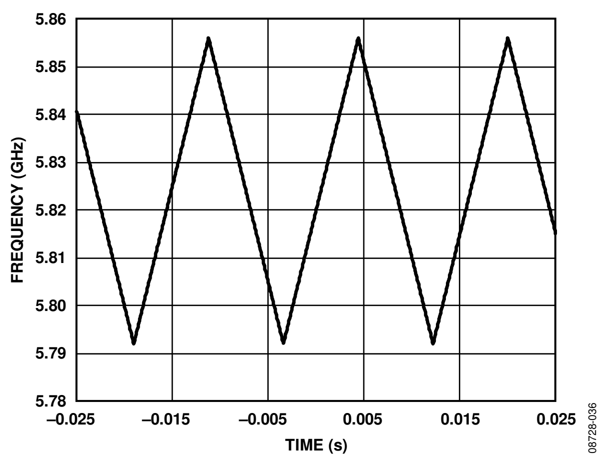


Figure 7. Triangular Waveform, PFD = 32 MHz, INT = 181, FRAC = 0, DEV Offset = 4, DEV Word = 20972, Step Word = 200, CLK_2 Divider = 10, CLK_1 Divider = 125

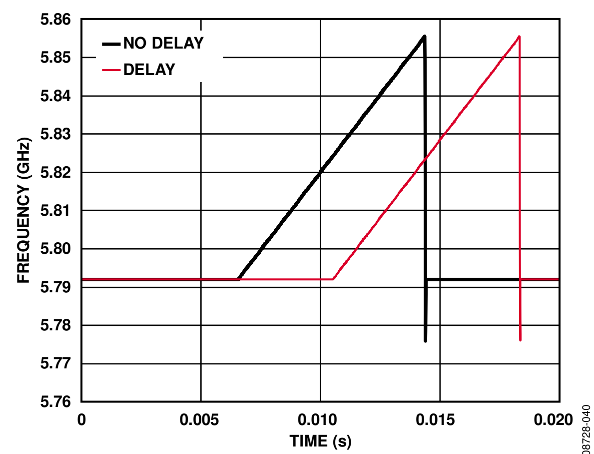


Figure 10. Delayed Start of Triangular Burst, PFD = 32 MHz, INT = 181, FRAC = 0, DEV Offset = 4, DEV Word = 20972, Step Word = 200, CLK_2 Divider = 10, CLK_1 Divider = 125, DEL Start Word = 1000

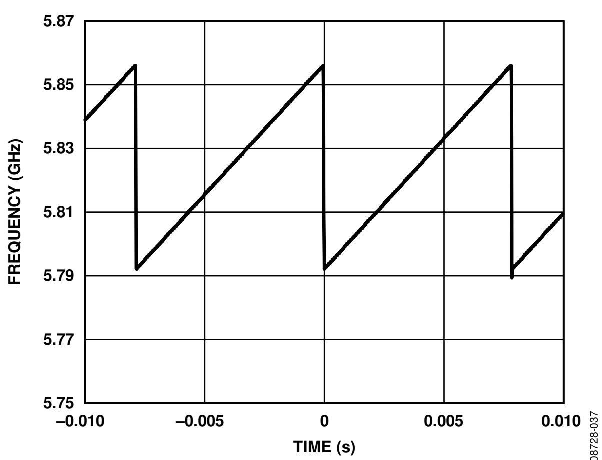


Figure 8. Sawtooth Waveform, PFD = 32 MHz, INT = 181, FRAC = 0, DEV Offset = 4, DEV Word = 20972, Step Word = 200, CLK_2 Divider = 10, CLK_1 Divider = 125

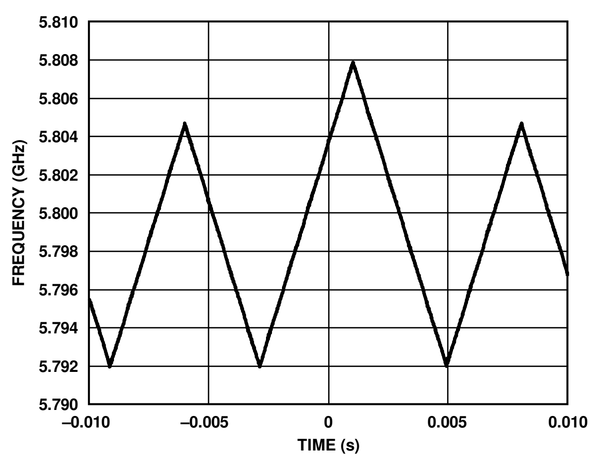


Figure 11. Dual Ramp Rate Waveform, PFD = 32 MHz, INT = 181, FRAC = 0, Ramp 1: DEV Offset = 3, DEV Word = 16777, Step Word = 100, Ramp 2: DEV Offset = 3, DEV Word = 20792, Step Word = 80

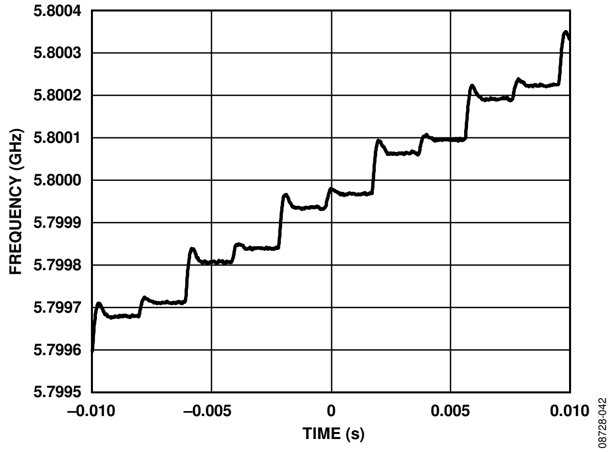


Figure 12. FSK Superimposed on Rising Edge of Triangular Waveform; Ramp Settings: PFD = 32 MHz, INT = 181, FRAC = 0, DEV Offset = 4, DEV Word = 20972, Step Word = 200, CLK DIV = 10, CLK_1 Divider = 125; FSK Settings: DEV Offset = 3, DEV Word = 4194

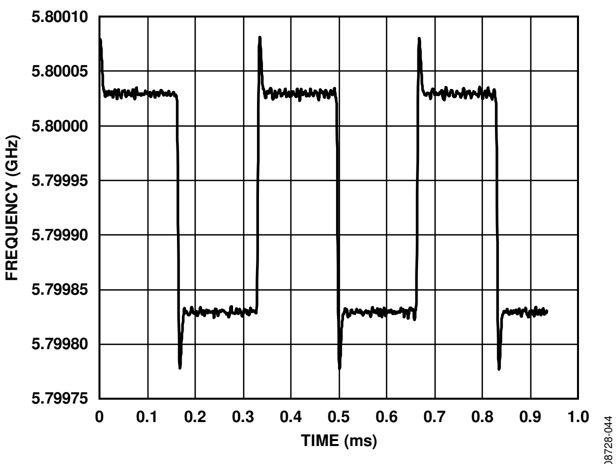


Figure 13. FSK; Settings: Frequency Deviation = 100 kHz, Data Rate = 3 kHz

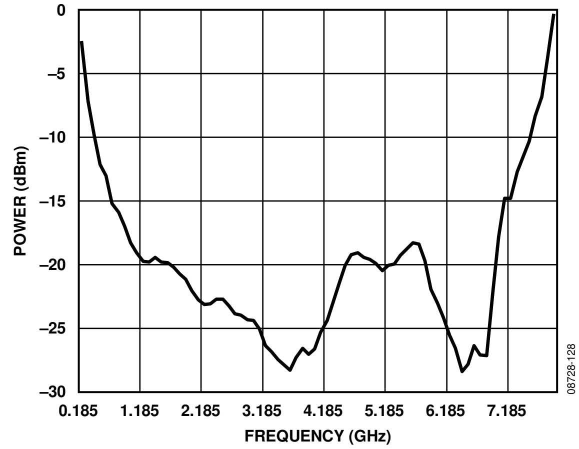


Figure 14. RF_{IN} Sensitivity-Average Over Temperature and V_{DD}

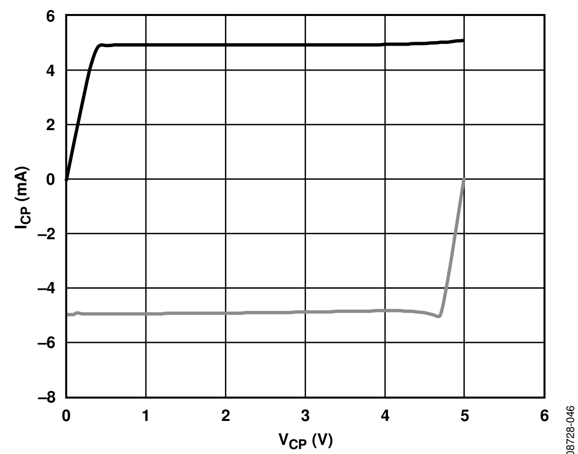


Figure 15. Charge Pump Output Characteristics

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 16. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

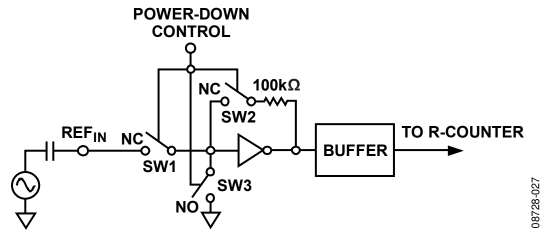


Figure 16. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 17. It is followed by a 2-stage limiting amplifier to generate the current-mode logic (CML) clock levels needed for the prescaler.

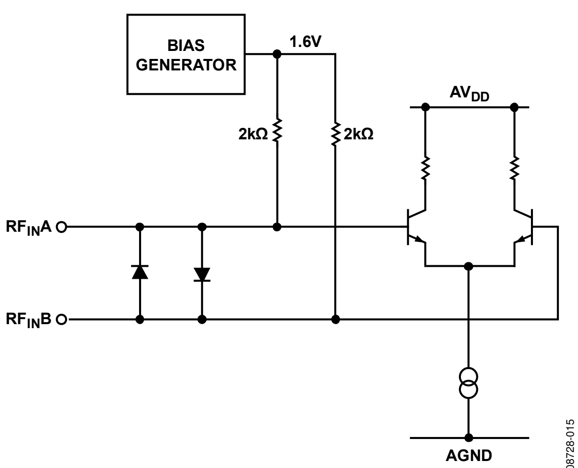


Figure 17. RF Input Stage

RF INT DIVIDER

The RF INT CMOS counter allows a division ratio in the PLL feedback counter. Division ratios from 23 to 4095 are allowed.

25-BIT FIXED MODULUS

The ADF4158 has a 25-bit fixed modulus. This allows output frequencies to be spaced with a resolution of

$$f_{RES} = f_{PFD}/2^{25} \quad (1)$$

where f_{PFD} is the frequency of the phase frequency detector (PFD). For example, with a PFD frequency of 10 MHz, frequency steps of 0.298 Hz are possible. Due to the architecture of the Σ-Δ modulator, there is a fixed + ($f_{PFD}/2^{26}$) offset on the VCO output. To remove this offset, see the Σ-Δ Modulator Mode section.

INT, FRAC, AND R RELATIONSHIP

The INT and FRAC values, in conjunction with the R-counter, make it possible to generate output frequencies that are spaced by fractions of the phase frequency detector (PFD). The RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = f_{PFD} \times (INT + (FRAC/2^{25})) \quad (2)$$

where:

RF_{OUT} is the output frequency of external voltage controlled oscillator (VCO).

INT is the preset divide ratio of binary 12-bit counter (23 to 4095).

FRAC is the numerator of the fractional division (0 to $2^{25} - 1$).

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (3)$$

where:

REF_{IN} is the reference input frequency.

D is the REF_{IN} doubler bit (0 or 1).

R is the preset divide ratio of the binary, 5-bit, programmable reference counter (1 to 32).

T is the REF_{IN} divide-by-2 bit (0 or 1).

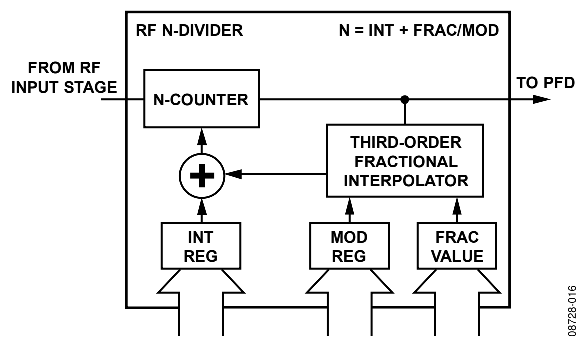


Figure 18. RF N-Divider

R-COUNTER

The 5-bit R-counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R-counter and N-counter and produces an output proportional to the phase and frequency difference between them. Figure 19 shows a simplified schematic of the PFD. The PFD includes a fixed delay element that sets the width of the antibacklash pulse, which is typically 3 ns. This pulse ensures that there is no dead zone in the PFD transfer function and gives a consistent reference spur level.

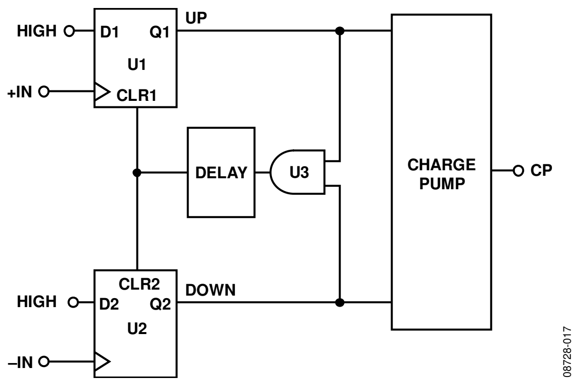


Figure 19. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4158 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by the M4, M3, M2, and M1 bits (see Figure 23). Figure 20 shows the MUXOUT section in block diagram form.

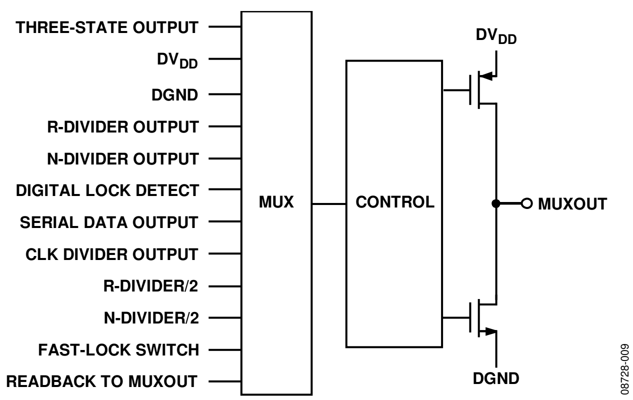


Figure 20. MUXOUT Schematic

INPUT SHIFT REGISTERS

The ADF4158 digital section includes a 5-bit RF R-counter, a 12-bit RF N-counter, and a 25-bit FRAC counter. Data is clocked into the 32-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of eight latches on the rising edge of LE. The destination latch is determined by the state of the three control bits (C3, C2, and C1) in the shift register. These are the three LSBs—DB2, DB1, and DB0—as shown in Figure 2. The truth table for these bits is shown in Table 6. Figure 21 and Figure 22 show a summary of how the latches are programmed.

PROGRAM MODES

Table 6 and Figure 23 through Figure 30 show how to set up the program modes in the ADF4158.

Several settings in the ADF4158 are double buffered. These include the LSB fractional value, R-counter value, reference doubler, current setting, and RDIV2. This means that two events must occur before the part uses a new value for any of the double-buffered settings. First, the new value is latched into the device by writing to the appropriate register. Second, a new write must be performed on Register R0.

For example, updating the fractional value can involve a write to the 13 LSB bits in R1 and the 12 MSB bits in R0. R1 should be written to first, followed by the write to R0. The frequency change begins after the write to R0. Double buffering ensures that the bits written to in R1 do not take effect until after the write to R0.

Table 6. C3, C2, and C1 Truth Table

Control Bits			
C3	C2	C1	Register
0	0	0	R0
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	R4
1	0	1	R5
1	1	0	R6
1	1	1	R7

REGISTER MAPS

FRAC/INT REGISTER (R0)

RAMP ON	MUXOUT CONTROL				12-BIT INTEGER VALUE (INT)												12-BIT MSB FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R1	M4	M3	M2	M1	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	C3(0)	C2(0)	C1(0)

LSB FRAC REGISTER (R1)

RESERVED				13-BIT LSB FRACTIONAL VALUE (FRAC) (DBB)													RESERVED												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	0	0	0	0	0	0	0	0	0	0	0	0	C3(0)	C2(0)	C1(1)

R-DIVIDER REGISTER (R2)

RESERVED			CSR EN	CP CURRENT SETTING (DBB)				RESERVED	PRESCALER	RDIV2 DBB	REFERENCE DOUBLER DBB	5-BIT R-COUNTER (DBB)					12-BIT CLK_1 DIVIDER												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	CR1	CPI4	CPI3	CPI2	CPI1	0	P1	U2	U1	R5	R4	R3	R2	R1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(0)	C2(1)	C1(0)

FUNCTION REGISTER (R3)

RESERVED																N SEL	SD RESET	RESERVED		RAMP MODE		PSK ENABLE	FSK ENABLE	LDP	PD POLARITY	POWER-DOWN	CP THREE-STATE	COUNTER RESET	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	NS1	U12	0	0	RM2	RM1	PE1	FE1	U11	U10	U9	U8	U7	C3(0)	C2(1)	C1(1)

NOTES
1. DBB = DOUBLE-BUFFERED BIT(S).

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Figure 21. Register Summary 1

TEST REGISTER (R4)

LE SEL	Σ-Δ MODULATOR MODE					RESERVED	NEG BLEED CURRENT		READ-BACK TO MUXOUT		CLK DIV MODE		12-BIT CLK_2 DIVIDER VALUE												RESERVED				CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
LS1	S5	S4	S3	S2	S1	0	NB2	NB1	R2	R1	C2	C1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	0	0	0	0	C3(1)	C2(0)	C1(0)

DEVIATION REGISTER (R5)

RESERVED		TX RAMP CLK	PAR RAMP	INTERRUPT		FSK RAMP EN	RAMP 2 EN	DEV SEL	4-BIT DEV OFFSET WORD				16-BIT DEVIATION WORD																CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	TR1	PR1	I2	I1	FRE1	R2E1	DS1	DO4	DO3	DO2	DO1	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(1)	C2(0)	C1(1)

STEP REGISTER (R6)

RESERVED								STEP SEL	20-BIT STEP WORD																				CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	SSE1	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	C3(1)	C2(1)	C1(0)

DELAY REGISTER (R7)

RESERVED													RAMP DEL FL	RAMP DEL	DEL CLK SEL	DEL START EN	12-BIT DELAY START DIVIDER												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	RDF1	RD1	DC1	DSE1	DS12	DS11	DS10	DS9	DS8	DS7	DS6	DS5	DS4	DS3	DS2	DS1	C3(1)	C2(1)	C1(1)

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Figure 22. Register Summary 2

FRAC/INT REGISTER (R0) MAP

With Register R0 DB[2:0] set to [0, 0, 0], the on-chip FRAC/INT register is programmed as shown in Figure 23.

Ramp On

Setting DB31 to 1 enables the ramp, setting DB31 to 0 disables the ramp.

MUXOUT Control

The on-chip multiplexer is controlled by DB[30:27] on the ADF4158. See Figure 23 for the truth table.

12-Bit Integer Value (INT)

These 12 bits control what is loaded as the INT value. This is used to determine the overall feedback division factor. It is used in Equation 2. See the INT, FRAC, and R Relationship section for more information.

12-Bit MSB Fractional Value (FRAC)

These 12 bits, along with Bits DB[27:15] in the LSB FRAC register (Register R1), control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall feedback division factor. It is also used in Equation 2. These 12 bits are the most significant bits (MSB) of the 25-bit FRAC value, and Bits DB[27:15] in the LSB FRAC register (Register R1) are the least significant bits (LSB). See the RF Synthesizer: A Worked Example section for more information.

RAMP ON	MUXOUT CONTROL				12-BIT INTEGER VALUE (INT)												12-BIT MSB FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R1	M4	M3	M2	M1	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	C3(0)	C2(0)	C1(0)

R1	RAMP ON
0	RAMP DISABLED
1	RAMP ENABLED

M4	M3	M2	M1	OUTPUT
0	0	0	0	THREE-STATE OUTPUT
0	0	0	1	DV_{DD}
0	0	1	0	DGND
0	0	1	1	R-DIVIDER OUTPUT
0	1	0	0	N-DIVIDER OUTPUT
0	1	0	1	RESERVED
0	1	1	0	DIGITAL LOCK DETECT
0	1	1	1	SERIAL DATA OUTPUT
1	0	0	0	RESERVED
1	0	0	1	RESERVED
1	0	1	0	CLK DIVIDER OUTPUT
1	0	1	1	RESERVED
1	1	0	0	FAST-LOCK SWITCH
1	1	0	1	R-DIVIDER/2
1	1	1	0	N-DIVIDER/2
1	1	1	1	READBACK TO MUXOUT

F25	F24	....	F15	F14	MSB FRACTIONAL VALUE (FRAC)*
0	0	....	0	0	0
0	0	....	0	1	1
0	0	....	1	0	2
0	0	....	1	1	3
.	.	....	.	.	.
.	.	....	.	.	.
.	.	....	.	.	.
1	1	....	0	0	4092
1	1	....	0	1	4093
1	1	....	1	0	4094
1	1	....	1	1	4095

*THE FRAC VALUE IS MADE UP OF THE 12-BIT MSB STORED IN REGISTER R0, AND THE 13-BIT LSB REGISTER STORED IN REGISTER R1. FRAC VALUE = 13-BIT LSB + 12-BIT MSB × 2^{13}.

N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	INTEGER VALUE (INT)
0	0	0	0	0	0	0	1	0	1	1	1	23
0	0	0	0	0	0	0	1	1	0	0	0	24
0	0	0	0	0	0	0	1	1	0	0	1	25
0	0	0	0	0	0	0	1	1	0	1	0	26
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	0	1	4093
1	1	1	1	1	1	1	1	1	1	1	0	4094
1	1	1	1	1	1	1	1	1	1	1	1	4095

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Figure 23. FRAC/INT Register (R0) Map

LSB FRAC REGISTER (R1) MAP

With Register R1 DB[2:0] set to [0, 0, 1], the on-chip LSB FRAC register is programmed as shown in Figure 24.

13-Bit LSB FRAC Value

These 13 bits, along with Bits DB[14:3] in the FRAC/INT register (Register R0), control what is loaded as the FRAC value into the fractional interpolator. This is part of what determines the overall feedback division factor. It is also used in Equation 2. These 13 bits are the least significant bits (LSB) of the 25-bit FRAC value, and Bits DB[14:3] in the INT/FRAC register are the most significant bits (MSB). See the RF Synthesizer: A Worked Example section for more information.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

RESERVED				13-BIT LSB FRACTIONAL VALUE (FRAC) (DBB)													RESERVED												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	0	0	0	0	0	0	0	0	0	0	0	0	C3(0)	C2(0)	C1(1)

F13	F12	....	F2	F1	LSB FRACTIONAL VALUE (FRAC)*
0	0	....	0	0	0
0	0	....	0	1	1
0	0	....	1	0	2
0	0	....	1	1	3
.	.	....	.	.	.
.	.	....	.	.	.
.	.	....	.	.	.
1	1	....	0	0	8188
1	1	....	0	1	8189
1	1	....	1	0	8190
1	1	....	1	1	8191

*THE FRAC VALUE IS MADE UP OF THE 12-BIT MSB STORED IN REGISTER R0, AND THE 13-BIT LSB REGISTER STORED IN REGISTER R1. FRAC VALUE = 13-BIT LSB + 12-BIT MSB × 2^{13}.

NOTES
1. DBB = DOUBLE-BUFFERED BITS.

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Figure 24. LSB FRAC Register (R1) Map

R-DIVIDER REGISTER (R2) MAP

With Register R2 DB[2:0] set to [0, 1, 0], the on-chip R-divider register is programmed as shown in Figure 25.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

CSR Enable

Setting this bit to 1 enables cycle slip reduction. This is a method for improving lock times. Note that the signal at the PFD must have a 50% duty cycle in order for cycle slip reduction to work. In addition, the charge pump current setting must be set to a minimum. See the Cycle Slip Reduction for Faster Lock Times section for more information.

Also note that the cycle slip reduction feature can only be operated when the phase detector polarity setting is positive (DB6 in Register R3). It cannot be used if the phase detector polarity is set to negative.

Charge Pump Current Setting

DB[27:24] set the charge pump current setting (see Figure 25). Set these bits to the charge pump current that the loop filter is designed with.

Prescaler (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the INT, FRAC, and MOD counters, determines the overall division ratio from the RF_{IN} to the PFD input.

Operating at CML levels, it takes the clock from the RF input stage and divides it down for the counters. It is based on a synchronous 4/5 core. When set to 4/5, the maximum RF frequency allowed is 3 GHz. Therefore, when operating the ADF4158 above 3 GHz, the prescaler must be set to 8/9. The prescaler limits the INT value.

With $P = 4/5$, $N_{MIN} = 23$.

With $P = 8/9$, $N_{MIN} = 75$.

RDIV2

Setting DB21 to 1 inserts a divide-by-2 toggle flip-flop between the R-counter and the PFD. This can be used to provide a 50% duty cycle signal at the PFD for use with cycle slip reduction.

Reference Doubler

Setting DB20 to 0 feeds the REF_{IN} signal directly to the 5-bit RF R-counter, disabling the doubler. Setting this bit to 1 multiplies the REF_{IN} frequency by a factor of 2 before feeding the signal into the 5-bit R-counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising edge and falling edge of REF_{IN} become active edges at the PFD input.

The maximum allowed REF_{IN} frequency when the doubler is enabled is 30 MHz.

5-Bit R-Counter

The 5-bit R-counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 32 are allowed.

12-Bit CLK_1 Divider

Bits DB[14:3] are used to program the CLK_1 divider, which determines the duration of the time step in ramp mode.

RESERVED			CSR EN	CP CURRENT SETTING (DBB)				RESERVED	PRESCALER	RDIV2 DBB	REFERENCE DOUBLER DBB	5-BIT R COUNTER (DBB)					12-BIT CLK_1 DIVIDER												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	CR1	CPI4	CPI3	CPI2	CPI1	0	P1	U2	U1	R5	R4	R3	R2	R1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(0)	C2(1)	C1(0)

CR1	CYCLE SLIP REDUCTION
0	DISABLED
1	ENABLED

U1	REFERENCE DOUBLER
0	DISABLED
1	ENABLED

U2	R DIVIDER
0	DISABLED
1	ENABLED

P1	PRESCALER
0	4/5
1	8/9

D12	D11	....	D2	D1	12-BIT CLK_1 DIVIDER VALUE
0	0	....	0	0	0
0	0	....	0	1	1
0	0	....	1	0	2
0	0	....	1	1	3
.	.	....	.	.	.
.	.	....	.	.	.
.	.	....	.	.	.
1	1	....	0	0	4092
1	1	....	0	1	4093
1	1	....	1	0	4094
1	1	....	1	1	4095

CPI4	CPI3	CPI2	CPI1	I_{CP} (mA) 5.1kΩ
0	0	0	0	0.31
0	0	0	1	0.63
0	0	1	0	0.94
0	0	1	1	1.25
0	1	0	0	1.57
0	1	0	1	1.88
0	1	1	0	2.19
0	1	1	1	2.5
1	0	0	0	2.81
1	0	0	1	3.13
1	0	1	0	3.44
1	0	1	1	3.75
1	1	0	0	4.06
1	1	0	1	4.38
1	1	1	0	4.69
1	1	1	1	5

R5	R4	R3	R2	R1	R-COUNTER DIVIDE RATIO
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
.	.	.	.	.	
.	.	.	.	.	
.	.	.	.	.	
1	1	1	0	1	29
1	1	1	1	.	30
1	1	1	1	1	31
0	0	0	0	0	32

NOTES
1. DBB = DOUBLE-BUFFERED BITS.

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Figure 25. R-Divider Register (R2) Map

FUNCTION REGISTER (R3) MAP

With Register R3 DB[2:0] set to [0, 1, 1], the on-chip function register is programmed as shown in Figure 26.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

N SEL

This setting is used to circumvent the issue of pipeline delay between an update of the integer and fractional values in the N-counter. Typically, the INT value is loaded first, followed by the FRAC value. This can cause the N-counter value to be at an incorrect value for a brief period of time equal to the pipeline delay (about four PFD cycles). This has no effect if the INT value has not been updated. However, if the INT value has been changed, this can cause the PLL to overshoot in frequency while it tries to lock to the temporarily incorrect N value. After the correct fractional value is loaded, the PLL quickly locks to the correct frequency. Introducing an additional delay to the loading of the INT value using the N SEL bit causes the INT and FRAC values to be loaded at the same time, preventing frequency overshoot. The delay is turned on by setting Bit DB15 to 1.

SD Reset

For most applications, DB14 should be set to 0. When DB14 is set to 0, the Σ-Δ modulator is reset on each write to Register R0. If it is not required that the Σ-Δ modulator be reset on each Register R0 write, set this bit to 1.

Ramp Mode

DB[11:10] determine the type of generated waveform.

PSK Enable

When DB9 is set to 1, PSK modulation is enabled. When set to 0, PSK modulation is disabled.

FSK Enable

When DB8 is set to 1, FSK modulation is enabled. When set to 0, FSK modulation is disabled.

Lock Detect Precision (LDP)

When DB7 is programmed to 0, 24 consecutive PFD cycles of 15 ns must occur before digital lock detect is set. When this bit is programmed to 1, 40 consecutive reference cycles of 15 ns must occur before digital lock detect is set.

Phase Detector (PD) Polarity

DB6 sets the phase detector polarity. When the VCO characteristics are positive, set this bit to 1. When the VCO characteristics are negative, set this bit to 0.

Power-Down

DB5 provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation. While in software power-down mode, the part retains all information in its registers. Only when supplies are removed are the register contents lost.

When a power-down is activated, the following events occur:

1. All active dc current paths are removed.
2. The synthesizer counters are forced to their load state conditions.
3. The charge pump is forced into three-state mode.
4. The digital lock-detect circuitry is reset.
5. The RF_{IN} input is debiased.
6. The input register remains active and capable of loading and latching data.

Charge Pump Three-State

DB4 puts the charge pump into three-state mode when programmed to 1. It should be set to 0 for normal operation.

Counter Reset

DB3 is the RF counter reset bit. When this bit is set to 1, the RF synthesizer counters are held in reset. For normal operation, set this bit to 0.

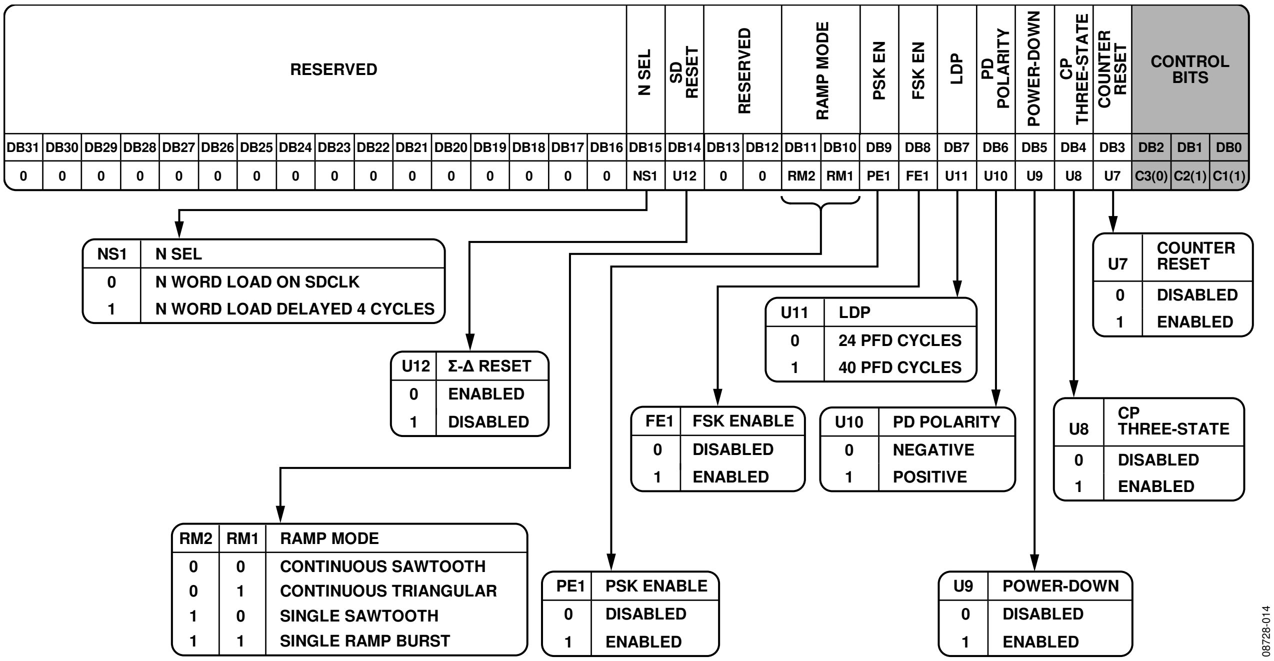

Figure 26. Function Register (R3) Map

TEST REGISTER (R4) MAP

With Register R4 DB[2:0] set to [1, 0, 0], the on-chip test register (R4) is programmed as shown in Figure 27.

LE SEL

In some applications, it is necessary to synchronize LE with the reference signal. To do this, DB31 should be set to 1. Synchronization is done internally on the part.

Σ-Δ Modulator Mode

To completely disable the Σ-Δ modulator, set Bits DB[30:26] to 0b01110, which puts the ADF4158 into integer-N mode, and the channel spacing becomes equal to the PFD frequency. Both the 12-bit MSB fractional value (Register R0, DB[14:3]) and the 13-bit LSB fractional value (Register R1, DB[27:15]) must be set to 0. After writing to Register 4, Register 3 must be written to twice to trigger a counter reset. (That is, write Register 3 with DB3 = 1, and then write Register 3 with DB3 = 0.)

All features driven by the Σ-Δ modulator are disabled, such as ramping, PSK, FSK, and phase adjust.

Disabling the Σ-Δ modulator also removes the fixed + ($f_{PFD}/2^{26}$) offset on the VCO output.

For normal operation, set these bits to 0b00000.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

Negative Bleed Current

Setting Bits DB[24:23] to 11 turns on the constant negative bleed current. This ensures that the charge pump operates out of the dead zone. Thus, the phase noise is not degraded and the level of spurs is lower. Enabling constant negative bleed current is particularly important on channels close to multiple PFD frequencies. Refer to the AN-1154 Application Note for more information on the negative bleed current. When using negative bleed current, readback to MUXOUT must be disabled.

Readback to MUXOUT

DB[22:21] enable or disable the readback to MUXOUT function. This function allows reading back the synthesizer's frequency at the moment of interrupt. When using readback to MUXOUT, negative bleed current must be off.

Clock Divider (DIV) Mode

Bits DB[20:19] are used to enable ramp divider mode or fast lock divider mode. If neither is being used, set these bits to 0b00.

12-Bit CLK_2 Divider Value

Bits DB[18:7] program the clock divider (the CLK_2 timer) when the part operates in ramp mode (see the Timeout Interval section). The CLK_2 timer also determines how long the loop remains in wideband mode when fast lock mode is used (see the Fast Lock Mode section).

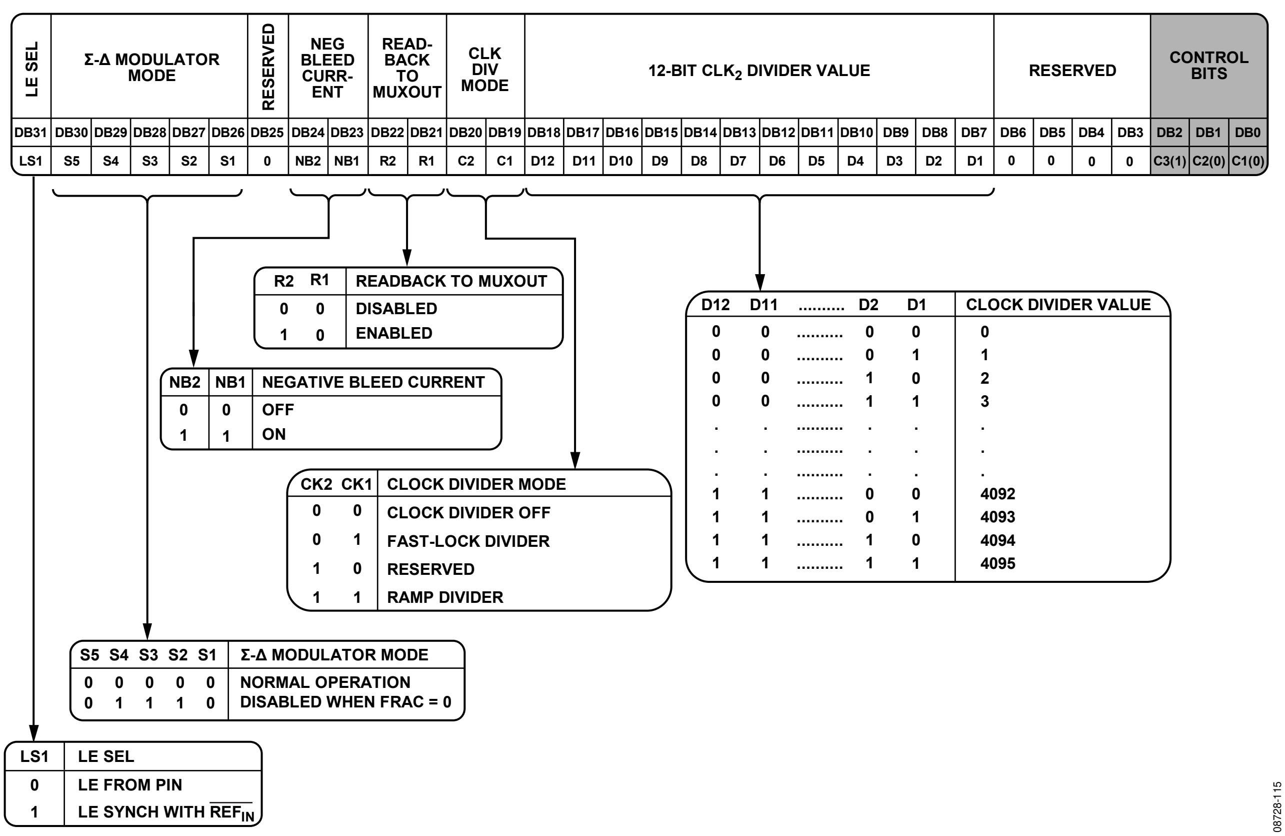

Figure 27. Test Register (R4) Map

DEVIATION REGISTER (R5) MAP

With Register R5 DB[2:0] set to [1, 0, 1], the on-chip deviation register is programmed as shown in Figure 28.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

Tx Ramp CLK

Setting DB29 to 0 uses the clock divider clock for clocking the ramp. Setting DB29 to 1 uses the Tx data clock for clocking the ramp.

PAR Ramp

Setting DB28 to 1 enables the parabolic ramp. Setting DB28 to 0 disables the parabolic ramp.

Interrupt

DB[27:26] determine which type of interrupt is used. This feature is used for reading back the INT and FARC value of a ramp at a given moment in time (rising edge on the TX_{DATA} pin triggers the interrupt). From these bits, frequency can be obtained. After readback, the sweep might continue or stop at the readback frequency.

FSK Ramp Enable

Setting DB25 to 1 enables the FSK ramp. Setting DB25 to 0 disables the FSK ramp.

Ramp 2 Enable

Setting DB24 to 1 enables the second ramp. Setting DB24 to 0 disables the second ramp.

Deviation Select

Setting DB23 to 0 chooses the first deviation word. Setting DB23 to 1 chooses the second deviation word.

4-Bit Deviation Offset Word

DB[22:19] determine the deviation offset. The deviation offset affects the deviation resolution.

16-Bit Deviation Word

DB[18:3] determine the signed deviation word. The deviation word defines the deviation step.

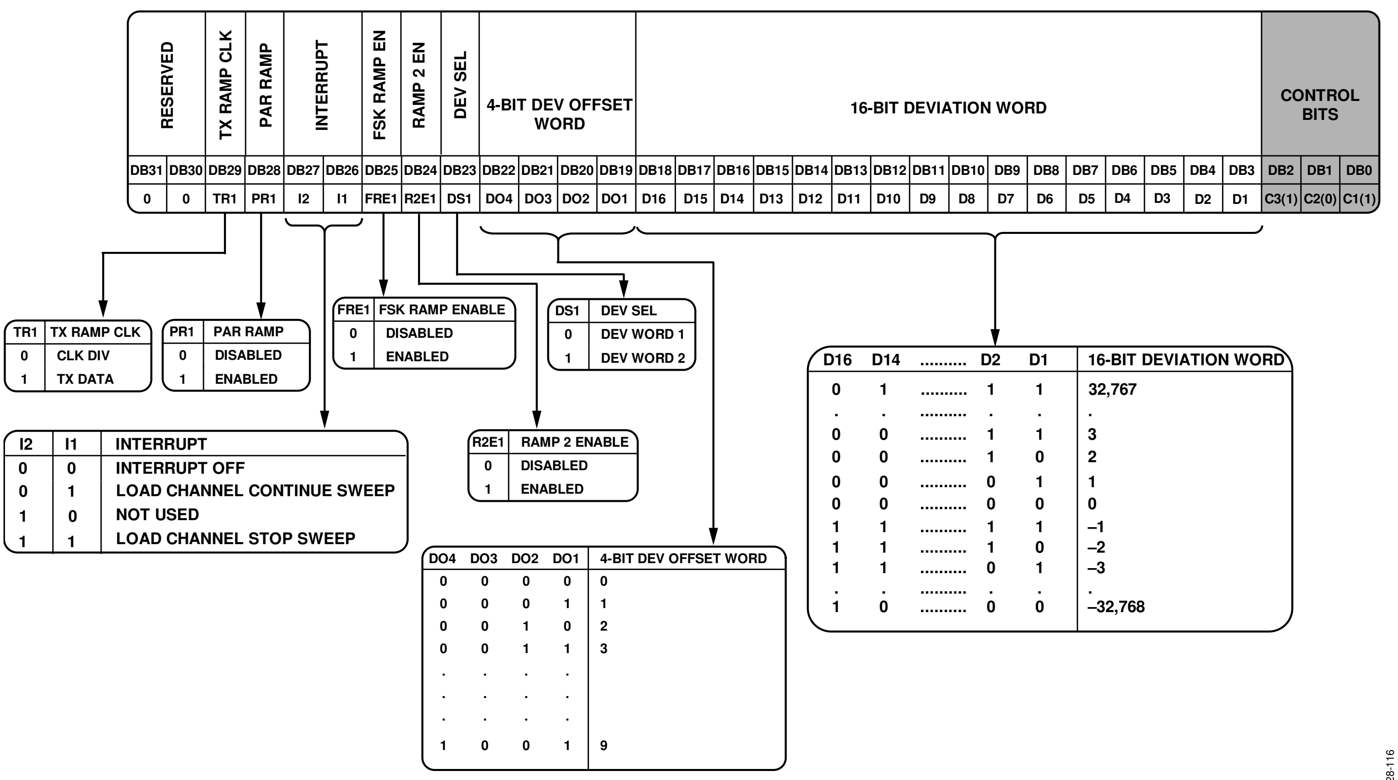

Figure 28. Deviation Register (R5) Map

STEP REGISTER (R6) MAP

With Register R6 DB[2:0] set to [1, 1, 0], the on-chip step register is programmed as shown in Figure 29.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

Step SEL

Setting DB23 to 0 chooses Step Word 1. Setting DB23 to 1 chooses Step Word 2.

20-Bit Step Word

DB[22:3] determine the step word. Step word is a number of steps in the ramp.

RESERVED								STEP SEL	20-BIT STEP WORD																				CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	SSE1	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	C3(1)	C2(1)	C1(0)

SSE1	STEP SEL
0	STEP WORD 1
1	STEP WORD 2

S20	S19	....	S2	S1	CLOCK DIVIDER VALUE
0	0	....	0	0	0
0	0	....	0	1	1
0	0	....	1	0	2
0	0	....	1	1	3
.	.	....	.	.	.
.	.	....	.	.	.
.	.	....	.	.	.
1	1	....	0	0	1048572
1	1	....	0	1	1048573
1	1	....	1	0	1048574
1	1	....	1	1	1048575

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Figure 29. Step Register (R6) Map

DELAY REGISTER (R7) MAP

With Register R7 DB[2:0] set to [1, 1, 1], the on-chip delay register is programmed as shown in Figure 30.

Reserved Bits

All reserved bits should be set to 0 for normal operation.

Ramp Delay Fast Lock

Setting DB18 to 1 enables the ramp delay fast-lock function. Setting DB18 to 0 disables this function.

Ramp Delay

Setting DB17 to 1 enables the ramp delay function. Setting DB17 to 0 disables this function.

Delay Clock Select

Setting DB16 to 0 selects the PFD clock as the delay clock. Setting DB16 to 1 selects PFD × CLK_1 (CLK_1 set by DB[14:3] in Register R2) as delay clock.

Delayed Start Enable

Setting DB15 to 1 enables delayed start. Setting DB15 to 0 disables delayed start.

12-Bit Delayed Start Word

DB[14:3] determine the delay start word. The delay start word affects the duration of the ramp start delay.

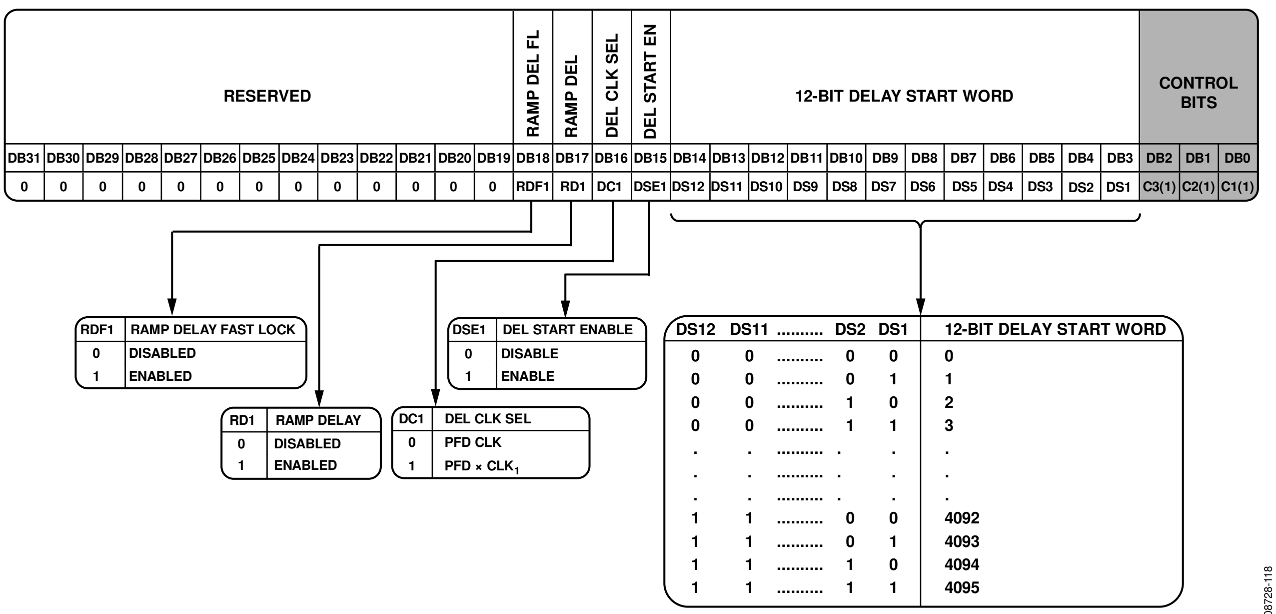

Figure 30. Delay Register (R7) Map