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Direct Modulation/Fast Waveform Generating, 13 GHz, Fractional-N Frequency Synthesizer

Data Sheet **ADF4159**

FEATURES

RF bandwidth to 13 GHz
High and low speed FMCW ramp generation
25-bit fixed modulus allows subhertz frequency resolution
PFD frequencies up to 110 MHz
Normalized phase noise floor of −224 dBc/Hz
FSK and PSK functions
Sawtooth, triangular, and parabolic waveform generation
Ramp superimposed with FSK
Ramp with 2 different sweep rates
Ramp delay, frequency readback, and interrupt functions
Programmable phase control
2.7 V to 3.45 V analog power supply
1.8 V digital power supply
Programmable charge pump currents
3-wire serial interface
Digital lock detect
ESD performance: 3000 V HBM, 1000 V CDM
Qualified for automotive applications

APPLICATIONS

FMCW radars
Communications test equipment
Communications infrastructure

GENERAL DESCRIPTION

The ADF4159 is a 13 GHz, fractional-N frequency synthesizer with modulation and both fast and slow waveform generation capability. The part uses a 25-bit fixed modulus, allowing subhertz frequency resolution.

The ADF4159 consists of a low noise digital phase frequency detector (PFD), a precision charge pump, and a programmable reference divider. The Σ-Δ-based fractional interpolator allows programmable fractional-N division. The INT and FRAC registers define an overall N divider as $N = INT + (FRAC/2^{25})$.

The ADF4159 can be used to implement frequency shift keying (FSK) and phase shift keying (PSK) modulation. Frequency sweep modes are also available to generate various waveforms in the frequency domain, for example, sawtooth and triangular waveforms. Sweeps can be set to run automatically or with each step manually triggered by an external pulse. The ADF4159 features cycle slip reduction circuitry, which enables faster lock times without the need for modifications to the loop filter.

Control of all on-chip registers is via a simple 3-wire interface. The ADF4159 operates with an analog power supply in the range of 2.7 V to 3.45 V and a digital power supply in the range of 1.62 V to 1.98 V. The device can be powered down when not in use.

FUNCTIONAL BLOCK DIAGRAM

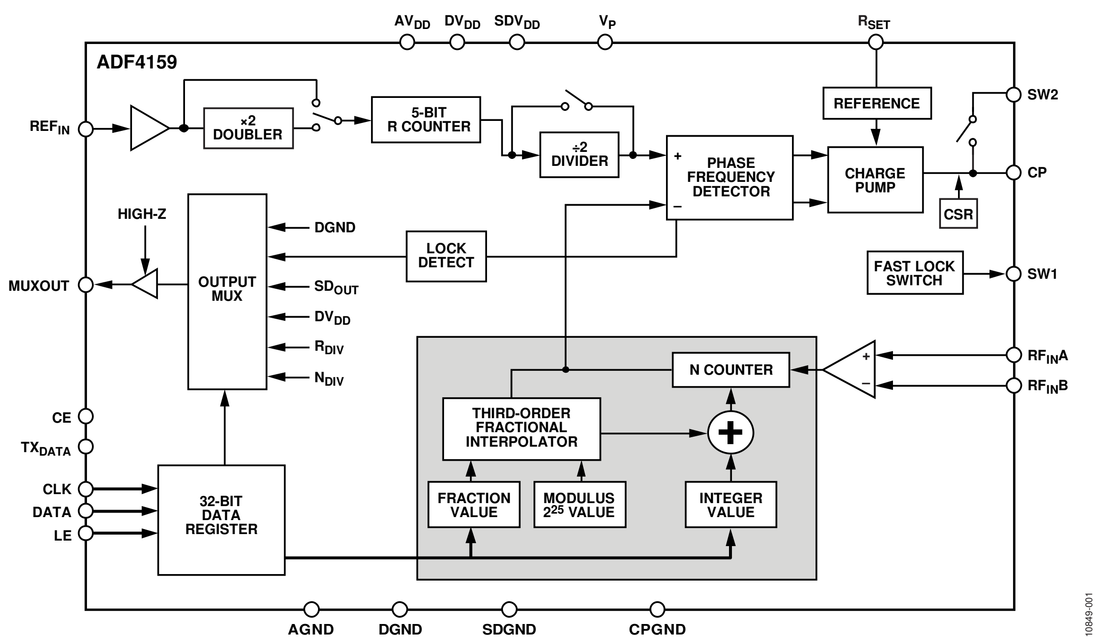

Figure 1.

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- ADF4159 Evaluation Board

DOCUMENTATION

Data Sheet

- ADF4159: Direct Modulation/Fast Waveform Generating, 13 GHz, Fractional-N Frequency Synthesizer Data Sheet

User Guides

- UG-383: Evaluating the ADF4159 Frequency Synthesizer for Phase-Locked Loops
- UG-476: PLL Software Installation Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADF4158 and ADF4159 Evaluation Board Software

TOOLS AND SIMULATIONS

- ADIsimPLL™

REFERENCE DESIGNS

- CN0302

REFERENCE MATERIALS

Press

- Analog Devices Advances RF and Microwave Designs from Bits to Antenna and Back at IMS2012
- Analog Devices Debuts Industry's Highest Performing 13 GHz PLL Synthesizer

Product Selection Guide

- RF Source Booklet

Technical Articles

- High Performance Integrated 24 GHz FMCW Radar Transceiver Chipset for Auto and Industrial Sensor Applications

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- ADF4159 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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REVISION HISTORY

SPECIFICATIONS

$AV_{DD} = V_P = 2.7$ V to 3.45 V, $DV_{DD} = SDV_{DD} = 1.8$ V, AGND = DGND = SDGND = CPGND = 0 V, $f_{PFD} = 110$ MHz, $T_A = T_{MIN}$ to T_{MAX}, dBm referred to 50 Ω, unless otherwise noted.

Table 1.

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
RF CHARACTERISTICS					
RF Input Frequency (RF_{IN})	0.5		13	GHz	−10 dBm min to 0 dBm max; for lower frequencies, ensure a slew rate ≥ 400 V/µs
Prescaler Output Frequency			2	GHz	For higher frequencies, use 8/9 prescaler
REFERENCE CHARACTERISTICS					
REF_{IN} Input Frequency	10		260	MHz	−5 dBm min to +9 dBm max biased at 1.8/2 (ac coupling ensures 1.8/2 bias); for frequencies < 10 MHz, use a dc-coupled, CMOS-compatible square wave with a slew rate > 25 V/µs
Reference Doubler Enabled	10		50	MHz	Bit DB20 in Register R2 set to 1
REF_{IN} Input Capacitance			1.2	pF	
REF_{IN} Input Current			±100	µA	
PHASE FREQUENCY DETECTOR (PFD)					
Phase Detector Frequency[2]			110	MHz	
CHARGE PUMP					
I_{CP} Sink/Source Current					Programmable
High Value		4.8		mA	$R_{SET} = 5.1$ kΩ
Low Value		300		µA	
Absolute Accuracy		2.5		%	$R_{SET} = 5.1$ kΩ
R_{SET} Range	4.59	5.1	5.61	kΩ	
I_{CP} Three-State Leakage Current		1		nA	Sink and source current
Sink and Source Matching		2		%	$0.5 \text{ V} < V_{CP} < V_P - 0.5 \text{ V}$
I_{CP} vs. V_{CP}		2		%	$0.5 \text{ V} < V_{CP} < V_P - 0.5 \text{ V}$
I_{CP} vs. Temperature		2		%	$V_{CP} = V_P/2$
LOGIC INPUTS					
Input High Voltage, V_{INH}	1.17			V	
Input Low Voltage, V_{INL}			0.4	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	$DV_{DD} - 0.4$			V	CMOS output selected
Output Low Voltage, V_{OL}			0.3	V	$I_{OL} = 500$ µA
Output High Current, I_{OH}			100	µA	
POWER SUPPLIES					
AV_{DD}	2.7		3.45	V	
DV_{DD}, SDV_{DD}	1.62	1.8	1.98	V	
V_P	2.7		3.45	V	
AI_{DD}		26	40	mA	Supply current drawn by AV_{DD}; $f_{PFD} = 110$ MHz
DI_{DD}		7.5	10	mA	Supply current drawn by DV_{DD}; $f_{PFD} = 110$ MHz
I_P		5.5	7	mA	Supply current drawn by V_P; $f_{PFD} = 110$ MHz
Power-Down Mode		2		µA	

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS					
Normalized Phase Noise Floor[3]					PLL loop BW = 1 MHz
Integer-N Mode		−224		dBc/Hz	FRAC = 0; see Σ-Δ Modulator Mode section
Fractional-N Mode		−217		dBc/Hz	
Normalized 1/f Noise (PN_{1_f})[4]		−120		dBc/Hz	Measured at 10 kHz offset, normalized to 1 GHz
Phase Noise Performance[5]					At VCO output
12,002 MHz Output[6]		−96		dBc/Hz	At 50 kHz offset, 100 MHz PFD frequency

[1] Operating temperature: −40°C to +125°C.
[2] Guaranteed by design. Sample tested to ensure compliance.
[3] This specification can be used to calculate phase noise for any application. Use the formula ((Normalized Phase Noise Floor) + 10 log(f_{PFD}) + 20 logN) to calculate in-band phase noise performance as seen at the VCO output.
[4] The PLL phase noise is composed of flicker (1/f) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency (f_{RF}) and at an offset frequency (f) is given by $PN = PN_{1\_f} + 10 \log(10 \text{ kHz}/f) + 20 \log(f_{RF}/1 \text{ GHz})$. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.
[5] The phase noise is measured with the EV-ADF4159EB3Z and the Rohde & Schwarz FSUP signal source analyzer.
[6] f_{REFIN} = 100 MHz; f_{PFD} = 100 MHz; offset frequency = 50 kHz; RF_{OUT} = 12,002 MHz; N = 120.02; loop bandwidth = 250 kHz.

TIMING SPECIFICATIONS

$AV_{DD} = V_P$ = 2.7 V to 3.45 V, $DV_{DD} = SDV_{DD}$ = 1.8 V, AGND = DGND = SDGND = CPGND = 0 V, $T_A = T_{MIN}$ to T_{MAX}, dBm referred to 50 Ω, unless otherwise noted.

Table 2. Write Timing

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Description
t_1	20	ns min	LE setup time
t_2	10	ns min	DATA to CLK setup time
t_3	10	ns min	DATA to CLK hold time
t_4	25	ns min	CLK high duration
t_5	25	ns min	CLK low duration
t_6	10	ns min	CLK to LE setup time
t_7	20	ns min	LE pulse width

Write Timing Diagram

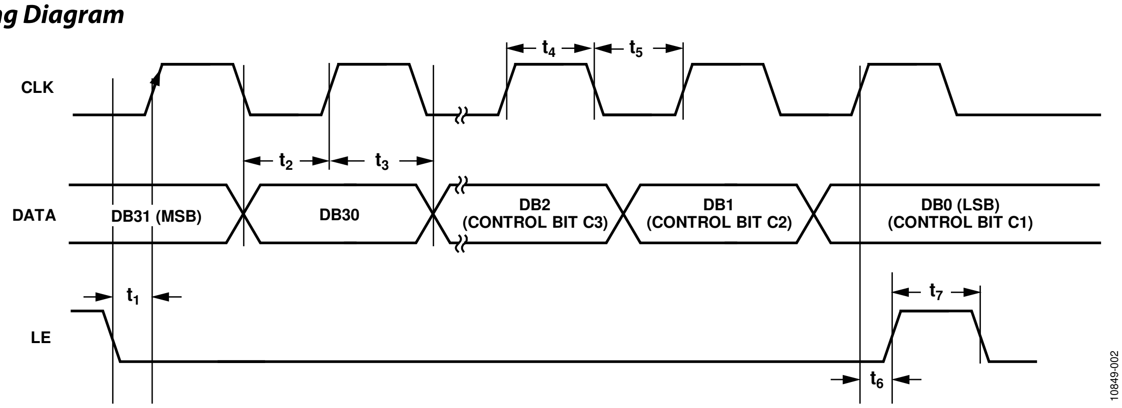


Figure 2. Write Timing Diagram

Table 3. Read Timing

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Description
t_1[1]	t_{PFD} + 20	ns min	TX_{DATA} setup time
t_2	20	ns min	CLK setup time to data (on MUXOUT)
t_3	25	ns min	CLK high duration
t_4	25	ns min	CLK low duration
t_5	10	ns min	CLK to LE setup time

[1] t_{PFD} is the period of the PFD frequency; for example, if the PFD frequency is 50 MHz, t_{PFD} = 20 ns.

Read Timing Diagram

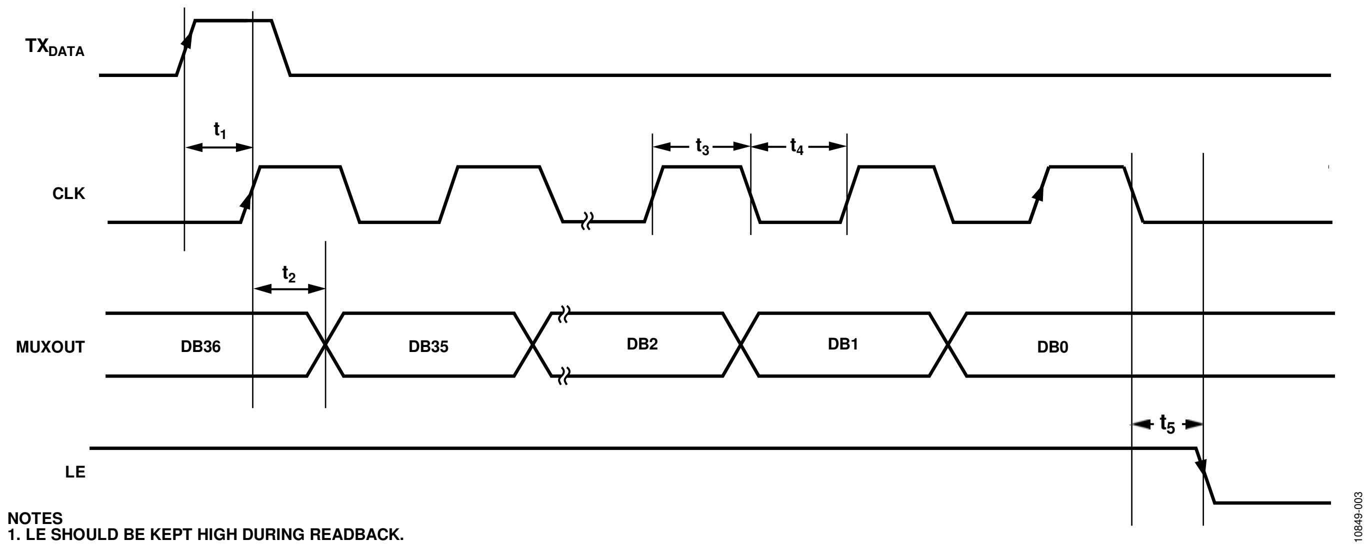


Figure 3. Read Timing Diagram

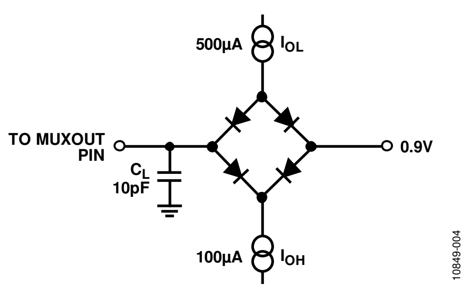


Figure 4. Load Circuit for MUXOUT Timing, C_L = 10 pF

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, GND = AGND = DGND = SDGND = CPGND = 0 V, unless otherwise noted.

Table 4.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +3.9 V
DV_{DD} to GND	−0.3 V to +2.4 V
V_P to GND	−0.3 V to +3.9 V
V_P to AV_{DD}	−0.3 V to +0.3 V
Digital I/O Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
REF_{IN} to GND	−0.3 V to DV_{DD} + 0.3 V
RF_{IN} to GND	−0.3 V to AV_{DD} + 0.3 V
Operating Temperature Range, Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD	
Charged Device Model	1000 V
Human Body Model	3000 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

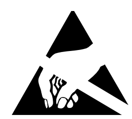
THERMAL RESISTANCE

Thermal impedance (θ_{JA}) is specified for a device with the exposed pad soldered to AGND.

Table 5. Thermal Resistance

Package Type	θ_{JA}	Unit
24-Lead LFCSP_WQ	56	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

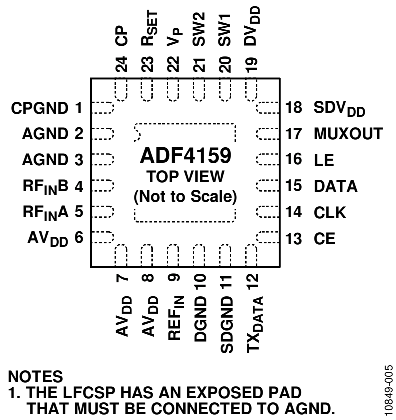


Figure 5. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CPGND	Charge Pump Ground. This pin is the ground return path for the charge pump.
2, 3	AGND	Analog Ground.
4	$RF_{IN}B$	Complementary Input to the RF Prescaler. Decouple this pin to the ground plane with a small bypass capacitor, typically 100 pF.
5	$RF_{IN}A$	Input to the RF Prescaler. This small signal input is normally ac-coupled from the VCO.
6, 7, 8	AV_{DD}	Positive Power Supply for the RF Section. Place decoupling capacitors to the ground plane as close as possible to these pins.
9	REF_{IN}	Reference Input. This CMOS input has a nominal threshold of $DV_{DD}/2$ and an equivalent input resistance of 100 kΩ. It can be driven from a TTL or CMOS crystal oscillator, or it can be ac-coupled.
10	DGND	Digital Ground.
11	SDGND	Digital Σ-Δ Modulator Ground. This pin is the ground return path for the Σ-Δ modulator.
12	TX_{DATA}	Transmit Data Pin. This pin provides the data to be transmitted in FSK or PSK mode and also controls some ramping functionality.
13	CE	Chip Enable (1.8 V Logic). A logic low on this pin powers down the device and places the charge pump output into three-state mode.
14	CLK	Serial Clock Input. This input is used to clock in the serial data to the registers. The data is latched into the input shift register on the CLK rising edge. This input is a high impedance CMOS input.
15	DATA	Serial Data Input. The serial data is loaded MSB first; the three LSBs are the control bits. This input is a high impedance CMOS input.
16	LE	Load Enable Input. When LE is high, the data stored in the input shift register is loaded into one of the eight latches; the latch is selected using the control bits. This input is a high impedance CMOS input.
17	MUXOUT	Multiplexer Output. This pin allows various internal signals to be accessed externally.
18	SDV_{DD}	Power Supply for the Digital Σ-Δ Modulator. Place decoupling capacitors to the ground plane as close as possible to this pin.
19	DV_{DD}	Positive Power Supply for the Digital Section. Place decoupling capacitors to the digital ground plane as close as possible to this pin.
20, 21	SW1, SW2	Switches for Fast Lock.
22	V_P	Charge Pump Power Supply. The voltage on this pin must be greater than or equal to AV_{DD}.
23	R_{SET}	Connecting a resistor between this pin and ground sets the maximum charge pump output current. The relationship between I_{CP} and R_{SET} is as follows: $I_{CP\_MAX} = 24.48/R_{SET}$ where: $I_{CP\_MAX} = 4.8$ mA. $R_{SET} = 5.1$ kΩ.
24	CP	Charge Pump Output. When the charge pump is enabled, this output provides $\pm I_{CP}$ to the external loop filter, which, in turn, drives the external VCO.
25	EPAD	Exposed Pad. The LFCSP has an exposed pad that must be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

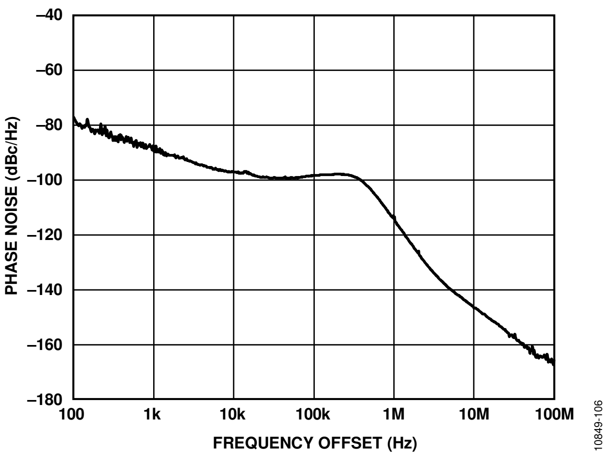


Figure 6. Phase Noise at 12.002 GHz, f_{PFD} = 100 MHz, I_{CP} = 2.5 mA, Loop Bandwidth = 250 kHz, Bleed Current = 11.03 µA

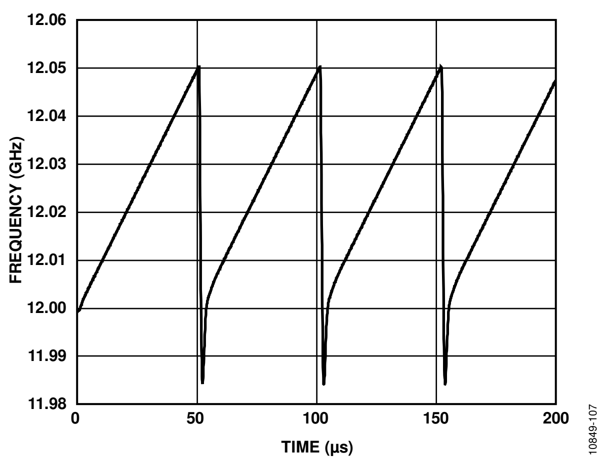


Figure 7. Sawtooth Ramp, f_{PFD} = 100 MHz, I_{CP} = 2.5 mA, Loop Bandwidth = 250 kHz, CLK_1 = 3, CLK_2 = 26, DEV = 1024, DEV_OFFSET = 8, Number of Steps = 64

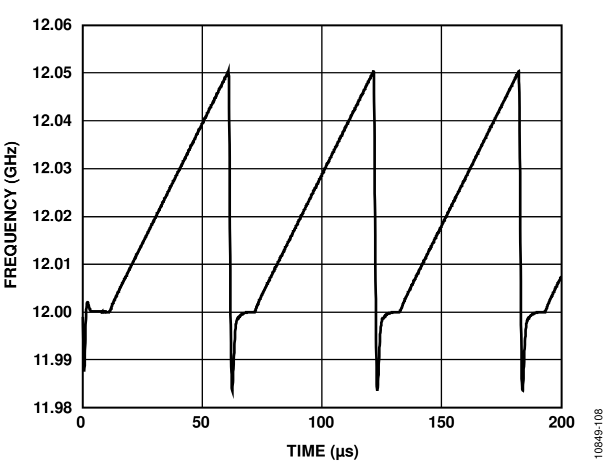


Figure 8. Sawtooth Ramp with Delay, f_{PFD} = 100 MHz, I_{CP} = 2.5 mA, Loop Bandwidth = 250 kHz, CLK_1 = 3, CLK_2 = 26, DEV = 1024, DEV_OFFSET = 8, Number of Steps = 64, Delay Word = 1000

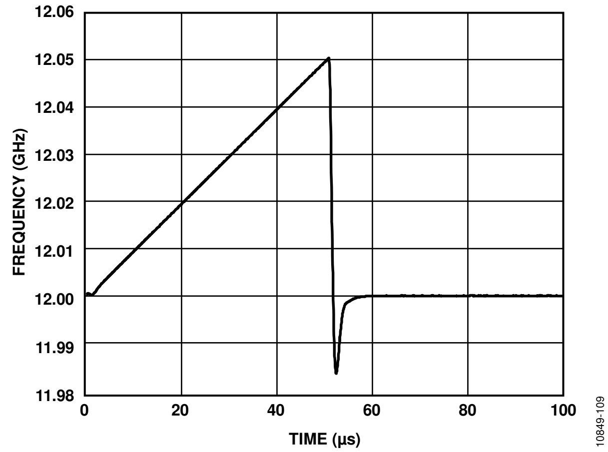


Figure 9. Sawtooth Burst, f_{PFD} = 100 MHz, I_{CP} = 2.5 mA, Loop Bandwidth = 250 kHz, CLK_1 = 3, CLK_2 = 26, DEV = 1024, DEV_OFFSET = 8, Number of Steps = 64

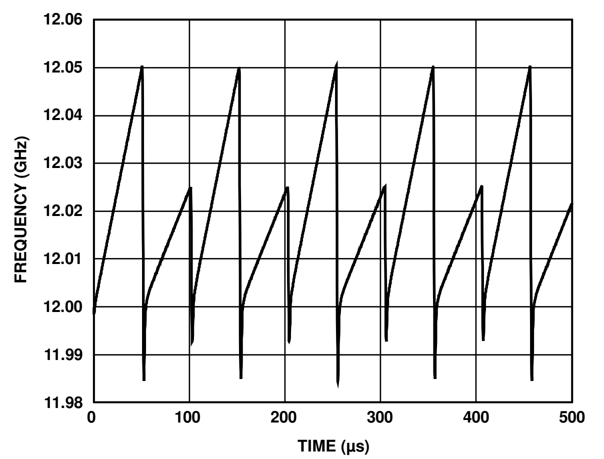


Figure 10. Dual Sawtooth Ramp, f_{PFD} = 100 MHz, I_{CP} = 2.5 mA, Loop Bandwidth = 250 kHz, CLK_1 = 3; First Ramp: CLK_2 = 26, DEV = 1024, DEV_OFFSET = 8, Number of Steps = 64; Second Ramp: CLK_2 = 52, DEV = 1024, DEV_OFFSET = 7, Number of Steps = 64

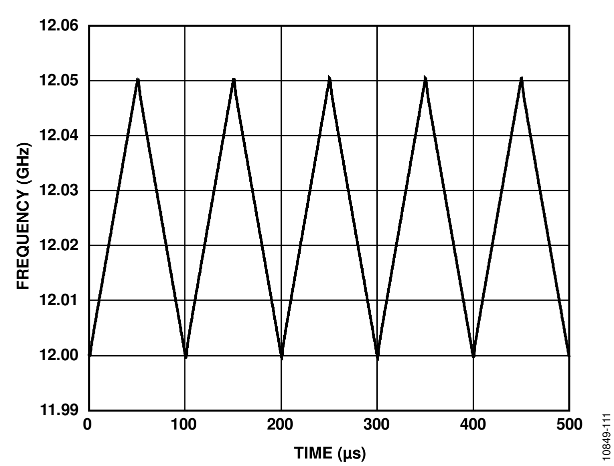


Figure 11. Triangle Ramp, f_{PFD} = 100 MHz, I_{CP} = 2.5 mA, Loop Bandwidth = 250 kHz, CLK_1 = 3, CLK_2 = 26, DEV = 1024, DEV_OFFSET = 8, Number of Steps = 64

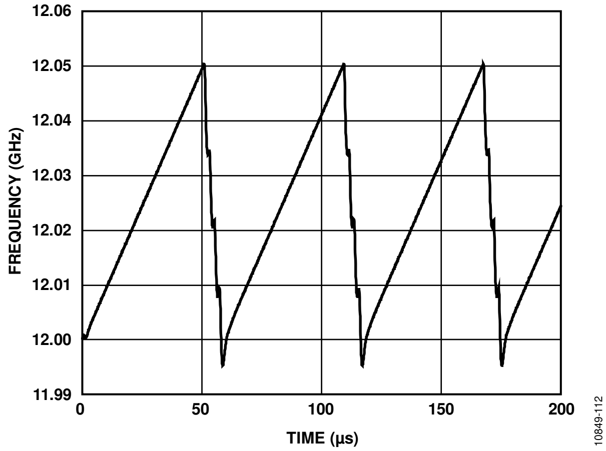


Figure 12. Fast Ramp (Triangle Ramp with Different Slopes), f_{PFD} = 100 MHz, I_{CP} = 2.5 mA, Loop Bandwidth = 250 kHz, CLK_1 = 3; Up Ramp: CLK_2 = 26, DEV = 1024, DEV_OFFSET = 8, Number of Steps = 64; Down Ramp: CLK_2 = 70, DEV = 16,384, DEV_OFFSET = 8, Number of Steps = 4

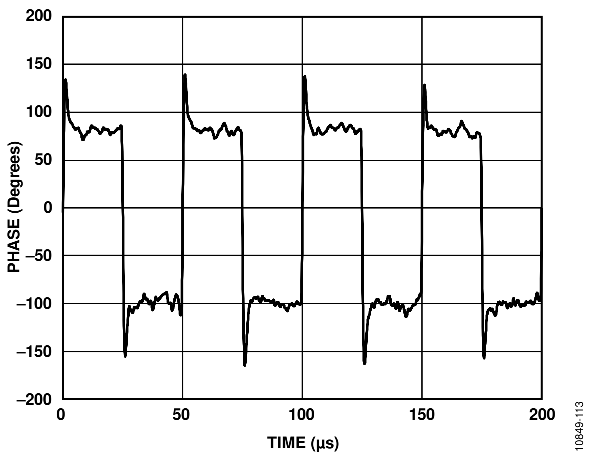


Figure 13. Phase Shift Keying (PSK), Loop Bandwidth = 250 kHz, Phase Value = 1024, Data Rate = 20 kHz

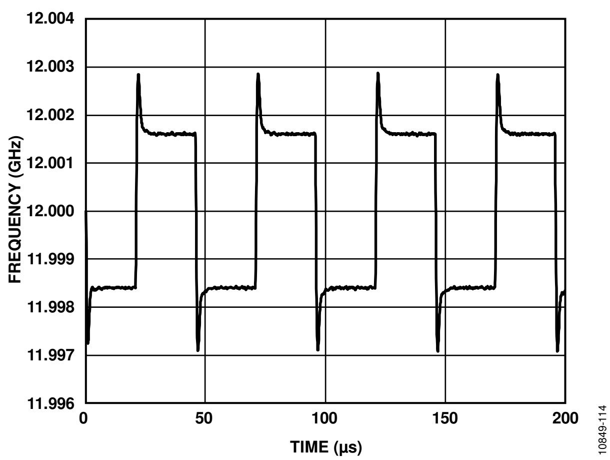


Figure 14. Frequency Shift Keying (FSK), Loop Bandwidth = 250 kHz, DEV = 1049, DEV_OFFSET = 9, Data Rate = 20 kHz

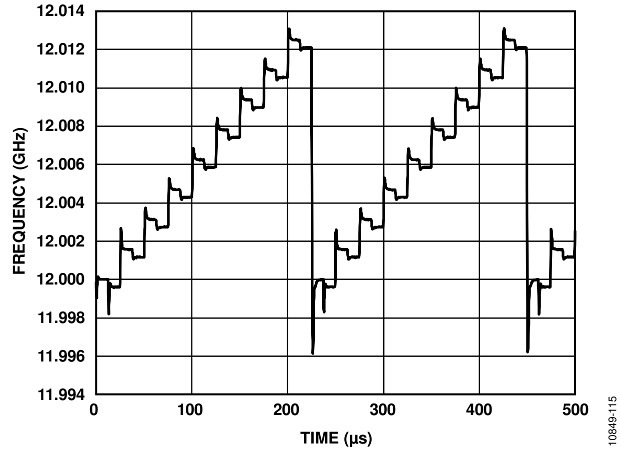


Figure 15. FSK Ramp, f_{PFD} = 100 MHz, I_{CP} = 2.5 mA, Loop Bandwidth = 250 kHz, CLK_1 = 3, CLK_2 = 26, DEV = 1024, DEV_OFFSET = 8, Number of Steps = 64; FSK: DEV = −512, DEV_OFFSET = 8

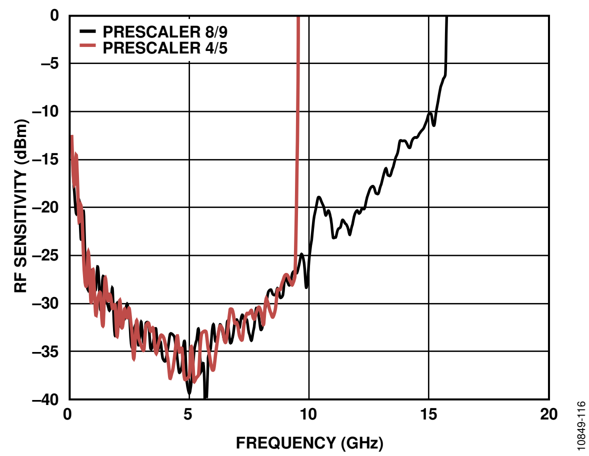


Figure 16. RF_{IN} Sensitivity at Nominal Temperature

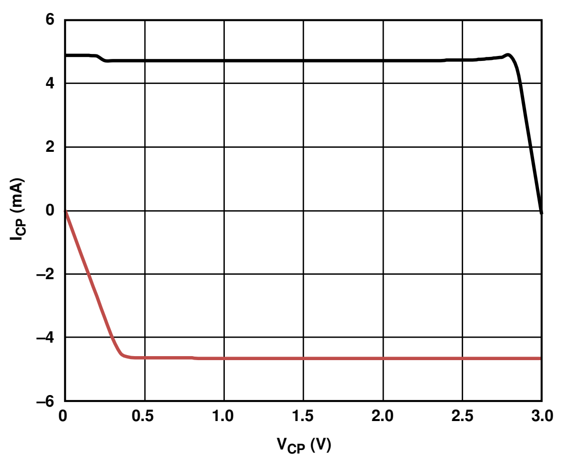


Figure 17. Charge Pump Output Characteristics

THEORY OF OPERATION

REFERENCE INPUT SECTION

Figure 18 shows the reference input stage. The SW1 and SW2 switches are normally closed (NC in Figure 18). The SW3 switch is normally open (NO in Figure 18). When power-down is initiated, SW3 is closed, and SW1 and SW2 are opened. In this way, no loading of the REF_{IN} pin occurs during power-down.

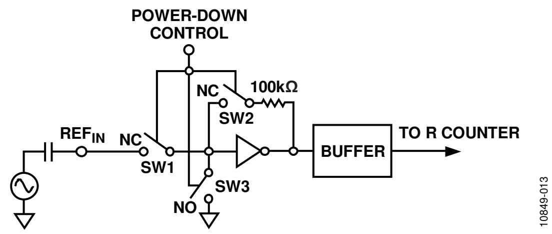


Figure 18. Reference Input Stage

RF INPUT STAGE

Figure 19 shows the RF input stage. The input stage is followed by a two-stage limiting amplifier to generate the current-mode logic (CML) clock levels required for the prescaler.

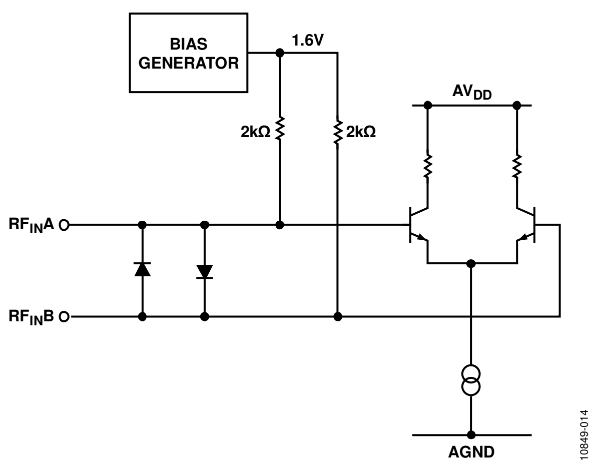


Figure 19. RF Input Stage

RF INT DIVIDER

The RF INT CMOS divider allows a division ratio in the PLL feedback counter. Division ratios from 23 to 4095 are allowed.

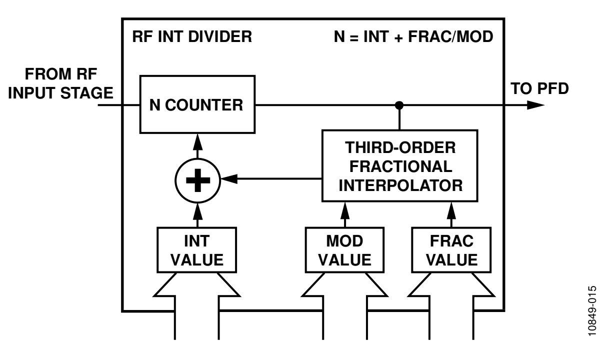


Figure 20. RF INT Divider

25-BIT FIXED MODULUS

The ADF4159 has a 25-bit fixed modulus. This modulus allows output frequencies to be spaced with a resolution of

$$f_{RES} = f_{PFD}/2^{25} \quad (1)$$

where f_{PFD} is the frequency of the phase frequency detector (PFD). For example, with a PFD frequency of 100 MHz, frequency steps of 2.98 Hz are possible. Due to the architecture of the Σ-Δ modulator, there is a fixed $+(f_{PFD}/2^{26})$ offset on the VCO output. To remove this offset, see the Σ-Δ Modulator Mode section.

INT, FRAC, AND R COUNTER RELATIONSHIP

The INT and FRAC values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the PFD frequency.

The RF VCO frequency (RF_{OUT}) equation is

$$RF_{OUT} = (INT + (FRAC/2^{25})) \times f_{PFD} \quad (2)$$

where:
RF_{OUT} is the output frequency of the external voltage controlled oscillator (VCO).
INT is the preset divide ratio of the binary 12-bit counter (23 to 4095).
$FRAC$ is the numerator of the fractional division (0 to $(2^{25} - 1)$).

The PFD frequency (f_{PFD}) equation is

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (3)$$

where:
REF_{IN} is the reference input frequency.
D is the REF_{IN} doubler bit (0 or 1).
R is the preset divide ratio of the binary 5-bit programmable reference (R) counter (1 to 32).
T is the REF_{IN} divide-by-2 bit (0 or 1).

R COUNTER

The 5-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to supply the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 21 shows a simplified schematic of the PFD.

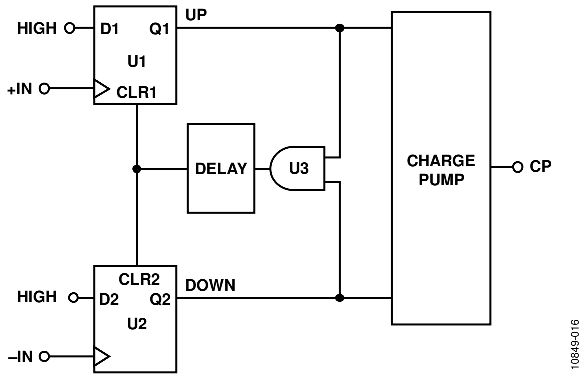


Figure 21. PFD Simplified Schematic

The PFD includes a fixed delay element that sets the width of the antibacklash pulse, which is typically 1 ns. This pulse ensures that there is no dead zone in the PFD transfer function and gives a consistent reference spur level.

MUXOUT AND LOCK DETECT

The multiplexer output on the ADF4159 allows the user to access various internal points on the chip. The state of MUXOUT is controlled by the M4, M3, M2, and M1 bits in Register R0 (see Figure 25). Figure 22 shows the MUXOUT section in block diagram form.

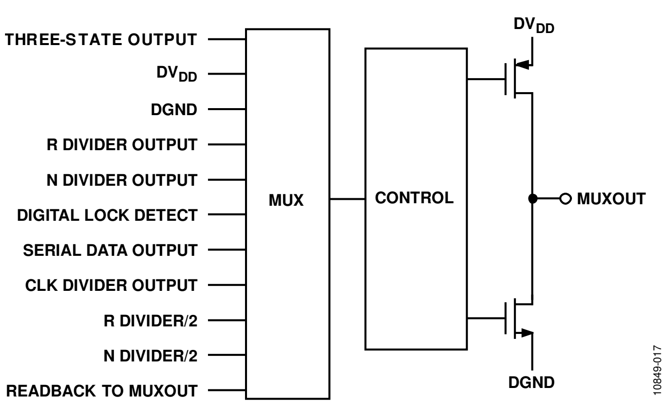


Figure 22. MUXOUT Schematic

INPUT SHIFT REGISTER

The ADF4159 digital section includes a 5-bit R counter, a 12-bit INT counter, and a 25-bit FRAC counter. Data is clocked into the 32-bit input shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the input shift register to one of eight latches on the rising edge of LE.

The destination latch is determined by the state of the three control bits (C3, C2, and C1) in the input shift register. As shown in Figure 2, the control bits are the three LSBs (DB2, DB1, and DB0, respectively). Table 7 shows the truth table for these bits. Figure 23 and Figure 24 provide a summary of how the latches are programmed.

Table 7. Truth Table for the C3, C2, and C1 Control Bits

Control Bits			
C3	**C2**	**C1**	**Register**
0	0	0	R0
0	0	1	R1
0	1	0	R2
0	1	1	R3
1	0	0	R4
1	0	1	R5
1	1	0	R6
1	1	1	R7

PROGRAM MODES

Table 7 and Figure 25 through Figure 32 show how the program modes are set up in the ADF4159.

The following settings in the ADF4159 are double buffered: LSB fractional value, phase value, charge pump current setting, reference divide-by-2, reference doubler, R counter value, and CLK_1 divider value. Before the part uses a new value for any double-buffered setting, the following two events must occur:

1. The new value is latched into the device by writing to the appropriate register.
2. A new write is performed to Register 0 (R0).

For example, updating the fractional value involves a write to the 13 LSB bits in R1 and the 12 MSB bits in R0. R1 must be written to first, followed by the write to R0. The frequency change begins after the write to R0. Double-buffering ensures that the bits written to R1 do not take effect until after the write to R0.

REGISTER MAPS

FRAC/INT REGISTER (R0)

RAMP ON	MUXOUT CONTROL				12-BIT INTEGER VALUE (INT)												12-BIT MSB FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R1	M4	M3	M2	M1	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	C3(0)	C2(0)	C1(0)

LSB FRAC REGISTER (R1)

RESERVED			PHASE ADJUST	DBB 13-BIT LSB FRACTIONAL VALUE (FRAC)													DBB 12-BIT PHASE VALUE												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	P1	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C3(0)	C2(0)	C1(1)

R DIVIDER REGISTER (R2)

RESERVED			CSR	DBB CP CURRENT SETTING				RESERVED	PRESCALER	RDIV2 DBB	REFERENCE DOUBLER DBB	DBB 5-BIT R COUNTER					DBB 12-BIT CLK_1 DIVIDER VALUE												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	CR1	CPI4	CPI3	CPI2	CPI1	0	P1	U2	U1	R5	R4	R3	R2	R1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(0)	C2(1)	C1(0)

FUNCTION REGISTER (R3)

RESERVED							NEG BLEED CURRENT			NEG BLEED ENABLE	RESERVED			RESERVED	LOL	N SEL	SD RESET	RESERVED		RAMP MODE		PSK	FSK	LDP	PD POLARITY	POWER-DOWN	CP THREE-STATE	COUNTER RESET	CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	NB3	NB2	NB1	0	0	0	0	1	L1	NS1	U12	0	0	RM2	RM1	0	0	U11	U10	U9	U8	U7	C3(0)	C2(1)	C1(1)

NOTES
1. DBB = DOUBLE-BUFFERED BITS.

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Figure 23. Register Summary 1

CLOCK REGISTER (R4)

LE SEL	Σ-Δ MODULATOR MODE					RAMP STATUS					CLK DIV MODE		12-BIT CLK_2 DIVIDER VALUE												CLK DIV SEL	RESERVED			CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
LS1	S5	S4	S3	S2	S1	R5	R4	R3	R2	R1	C2	C1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	CS1	0	0	0	C3(1)	C2(0)	C1(0)

DEVIATION REGISTER (R5)

RESERVED	TX_{DATA} INVERT	TX RAMP CLK	PARABOLIC RAMP	INTERRUPT		FSK RAMP	DUAL RAMP	DEV SEL	4-BIT DEVIATION OFFSET WORD				16-BIT DEVIATION WORD																CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	TR1	0	I2	I1	0	0	DS1	DO4	DO3	DO2	DO1	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(1)	C2(0)	C1(1)

STEP REGISTER (R6)

RESERVED								STEP SEL	20-BIT STEP WORD																				CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	SSE1	S20	S19	S18	S17	S16	S15	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	C3(1)	C2(1)	C1(0)

DELAY REGISTER (R7)

RESERVED								TX_{DATA} TRIGGER DELAY	TRI DELAY	SING FULL TRI	TX_{DATA} TRIGGER	FAST RAMP	RAMP DELAY FL	RAMP DELAY	DEL CLK SEL	DEL START EN	12-BIT DELAY START WORD												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	TD1	ST1	TR1	FR1	0	RD1	DC1	DSE1	DS12	DS11	DS10	DS9	DS8	DS7	DS6	DS5	DS4	DS3	DS2	DS1	C3(1)	C2(1)	C1(1)

NOTES
1. DBB = DOUBLE-BUFFERED BITS.

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Figure 24. Register Summary 2

FRAC/INT REGISTER (R0) MAP

When Bits DB[2:0] are set to 000, the on-chip FRAC/INT register (Register R0) is programmed (see Figure 25).

Ramp On

When Bit DB31 is set to 1, the ramp function is enabled. When Bit DB31 is set to 0, the ramp function is disabled.

MUXOUT Control

The on-chip multiplexer of the ADF4159 is controlled by Bits DB[30:27]. See Figure 25 for the truth table.

12-Bit Integer Value (INT)

Bits DB[26:15] set the INT value, which forms part of the overall feedback division factor. For more information, see the INT, FRAC, and R Counter Relationship section.

12-Bit MSB Fractional Value (FRAC)

Bits DB[14:3], along with Bits DB[27:15] in the LSB FRAC register (Register R1), set the FRAC value that is loaded into the fractional interpolator. The FRAC value forms part of the overall feedback division factor. These 12 bits are the most significant bits (MSBs) of the 25-bit FRAC value; Bits DB[27:15] in the LSB FRAC register (Register R1) are the least significant bits (LSBs). For more information, see the RF Synthesizer Worked Example section.

RAMP ON	MUXOUT CONTROL				12-BIT INTEGER VALUE (INT)												12-BIT MSB FRACTIONAL VALUE (FRAC)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R1	M4	M3	M2	M1	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	F25	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	C3(0)	C2(0)	C1(0)

R1	RAMP ON
0	RAMP DISABLED
1	RAMP ENABLED

M4	M3	M2	M1	OUTPUT
0	0	0	0	THREE-STATE OUTPUT
0	0	0	1	DV_{DD}
0	0	1	0	DGND
0	0	1	1	R DIVIDER OUTPUT
0	1	0	0	N DIVIDER OUTPUT
0	1	0	1	RESERVED
0	1	1	0	DIGITAL LOCK DETECT
0	1	1	1	SERIAL DATA OUTPUT
1	0	0	0	RESERVED
1	0	0	1	RESERVED
1	0	1	0	CLK DIVIDER OUTPUT
1	0	1	1	RESERVED
1	1	0	0	RESERVED
1	1	0	1	R DIVIDER/2
1	1	1	0	N DIVIDER/2
1	1	1	1	READBACK TO MUXOUT

F25	F24	...	F15	F14	MSB FRACTIONAL VALUE (FRAC)*
0	0	...	0	0	0
0	0	...	0	1	1
0	0	...	1	0	2
0	0	...	1	1	3
.	.	...	.	.	.
.	.	...	.	.	.
.	.	...	.	.	.
1	1	...	0	0	4092
1	1	...	0	1	4093
1	1	...	1	0	4094
1	1	...	1	1	4095

*THE FRAC VALUE IS MADE UP OF THE 12-BIT MSB STORED IN REGISTER R0 AND THE 13-BIT LSB STORED IN REGISTER R1. FRAC VALUE = 13-BIT LSB + 12-BIT MSB × 2^{13}.

N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	INTEGER VALUE (INT)
0	0	0	0	0	0	0	1	0	1	1	1	23
0	0	0	0	0	0	0	1	1	0	0	0	24
0	0	0	0	0	0	0	1	1	0	0	1	25
0	0	0	0	0	0	0	1	1	0	1	0	26
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	1	1	0	1	4093
1	1	1	1	1	1	1	1	1	1	1	0	4094
1	1	1	1	1	1	1	1	1	1	1	1	4095

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Figure 25. FRAC/INT Register (R0) Map

LSB FRAC REGISTER (R1) MAP

When Bits DB[2:0] are set to 001, the on-chip LSB FRAC register (Register R1) is programmed (see Figure 26).

Reserved Bits

All reserved bits must be set to 0 for normal operation.

Phase Adjustment

Bit DB28 enables and disables phase adjustment. The phase shift is generated by the value programmed in Bits DB[14:3].

13-Bit LSB Fractional Value (FRAC)

Bits DB[27:15], along with Bits DB[14:3] in the FRAC/INT register (Register R0), set the FRAC value that is loaded into the fractional interpolator. The FRAC value forms part of the overall feedback division factor.

These 13 bits are the least significant bits (LSBs) of the 25-bit FRAC value; Bits DB[14:3] in the FRAC/INT register are the most significant bits (MSBs). For more information, see the RF Synthesizer Worked Example section.

12-Bit Phase Value

Bits DB[14:3] control the phase word. The phase word is used to increase the RF output phase relative to the current phase. The phase change occurs after a write to Register R0.

$$\textit{Phase Shift} = (\textit{Phase Value} \times 360°)/2^{12}$$

For example, Phase Value = 512 increases the phase by 45°.

To use phase adjustment, Bit DB28 must be set to 1. If phase adjustment is not used, it is recommended that the phase value be set to 0.

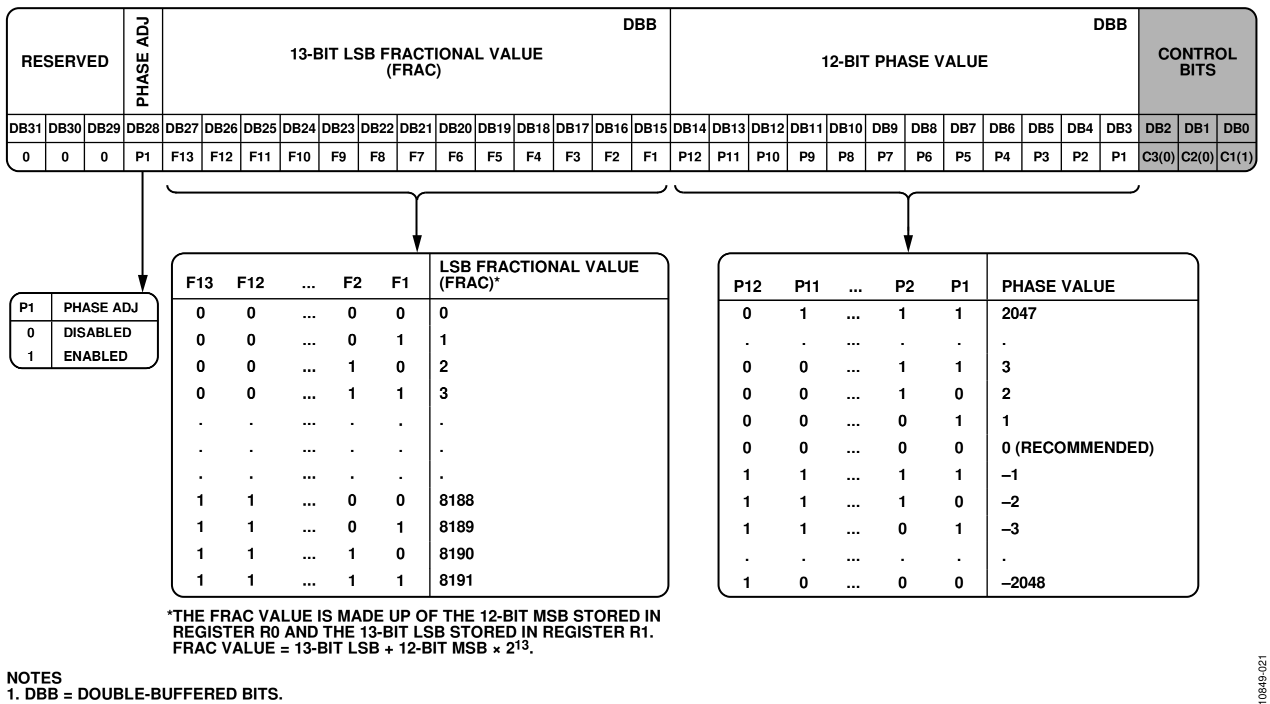

Figure 26. LSB FRAC Register (R1) Map

R DIVIDER REGISTER (R2) MAP

When Bits DB[2:0] are set to 010, the on-chip R divider register (Register R2) is programmed (see Figure 27).

Reserved Bits

All reserved bits must be set to 0 for normal operation.

CSR Enable

When Bit DB28 is set to 1, cycle slip reduction (CSR) is enabled. Cycle slip reduction is a method for improving lock times. Note that the signal at the PFD must have a 50% duty cycle for cycle slip reduction to work. In addition, the charge pump current setting must be set to its minimum value. For more information, see the Cycle Slip Reduction for Faster Lock Times section.

The cycle slip reduction feature can be used only when the phase detector polarity setting is positive (Bit DB6 = 1 in Register R3). CSR cannot be used if the phase detector polarity setting is negative (Bit DB6 = 0 in Register R3).

Charge Pump Current Setting

Bits DB[27:24] set the charge pump current (see Figure 27). Set these bits to the charge pump current that the loop filter is designed with. Best practice is to design the loop filter for a charge pump current of 2.5 mA or 2.81 mA and then use the programmable charge pump current to tweak the frequency response. See the Reference Doubler section for information on setting the charge pump current when the doubler is enabled.

Prescaler (P/P + 1)

The dual-modulus prescaler (P/P + 1), along with the INT, FRAC, and fixed modulus values, determines the overall division ratio from RF_{IN} to the PFD input. Bit DB22 sets the prescaler value.

Operating at CML levels, the prescaler takes the clock from the RF input stage and divides it down for the counters. The prescaler is based on a synchronous 4/5 core. When the prescaler is set to 4/5, the maximum RF frequency allowed is 8 GHz. Therefore, when operating the ADF4159 at frequencies greater than 8 GHz, the prescaler must be set to 8/9. The prescaler limits the INT value as follows:

- Prescaler = 4/5: N_{MIN} = 23
- Prescaler = 8/9: N_{MIN} = 75

RDIV2

When Bit DB21 is set to 1, a divide-by-2 toggle flip-flop is inserted between the R counter and the PFD. This feature can be used to provide a 50% duty cycle signal at the PFD.

Reference Doubler

When Bit DB20 is set to 0, the reference doubler is disabled, and the REF_{IN} signal is fed directly to the 5-bit R counter. When Bit DB20 is set to 1, the reference doubler is enabled, and the REF_{IN} frequency is multiplied by a factor of 2 before the signal is fed into the 5-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of REF_{IN} become active edges at the PFD input.

When the reference doubler is enabled, for optimum phase noise performance, it is recommended to only use charge pump current settings 0b0000 to 0b0111, that is, 0.31 mA to 2.5 mA. In this case, best practice is to design the loop filter to for a charge pump current of 1.25 mA or 1.57 mA and then use the programmable charge pump current to tweak the frequency response.

5-Bit R Counter

The 5-bit R counter (Bits DB[19:15]) allows the input reference frequency (REF_{IN}) to be divided down to supply the reference clock to the PFD. Division ratios from 1 to 32 are allowed.

12-Bit CLK_1 Divider Value

Bits DB[14:3] program the CLK_1 divider value, which determines the duration of the time step in ramp mode.

RESERVED			CSR	CP CURRENT SETTING (DBB)				RESERVED	PRESCALER	RDIV2 DBB	REFERENCE DOUBLER DBB	5-BIT R COUNTER (DBB)					12-BIT CLK_1 DIVIDER VALUE (DBB)												CONTROL BITS		
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	CR1	CPI4	CPI3	CPI2	CPI1	0	P1	U2	U1	R5	R4	R3	R2	R1	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	C3(0)	C2(1)	C1(0)

CR1	CYCLE SLIP REDUCTION
0	DISABLED
1	ENABLED

U1	REFERENCE DOUBLER
0	DISABLED
1	ENABLED

U2	R DIVIDER
0	DISABLED
1	ENABLED

P1	PRESCALER
0	4/5
1	8/9

CPI4	CPI3	CPI2	CPI1	I_{CP} (mA) 5.1kΩ
0	0	0	0	0.31
0	0	0	1	0.63
0	0	1	0	0.94
0	0	1	1	1.25
0	1	0	0	1.57
0	1	0	1	1.88
0	1	1	0	2.19
0	1	1	1	2.5
1	0	0	0	2.81
1	0	0	1	3.13
1	0	1	0	3.44
1	0	1	1	3.75
1	1	0	0	4.06
1	1	0	1	4.38
1	1	1	0	4.69
1	1	1	1	5.0

D12	D11	...	D2	D1	CLK_1 DIVIDER VALUE
0	0	...	0	0	0
0	0	...	0	1	1
0	0	...	1	0	2
0	0	...	1	1	3
.	.	...	.	.	.
.	.	...	.	.	.
.	.	...	.	.	.
1	1	...	0	0	4092
1	1	...	0	1	4093
1	1	...	1	0	4094
1	1	...	1	1	4095

R5	R4	R3	R2	R1	R COUNTER DIVIDE RATIO
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
.	.	.	.	.	
.	.	.	.	.	
.	.	.	.	.	
1	1	1	0	1	29
1	1	1	1	0	30
1	1	1	1	1	31
0	0	0	0	0	32

NOTES
1. DBB = DOUBLE-BUFFERED BITS.

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Figure 27. R Divider Register (R2) Map

FUNCTION REGISTER (R3) MAP

When Bits DB[2:0] are set to 011, the on-chip function register (Register R3) is programmed (see Figure 28).

Reserved Bits

All reserved bits except Bit DB17 must be set to 0 for normal operation. Bit DB17 must be set to 1 for normal operation.

Negative Bleed Current

Bits DB[24:22] set the negative bleed current value (I_{BLEED}). Calculate I_{BLEED} using the following formula, and then select the value of Bits DB[24:22] that is closest to the calculated value.

$$I_{BLEED} = (4 \times I_{CP})/N$$

where:
I_{CP} is the charge pump current.
N is the N counter value.

Negative Bleed Current Enable

DB21 enables a negative bleed current in the charge pump. When the charge pump is operating in a nonlinear region, phase noise and spurious performance can degrade. Negative bleed current operates by pushing the charge pump operation region away from this nonlinear region. The programmability feature controls how far the region of operation is moved. If the current is too little, the charge pump will remain in the nonlinear region; if the current is too high, the charge pump will become unstable or degrade the maximum PFD frequency. It is necessary to experiment with various charge pump currents to find the optimum.

The formula for calculating the optimum negative bleed current is shown in the Negative Bleed Current section; however, experimentation may show a different current gives the optimum result.

Loss of Lock (LOL)

Bit DB16 enables or disables the loss of lock indication. When this bit is set to 0, the part indicates loss of lock even when the reference is removed. This feature provides an advantage over the standard implementation of lock detect. For more robust operation, set this bit to 1. The loss of lock does not operate as expected when negative bleed current is enabled.

N SEL

Bit DB15 can be used to circumvent the issue of pipeline delay between updates of the integer and fractional values in the N counter. Typically, the INT value is loaded first, followed by the FRAC value. This can cause the N counter value to be incorrect for a brief period of time equal to the pipeline delay (about four PFD cycles). This delay has no effect if the INT value was not updated. However, if the INT value has changed, this incorrect N counter value can cause the PLL to overshoot in frequency while it tries to lock to the temporarily incorrect N counter value. After the correct fractional value is loaded, the PLL quickly locks to the correct frequency. Introducing an additional delay to the loading of the INT value using the N SEL bit causes the INT and FRAC values to be loaded at the same time, preventing frequency overshoot. The delay is turned on by setting Bit DB15 to 1.

Σ-Δ Reset

For most applications, Bit DB14 should be set to 0. When this bit is set to 0, the Σ-Δ modulator is reset on each write to Register R0. If it is not required that the Σ-Δ modulator be reset on each write to Register R0, set this bit to 1.

Ramp Mode

Bits DB[11:10] determine the type of generated waveform (see Figure 28 and the Waveform Generation section).

PSK Enable

When Bit DB9 is set to 1, PSK modulation is enabled. When this bit is set to 0, PSK modulation is disabled. For more information, see the Phase Shift Keying (PSK) section.

FSK Enable

When Bit DB8 is set to 1, FSK modulation is enabled. When this bit is set to 0, FSK modulation is disabled. For more information, see the Frequency Shift Keying (FSK) section.

Lock Detect Precision (LDP)

The digital lock detect circuit monitors the PFD up and down pulses (logical OR of the up and down pulses; see Figure 21). Every 32nd pulse is measured. The LDP bit (Bit DB7) specifies the length of each lock detect reference cycle.

- LDP = 0: if five consecutive pulses of less than 14 ns are measured, digital lock detect is asserted.
- LDP = 1: if five consecutive pulses of less than 6 ns are measured, digital lock detect is asserted.

Digital lock detect remains asserted until the pulse width exceeds 22 ns, a write to Register R0 occurs, or the part is powered down. For more robust operation, set LDP = 1.

Phase Detector (PD) Polarity

Bit DB6 sets the phase detector polarity. When the VCO characteristics are positive, set this bit to 1. When the VCO characteristics are negative, set this bit to 0.

Power-Down

Bit DB5 provides the programmable power-down mode. Setting this bit to 1 performs a power-down. Setting this bit to 0 returns the synthesizer to normal operation. When the part is in software power-down mode, it retains all information in its registers. The register contents are lost only when the supplies are removed.

When power-down is activated, the following events occur:

- All active dc current paths are removed.
- The RF synthesizer counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry is reset.
- The RF_{IN} input is debiased.
- The input shift register remains active and capable of loading and latching data.

Charge Pump Three-State

When Bit DB4 is set to 1, the charge pump is placed into three-state mode. For normal charge pump operation, set this bit to 0.

Counter Reset

Bit DB3 is the RF counter reset bit. When this bit is set to 1, the RF synthesizer counters are held in reset. For normal operation, set this bit to 0.

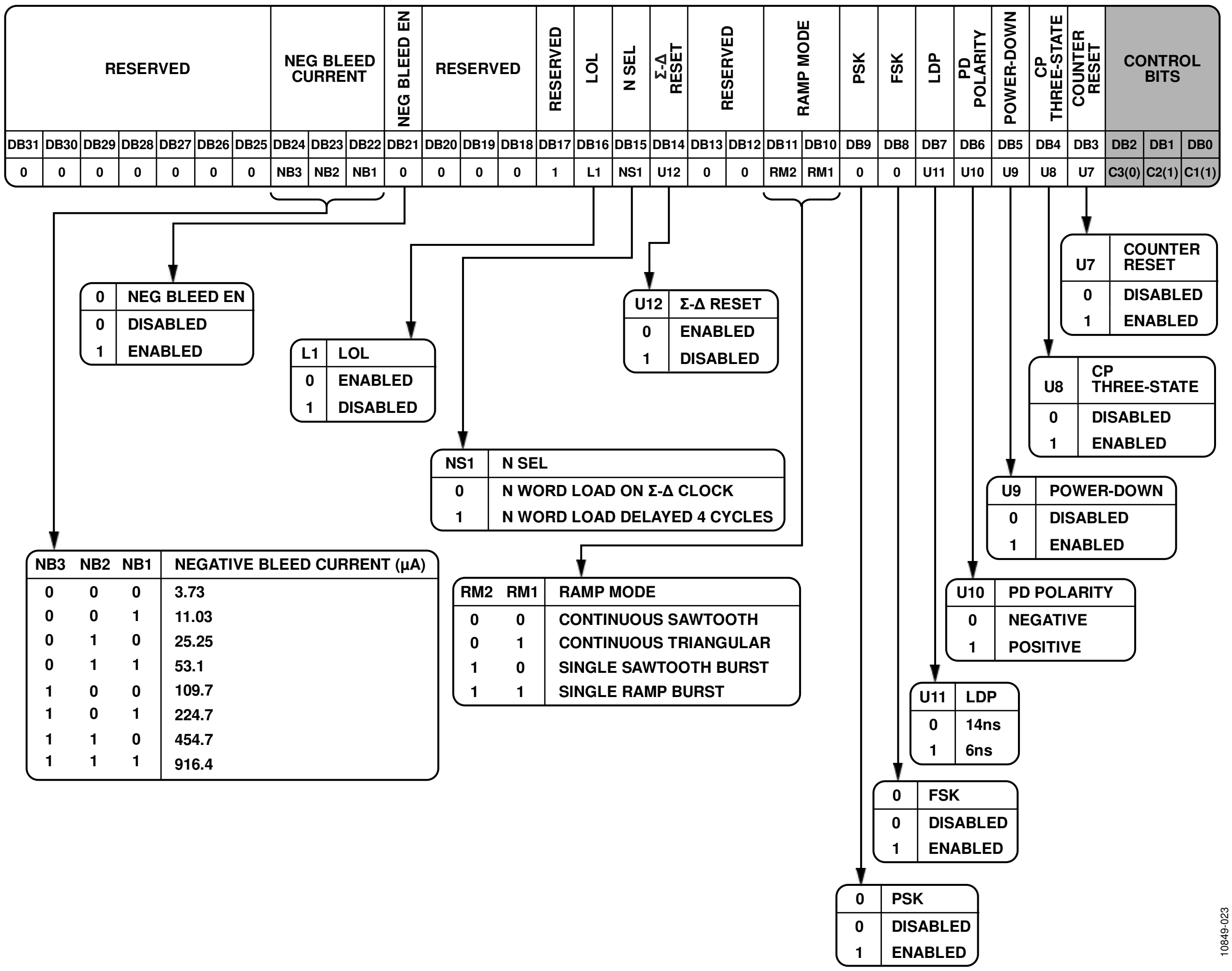

Figure 28. Function Register (R3) Map

CLOCK REGISTER (R4) MAP

When Bits DB[2:0] are set to 100, the on-chip clock register (Register R4) is programmed (see Figure 29).

LE SEL

In some applications, it is necessary to synchronize the LE pin with the reference signal. To do this, Bit DB31 must be set to 1. Synchronization is done internally on the part.

Σ-Δ Modulator Mode

To completely disable the Σ-Δ modulator, set Bits DB[30:26] to 0b01110, which puts the ADF4159 into integer-N mode, and the channel spacing becomes equal to the PFD frequency. Both the 12-bit MSB fractional value (Register R0, DB[14:3]) and the 13-bit LSB fractional value (Register R1, DB[27:15]) must be set to 0. After writing to Register 4, Register 3 must be written to twice, to trigger a counter reset. (That is, write Register 3 with DB3 = 1, then write Register 3 with DB3 = 0.)

All features driven by the Σ-Δ modulator are disabled, such as ramping, PSK, FSK, and phase adjust.

Disabling the Σ-Δ modulator also removes the fixed $+(f_{PFD}/2^{26})$ offset on the VCO output.

For normal operation, set these bits to 0b00000.

Ramp Status

Bits DB[25:21] provide access to the following advanced features (see Figure 29):

- Readback to MUXOUT option: the synthesizer frequency at the moment of interruption can be read back (see the Interrupt Modes and Frequency Readback section).
- Ramp complete to MUXOUT option: a logic high pulse is output on the MUXOUT pin at the end of each ramp.
- Charge pump up and charge pump down options: the charge pump is forced to constantly output up or down pulses, respectively.

When using the readback to MUXOUT or ramp complete to MUXOUT option, the MUXOUT bits in Register R0 (Bits DB[30:27]) must be set to 1111.

Clock Divider Mode

Bits DB[20:19] are used to enable Ramp Divider mode or Fast Lock Divider mode. If neither is being used, set these bits to 0b00.

12-Bit CLK_2 Divider Value

Bits DB[18:7] program the clock divider (the CLK_2 timer) when the part operates in ramp mode (see the Timeout Interval section). The CLK_2 timer also determines how long the loop remains in wideband mode when fast lock mode is used (see the Fast Lock Mode section).

Clock Divider Select

When Bit DB6 is set to 0, CLK_2 is used as the CLK_2 value for a standard ramp, such as sawtooth or triangular. When Bit DB6 is set to 1, CLK_2 is used as the CLK_2 value for the second ramp of the Fast Ramp or Dual Ramp functions. For more information, see the Waveform Deviations and Timing section.

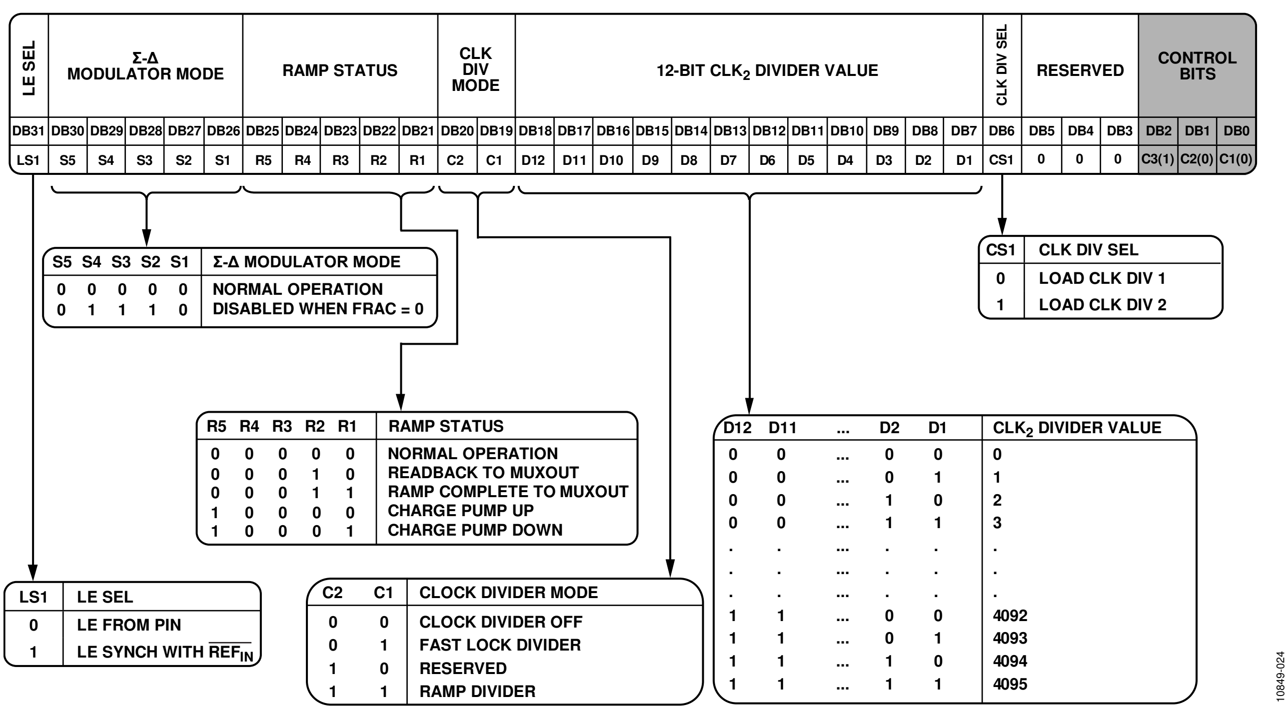

Figure 29. Clock Register (R4) Map

DEVIATION REGISTER (R5) MAP

When Bits DB[2:0] are set to 101, the on-chip deviation register (Register R5) is programmed (see Figure 30).

Reserved Bit

The reserved bit must be set to 0 for normal operation.

TX_{DATA} Invert

When Bit DB30 is set to 0, events triggered by TX_{DATA} occur on the rising edge of the TX_{DATA} pulse. When Bit DB30 is set to 1, events triggered by TX_{DATA} occur on the falling edge of the TX_{DATA} pulse.

TX_{DATA} Ramp Clock

When Bit DB29 is set to 0, the clock divider clock is used to clock the ramp. When Bit DB29 is set to 1, the TX_{DATA} clock is used to clock the ramp.

Parabolic Ramp

When Bit DB28 is set to 1, the parabolic ramp is enabled. When Bit DB28 is set to 0, the parabolic ramp is disabled. For more information, see the Parabolic (Nonlinear) Ramp Mode section.

Interrupt

Bits DB[27:26] determine which type of interrupt is used. This feature is used for reading back the INT and FRAC value of a ramp at a given moment in time (a rising edge on the TX_{DATA} pin triggers the interrupt). From the INT and FRAC bits, the frequency can be obtained. After readback, the sweep can continue or stop at the readback frequency. For more information, see the Interrupt Modes and Frequency Readback section.

FSK Ramp Enable

When Bit DB25 is set to 1, the FSK ramp is enabled. When Bit DB25 is set to 0, the FSK ramp is disabled.

Dual Ramp Enable

When Bit DB24 is set to 1, the second ramp is enabled. When Bit DB24 is set to 0, the second ramp is disabled.

Deviation Select

When Bit DB23 is set to 0, the first deviation word is selected. When Bit DB23 is set to 1, the second deviation word is selected.

4-Bit Deviation Offset Word

Bits DB[22:19] determine the deviation offset word. The deviation offset word affects the deviation resolution.

16-Bit Deviation Word

Bits DB[18:3] determine the signed deviation word. The deviation word defines the deviation step.

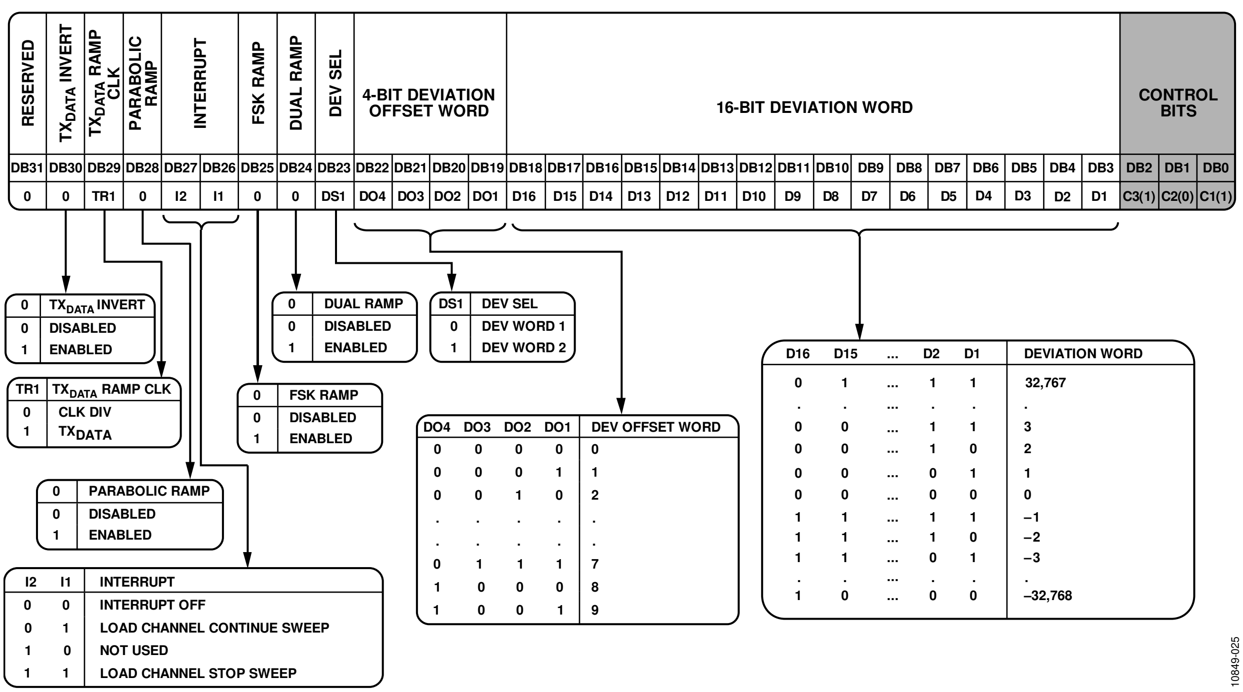

Figure 30. Deviation Register (R5) Map

STEP REGISTER (R6) MAP

When Bits DB[2:0] are set to 110, the on-chip step register (Register R6) is programmed (see Figure 31).

Reserved Bits

All reserved bits must be set to 0 for normal operation.

Step Select

When Bit DB23 is set to 0, Step Word 1 is selected. When Bit DB23 is set to 1, Step Word 2 is selected.

20-Bit Step Word

Bits DB[22:3] determine the step word. The step word is the number of steps in the ramp.

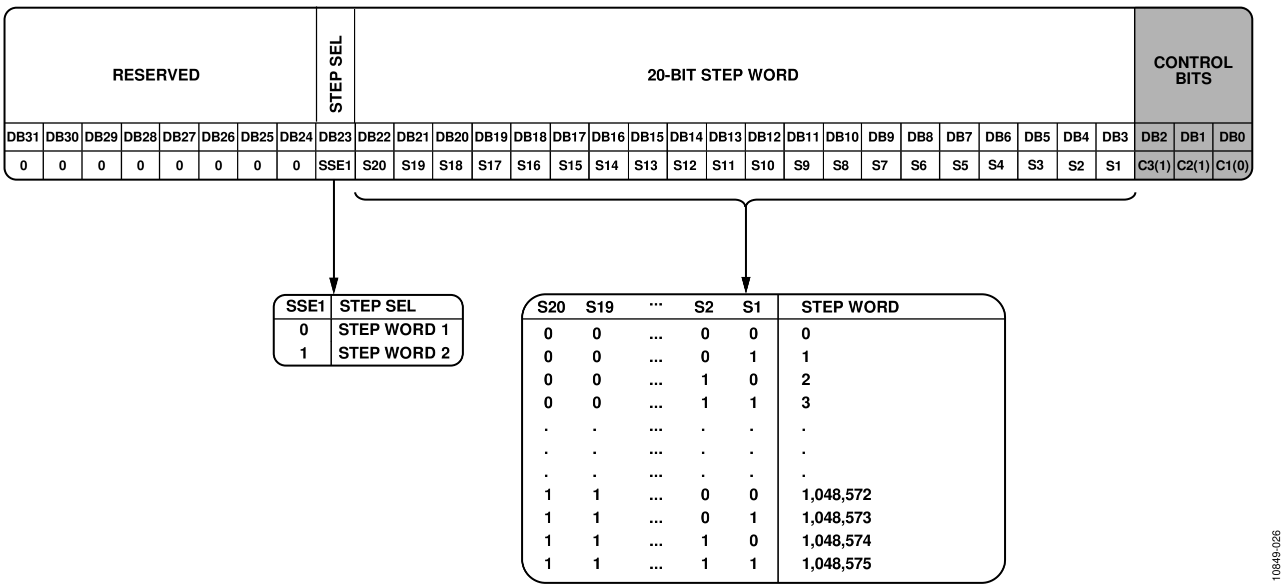

Figure 31. Step Register (R6) Map

DELAY REGISTER (R7) MAP

When Bits DB[2:0] are set to 111, the on-chip delay register (Register R7) is programmed (see Figure 32).

Reserved Bits

All reserved bits must be set to 0 for normal operation.

TX_{DATA} Trigger Delay

When Bit DB23 is set to 0, there is no delay before the start of the ramp when using TX_{DATA} to trigger a ramp. When Bit DB23 is set to 1, a delay is enabled before the start of the ramp if the delayed start is enabled via Bit DB15.

Triangular Delay

When Bit DB22 is set to 1, a delay is enabled between each section of a triangular ramp, resulting in a clipped ramp. This setting works only for triangular ramps and when the ramp delay is activated. When Bit DB22 is set to 0, the delay between triangular ramps is disabled.

Single Full Triangle

When Bit DB21 is set to 1, the single full triangle function is enabled. When Bit DB21 is set to 0, this function is disabled. To use the single full triangle function, Ramp Mode (Register 3, DB[11:10]) must be set to 0b11, Single Ramp Burst. For more information, see the Waveform Generation section.

TX_{DATA} Trigger

When Bit DB20 is set to 1, a logic high on TX_{DATA} activates the ramp. When Bit DB20 is set to 0, this function is disabled.

Fast Ramp

When Bit DB19 is set to 1, the triangular waveform is activated with two different slopes. This waveform can be used as an alternative to the sawtooth ramp because it mitigates the overshoot at the end of the ramp in a waveform. Fast ramp is achieved by changing the top frequency to the bottom frequency in a series of small steps instead of one big step. When Bit DB19 is set to 0, the fast ramp function is disabled (see the Fast Ramp Mode section).

Ramp Delay Fast Lock

When Bit DB18 is set to 1, the ramp delay fast lock function is enabled. When Bit DB18 is set to 0, this function is disabled.

Ramp Delay

When Bit DB17 is set to 1, the delay between ramps function is enabled. When Bit DB17 is set to 0, this function is disabled.

Delay Clock Select

When Bit DB16 is set to 0, the PFD clock is selected as the delay clock. When Bit DB16 is set to 1, PFD clock × CLK_1 is selected as the delay clock. (CLK_1 is set by Bits DB[14:3] in Register R2.)

Delayed Start Enable

When Bit DB15 is set to 1, the delayed start is enabled. When Bit DB15 is set to 0, the delayed start is disabled.

12-Bit Delay Start Word

Bits DB[14:3] determine the delay start word. The delay start word affects the duration of the ramp start delay.

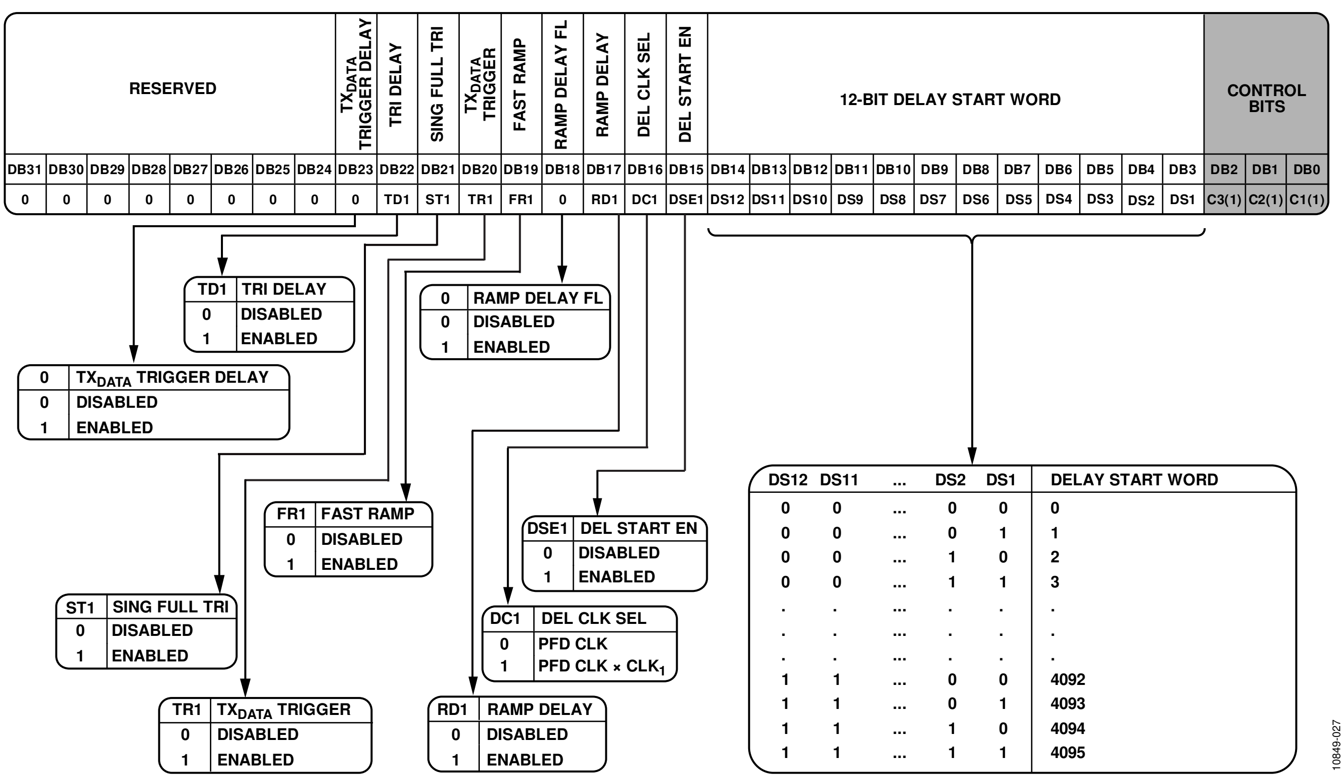

Figure 32. Delay Register (R7) Map