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Low Phase Noise, Fast Settling PLL Frequency Synthesizer

Data Sheet

ADF4193

FEATURES

- New, fast settling, fractional-N PLL architecture
- Single PLL replaces ping-pong synthesizers
- Frequency hop across GSM band in 5 µs with phase settled by 20 µs
- 0.5° rms phase error at 2 GHz RF output
- Digitally programmable output phase
- RF input range up to 3.5 GHz
- 3-wire serial interface
- On-chip, low noise differential amplifier
- Phase noise figure of merit: −216 dBc/Hz
- Loop filter design possible using ADIsimPLL™
- Qualified for automotive applications

APPLICATIONS

- GSM/EDGE base stations
- PHS base stations
- Instrumentation and test equipment

GENERAL DESCRIPTION

The ADF4193 frequency synthesizer can be used to implement local oscillators in the upconversion and downconversion sections of wireless receivers and transmitters. Its architecture is specifically designed to meet the GSM/EDGE lock time requirements for base stations. It consists of a low noise, digital phase frequency detector (PFD), and a precision differential charge pump. There is also a differential amplifier to convert the differential charge pump output to a single-ended voltage for the external voltage-controlled oscillator (VCO).

The Σ-Δ based fractional interpolator, working with the N divider, allows programmable modulus fractional-N division. Additionally, the 4-bit reference (R) counter and on-chip frequency doubler allow selectable reference signal (REFIN) frequencies at the PFD input. A complete phase-locked loop (PLL) can be implemented if the synthesizer is used with an external loop filter and a VCO. The switching architecture ensures that the PLL settles inside the GSM time slot guard period, removing the need for a second PLL and associated isolation switches. This decreases cost, complexity, PCB area, shielding, and characterization on previous ping-pong GSM PLL architectures.

FUNCTIONAL BLOCK DIAGRAM

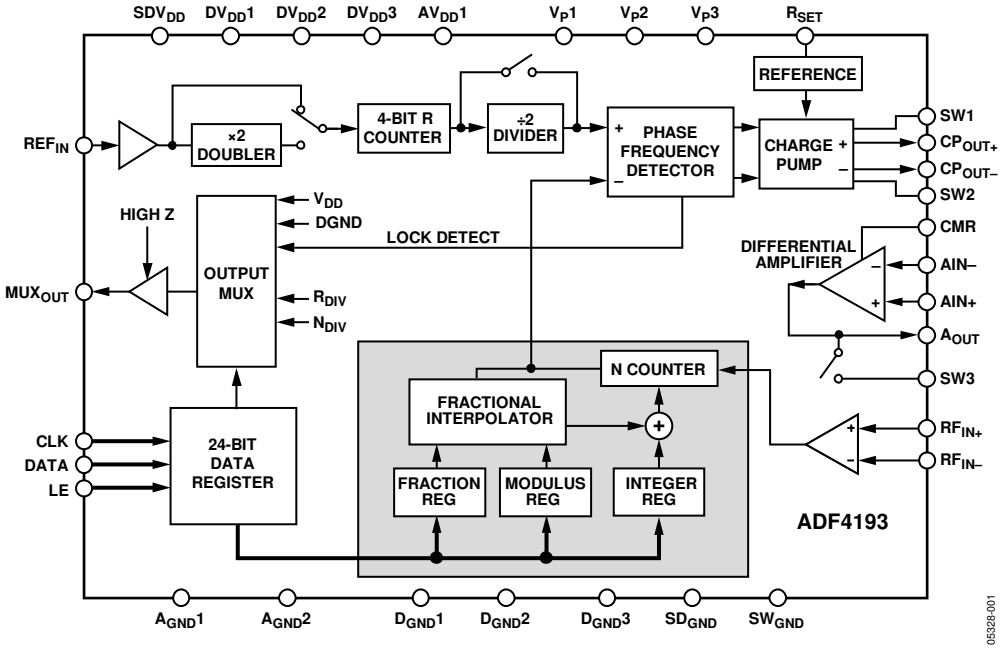

Figure 1.

Document Feedback

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- ADF4193 Evaluation Boards

DOCUMENTATION

Application Notes

- AN-0974: Multicarrier TD-SCMA Feasibility
- AN-873: Lock Detect on the ADF4xxx Family of PLL Synthesizers

Data Sheet

- ADF4193: Low Phase Noise, Fast Settling PLL Frequency Synthesizer Data Sheet

User Guides

- UG-476: PLL Software Installation Guide
- UG-536: Evaluating the ADF4193 and ADF4196 Frequency Synthesizers for Phase-Locked Loops

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

REFERENCE MATERIALS

Press

- New Analog Devices' PLL Synthesizers Deliver Utmost Flexibility and Phase Noise Performance

Product Selection Guide

- RF Source Booklet

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- ADF4193 Material Declaration
- PCN-PDN Information
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SPECIFICATIONS

AV_{DD} = DV_{DD} = SDV_{DD} = 3 V ± 10%, V_P1, V_P2 = 5 V ± 10%, V_P3 = 5.35 V ± 5%, AGND = DGND = GND = 0 V, R_{SET} = 2.4 kΩ, dBm referred to 50 Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1]	C Version[2]	Unit	Test Conditions/Comments
RF CHARACTERISTICS				
RF Input Frequency (RF_{IN})	0.4/3.5	0.4/3.5	GHz min/max	See Figure 21 for input circuit
RF Input Sensitivity	−10/0	−10/0	dBm min/max	
Maximum Allowable Prescaler Output Frequency[3]	470	470	MHz max	
REF_{IN} CHARACTERISTICS				
REF_{IN} Input Frequency	10/300	10/300	MHz min/max	For f > 120 MHz, set REF/2 bit = 1. For f < 10 MHz, use a dc-coupled square wave
REF_{IN} Edge Slew Rate	300	300	V/µs min	
REF_{IN} Input Sensitivity	0.7/V_{DD}	0.7/V_{DD}	V p-p min/max	AC-coupled
	0 to V_{DD}	0 to V_{DD}	V max	CMOS-compatible
REF_{IN} Input Capacitance	10	10	pF max	
REF_{IN} Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency	26	30	MHz max	
CHARGE PUMP				
I_{CP} Up/Down				
High Value	6.6	6.6	mA typ	With R_{SET} = 2.4 kΩ
Low Value	104	104	µA typ	With R_{SET} = 2.4 kΩ
Absolute Accuracy	5	5	% typ	
R_{SET} Range	1/4	1/4	kΩ min/max	Nominally R_{SET} = 2.4 kΩ
I_{CP} Three-State Leakage	1	1	nA typ	
I_{CP} Up vs. Down Matching	0.1	0.1	% typ	0.75 V ≤ V_{CP} ≤ V_P − 1.5 V
I_{CP} vs. V_{CP}	1	1	% typ	0.75 V ≤ V_{CP} ≤ V_P − 1.5 V
I_{CP} vs. Temperature	1	1	% typ	0.75 V ≤ V_{CP} ≤ V_P − 1.5 V
DIFFERENTIAL AMPLIFIER				
Input Current	1	1	nA typ	
Output Voltage Range	1.4/(V_P3 − 0.3)	1.4/(V_P3 − 0.3)	V min/max	
VCO Tuning Range	1.8/(V_P3 − 0.8)	1.8/(V_P3 − 0.8)	V min/max	
Output Noise	7	7	nV/√Hz typ	At 20 kHz offset
LOGIC INPUTS				
V_{IH}, Input High Voltage	1.4	1.4	V min	
V_{IL}, Input Low Voltage	0.7	0.7	V max	
I_{INH}, I_{INL}, Input Current	±1	±2	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	V_{DD} − 0.4	V_{DD} − 0.4	V min	I_{OH} = 500 µA
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{OL} = 500 µA
POWER SUPPLIES				
AV_{DD}	2.7/3.3	2.7/3.3	V min/V max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P1, V_P2	4.5/5.5	4.5/5.5	V min/V max	AV_{DD} ≤ V_P1, V_P2 ≤ 5.5 V
V_P3	5.0/5.65	5.0/5.65	V min/V max	V_P1, V_P2 ≤ V_P3 ≤ 5.65 V
I_{DD} (AV_{DD} + DV_{DD} + SDV_{DD})	27	35	mA max	22 mA typ
I_{DD} (V_P1 + V_P2)	27	30	mA max	22 mA typ
I_{DD} (V_P3)	30	35	mA max	24 mA typ
I_{DD} Power-Down	10	10	µA typ	

Parameter	B Version[1]	C Version[2]	Unit	Test Conditions/Comments
SW1, SW2, and SW3				
R_{ON} (SW1 and SW2)	65	65	Ω typ	
R_{ON} SW3	75	75	Ω typ	
NOISE CHARACTERISTICS				
Output				
900 MHz[4]	−108	−108	dBc/Hz typ	At 5 kHz offset and 26 MHz PFD frequency
1800 MHz[5]	−102	−102	dBc/Hz typ	At 5 kHz offset and 13 MHz PFD frequency
Phase Noise				
Normalized Phase Noise Floor (PN_{SYNTH})[6]	−216	−216	dBc/Hz typ	At VCO output with dither off, PLL loop bandwidth = 500 kHz
Normalized 1/f Noise (PN_{1_f})[7]	−110	−110	dBc/Hz typ	Measured at 10 kHz offset, normalized to 1 GHz

[1] Operating temperature range is from −40°C to +85°C.
[2] Operating temperature range is from −40°C to +105°C
[3] The prescaler value is chosen to ensure that the RF input is divided down to a frequency that is less than this value.
[4] $f_{REF_{IN}}$ = 26 MHz; f_{STEP} = 200 kHz; f_{RF} = 900 MHz; loop bandwidth = 40 kHz.
[5] $f_{REF_{IN}}$ = 13 MHz; f_{STEP} = 200 kHz; f_{RF} = 1800 MHz; loop bandwidth = 60 kHz.
[6] The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 log(N) (where N is the N divider value) and 10 log(f_{PFD}). $PN_{SYNTH} = PN_{TOT} - 10\log(f_{PFD}) - 20\log(N)$.
[7] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency, f_{RF}, and at an offset frequency, f, is given by $PN = P_{1\_f} + 10\log(10\text{ kHz}/f) + 20\log(f_{RF}/1\text{ GHz})$. Both the normalized phase noise floor and flicker noise are modeled in ADIsimPLL.

TIMING CHARACTERISTICS

$AV_{DD} = DV_{DD} = 3\text{ V} \pm 10\%$, V_P1, $V_P2 = 5\text{ V} \pm 10\%$, $V_P3 = 5.35\text{ V} \pm 5\%$, AGND = DGND = GND = 0 V, $R_{SET} = 2.4\text{ k}\Omega$, dBm referred to 50 Ω, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Limit (B Version)[1]	Limit (C Version)[2]	Unit	Test Conditions/Comments
t_1	10	10	ns min	LE setup time
t_2	10	10	ns min	DATA to CLOCK setup time
t_3	10	10	ns min	DATA to CLOCK hold time
t_4	15	15	ns min	CLOCK high duration
t_5	15	15	ns min	CLOCK low duration
t_6	10	10	ns min	CLOCK to LE setup time
t_7	15	15	ns min	LE pulse width

[1] Operating temperature is from −40°C to +85°C.
[2] Operating temperature is from −40°C to +105°C.

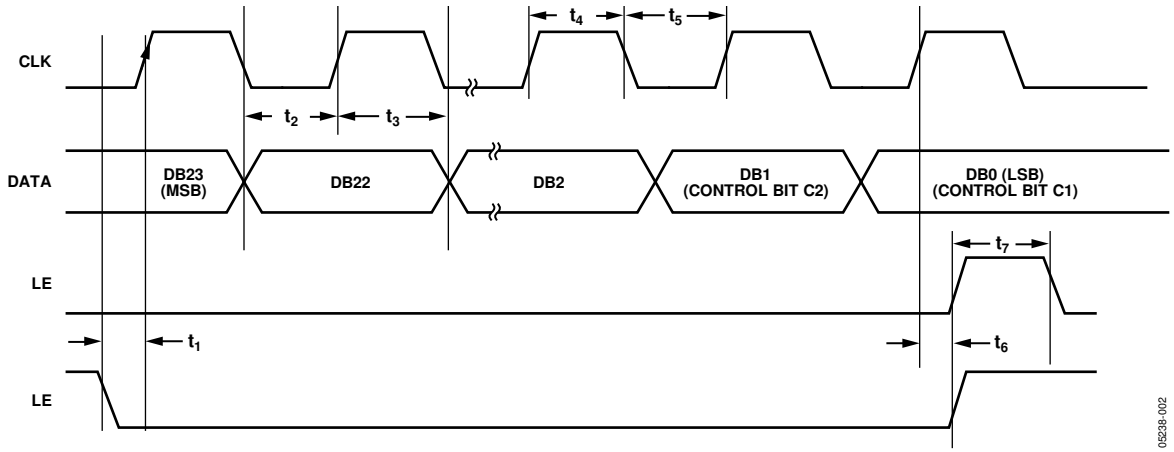

Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
AV_{DD} to GND	−0.3 V to +3.6 V
AV_{DD} to DV_{DD}, SDV_{DD}	−0.3 V to +0.3 V
V_P to GND	−0.3 V to +5.8 V
V_P to AV_{DD}	−0.3 V to +5.8 V
Digital I/O Voltage to GND	−0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	−0.3 V to V_P + 0.3 V
REF_{IN}, RF_{IN+}, RF_{IN-} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Operating Temperature Range Automotive (W Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance (Paddle Soldered)	27.3°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions need to be taken for handling and assembly.

Transistor Count

75,800 (MOS), 545 (BJT).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

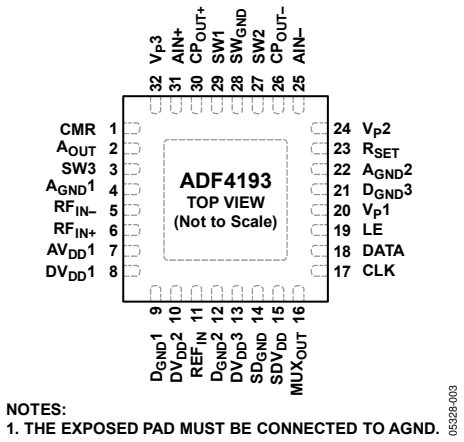

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CMR	Common-Mode Reference Voltage for the Differential Amplifier's Output Voltage Swing. Internally biased to three-fifths of V_P3. Requires a 0.1 µF capacitor to ground.
2	A_{OUT}	Differential Amplifier Output to Tune the External VCO.
3	SW3	Fast-Lock Switch 3. Closed while SW3 timeout counter is active.
4	$A_{GND}1$	Analog Ground. This is the ground return pin for the differential amplifier and the RF section.
5	RF_{IN-}	Complementary Input to the RF Prescaler. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF.
6	RF_{IN+}	Input to the RF Prescaler. This small signal input is ac-coupled to the external VCO.
7	$AV_{DD}1$	Power Supply Pin for the RF Section. Nominally 3 V. A 100 pF decoupling capacitor to the ground plane should be placed as close as possible to this pin.
8	$DV_{DD}1$	Power Supply Pin for the N Divider. Should be the same voltage as $AV_{DD}1$. A 0.1 µF decoupling capacitor to ground should be placed as close as possible to this pin.
9	$D_{GND}1$	Ground Return Pin for $DV_{DD}1$.
10	$DV_{DD}2$	Power Supply Pin for the REF_{IN} Buffer and R Divider. Nominally 3 V. A 0.1 µF decoupling capacitor to ground should be placed as close as possible to this pin.
11	REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and a dc equivalent input resistance of 100 kΩ (see Figure 15). This input can be driven from a TTL or CMOS crystal oscillator or it can be ac-coupled.
12	$D_{GND}2$	Ground Return Pin for $DV_{DD}2$ and $DV_{DD}3$.
13	$DV_{DD}3$	Power Supply Pin for the Serial Interface Logic. Nominally 3 V.
14	SD_{GND}	Ground Return Pin for the Σ-Δ Modulator.
15	SDV_{DD}	Power Supply Pin for the Digital Σ-Δ Modulator. Nominally 3 V. A 0.1 µF decoupling capacitor to the ground plane should be placed as close as possible to this pin.
16	MUX_{OUT}	Multiplexer Output. This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally (see Figure 35).
17	CLK	Serial Clock Input. Data is clocked into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
18	DATA	Serial Data Input. The serial data is loaded MSB first with the three LSBs as the control bits. This input is a high impedance CMOS input.
19	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift register is loaded into the register that is selected by the three LSBs.
20	V_P1	Power Supply Pin for the Phase Frequency Detector (PFD). Nominally 5 V, should be at the same voltage at V_P2. A 0.1 µF decoupling capacitor to ground should be placed as close as possible to this pin.
21	$D_{GND}3$	Ground Return Pin for V_P1.
22	$A_{GND}2$	Ground Return Pin for V_P2.

Pin No.	Mnemonic	Description
23	R_{SET}	Connecting a resistor between this pin and GND sets the charge pump output current. The nominal voltage bias at the R_{SET} pin is 0.55 V. The relationship between I_{CP} and R_{SET} is $I_{CP} = 0.25/R_{SET}$ So, with R_{SET} = 2.4 kΩ, I_{CP} = 104 µA.
24	V_P2	Power Supply Pin for the Charge Pump. Nominally 5 V, should be at the same voltage at V_P1. A 0.1 µF decoupling capacitor to ground should be placed as close as possible to this pin.
25	AIN−	Differential Amplifier's Negative Input Pin.
26	CP_{OUT-}	Differential Charge Pump's Negative Output Pin. Should be connected to AIN− and the loop filter.
27	SW2	Fast Lock Switch 2. This switch is closed to SW_{GND} while the SW1/SW2 timeout counter is active.
28	SW_{GND}	Common for SW1 and SW2 Switches. Should be connected to the ground plane.
29	SW1	Fast Lock Switch 1. This switch is closed to SW_{GND} while the SW1/SW2 timeout counter is active.
30	CP_{OUT+}	Differential Charge Pump's Positive Output Pin. Should be connected to AIN+ and the loop filter.
31	AIN+	Differential Amplifier's Positive Input Pin.
32	V_P3	Power Supply Pin for the Differential Amplifier. This can range from 5.0 V to 5.5 V. A 0.1 µF decoupling capacitor to ground should be placed as close as possible to this pin. Also requires a 10 µF decoupling capacitor to ground.
	EP	Exposed Pad. The exposed pad must be connected to AGND.

TYPICAL PERFORMANCE CHARACTERISTICS

FREQ. UNIT GHz KEYWORD R
PARAM TYPE S IMPEDANCE 50
DATA FORMAT MA

FREQ.	MAGS11	ANGS11	FREQ.	MAGS11	ANGS11
0.5	0.8897	–16.6691	2.3	0.67107	–75.8206
0.6	0.87693	–19.9279	2.4	0.66556	–77.6851
0.7	0.85834	–23.561	2.5	0.6564	–80.3101
0.8	0.85044	–26.9578	2.6	0.6333	–82.5082
0.9	0.83494	–30.8201	2.7	0.61406	–85.5623
1.0	0.81718	–34.9499	2.8	0.5977	–87.3513
1.1	0.80229	–39.0436	2.9	0.5655	–89.7605
1.2	0.78917	–42.3623	3.0	0.5428	–93.0239
1.3	0.77598	–46.322	3.1	0.51733	–95.9754
1.4	0.75578	–50.3484	3.2	0.49909	–99.1291
1.5	0.74437	–54.3545	3.3	0.47309	–102.208
1.6	0.73821	–57.3785	3.4	0.45694	–106.794
1.7	0.7253	–60.695	3.5	0.44698	–111.659
1.8	0.71365	–63.9152	3.6	0.43589	–117.986
1.9	0.70699	–66.4365	3.7	0.42472	–125.62
2.0	0.7038	–68.4453	3.8	0.41175	–133.291
2.1	0.69284	–70.7986	3.9	0.41055	–140.585
2.2	0.67717	–73.7038	4.0	0.40983	–147.97

05328-038

Figure 4. S Parameter Data for the RF Input

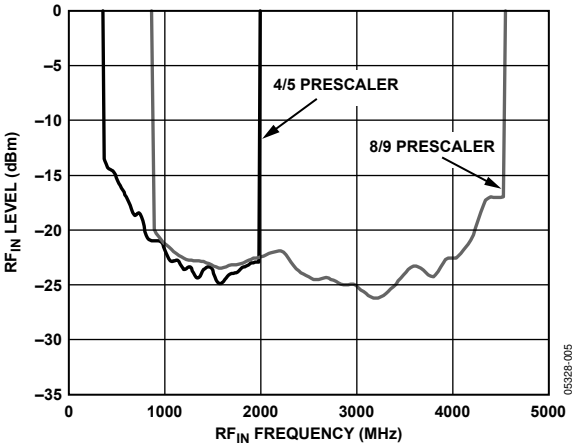

Figure 7. RF Input Sensitivity

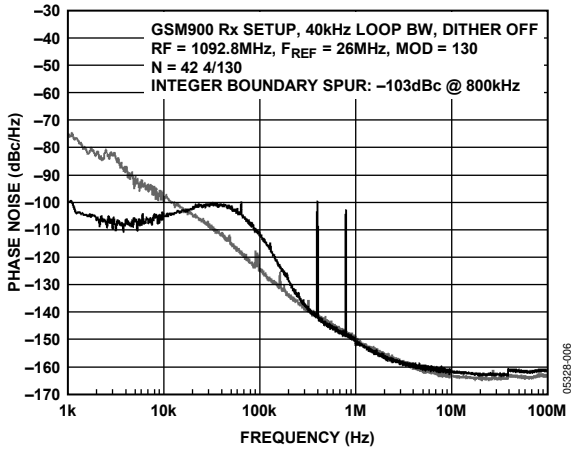

Figure 5. SSB Phase Noise Plot at 1092.8 MHz (GSM900 Rx Setup) vs. Free Running VCO Noise

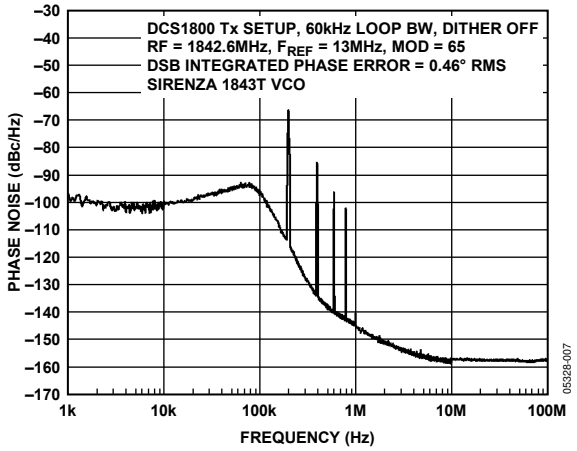

Figure 8. SSB Phase Noise Plot at 1842.6 MHz (DCS1800 Tx Setup)

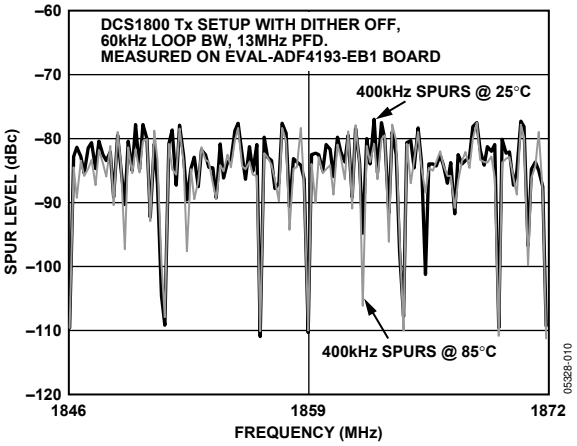

Figure 6. 400 kHz Fractional Spur Levels Across All DCS1800 Tx Channels Over Two-Integer Multiples of the PFD Reference

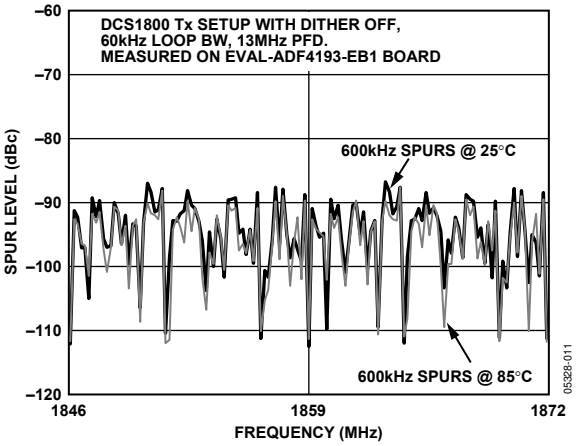

Figure 9. 600 kHz Fractional Spur Levels Across All DCS1800 Tx Channels Over Two-Integer Multiples of the PFD Reference

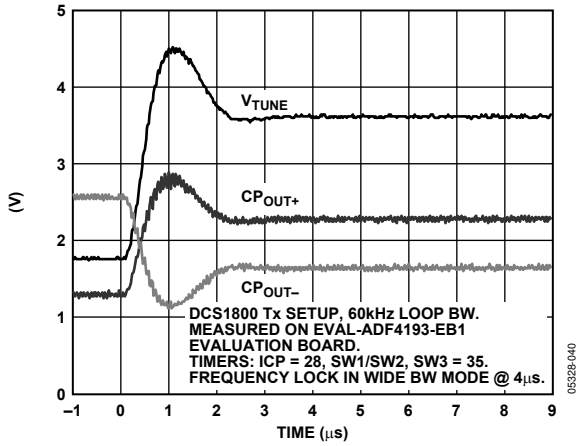

Figure 10. V_{TUNE} Settling Transient for a 75 MHz Jump from 1818 MHz to 1893 MHz with Sirenza 1843T VCO

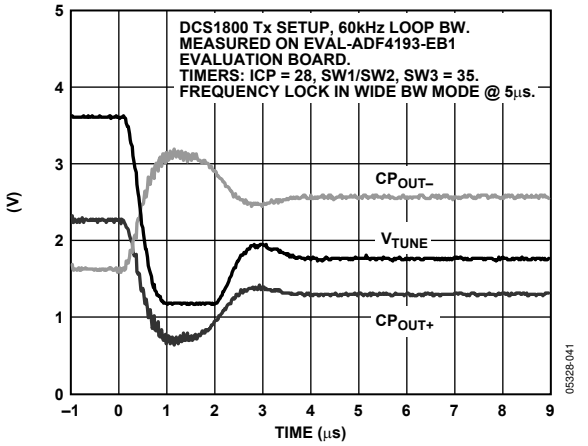

Figure 13. V_{TUNE} Settling Transient for a 75 MHz Jump Down from 1893 MHz to 1818 MHz, the Bottom of the Allowed Tuning Range with the Sirenza 1843T VCO

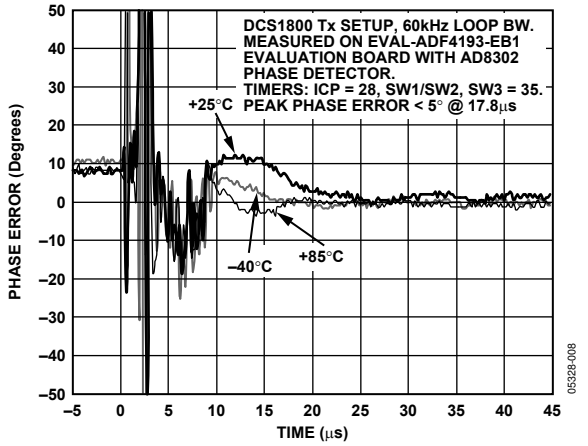

Figure 11. Phase Settling Transient for a 75 MHz Jump from 1818 MHz to 1893 MHz (V_{TUNE} 1.8 V to 3.7 V with Sirenza 1843T VCO)

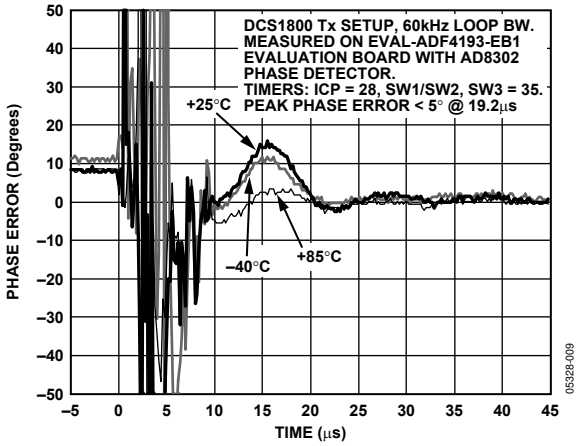

Figure 14. Phase Settling Transient for a 75 MHz Jump from 1893 MHz to 1818 MHz (V_{TUNE} = 3.7 V to 1.8 V with Sirenza 1843T VCO)

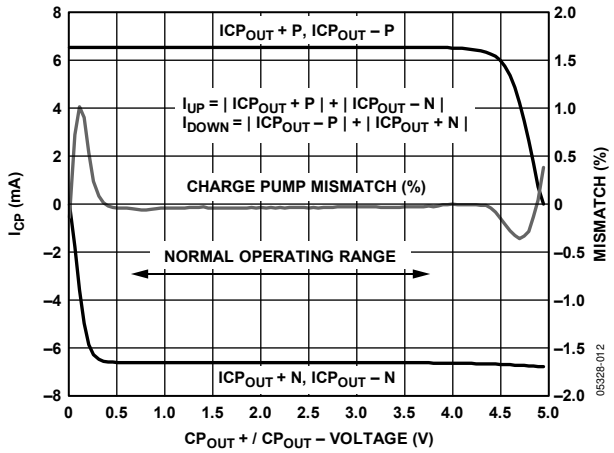

Figure 12. Differential Charge Pump Output Compliance Range and Charge Pump Mismatch with $V_P1 = V_P2 = 5$ V

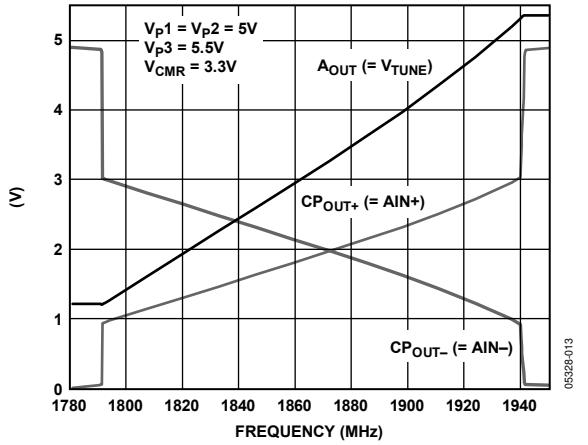

Figure 15. Tuning Range with a Sirenza 1843T VCO and a 5.5 V Differential Amplifier Power Supply Voltage

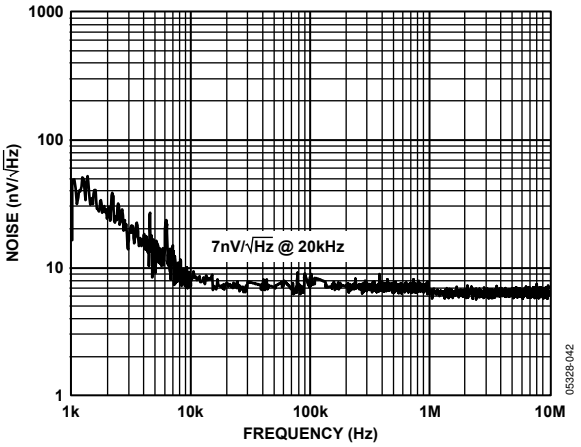

Figure 16. Voltage Noise Density Measured at the Differential Amplifier Output

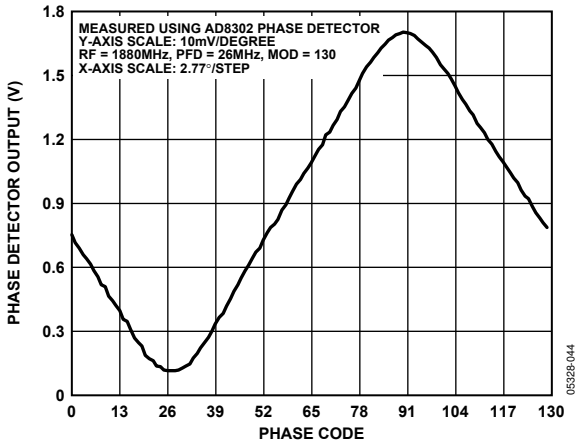

Figure 18. Detected RF Output Phase for Phase Code Sweep from 0 to MOD

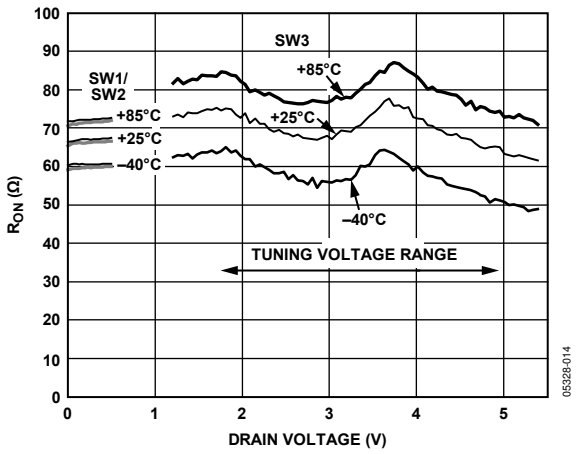

Figure 17. On Resistance of Loop Filter Switches SW1/SW2 and SW3

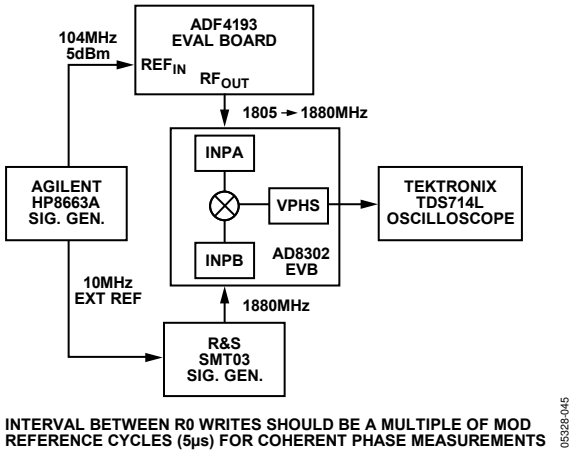

Figure 19. Test Setup for Phase Lock Time Measurement

THEORY OF OPERATION

The ADF4193 is targeted at GSM base station requirements, specifically to eliminate the need for ping-pong solutions. It works based on fast lock, using a wide loop bandwidth during a frequency change and narrowing the loop bandwidth once frequency lock is achieved. Widening the loop bandwidth is achieved by increasing the charge pump current. Switches are included to change the loop filter component values to maintain stability with the changing charge pump current. The narrow loop bandwidth ensures that phase noise and spur specifications are met. A differential charge pump and loop filter topology are used to ensure that the fast lock time benefit from widening the loop bandwidth is maintained when the loop is restored to narrow bandwidth mode for normal operation.

REFERENCE INPUT SECTION

The reference input stage is shown in Figure 20. Switches S1 and S2 are normally closed, and S3 is normally open. During power-down, S3 is closed, and S1 and S2 are opened to ensure that there is no loading of the REF_{IN} pin. The falling edge of REF_{IN} is the active edge at the positive edge triggered PFD.

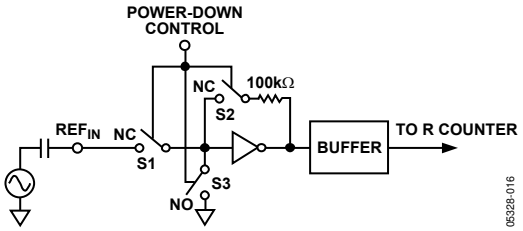

Figure 20. Reference Input Stage

R Counter and Doubler

The 4-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). A toggle flip-flop can be optionally inserted after the R counter to give a further divide-by-2. Using this option has the additional advantage of ensuring that the PFD reference clock has a 50/50 mark-space ratio. This ratio gives the maximum separation between the fast lock timer clock, which is generated off the falling edge of the PFD reference, and the rising edge, which is the active edge in the PFD. It is recommended that this toggle flip-flop be enabled for all even R divide values greater than 2. It must be enabled if dividing down a REF_{IN} frequency that is greater than 120 MHz.

An optional doubler before the 4-bit R counter can be used for low REF_{IN} frequencies, up to 20 MHz. With these programmable options, reference division ratios from 0.5 to 30 between REF_{IN} and the PFD are possible.

RF INPUT STAGE

The RF input stage is shown in Figure 21. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler. Two prescaler options are selectable: a 4/5 and an 8/9. The 8/9 prescaler is selected for N divider values greater than 80.

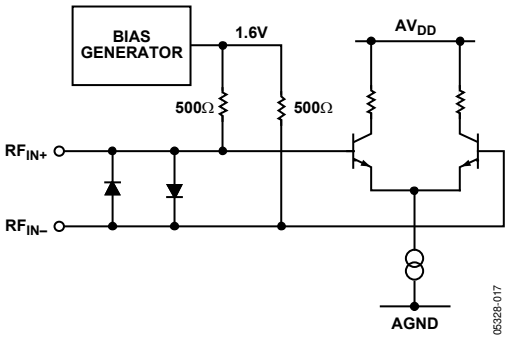

Figure 21. RF Input Stage

RF N Divider

The RF N divider allows a fractional division ratio in the PLL feedback path. The integer and fractional parts of the division are programmed using separate registers, as shown in Figure 22 and described in the INT, FRAC, and MOD Relationship section. Integer division ratios from 26 to 255 are allowed and a third-order, Σ-Δ modulator interpolates the fractional value between the integer steps.

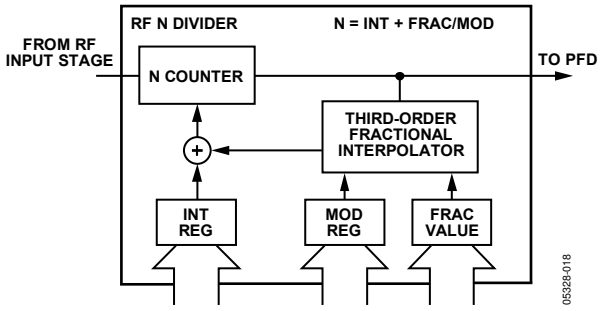

Figure 22. Fractional-N Divider

INT, FRAC, and MOD Relationship

The INT, FRAC, and MOD values, programmed through the serial interface, make it possible to generate RF output frequencies that are spaced by fractions of the PFD reference frequency. The N divider value, shown inside the brackets of the following equation for the RF VCO frequency (RF_{OUT}), is made up of an integer part (INT) and a fractional part (FRAC/MOD):

$$RF_{OUT} = F_{PFD} \times [INT + (FRAC/MOD)]$$

where:

RF_{OUT} is the output frequency of the external VCO.
F_{PFD} is the PFD reference frequency.

The value of MOD is chosen to give the desired channel step with the available reference frequency. Thereafter, program the INT and FRAC words for the desired RF output frequency. See the Worked Example section for more information.

PFD and Charge Pump

The PFD takes inputs from the R divider and N divider and produces up and down outputs with a pulse width difference proportional to the phase difference between the inputs. The charge pump outputs a net up or down current pulse of a width equal to this difference, to pump up or pump down the voltage that is integrated onto the loop filter, which in turn increases or decreases the VCO output frequency. If the N divider phase lags the R divider phase, a net up current pulse is produced that increases the VCO frequency (and thus the phase). If the N divider phase leads the R divider edge, then a net down pulse is produced to reduce the VCO frequency and phase. Figure 23 is a simplified schematic of the PFD and charge pump. The charge pump is made up of an array of 64 identical cells, each of which is fully differential. All 64 cells are active during fast lock, but only one is active during normal operation. Because a single-ended control voltage is required to tune the VCO, an on-chip, differential-to-single-ended amplifier is provided for this purpose. In addition, because the phase-lock loop only controls the differential voltage generated across the charge pump outputs, an internal common-mode feedback (CMFB) loop biases the charge pump outputs at a common-mode voltage of approximately 2 V.

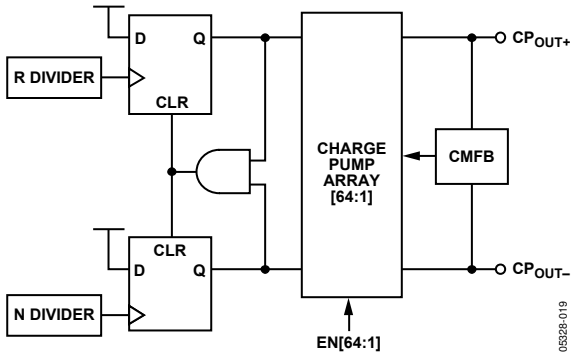

Figure 23. PFD and Differential Charge Pump Simplified Schematic

Differential Charge Pump

The charge pump cell (see Figure 24) has a fully differential design for best up-to-down current matching. Good matching is essential to minimize the phase offset created when switching the charge pump current from its high value (in fast lock mode) to its nominal value (in normal mode).

To pump up, the up switches are on and PMOS current is sourced out through CP_{OUT+}; this increases the voltage on the external loop filter capacitors connected to CP_{OUT+}. Similarly, the NMOS current sink on CP_{OUT-} decreases the voltage on the external loop filter capacitors connected to CP_{OUT-}. Therefore, the differential voltage between CP_{OUT+} and CP_{OUT-} increases. To pump down, PMOS current sources out through CP_{OUT-} and NMOS current sinks in through CP_{OUT+}, which decreases the (CP_{OUT+}, CP_{OUT-}) differential voltage. The charge pump up/down matching is improved by an order of magnitude over the conventional single-ended charge pump that depended on the matching of two different device types. The up/down matching in this structure depends on how a PMOS matches a PMOS and an NMOS matches an NMOS.

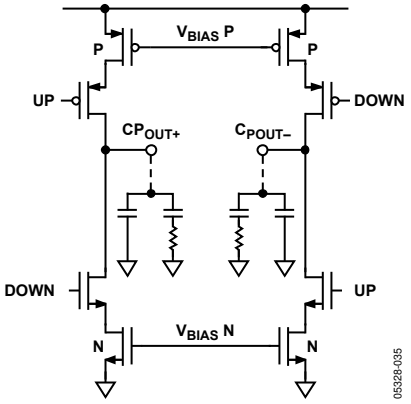

Figure 24. Differential Charge Pump Cell with External Loop Filter Components

Fast Lock Timeout Counters

Timeout counters, clocked at one quarter the PFD reference frequency, are provided to precisely control the fast locking operation (see Figure 25). Whenever a new frequency is programmed, the fast lock timers start and the PLL locks into wide BW mode with the 64 identical 100 µA charge pump cells active (6.4 mA total). When the ICP counter times out, the charge pump current is reduced to 1× by deselecting cells in binary steps over the next six timer clock cycles, until just one 100 µA cell is active. The charge pump current switching from 6.4 mA to 100 µA equates to an 8-to-1 change in loop bandwidth. The loop filter must be changed to ensure stability when this happens. That is the job of the SW1, SW2, and SW3 switches. The application circuit (shown in Figure 36) shows how they can be used to reconfigure the loop filter time constants. The application circuits close to short out external loop filter resistors during fast lock and open when their counters time out to restore the filter time constants to their normal values for the 100 µA charge pump current. Because it takes six timer clock cycles to reduce the charge pump current to 1×, it is recommended that both switch timers be programmed to the value of the ICP timer + 7.

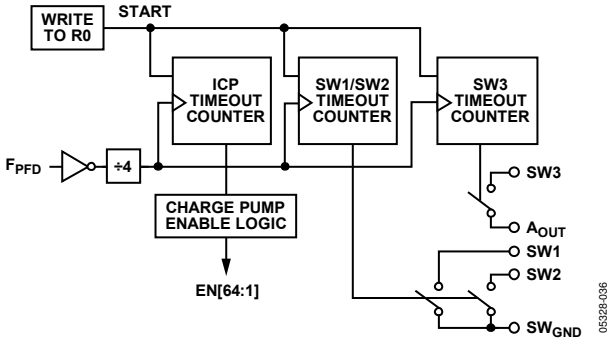

Figure 25. Fast Lock Timeout Counters

Differential Amplifier

The internal, low noise, differential-to-single-ended amplifier is used to convert the differential charge pump output to a single-ended control voltage for the tuning port of the VCO. Figure 26 shows a simplified schematic of the differential amplifier. The output voltage is equal to the differential voltage, offset by the voltage on the CMR pin, according to

$$V_{AOUT} = (V_{AIN+} - V_{AIN-}) + V_{CMR}$$

The CMR offset voltage is internally biased to three-fifths of V_P3, the differential amplifier power supply voltage, as shown in Figure 26. Connect a 0.1 µF capacitor to ground to the CMR pin to roll off the thermal noise of the biasing resistors.

As can be seen in Figure 15, the differential amplifier output voltage behaves according to the previous equation over a 4 V range from approximately 1.2 V minimum up to V_P3 − 0.3 V. However, fast settling is guaranteed only over a tuning voltage range from 1.8 V up to V_P3 − 0.8 V. This is to allow sufficient room for overshoot in the PLL frequency settling transient.

Noise from the differential amplifier is suppressed inside the PLL bandwidth. For loop bandwidths >20 kHz, the 1/f noise has a negligible effect on the PLL output phase noise. Outside the loop bandwidth, the differential amplifier's noise FM modulates the VCO. The passive filter network following the differential amplifier, shown in Figure 36, suppresses this noise contribution to below the VCO noise from offsets of 400 kHz and above. This network has a negligible effect on lock time because it is bypassed when SW3 is closed while the loop is locking.

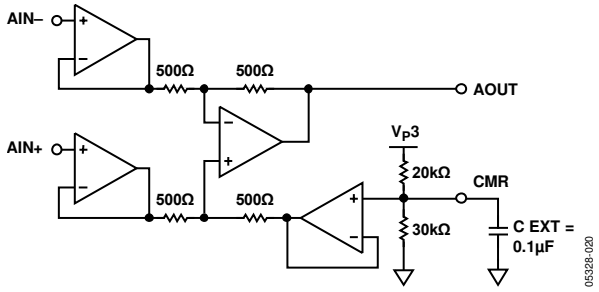

Figure 26. Differential Amplifier Block Diagram

MUX_{OUT} and Lock Detect

The output multiplexer on the ADF4193 allows the user to access various internal points on the chip. The state of MUX_{OUT} is controlled by M4 to M1 in the MUX register. Figure 35 shows the full truth table. Figure 27 shows the MUX_{OUT} section in block diagram form.

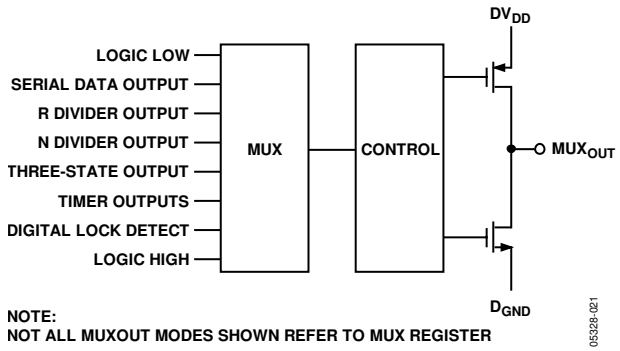

Figure 27. MUX_{OUT} Circuit

Lock Detect

MUX_{OUT} can be programmed to provide a digital lock detect signal. Digital lock detect is active high. Its output goes high if there are 40 successive PFD cycles with an input error of less than 3 ns. For reliable lock detect operation with RF frequencies <2 GHz, it is recommended that this threshold be increased to 10 ns by programming Register R6. The digital lock detect goes low again when a new channel is programmed or when the error at the PFD input exceeds 30 ns for one or more cycles.

Input Shift Register

The ADF4193 serial interface section includes a 24-bit input shift register. Data is clocked in MSB first on each rising edge of CLK. Data from the shift register is latched into one of eight control registers, R0 to R7, on the rising edge of latch enable (LE). The destination register is determined by the state of the three control bits (Control Bit C3, Control Bit C2, and Control Bit C1) in the shift register. The three LSBs are Bit DB2, Bit DB1, and Bit DB0, as shown in the timing diagram of Figure 2. The truth table for these bits is shown in Table 5. Figure 28 shows a summary of how the registers are programmed.

Table 5. C3, C2, and C1 Truth Table

Control Bits				
C3	C2	C1	Name	Register
0	0	0	FRAC/INT	R0
0	0	1	MOD/R	R1
0	1	0	Phase	R2
0	1	1	Function	R3
1	0	0	Charge Pump	R4
1	0	1	Power-Down	R5
1	1	0	Mux	R6
1	1	1	Test Mode	R7

REGISTER MAP

FRAC/INT REGISTER (R0)

RESERVED	8-BIT RF INT VALUE								12-BIT RF FRAC VALUE												CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3 (0)	C2 (0)	C1 (0)

MOD/R REGISTER (R1)

DBB CP ADJ	DBB REF/2	RESERVED	PRESCALER	DBB DOUBLER ENABLE	DBB 4-BIT RF R COUNTER				DBB 12-BIT MODULUS												CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
F5	F4	0	F2	F1	R4	R3	R2	R1	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C3 (0)	C2 (0)	C1 (1)

PHASE REGISTER (R2)

RESERVED	DBB 12-BIT PHASE												CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C3 (0)	C2 (1)	C1 (0)

FUNCTION REGISTER (R3)

RESERVED										CPO GND	RESERVED	PFD POLARITY	CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1	F3	1	F1	C3 (0)	C2 (1)	C1 (1)

CHARGE PUMP REGISTER (R4)

RESERVED										9-BIT TIMEOUT COUNTER									TIMER SELECT		CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1	C9	C8	C7	C6	C5	C4	C3	C2	C1	F2	F1	C3 (1)	C2 (0)	C1 (0)

POWER-DOWN REGISTER (R5)

PD DIFF AMP	PD CHARGE PUMP	CP 3-STATE	COUNTER RESET	CONTROL BITS		
DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
F5	F4	F3	F2	F1	C3 (1)	C2 (0)	C1 (1)

MUX REGISTER (R6)

SIGMA-DELTA AND LOCK DETECT MODES				RESERVED					MUX_{OUT}				CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
M13	M12	M11	M10	0	0	0	0	0	M4	M3	M2	M1	C3 (1)	C2 (1)	C1 (0)

TEST MODE REGISTER (R7)

RESERVED													CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	0	0	0	C3 (1)	C2 (1)	C1 (1)

DBB = DOUBLE BUFFERED BIT(S)

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Figure 28. Register Map

FRAC/INT REGISTER (R0)

RESERVED	8-BIT RF INT VALUE								12-BIT RF FRAC VALUE												CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	N8	N7	N6	N5	N4	N3	N2	N1	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C3 (0)	C2 (0)	C1 (0)

F12	F11	F10		F3	F2	F1	FRACTIONAL VALUE (FRAC)
0	0	0	.....	0	0	0	0
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

0 = < FRAC < MOD

N8	N7	N6	N5	N4	N3	N2	N1	INTEGER VALUE (INT)
0	0	0	1	1	0	1	0	26
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.
1	1	1	1	1	1	1	1	255

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Figure 29. FRAC/INT Register (R0)

R0, the FRAC/INT register, is used to program the synthesizer output frequency. On the next PFD cycle following a write to R0, the N divider section is updated with the new INT and FRAC values. At the same time, the PLL automatically enters fast lock mode and the charge pump current is increased to its maximum value and stays at this value until the ICP timeout counter times out, and switches SW1, SW2, and SW3 closed and remains closed until the SW1, SW2, and SW3 timeout counters time out.

Once all registers are programmed during the initialization sequence (see Table 8), all that is required thereafter to program a new channel is a write to R0. However, as described in the Programming section, it can also be desirable to program R1 and R2 register settings on a channel-by-channel basis. These settings are double buffered by the write to R0. This means that while the data is loaded through the serial interface on the respective R1 and R2 write cycles, the synthesizer is not updated with their data until the next write to Register R0.

Control Bits

The three LSBs, Control Bit C3, Control Bit C2, and Control Bit C1, should be set to 0, 0, 0, respectively, to select R0, the FRAC/INT register.

Reserved Bit

Bit DB23 is reserved and must be set to 0.

8-Bit INT Value

These eight bits set the INT value, which determines the integer part of the feedback division factor. All integer values from 26 to 255 are allowed. See the Worked Example section.

12-Bit FRAC Value

The 12 FRAC bits set the numerator of the fraction that is input to the Σ-Δ modulator. This, along with INT, specifies the new frequency channel that the synthesizer locks to, as shown in the Worked Example section. FRAC values from 0 to MOD − 1 cover channels over a frequency range equal to the PFD reference frequency.

MOD/R REGISTER (R1)

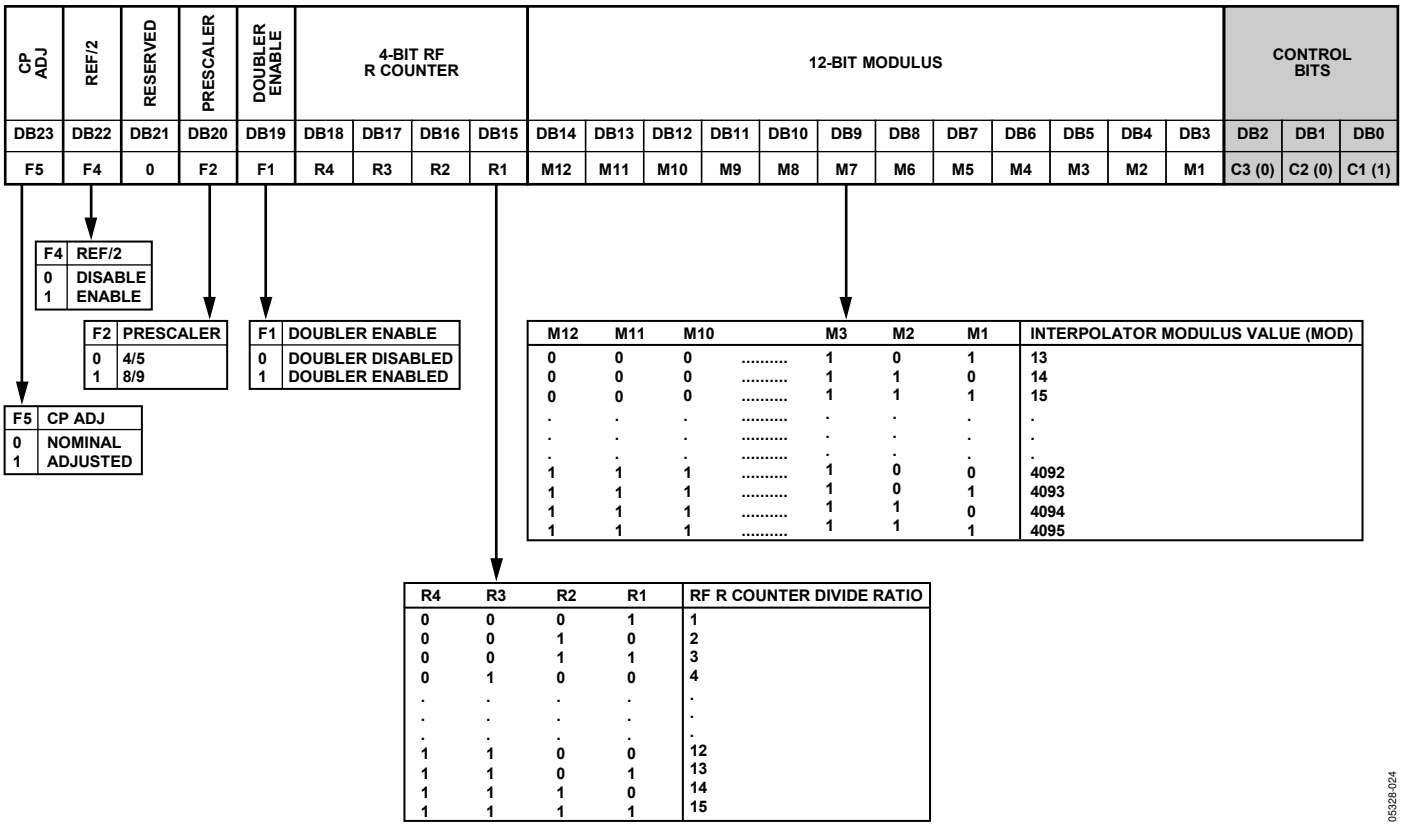

Figure 30. MOD/R Register (R1)

This register is used to set the PFD reference frequency and the channel step size, which is determined by the PFD frequency divided by the fractional modulus. Note that the MOD, R counter, REF/2, CP ADJ, and doubler enable bits are double buffered. They do not take effect until the next write to R0 (FRAC/INT register) is complete.

Control Bits

With C3, C2, and C1 set to 0, 0, 1, respectively, the MOD/R register (R1) is programmed.

CP ADJ

When this bit is set to 1, the charge pump current is scaled up 25% from its nominal value on the next write to R0. When this bit is set to 0, the charge pump current stays at its nominal value on the next write to R0. See the Programming section for more information on how this feature can be used.

REF/2

Setting this bit to 1 inserts a divide-by-2, toggle flip-flop between the R counter and PFD, which extends the maximum REF_{IN} input rate.

Reserved Bit

Reserved Bit DB21 must be set to 0.

Doubler Enable

Setting this bit to 1 inserts a frequency doubler between REF_{IN} and the 4-bit R counter. Setting this bit to 0 bypasses the doubler.

4-Bit RF R Counter

It allows the REF_{IN} frequency to be divided down to produce the reference clock to the PFD. All integer values from 1 to 15 are allowed. See the Worked Example section.

12-Bit Interpolator Modulus

For a given PFD reference frequency, the fractional denominator or modulus sets the channel step resolution at the RF output. All integer values from 13 to 4095 are allowed. See the Programming section for additional information and guidelines for selecting the value of MOD.

PHASE REGISTER (R2)

RESERVED	12-BIT PHASE												CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C3 (0)	C2 (1)	C1 (0)

P12	P11	P10		P3	P2	P1	PHASE VALUE[1]
0	0	0	.....	0	0	0	0
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	4092
1	1	1	.....	1	0	1	4093
1	1	1	.....	1	1	0	4094
1	1	1	.....	1	1	1	4095

[1]0 = < PHASE VALUE < MOD

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Figure 31. Phase Register (R2)

12-Bit Phase

The phase word sets the seed value of the Σ-Δ modulator. It can be programmed to any integer value from 0 to MOD. As the phase word is swept from 0 to MOD, the phase of the VCO output sweeps over a 360° range in steps of 360°/MOD.

Note that the phase bits are double buffered. They do not take effect until the LE of the next write to R0 (FRAC/INT register). Therefore, if it is desired to change the phase of the VCO output frequency, it is necessary to rewrite the INT and FRAC values to R0, following the write to R2.

The output of a fractional-N PLL can settle to any one of the MOD possible phase offsets with respect to the reference, where MOD is the fractional modulus.

If it is desired to keep the output at the same phase offset with respect to the reference, each time that particular output frequency is programmed, then the interval between writes to R0 must be an integer multiple of MOD reference cycles.

If it is desired to keep the outputs of two ADF4193-based synthesizers phase coherent with each other, but not necessarily with their common reference, then it is only required to ensure that the write to R0 on both chips is performed during the same reference cycle. The interval between R0 writes in this case does not have to be an integer multiple of the MOD cycles.

Reserved Bit

The reserved bit, Bit DB15, should be set to 0.

FUNCTION REGISTER (R3)

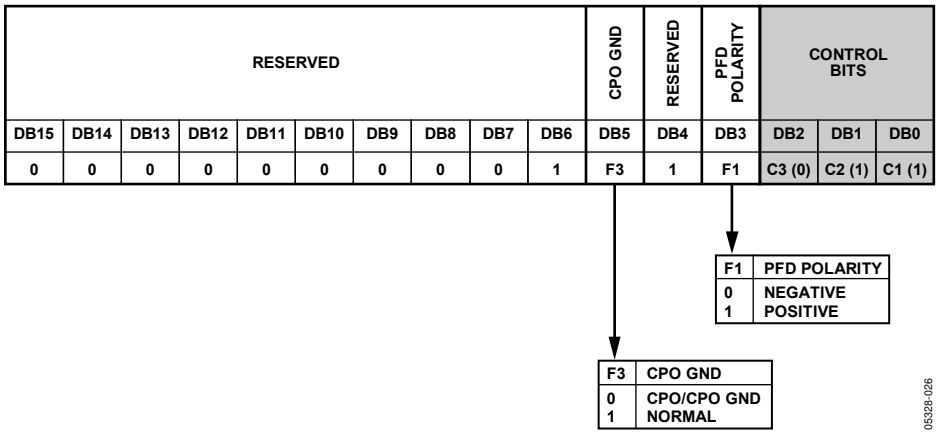

Figure 32. Function Register (R3)

R3, the function register (C3, C2, C1 set to 0, 1, 1, respectively), only needs to be programmed during the initialization sequence (see Table 8).

CPO GND

When the CPO GND bit is low, the charge pump outputs are internally pulled to ground. This is invoked during the initialization sequence to discharge the loop filter capacitors. For normal operation, this bit should be high.

PFD Polarity

This bit should be set to 1 for positive polarity and set to 0 for negative polarity.

Reserved Bits

The Bit DB15 to Bit DB6 are reserved bits and should be programmed to hex code 001, and Reserved Bit DB4 should be set to 1.

CHARGE PUMP REGISTER (R4)

RESERVED										9-BIT TIMEOUT COUNTER									TIMER SELECT		CONTROL BITS		
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1	C9	C8	C7	C6	C5	C4	C3	C2	C1	F2	F1	C3 (1)	C2 (0)	C1 (0)

F2	F1	TIMER SELECT
0	0	SW1/SW2
0	1	SW3
1	0	ICP
1	1	NOT USED

C9	C8	C7		C3	C2	C1	TIMEOUT COUNTER	xPFD CYCLES	DELAY µs[1]
0	0	0	.....	0	0	0	0	0	0
0	0	0	.....	0	0	1	1	4	0.15
0	0	0	.....	0	1	0	2	8	0.30
0	0	0	.....	0	1	1	3	12	0.46
.	.	.	.....	.	.	.	.	.	.
.	.	.	.....	.	.	.	.	.	.
.	.	.	.....	.	.	.	.	.	.
1	1	1	.....	1	0	0	508	2032	78.15
1	1	1	.....	1	0	1	509	2036	78.30
1	1	1	.....	1	1	0	510	2040	78.46
1	1	1	.....	1	1	1	511	2044	78.61

[1]DELAY WITH 26MHz PFD

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Figure 33. Charge Pump Register (R4)

Reserved Bits

Bit DB23 to Bit DB14 are reserved and should be set to hex code 001 for normal operation.

9-Bit Timeout Counter

These bits are used to program the fast lock timeout counters. The counters are clocked at one-quarter the PFD reference frequency, therefore, their time delay scales with the PFD frequency according to

$$Delay(s) = (Timeout\ Counter\ Value \times 4)/(PFD\ Frequency)$$

For example, if 35 were loaded with timer select (00) with a 13 MHz PFD, then SW1/SW2 would be switched after

$$(35 \times 4)/13\ MHz = 10.8\ \mu s$$

Timer Select

These two address bits select the timeout counter to be programmed. Note that to set up the ADF4193 correctly requires setup of these three timeout counters; therefore, three writes to this register are required in the initialization sequence. Table 6 shows example values for a GSM Tx synthesizer with a 60 kHz final loop BW. See the Applications section for more information.

Table 6. Recommended Values for a GSM Tx LO

Timer Select	Timeout Counter	Value	Time (µs) with PFD = 13 MHz
10	ICP	28	8.6
01	SW1/2	35	10.8
00	SW3	35	10.8

On each write to R0, the timeout counters start. Switch SW3 closes until the SW3 counter times out. Similarly, switches SW1/SW2 close until the SW1/SW2 counter times out. When the ICP counter times out, the charge pump current is ramped down from 64× to 1× in six binary steps. It is recommended that the SW1, SW2, and SW3 timeout counter values are set equal to the ICP timeout counter value plus 7, as in the example of Table 6.

POWER-DOWN REGISTER (R5)

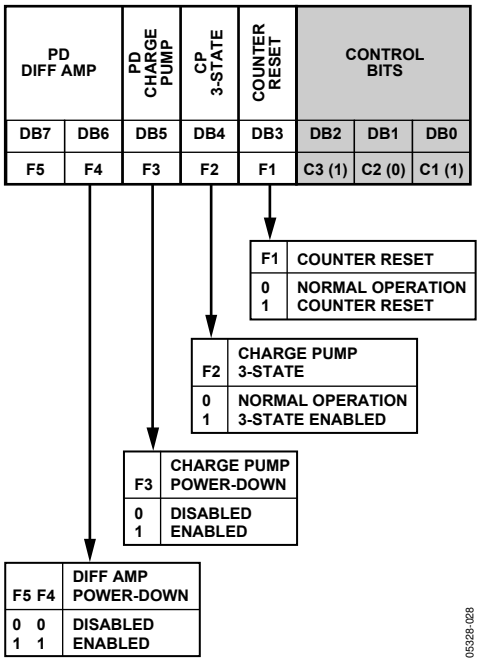

Figure 34. Power-Down Register (R5)

R5, the power-down register (C3, C2, C1 set to 1, 0, 1, respectively) can be used to software power down the PLL and differential amplifier sections. After power is initially applied, there must be writes to R5 to clear the power-down bits and to R2, R1, and R0 before the ADF4193 comes out of power-down.

Power-Down Differential Amplifier

When Bit DB6 and Bit DB7 are set high, the differential amplifier is put into power-down. When Bit DB6 and Bit DB7 are set low, normal operation is resumed.

Power-Down Charge Pump

Setting Bit DB5 high activates a charge pump power-down and the following events occur:

- All active dc current paths are removed, except for the differential amplifier.
- The R and N divider counters are forced to their load state conditions.
- The charge pump is powered down with its outputs in three-state mode.
- The digital lock detect circuitry is reset.
- The RF_{IN} input is debiased.
- The reference input buffer circuitry is disabled.
- The serial interface remains active and capable of loading and latching data.

For normal operation, Bit DB5 should be set to 0, followed by a write to R0.

CP Three-State

When this bit is set high, the charge pump outputs are put into three-state. With the bit set low, the charge pump outputs are enabled.

Counter Reset

When this bit is set to 1, the counters are held in reset. For normal operation, this bit should be 0, followed by a write to R0.

MUX REGISTER (R6)

SIGMA-DELTA AND LOCK DETECT MODES				RESERVED					MUX_{OUT}				CONTROL BITS		
DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
M13	M12	M11	M10	0	0	0	0	0	M4	M3	M2	M1	C3 (1)	C2 (1)	C1 (0)

M13	M12	M11	M10	SIGMA-DELTA MODES
0	0	0	0	INIT STATE, DITHER OFF, 3ns LOCK DETECT THRESHOLD
0	0	1	1	DITHER ON
1	0	0	1	10ns LOCK DETECT THRESHOLD
ALL OTHER STATES				RESERVED

M4	M3	M2	M1	MUX_{OUT}
0	0	0	0	3-STATE
0	0	0	1	DIGITAL LOCK DETECT
0	0	1	0	N DIVIDER OUTPUT
0	0	1	1	LOGIC HIGH
0	1	0	0	R COUNTER
0	1	0	1	RESERVED
0	1	1	0	SERIAL DATA OUT
0	1	1	1	LOGIC LOW
1	0	0	0	R DIVIDER/2 OUTPUT
1	0	0	1	N DIVIDER/2 OUTPUT
1	0	1	0	RESERVED
1	0	1	1	RESERVED
1	1	0	0	ICP TIMEOUT SIGNAL
1	1	0	1	SW1/2 TIMEOUT SIGNAL
1	1	1	0	SW3 TIMEOUT SIGNAL
1	1	1	1	RESERVED

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Figure 35. MUX Register (R6)

With C3, C2, and C1 set to 1, 1, 0, respectively, the MUX register is programmed.

Σ-Δ and Lock Detect Modes

Bit DB15 to Bit DB12 are used to reconfigure certain PLL operating modes. In the initialization sequence after power is applied to the chip, the four bits must first be programmed to all zeros. This initializes the PLL to a known state with dither off in the Σ-Δ modulator and a 3 ns PFD error threshold in the lock detect circuit.

To turn on dither in the Σ-Δ modulator, an additional write should be made to Register R6 to program bits [DB15:DB12] = [0011]. However, for lowest noise operation, it is best to leave dither off.

To change the lock detect threshold from 3 ns to 10 ns, a separate write to R6 should be performed to program bits [DB15:DB12] = [1001]. This should be done for reliable lock detect operation when the RF frequency is <2 GHz.

A write to R6 that programs bits [DB15:DB12] = [0000] returns operation to the default state with both dither off and a 3 ns lock detect threshold.

Reserved Bits

The reserved bits must all be set to 0 for normal operation.

MUX_{OUT} Modes

These bits control the on-chip multiplexer. See Figure 35 for the truth table. This pin is useful for diagnosis because it allows the user to look at various internal points of the chip, such as the R divider and INT divider outputs.

In addition, it is possible to monitor the programmed timeout counter intervals on MUX_{OUT}. For example, if the ICP timeout counter was programmed to 65 (with a 26 MHz PFD), then following the next write to R0, a pulse width of 10 µs would be observed on the MUX_{OUT} pin.

Digital lock detect is available via the MUX_{OUT} pin.

PROGRAMMING

The ADF4193 can synthesize output frequencies with a channel step or resolution that is a fraction of the input reference frequency. For a given input reference frequency and a desired output frequency step, the first choice to make is the PFD reference frequency and the MOD. Once these are chosen, the desired output frequency channels are set by programming the INT and FRAC values.

WORKED EXAMPLE

In this example of a GSM900 RX system, it is required to generate RF output frequencies with channel steps of 200 kHz. A 104 MHz reference frequency input (REF_{IN}) is available. The R divider setting that set the PFD reference is shown in Equation 1.

$$F_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (1)$$

where:

REF_{IN} is the input reference frequency.

D is the doubler enable bit (0 or 1).

R is the 4-bit R counter code (0…15).

T is the REF/2 bit (0 or 1).

A PFD frequency of 26 MHz is chosen and the following settings are programmed to give an R divider value of 4:

Doubler enable = 0

R = 2

REF/2 = 1

Next, the modulus is chosen to allow fractional steps of 200 kHz.

$$MOD = 26 \text{ MHz}/200 \text{ kHz} = 130 \quad (2)$$

Once the channel step is defined, the following equation shows how output frequency channels are programmed:

$$RF_{OUT} = [INT + (FRAC/MOD)] \times [F_{PFD}] \quad (3)$$

where:

RF_{OUT} is the desired RF output frequency.

INT is the integer part of the division.

$FRAC$ is the numerator part of the fractional division.

MOD is the modulus or denominator part of the fractional division.

For example, the frequency channel at 962.4 MHz is synthesized by programming the following values:

INT = 37

FRAC = 2

SPUR MECHANISMS

The Fractional Spurs, Integer Boundary Spurs, and Reference Spurs sections describe the three different spur mechanisms that arise with a fractional-N synthesizer and how the ADF4193 can be programmed to minimize them.

Fractional Spurs

The fractional interpolator in the ADF4193 is a third-order, Σ-Δ modulator (SDM) with a modulus (MOD) that is programmable to any integer value from 13 to 4095. If dither is enabled, then the minimum allowed value of MOD is 50. The SDM is clocked at the PFD reference rate (f_{PFD}) that allows PLL output frequencies to be synthesized at a channel step resolution of f_{PFD}/MOD.

With dither turned off, the quantization noise from the Σ-Δ modulator appears as fractional spurs. The interval between spurs is f_{PFD}/L, where L is the repeat length of the code sequence in the digital Σ-Δ modulator. For the third-order modulator used in the ADF4193, the repeat length depends on the value of MOD, as shown in Table 7.

Table 7. Fractional Spurs with Dither Off

Condition (Dither Off)	Repeat Length	Spur Interval
If MOD is divisible by 2, but not 3	2 × MOD	Channel step/2
If MOD is divisible by 3, but not 2	3 × MOD	Channel step/3
If MOD is divisible by 6	6 × MOD	Channel step/6
Otherwise	MOD	Channel step

With dither enabled, the repeat length is extended to 221 cycles, regardless of the value of MOD, which makes the quantization error spectrum look like broadband noise. This can degrade the in-band phase noise at the PLL output by as much as 10 dB. Therefore, for the lowest noise, dither off is a better choice, particularly when the final loop BW is low enough to attenuate even the lowest frequency fractional spur. The wide loop bandwidth range available with the ADF4193 makes this possible in most applications.

Integer Boundary Spurs

Another mechanism for fractional spur creation involves interactions between the RF VCO frequency and the reference frequency. When these frequencies are not integer related, spur sidebands appear on the VCO output spectrum at an offset frequency that corresponds to the beat note or difference frequency between an integer multiple of the reference and the VCO frequency.

These spurs are attenuated by the loop filter and are more noticeable on channels close to integer multiples of the reference where the difference frequency can be inside the loop bandwidth, thus the name integer boundary spurs.

The 8:1 loop bandwidth switching ratio of the ADF4193 makes it possible to attenuate all spurs to sufficiently low levels for most applications. The final loop BW can be chosen to ensure that all spurs are far enough out of band while meeting the lock time requirements with the 8× bandwidth boost.

The ADF4193 programmable modulus and R divider can also be used to avoid integer boundary channels. This option is described in the Avoiding Integer Boundary Channels section.

Reference Spurs

Reference spurs are generally not a problem in fractional-N synthesizers as the reference offset is far outside the loop bandwidth. However, any reference feedthrough mechanism that bypasses the loop can cause a problem. One such mechanism is feedthrough of low levels of on-chip reference switching noise out through the RF_{IN} pin back to the VCO, resulting in reference spur levels as high as –90 dBc. These spurs can be suppressed below –110 dBc by inserting sufficient reverse isolation, for example, through an RF buffer between the VCO and RF_{IN} pin. In addition, care should be taken in the printed circuit board (PCB) layout to ensure that the VCO is well separated from the input reference to avoid a possible feedthrough path on the board.

POWER-UP INITIALIZATION

After applying power to the ADF4193, a 14-step sequence is recommended, as described in Table 8.

The divider and timer setting used in the example in Table 8 is for a DCS1800 Tx synthesizer with a 104 MHz REF_{IN} frequency.

Table 8. Power-Up Initialization Sequence

Step	Register Bits	Hex Codes	Description
1	R5 [7:0]	FD	Set all power-down bits.
2	R3 [15:0]	005B	PD polarity = 1, ground CP_{OUT+}/ CP_{OUT-}.
Wait 10 ms			Allow time for loop filter capacitors to discharge.
3	R7 [15:0]	0007	Clear test modes.
4	R6 [15:0]	000E	Initialize PLL modes, digital lock detect on MUX_{OUT}.
5	R6 [15:0]	900E	10 ns lock detect threshold, digital lock detect on MUX_{OUT}.
6	R4 [23:0]	004464	SW1/SW2 timer = 10.8 µs.
7	R4 [23:0]	00446C	SW3 timer = 10.8 µs.
8	R4 [23:0]	004394	ICP timer = 8.6 µs.
9	R2 [15:0]	00D2	Phase = 26.
10	R1 [23:0]	520209	8/9 prescaler, doubler disabled, R = 4, toggle FF on, MOD = 65.
11	R0 [23:0]	480140	INT = 144, FRAC = 40 for 1880 MHz output frequency.
12	R3 [15:0]	007B	PD polarity = 1, release CP_{OUT+}/ CP_{OUT-}.
13	R5 [7:0]	05	Clear all power-down bits.
14	R0 [23:0]	480140	INT = 144, FRAC = 40 for 1880 MHz output frequency.

The ADF4193 powers up after Step 13. It locks to the programmed channel frequency after Step 14.

CHANGING THE FREQUENCY OF THE PLL AND THE PHASE LOOK-UP TABLE

Once the ADF4193 is initialized, a write to Register R0 is all that is required to program a new output frequency. The N divider is updated with the values of INT and FRAC on the next PFD cycle following the LE edge that latches in the R0 word. However, the settling time and spurious performance of the synthesizer can be further optimized by modifying R1 and R2 register settings on a channel-by-channel basis. These settings are double buffered by the write to R0. This means that while the data is loaded in through the serial interface on the respective R1 and R2 write cycles, the synthesizer is not updated with their data until the next write to Register R0.

The R2 register can be used to digitally adjust the phase of the VCO output relative to the reference edge. The phase can be adjusted over the full 360° range at RF with a resolution of 360°/MOD. In most frequency synthesizer applications, the actual phase offset of the VCO output with respect to the reference is unknown and does not matter. In such applications, the phase adjustment capability of the R2 register can instead be used to optimize the settling time performance, as described in the Phase Look-Up Table section.

Phase Look-Up Table

The ADF4193's fast lock sequence is initiated following the write to Register R0. The fast lock timers are programmed so that after the PLL has settled in wide BW mode, the charge pump current is reduced and loop filter resistor switches are opened to reduce the loop BW. The reference cycle on which these events occur is determined by the values preprogrammed into the timeout counters.

Figure 10 and Figure 13 show that the lock time to final phase is dominated by the phase swing that occurs when the BW is reduced. Once the PLL has settled to final frequency and phase, in wide BW mode, this phase swing is the same, regardless of the size of the synthesizer's frequency jump. The amplitude of the phase swing is related to the current flowing through the loop filter zero resistors on the PFD reference cycle that the SW1/SW2 switches are opened. In an integer-N PLL, this current is zero once the PLL has settled. In a fractional-N PLL, the current is zero on average but varies from one reference cycle to the next, depending on the quantization error sequence output from the digital Σ-Δ modulator. Because the Σ-Δ modulator is all digital logic, clocked at the PFD reference rate, for a given value of MOD, the actual quantization error on any given reference cycle is determined by the value of FRAC and the PHASE word that the modulator is seeded with, following the write to R0. By choosing an appropriate value of PHASE, corresponding to the value of FRAC, that is programmed on the next write to R0, the size of the error current on the PFD reference cycle the SW1/SW2 switches opened, and thus the phase swing that occurs when the BW is reduced can be minimized.