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FEATURES

- RF output frequency range: 51.5625 MHz to 6600 MHz**
- Fractional-N synthesizer and integer-N synthesizer**
- High resolution 38-bit modulus**
- Low phase noise, voltage controlled oscillator (VCO)**
- Programmable divide by 1, 2, 4, 8, 16, 32, or 64 output**
- All power supplies: 3.3 V**
- Logic compatibility: 1.8 V**
- Programmable dual modulus prescaler of 4/5 or 8/9**
- Programmable output power level**
- RF output mute function**
- 3-wire serial interface**
- Analog and digital lock detect**

APPLICATIONS

- Wireless infrastructure (W-CDMA, TD-SCDMA, WiMAX, GSM, PCS, DCS, DECT)**
- Point to point/multipoint microwave links**
- Satellites/VSATs**
- Test equipment/instrumentation**
- Clock generation**

GENERAL DESCRIPTION

The **ADF4355-3** allows the implementation of fractional-N or integer-N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter and an external reference frequency. A series of frequency dividers at the output provide operation from 51.5625 MHz to 6600 MHz.

The **ADF4355-3** has an integrated VCO with a fundamental output frequency ranging from 3300 MHz to 6600 MHz. In addition, the VCO frequency is connected to divide by 1, 2, 4, 8, 16, 32, or 64 circuits that allow the user to generate RF output frequencies as low as 51.5625 MHz. For applications that require isolation, the RF output stage can be muted. The mute function is both pin- and software-controllable.

Control of all on-chip registers is through a simple 3-wire interface. The **ADF4355-3** operates with analog, digital, charge pump, and VCO power supplies ranging from 3.1515 V to 3.4485 V. The **ADF4355-3** also contains hardware and software power-down modes.

FUNCTIONAL BLOCK DIAGRAM

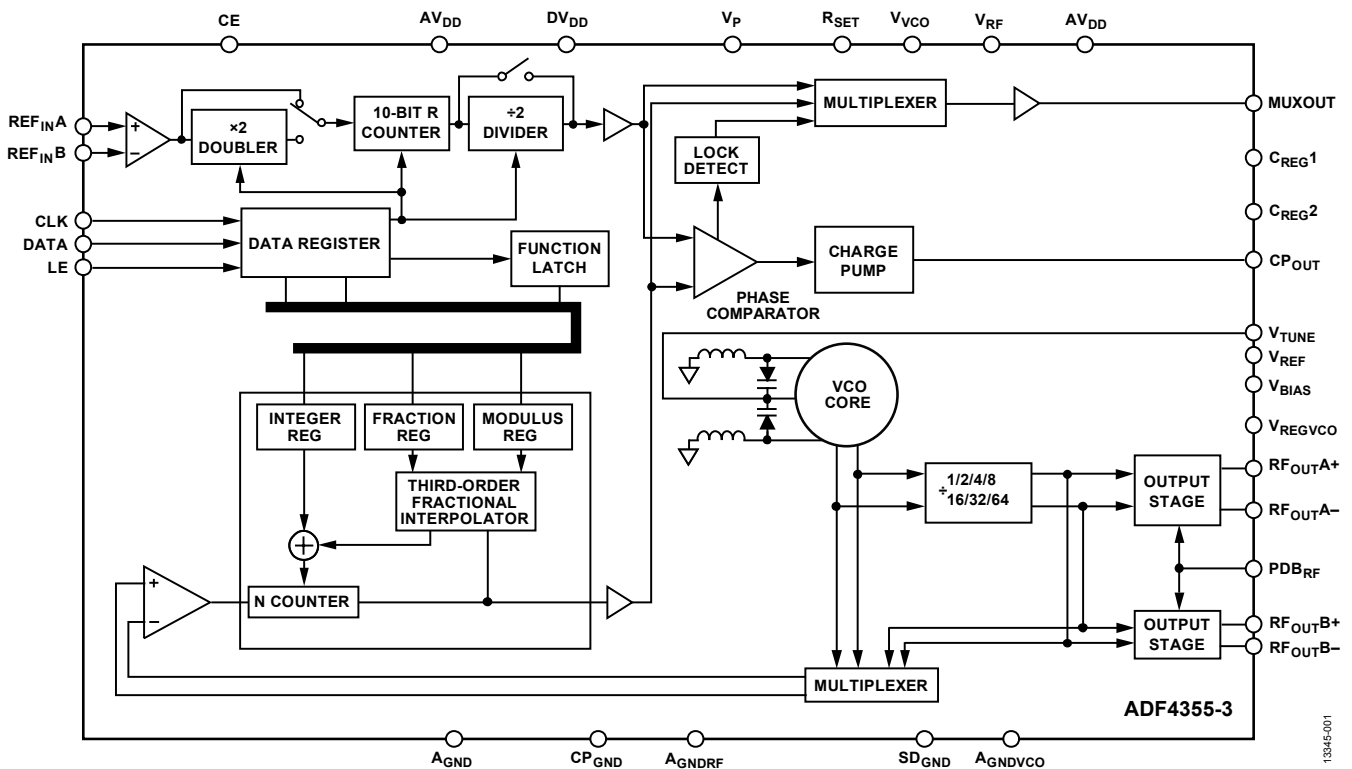


Figure 1.

Rev. A

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ADF4355-3* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADF4355-3 Evaluation Board

DOCUMENTATION

Data Sheet

- ADF4355-3: Microwave Wideband Synthesizer with Integrated VCO Data Sheet

User Guides

- UG-873: Evaluating the ADF4355-3 Fractional-N/Integer-N PLL Frequency Synthesizer

DESIGN RESOURCES

- ADF4355-3 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADF4355-3 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

1/16—Rev. 0 to Rev. A

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7/15—Revision 0: Initial Version

SPECIFICATIONS

$AV_{DD} = DV_{DD} = V_{RF} = V_P = V_{VCO} = V_{REGVCO} = 3.3 \text{ V} \pm 4.5\%$, $A_{GND} = CP_{GND} = A_{GNDVCO} = SD_{GND} = A_{GNDRF} = 0 \text{ V}$, $R_{SET} = 5.1 \text{ k}\Omega$, dBm referred to 50Ω , $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
REF_{INA}/REF_{INB} CHARACTERISTICS						
Input Frequency	REF _{IN}					For $f < 10 \text{ MHz}$, ensure that the slew rate $> 21 \text{ V}/\mu\text{s}$
Single-Ended Mode		10		250	MHz	
Differential Mode		10		600	MHz	
Doubler Enabled				100	MHz	Doubler is set in Register 4, Bit DB26
Input Sensitivity						
Single-Ended Mode		0.4		AV_{DD}	V p-p	REF _{INA} biased at $AV_{DD}/2$; ac coupling ensures $AV_{DD}/2$ bias
Differential Mode		0.4		1.8	V p-p	LVDS and LVPECL compatible, REF _{INA} /REF _{INB} biased at 2.1 V; ac coupling ensures 2.1 V bias
Input Capacitance						
Single-Ended Mode			6.9		pF	
Differential Mode			1.4		pF	
Input Current				± 60	μA	Single-ended reference programmed
				± 250	μA	Differential reference programmed
Phase Detector Frequency				125	MHz	
CHARGE PUMP (CP)						
Charge Pump Current, Sink/Source	I_{CP}					$R_{SET} = 5.1 \text{ k}\Omega$
High			4.8		mA	
Low			0.3		mA	
R_{SET} Range			5.1		k Ω	Fixed
Current Matching			3		%	$0.5 \text{ V} \leq V_{CP1} \leq V_P - 0.5 \text{ V}$
I_{CP} vs. V_{CP1}			3		%	$0.5 \text{ V} \leq V_{CP1} \leq V_P - 0.5 \text{ V}$
I_{CP} vs. Temperature			1.5		%	$V_{CP1} = 2.5 \text{ V}$
LOGIC INPUTS						
Input Voltage						1.8 V and 3.3 V compatible
High	V_{INH}	1.5		DV_{DD}	V	
Low	V_{INL}			0.6	V	
Input Current	I_{INH}/I_{INL}			± 1	μA	
Input Capacitance	C_{IN}		3.0		pF	
LOGIC OUTPUTS						
Output Voltage						
High	V_{OH}	$DV_{DD} - 0.4$	1.8		V	3.3 V output selected
		1.5			V	1.8 V output selected
Low	V_{OL}			0.4	V	$I_{OL}^2 = 500 \mu\text{A}$
Output High Current	I_{OH}			500	μA	
POWER SUPPLIES						
Analog Power	AV_{DD}	3.1515	3.3	3.4485	V	$3.3 \text{ V} \pm 4.5\%$
Digital Power, RF Supply, Charge Pump, and VCO Supply Voltage	$DV_{DD}, V_{RF}, V_P, V_{VCO}$		AV_{DD}			Voltages must equal AV_{DD}
Charge Pump Supply Current	I_P		3.1	5	mA	
$DI_{DD} + AI_{DD}^3$			66	75	mA	Supply current drawn by DV_{DD} plus supply current drawn by AV_{DD}
Output Dividers						See Table 6
VCO Supply Current	I_{VCO}		52	70	mA	
RF _{OUTA} \pm /RF _{OUTB} \pm Supply Current	$I_{RF_{OUTX}\pm}$		13/19/ 25/31	20/27/ 34/41	mA	RF output stage is programmable; RF _{OUTB+} /RF _{OUTB-} powered off
Low Power Sleep Mode			1500		μA	Hardware power-down
			1950		μA	Software power-down

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RF OUTPUT CHARACTERISTICS						
VCO Frequency Range		3300		6600	MHz	Fundamental VCO range
RF Output Frequency	f_{RF}	51.5625		6600	MHz	
VCO Sensitivity	K_v		63		MHz/V	
Frequency Pushing (Open-Loop)			22		MHz/V	
Frequency Pulling (Open-Loop)			0.54		MHz	Voltage standing wave ratio (VSWR) = 2:1
Harmonic Content						
Second			-27		dBc	Fundamental VCO output (RF _{OUTA+})
Third			-22		dBc	Divided VCO output (RF _{OUTA+})
Third			-20		dBc	Fundamental VCO output (RF _{OUTA+})
Third			-12		dBc	Divided VCO output (RF _{OUTA+})
RF Output Power ⁴			8		dBm	RF _{OUTA+} = 1 GHz. 7.5 nH inductor to V _{RF}
RF Output Power ⁴			3		dBm	RF _{OUTA+} /RF _{OUTA-} = 4.4 GHz. 7.5 nH inductor to V _{RF}
RF Output Power Variation			±1		dB	RF _{OUTA+} /RF _{OUTA-} = 4.4 GHz
Over Frequency			±3		dB	RF _{OUTA+} /RF _{OUTA-} = 1 GHz to 4.4 GHz
Level of Signal with Output Disabled			-60		dBm	RF _{OUTA+} /RF _{OUTA-} = 1 GHz, VCO = 4 GHz
Level of Signal with Output Disabled			-30		dBm	RF _{OUTA+} /RF _{OUTA-} = 4.4 GHz, VCO = 4.4 GHz
NOISE CHARACTERISTICS						
Fundamental VCO Phase Noise Performance						VCO noise in open-loop conditions
3.3 GHz Carrier			-113		dBc/Hz	100 kHz offset from 3.3 GHz carrier
3.3 GHz Carrier			-133		dBc/Hz	800 kHz offset from 3.3 GHz carrier
3.3 GHz Carrier			-135		dBc/Hz	1 MHz offset from 3.3 GHz carrier
3.3 GHz Carrier			-153		dBc/Hz	10 MHz offset from 3.3 GHz carrier
5.0 GHz Carrier			-110		dBc/Hz	100 kHz offset from 5.0 GHz carrier
5.0 GHz Carrier			-130		dBc/Hz	800 kHz offset from 5.0 GHz carrier
5.0 GHz Carrier			-132		dBc/Hz	1 MHz offset from 5.0 GHz carrier
5.0 GHz Carrier			-151		dBc/Hz	10 MHz offset from 5.0 GHz carrier
6.6 GHz Carrier			-107		dBc/Hz	100 kHz offset from 6.6 GHz carrier
6.6 GHz Carrier			-127		dBc/Hz	800 kHz offset from 6.6 GHz carrier
6.6 GHz Carrier			-129		dBc/Hz	1 MHz offset from 6.6 GHz carrier
6.6 GHz Carrier			-148		dBc/Hz	10 MHz offset from 6.6 GHz carrier
Normalized In-Band Phase Noise Floor						
Fractional Channel ⁵			-221		dBc/Hz	
Integer Channel ⁶			-223		dBc/Hz	
Normalized 1/f Noise ⁷	$PN_{1/f}$		-116		dBc/Hz	10 kHz offset, normalized to 1 GHz
Integrated RMS Jitter			200		fs	
Spurious Signals due to Phase Frequency Detector (PFD) Frequency			-85		dBc	

¹ V_{CP} is the voltage at the CP_{OUT} pin.

² I_{OL} is the output low current.

³ T_A = 25°C; AV_{DD} = DV_{DD} = V_{RF} = V_{VCO} = V_P = 3.3 V; prescaler = 4/5; f_{REFIN} = 122.88 MHz; f_{PFD} = 61.44 MHz; and f_{RF} = 1650 MHz.

⁴ RF output power using the EV-ADF4355-3SD1Z evaluation board measured into a spectrum analyzer, with board and cable losses de-embedded. Unused RF output pins are terminated in 50 Ω.

⁵ Use this figure to calculate the phase noise for any application. To calculate in-band phase noise performance as seen at the VCO output, use the following formula: -221 + 10log(f_{PFD}) + 20logN. The value given is the lowest noise mode for the fractional channel.

⁶ Use this figure to calculate the phase noise for any application. To calculate in-band phase noise performance as seen at the VCO output, use the following formula: -223 + 10log(f_{PFD}) + 20logN. The value given is the lowest noise mode for the integer channel.

⁷ The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency (f_{RF}) and at a frequency offset (f) is given by PN = P_{1/f} + 10log(10 kHz/f) + 20log(f_{RF}/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in the ADIsimPLL™ design tool.

TIMING CHARACTERISTICS

$AV_{DD} = DV_{DD} = V_{RF} = V_P = V_{VCO} = 3.3\text{ V} \pm 4.5\%$, $A_{GND} = CP_{GND} = A_{GNDVCO} = SD_{GND} = A_{GNDRF} = 0\text{ V}$, $R_{SET} = 5.1\text{ k}\Omega$, dBm referred to $50\ \Omega$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

Table 2. Write Timing

Parameter	Limit	Unit	Description
f_{CLK}	50	MHz max	SPI CLK frequency
t_1	10	ns min	LE setup time
t_2	5	ns min	DATA to CLK setup time
t_3	5	ns min	DATA to CLK hold time
t_4	10	ns min	CLK high duration
t_5	10	ns min	CLK low duration
t_6	5	ns min	CLK to LE setup time
t_7	20 or $(2/f_{PFD})$, whichever is longer	ns min	LE pulse width

Write Timing Diagram

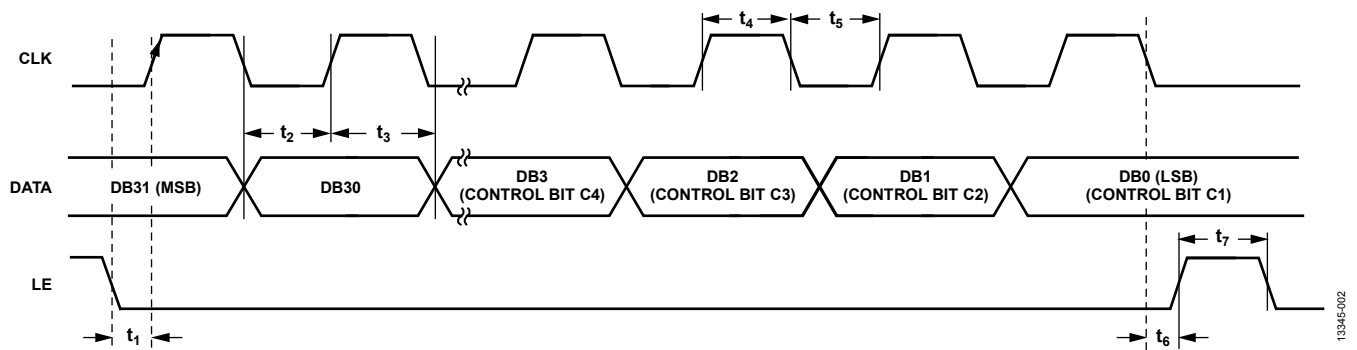


Figure 2. Write Timing Diagram

133445-002

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter ¹	Rating
V_{RF} , DV_{DD} , AV_{DD} to GND	-0.3 V to +3.6 V
AV_{DD} to DV_{DD}	-0.3 V to +0.3 V
V_P , V_{VCO} , V_{REGVCO} to GND	-0.3 V to +3.6 V
CP_{OUT} to GND ¹	-0.3 V to $V_P + 0.3$ V
Digital Input/Output Voltage to GND	-0.3 V to $DV_{DD} + 0.3$ V
Analog Input/Output Voltage to GND	-0.3 V to $AV_{DD} + 0.3$ V
$REF_{IN,A}$, $REF_{IN,B}$ to GND	-0.3 V to $AV_{DD} + 0.3$ V
$REF_{IN,A}$ to $REF_{IN,B}$	± 2.1 V
Operating Temperature Range	-40°C to $+105^\circ\text{C}$
Storage Temperature Range	-65°C to $+125^\circ\text{C}$
Maximum Junction Temperature	150°C
θ_{JA} , Thermal Impedance Pad Soldered to GND	27.3°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Electrostatic Discharge (ESD)	
Charged Device Model	500 V
Human Body Model	2500 V

¹ $GND = A_{GND} = SD_{GND} = A_{GNDRF} = A_{GNDVCO} = CP_{GND} = 0$ V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

The ADF4355-3 is a high performance RF integrated circuit with an ESD rating of 2500 V and is ESD sensitive. Take proper precautions for handling and assembly.

TRANSISTOR COUNT

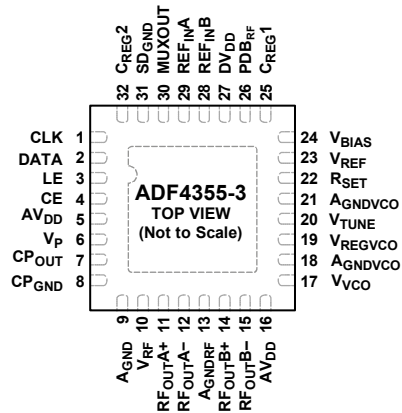
The transistor count for the ADF4355-3 is 103,665 (CMOS) and 3214 (bipolar).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES
1. THE EXPOSED PAD MUST BE CONNECTED TO AGND.

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Serial Clock Input. Data is clocked into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
2	DATA	Serial Data Input. The serial data is loaded most significant bit (MSB) first with the four least significant bits (LSBs) as the control bits. This input is a high impedance CMOS input.
3	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift register is loaded into the register that is selected by the four LSBs.
4	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump into three-state mode. A logic high on this pin powers up the device, depending on the status of the power-down bits.
5, 16	AV _{DD}	Analog Power Supplies. These pins range from 3.1515 V to 3.4485 V. Connect decoupling capacitors to the analog ground plane as close to these pins as possible. AV _{DD} must have the same value as DV _{DD} .
6	V _P	Charge Pump Power Supply. V _P must have the same value as V _{VCO} . Connect decoupling capacitors to the ground plane as close to this pin as possible.
7	CP _{OUT}	Charge Pump Output. When enabled, this output provides $\pm I_{CP}$ to the external loop filter. The output of the loop filter is connected to V _{TUNE} to drive the internal VCO.
8	CP _{GND}	Charge Pump Ground. This output is the ground return pin for CP _{OUT} .
9	AG _{ND}	Analog Ground. Ground return pin for AV _{DD} .
10	V _{RF}	Power Supply for the RF Output. Connect decoupling capacitors to the analog ground plane as close to this pin as possible. V _{RF} must have the same value as AV _{DD} . For optimum spurious performance, V _{RF} and DV _{DD} must originate from different regulators.
11	RF _{OUTA+}	VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available.
12	RF _{OUTA-}	Complementary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available.
13	AG _{NDRF}	RF Output Stage Ground. This pin is the ground return for the RF output stage.
14	RF _{OUTB+}	Auxiliary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available.
15	RF _{OUTB-}	Complementary Auxiliary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available.
17	V _{VCO}	Power Supply for the VCO. The voltage on this pin ranges from 3.1515 V to 3.4485 V. Connect decoupling capacitors to the analog ground plane as close to this pin as possible.
18, 21	AG _{NDVCO}	VCO Ground. This pin is the ground return path for the VCO.
19	V _{REGVCO}	VCO Compensation Node. Connect decoupling capacitors to the ground plane as close to this pin as possible. Connect this pin directly to V _{VCO} .
20	V _{TUNE}	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CP _{OUT} output voltage. The capacitance at this pin (V _{TUNE} input capacitance) is 7 pF.

Pin No.	Mnemonic	Description
22	R _{SET}	Bias Current Resistor. Connecting a resistor between this pin and ground sets the charge pump output current.
23	V _{REF}	Internal Compensation Node. V _{REF} is dc biased at half of the tuning range. Connect decoupling capacitors to the ground plane as close to this pin as possible. The recommended capacitor values are 10 pF, 1 nF, and 4.7 μF.
24	V _{BIAS}	Reference Voltage. Connect decoupling capacitors to the ground plane as close to this pin as possible. The recommended capacitor values are 10 pF, 1 nF, and 1 μF.
25, 32	C _{REG1} , C _{REG2}	Outputs from the LDO Regulator. Pin 25 and Pin 32 are the supply voltages to the digital circuits, and have a nominal voltage of 1.8 V. Decoupling capacitors of 100 nF connected to A _{GND} are required for these pins.
26	PDB _{RF}	RF Power-Down. A logic low on this pin mutes the RF outputs. This mute function is also software-controllable.
27	DV _{DD}	Digital Power Supply. This pin must be at the same voltage as AV _{DD} . Place decoupling capacitors to the ground plane as close to this pin as possible. For optimum spurious performance, V _{REF} and DV _{DD} must originate from different regulators.
28	REF _{INB}	Complementary Reference Input. If unused, ac-couple this pin to A _{GND} .
29	REF _{INA}	Reference Input.
30	MUXOUT	Multiplexer Output. The multiplexer output allows the digital lock detect, the analog lock detect, scaled RF, or the scaled reference frequency to be externally accessible.
31	SD _{GND}	Digital Σ-Δ Modulator Ground. Pin 31 is the ground return path for the Σ-Δ modulator.
	EP	Exposed Pad. The exposed pad must be connected to A _{GND} .

TYPICAL PERFORMANCE CHARACTERISTICS

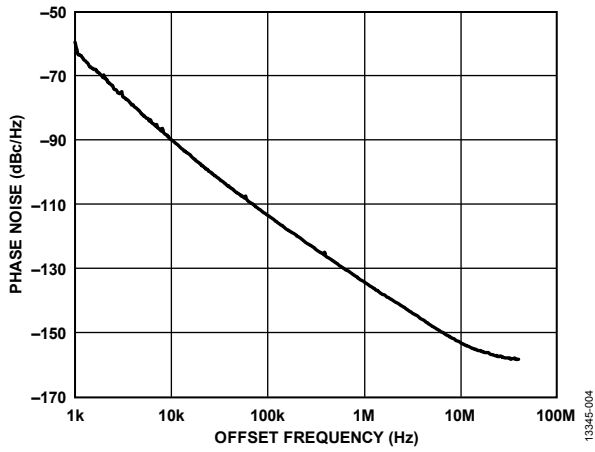


Figure 4. Open-Loop VCO Phase Noise, 3.3 GHz

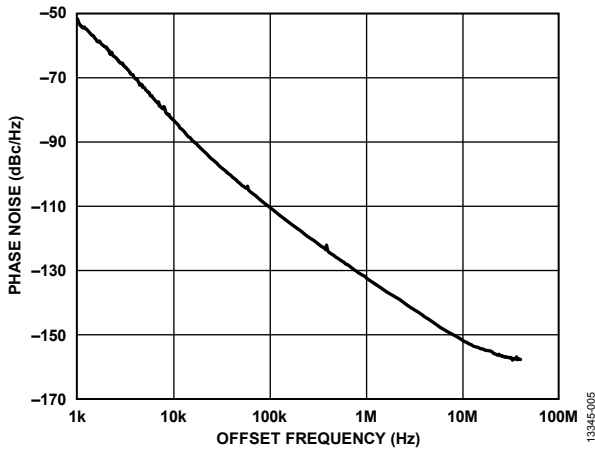


Figure 5. Open-Loop VCO Phase Noise, 5.0 GHz

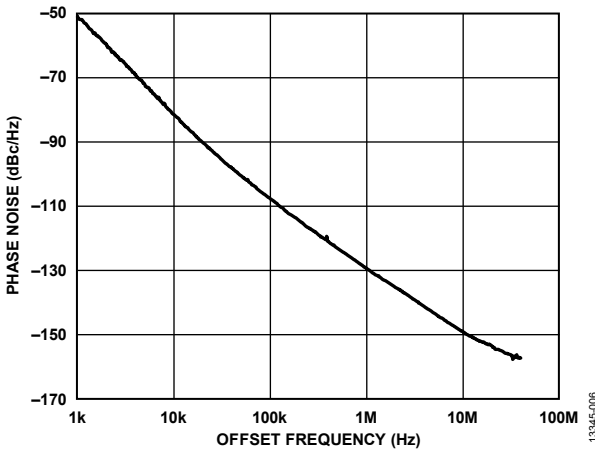


Figure 6. Open-Loop VCO Phase Noise, 6.6 GHz

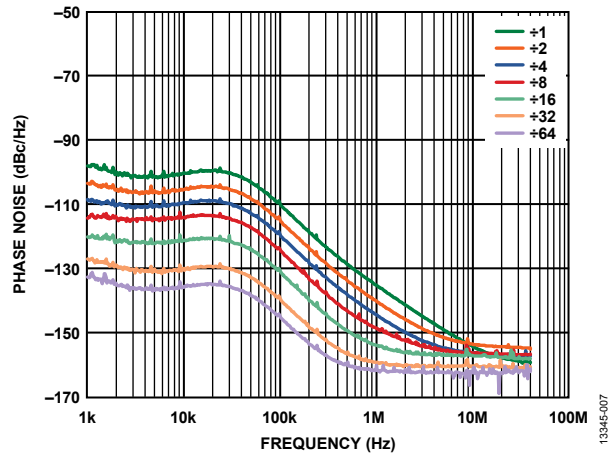


Figure 7. Closed-Loop Phase Noise, RF_{OUTA+} , Fundamental VCO and Dividers, VCO = 3.3 GHz, $f_{PFD} = 61.44$ MHz, Loop Bandwidth = 35 kHz

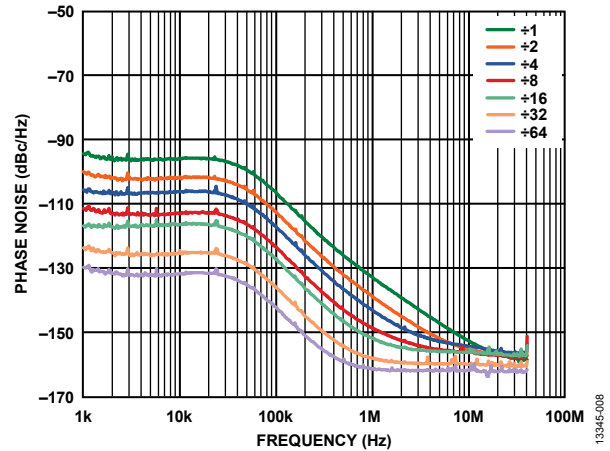


Figure 8. Closed-Loop Phase Noise, RF_{OUTA+} , Fundamental VCO and Dividers, VCO = 5.0 GHz, $f_{PFD} = 61.44$ MHz, Loop Bandwidth = 35 kHz

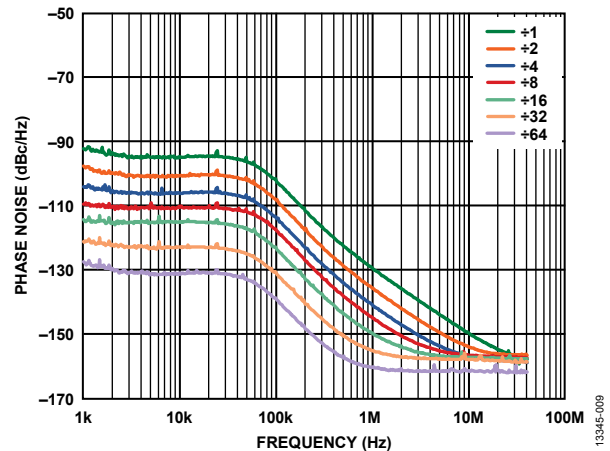


Figure 9. Closed-Loop Phase Noise, RF_{OUTA+} , Fundamental VCO and Dividers, VCO = 6.6 GHz, $f_{PFD} = 61.44$ MHz, Loop Bandwidth = 35 kHz

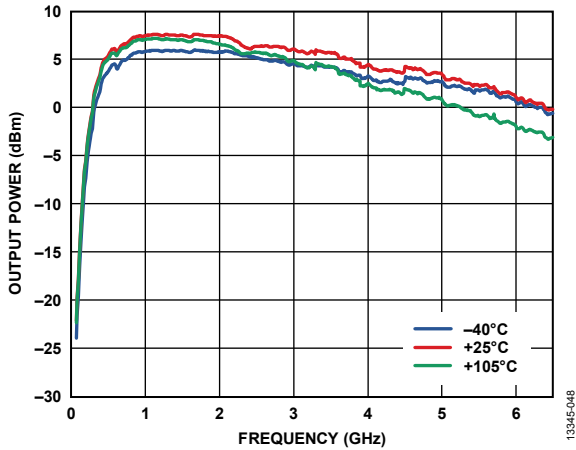


Figure 10. Output Power vs. Frequency, $R_{F_{OUTA+}}/R_{F_{OUTA-}}$ (7.5 nH Inductors, 10 pF Bypass Capacitors, Board Losses De-Embedded)

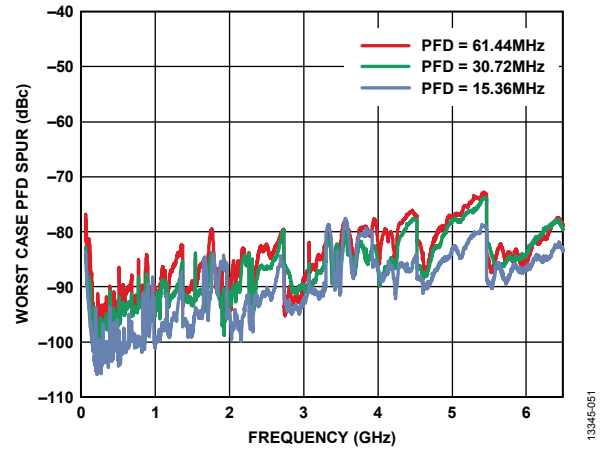


Figure 13. Worst Case PFD Spur vs. Frequency, $f_{PFD} = 15.36$ MHz, 30.72 MHz, and 61.44 MHz, Loop Filter = 35 kHz

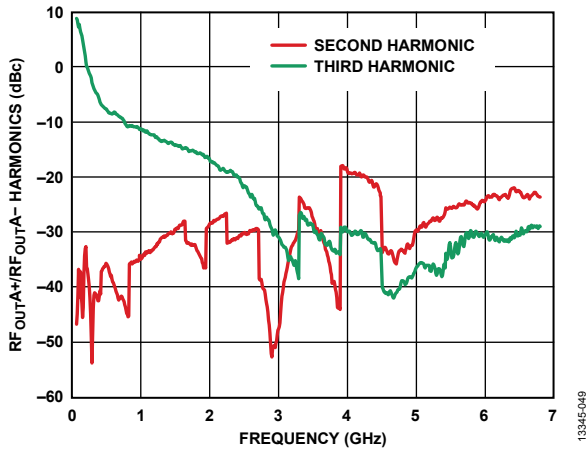


Figure 11. $R_{F_{OUTA+}}/R_{F_{OUTA-}}$ Harmonics vs. Frequency (7.5 nH Inductors, 10 pF Bypass Capacitors, Board Losses De-Embedded)

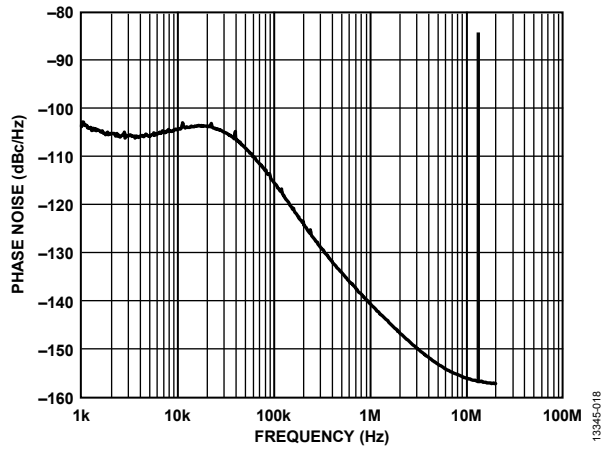


Figure 14. Spur Performance, GSM1800 Band, $R_{F_{OUTA+}} = 1550.2$ MHz, $R_{F_{IN}} = 122.88$ MHz, $f_{PFD} = 61.44$ MHz, Output Divide by 4 Selected, Loop Filter Bandwidth = 35 kHz, Channel Spacing = 20 kHz

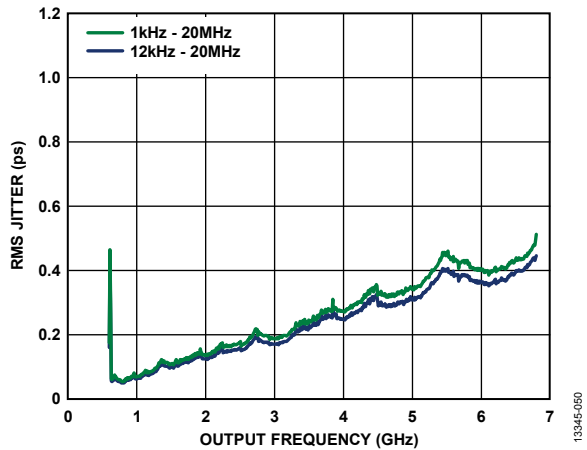


Figure 12. RMS Jitter vs. Output Frequency, $f_{PFD} = 61.44$ MHz, Loop Filter = 35 kHz

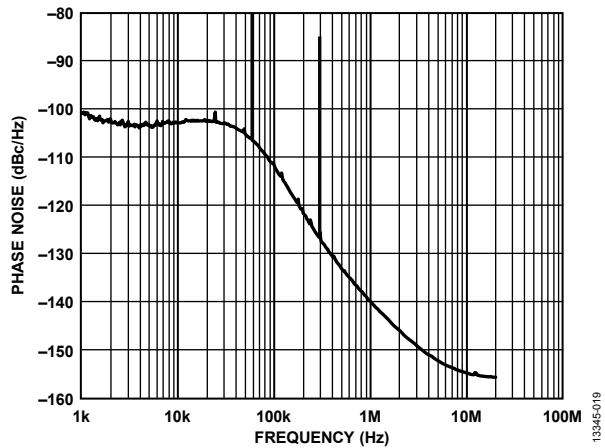


Figure 15. Spur Performance, W-CDMA Band, $R_{F_{OUTA+}} = 2113.5$ MHz, $R_{F_{IN}} = 122.88$ MHz, $f_{PFD} = 61.44$ MHz, Output Divide by 2 Selected, Loop Filter Bandwidth = 35 kHz, Channel Spacing = 20 kHz

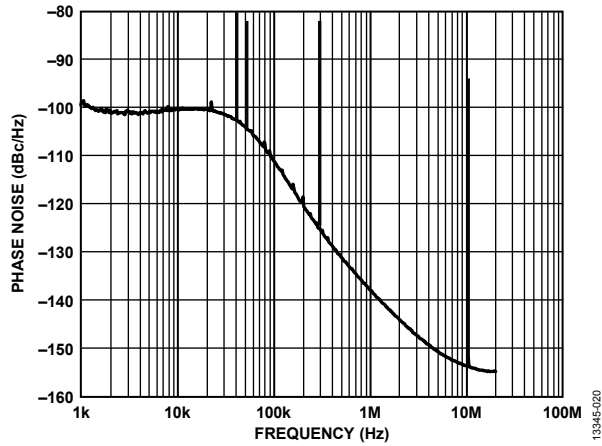


Figure 16. Spur Performance, $R_{F_{OUTA+}} = 2.591$ GHz, $R_{F_{IN}} = 122.88$ MHz, $f_{PFD} = 61.44$ MHz, Output Divide-by-2 Selected, Loop Filter Bandwidth = 35 kHz, Channel Spacing = 20 kHz

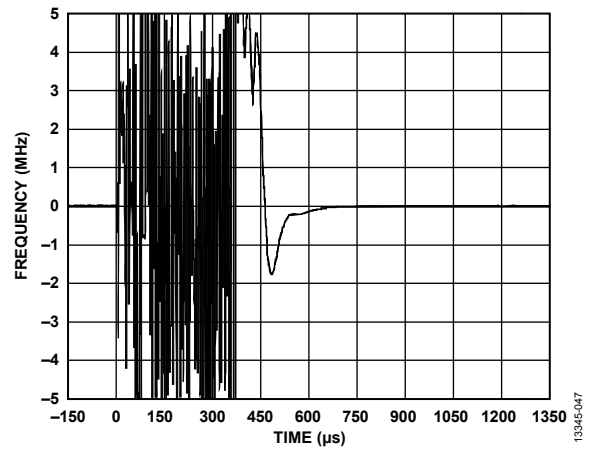


Figure 17. Lock Time for 100 MHz Jump from 3300 MHz to 6600 MHz, Loop Bandwidth = 3 kHz

THEORY OF OPERATION

REFERENCE INPUT SECTION

Figure 18 shows the reference input section of the ADF4355-3. The reference input can accept both single-ended and differential signals. Use the reference mode bit (Register 4, Bit DB9) to select the signal. To use a differential signal on the reference input, program this bit high. In this case, SW1 and SW2 are open, SW3 and SW4 are closed, and the current source that drives the differential pair of transistors switches on. The differential signal is buffered, and it is provided to an emitter coupled logic (ECL) to a CMOS converter. When a single-ended signal is the reference, connect the reference signal to REF_{IN}A and program Bit DB9 in Register 4 to 0. In this case, SW1 and SW2 are closed, SW3 and SW4 are open, and the current source that drives the differential pair of transistors switches off. Single-ended mode results in lower integer boundary spurs.

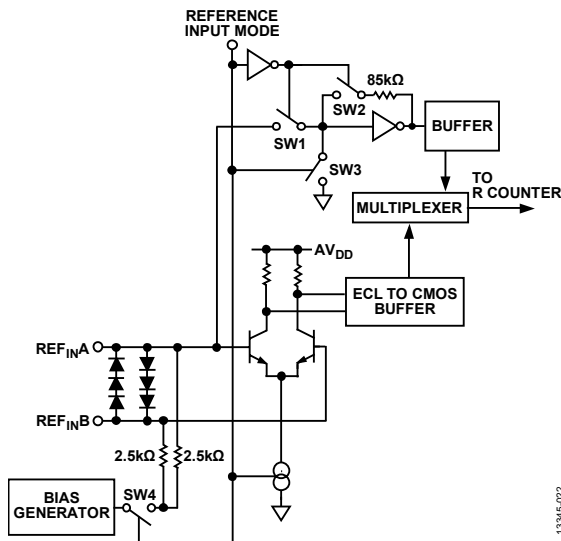


Figure 18. Reference Input Stage

RF N DIVIDER

The RF N divider allows a division ratio in the PLL feedback path. Determine the division ratio by the INT, FRAC1, FRAC2, and MOD2 values that this divider comprises.

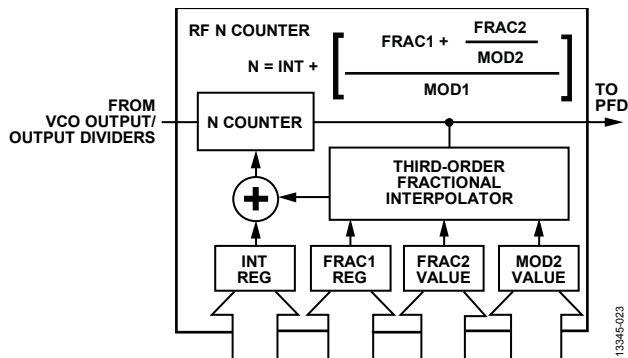


Figure 19. RF N Divider

INT, FRACx, MODx, and R Counter Relationship

The INT, FRAC1, FRAC2, MOD1, and MOD2 values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the PFD frequency (f_{PFD}). For more information, see the RF Synthesizer—A Worked Example section.

Calculate the RF VCO frequency (VCO_{OUT}) by

$$VCO_{OUT} = f_{PFD} \times N \tag{1}$$

where:

VCO_{OUT} is the output frequency of the VCO (without using the output divider).

f_{PFD} is the frequency of the phase frequency detector.

N is the desired value of the feedback counter, N .

Calculate f_{PFD} by

$$f_{PFD} = REF_{IN} \times ((1 + D)/(R \times (1 + T))) \tag{2}$$

where:

REF_{IN} is the reference input frequency.

D is the REF_{IN} doubler bit.

R is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023).

T is the REF_{IN} divide by 2 bit (0 or 1).

N comprises

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \tag{3}$$

where:

INT is the 16-bit integer value (23 to 32,767 for the 4/5 prescaler, and 75 to 65,535 for the 8/9 prescaler).

$FRAC1$ is the numerator of the primary modulus (0 to 16,777,215).

$FRAC2$ is the numerator of the 14-bit auxiliary modulus (0 to 16,383).

$MOD2$ is the programmable, 14-bit auxiliary fractional modulus (2 to 16,383).

$MOD1$ is a 24-bit primary modulus with a fixed value of $2^{24} = 16,777,216$.

Equation 3 results in a very fine frequency resolution with no residual frequency error. Apply this formula using the following steps:

1. Calculate N by dividing VCO_{OUT}/f_{PFD} . The integer value of this number forms INT .
2. Subtract the INT value from the full N value.
3. Multiply the remainder by 2^{24} . The integer value of this number forms $FRAC1$.
4. Calculate the $MOD2$ based on the channel spacing (f_{CHSP}) by

$$MOD2 = f_{PFD} / GCD(f_{PFD}, f_{CHSP}) \tag{4}$$

where:

f_{CHSP} is the desired channel spacing.

$GCD(f_{PFD}, f_{CHSP})$ is the greatest common divisor of the PFD frequency and the channel spacing frequency.

5. Calculate FRAC2 by the following equation:

$$FRAC2 = ((N - INT) \times 2^{24} - FRAC1) \times MOD2 \quad (5)$$

The FRAC2 and MOD2 fraction results in outputs with zero frequency error for channel spacings when

$$f_{PFD}/GCD(f_{PFD}/f_{CHSP}) < 16,383 \quad (6)$$

where:

f_{PFD} is the frequency of the phase frequency detector.

GCD is a greatest common divider function.

f_{CHSP} is the desired channel spacing.

If zero frequency error is not required, the MOD1 and MOD2 denominators operate together to create a 38-bit resolution modulus.

INT N Mode

When FRAC1 and FRAC2 = 0, the synthesizer operates in integer-N mode.

R Counter

The 10-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 20 is a simplified schematic of the phase frequency detector. The PFD includes a fixed delay element that sets the width of the antibacklash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and provides a consistent reference spur level. Set the phase detector polarity to positive on this device because of the positive tuning of the VCO.

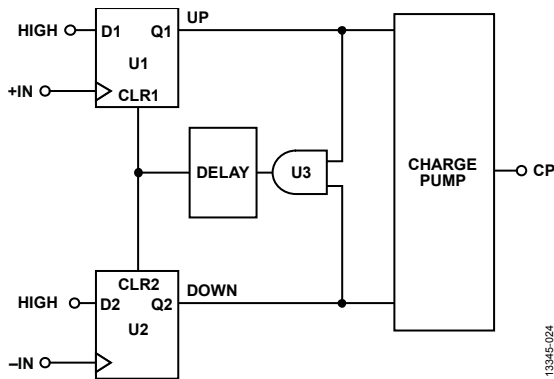


Figure 20. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4355-3 allows the user to access various internal points on the chip. The M3, M2, and M1 bits in Register 4 control the state of MUXOUT. Figure 21 shows the MUXOUT section in block diagram form.

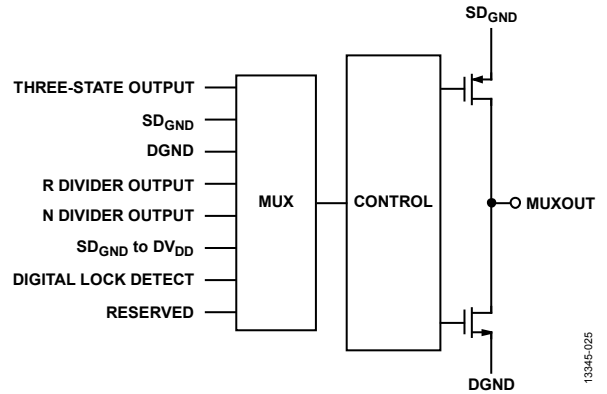


Figure 21. MUXOUT Block Diagram

If negative bleed is enabled, lock detect is not reliable for low PFD frequencies.

INPUT SHIFT REGISTERS

The ADF4355-3 digital section includes a 10-bit R counter, a 16-bit RF integer-N counter, a 24-bit FRAC1 counter, a 14-bit auxiliary fractional counter, and a 14-bit auxiliary modulus counter. Data clocks into the 32-bit shift register on each rising edge of CLK. The data clocks in MSB first. Data transfers from the shift register to one of 13 latches on the rising edge of LE. The state of the four control bits (C4, C3, C2, and C1) in the shift register determines the destination latch. As shown in Figure 2, the four least significant bits (LSBs) are DB3, DB2, DB1, and DB0. The truth table for these bits is shown in Table 5. Figure 24 and Figure 25 summarize the programming of the latches.

Table 5. Truth Table for the C4, C3, C2, and C1 Control Bits

Control Bits				Register
C4	C3	C2	C1	
0	0	0	0	Register 0
0	0	0	1	Register 1
0	0	1	0	Register 2
0	0	1	1	Register 3
0	1	0	0	Register 4
0	1	0	1	Register 5
0	1	1	0	Register 6
0	1	1	1	Register 7
1	0	0	0	Register 8
1	0	0	1	Register 9
1	0	1	0	Register 10
1	0	1	1	Register 11
1	1	0	0	Register 12

PROGRAM MODES

Table 5 and Figure 24 through Figure 38 show the program modes that must be set up in the ADF4355-3.

The following settings in the ADF4355-3 are double buffered: main fractional value (FRAC1), auxiliary modulus value (MOD2), auxiliary fractional value (FRAC2), reference doubler, reference divide by 2 (RDIV2), phase value, R counter value, and charge pump current setting. Two events must occur before the ADF4355-3 uses a new value for any of the double buffered settings. First, the new value must latch into the device by writing to the appropriate register, and second, a new write to Register 0 must be performed.

For example, to ensure that the modulus value loads correctly, every time the modulus value updates, Register 0 must be written to. The RF divider select in Register 6 is also double buffered, but only when DB14 of Register 4 is high.

VCO

The VCO core in the ADF4355-3 consists of four separate VCOs, each of which uses 256 overlapping bands, which allows covering a wide frequency range without a large VCO sensitivity (K_V) and without resulting poor phase noise and spurious performance.

The correct VCO and band are chosen automatically by the VCO and band select logic when Register 0 is updated and autocalibration is enabled. The VCO V_{TUNE} is disconnected from the output of the loop filter and is connected to an internal reference voltage.

The R counter output is the clock for the band select logic. After band selection, normal PLL action resumes. The nominal value of K_V is 63 MHz/V when the N divider is driven from the VCO output, or the K_V value is divided by D. D is the output divider value if the N divider is driven from the RF output divider (chosen by programming Bits[D23:D21] in Register 6).

The VCO shows the variation of K_V as the tuning voltage, V_{TUNE} , varies within the band and from band to band. For wideband applications covering a wide frequency range (and changing output dividers), a value of 63 MHz/V provides the most accurate K_V , because this value is closest to the average value. Figure 22 shows how K_V varies with fundamental VCO frequency along with an average value for the frequency band. Users may prefer this figure when using narrow-band designs.

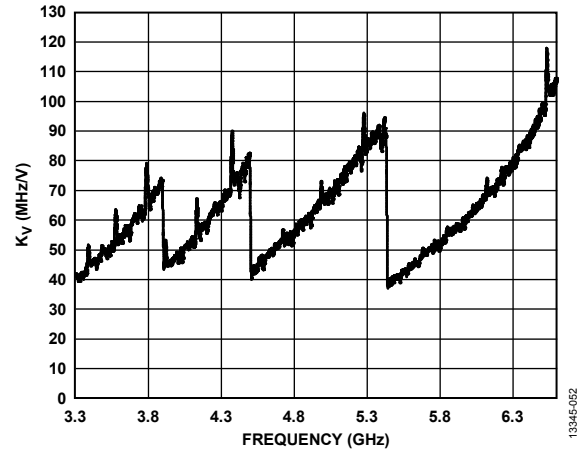


Figure 22. K_V vs. VCO Frequency

OUTPUT STAGE

The RF_{OUTA+} and RF_{OUTA-} pins of the ADF4355-3 connect to the collectors of an NPN differential pair driven by buffered outputs of the VCO, as shown in Figure 23. In this scheme, the ADF4355-3 contains internal 50 Ω resistors connected to the V_{RF} pin. To optimize the power dissipation vs. the output power requirements, the tail current of the differential pair is programmable using Bits[DB5:DB4] in Register 6. Four current levels can be set. These levels give the approximate output power levels of -4 dBm, -1 dBm, +2 dBm, and +5 dBm, respectively, using a 50 Ω resistor to V_{RF} and ac coupling into a 50 Ω load. For accurate power levels, see the Typical Performance Characteristics section. Add an external shunt inductor to provide higher power levels; however, this is less wideband than the internal bias only. Terminate the unused complementary output with a similar circuit to the used output.

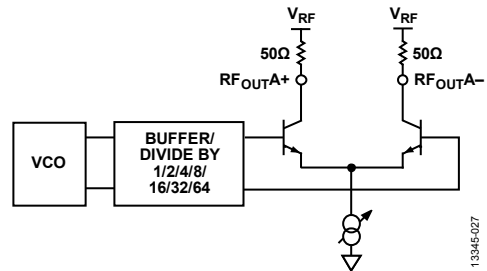


Figure 23. Output Stage

Another feature of the ADF4355-3 is that the supply current to the output stages can shut down until the ADF4355-3 achieves lock as measured by the digital lock detect circuitry. The mute until lock detect (MTLD) bit (Bit DB11) in Register 6 enables this function.

The RF_{OUTB+}/RF_{OUTB-} pins are duplicate outputs that can be used independently or in addition to the RF_{OUTA+}/RF_{OUTA-} pins.

LOOP FILTER

Use only passive loop filters. For information on designing a loop filter, use the ADIsimPLL design tool.

Table 6. Total I_{DD} (RF_{OUTA±} Refers to RF_{OUTA+}/RF_{OUTA-})

Divide By	RF_{OUTA±} Off	RF_{OUTA±} = -4 dBm	RF_{OUTA±} = -1 dBm	RF_{OUTA±} = +2 dBm	RF_{OUTA±} = +5 dBm
I _{VCO} and I _P	49.4 mA	49.4 mA	49.4 mA	49.4 mA	49.4 mA
A _{DD} , D _{DD} , I _{RF}					
1	91.8 mA	103.3 mA	106.5 mA	111.7 mA	116.9 mA
2	100.9 mA	113.6 mA	117.0 mA	122.8 mA	128.4 mA
4	110.8 mA	123.9 mA	127.5 mA	133.6 mA	139.8 mA
8	118.9 mA	132.1 mA	135.6 mA	141.8 mA	148.0 mA
16	124.0 mA	137.3 mA	140.8 mA	147.0 mA	153.3 mA
32	128.0 mA	141.4 mA	144.9 mA	151.1 mA	157.5 mA
64	130.4 mA	144.0 mA	147.4 mA	153.6 mA	160.0 mA

REGISTER MAPS

REGISTER 0

RESERVED										AUTOCAL	PRESALER	16-BIT INTEGER VALUE (INT)														CONTROL BITS						
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	0	0	0	0	0	0	0	0	AC1	PR1	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	C4(0)	C3(0)	C2(0)	C1(0)

REGISTER 1

RESERVED				24-BIT MAIN FRACTIONAL VALUE (FRAC1) DBR ¹																								CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C4(0)	C3(0)	C2(0)	C1(1)

REGISTER 2

14-BIT AUXILIARY FRACTIONAL VALUE (FRAC2) DBR ¹														14-BIT AUXILIARY MODULUS VALUE (MOD2) DBR ¹														CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C4(0)	C3(0)	C2(1)	C1(0)

REGISTER 3

RESERVED	SD LOAD RESET	PHASE RESYNC	PHASE ADJUST	24-BIT PHASE VALUE (PHASE) DBR ¹																								CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	SD1	PR1	PA1	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C4(0)	C3(0)	C2(1)	C1(1)

REGISTER 4

RESERVED	MUXOUT			REFERENCE DOUBLER DBR ¹	RDIV2 DBR ¹	10-BIT R COUNTER DBR ¹														DOUBLE BUFF	CURRENT SETTING DBR ¹			REF. MODE	MUX LOGIC	PD POLARITY	POWER-DOWN	CP THREE-STATE	COUNTER RESET	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
0	0	M3	M2	M1	RD2	RD1	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	D1	CP4	CP3	CP2	CP1	U6	U5	U4	U3	U2	U1	C4(0)	C3(1)	C2(0)	C1(0)		

REGISTER 5

RESERVED																												CONTROL BITS					
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	C4(0)	C3(1)	C2(0)	C1(1)

REGISTER 6

RESERVED	GATED BLEED	NEGATIVE BLEED	RESERVED				FEEDBACK SELECT	RF DIVIDER SELECT ²	CHARGE PUMP BLEED CURRENT										RESERVED	MTLD	RESERVED	AUX RF OUTPUT ENABLE	AUX RF OUTPUT POWER	RF OUTPUT ENABLE	RF OUTPUT POWER	CONTROL BITS					
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	BL10	BL9	1	0	1	0	D13	D12	D11	D10	BL8	BL7	BL6	BL5	BL4	BL3	BL2	BL1	0	D8	0	D6	D5	D4	D3	D2	D1	C4(0)	C3(1)	C2(1)	C1(0)

¹DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.
²DBB = DOUBLE BUFFERED BITS—BUFFERED BY A WRITE TO REGISTER 0 WHEN BIT DB14 OF REGISTER 4 IS HIGH.

Figure 24. Register Summary (Register 0 to Register 6)

REGISTER 7

RESERVED																		LD CYCLE COUNT	LOL MODE	FRAC-N LD PRECISION	LDO MODE	CONTROL BITS										
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	0	1	0	0	LE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD5	LD4	LOL	LD3	LD2	LD1	C4(0)	C3(1)	C2(1)	C1(1)

REGISTER 8

RESERVED																												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	1	1	C4(1)	C3(0)	C2(0)	C1(0)

REGISTER 9

VCO BAND DIVISION						TIMEOUT						RESERVED						SYNTHESIZER LOCK TIMEOUT				CONTROL BITS									
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1	TL10	TL9	TL8	TL7	TL6	TL5	TL4	TL3	TL2	TL1	1	1	1	1	1	SL5	SL4	SL3	SL2	SL1	C4(1)	C3(0)	C2(0)	C1(1)

REGISTER 10

RESERVED																		ADC CLOCK DIVIDER						ADC CONVERSION	ADC ENABLE	CONTROL BITS					
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AE2	AE1	C4(1)	C3(0)	C2(1)	C1(0)

REGISTER 11

RESERVED																												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(1)	C1(1)

REGISTER 12

RESYNC CLOCK																RESERVED												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	0	0	0	0	0	1	0	1	0	0	0	0	C4(1)	C3(1)	C2(0)	C1(0)

Figure 25. Register Summary (Register 7 to Register 12)

13445-029

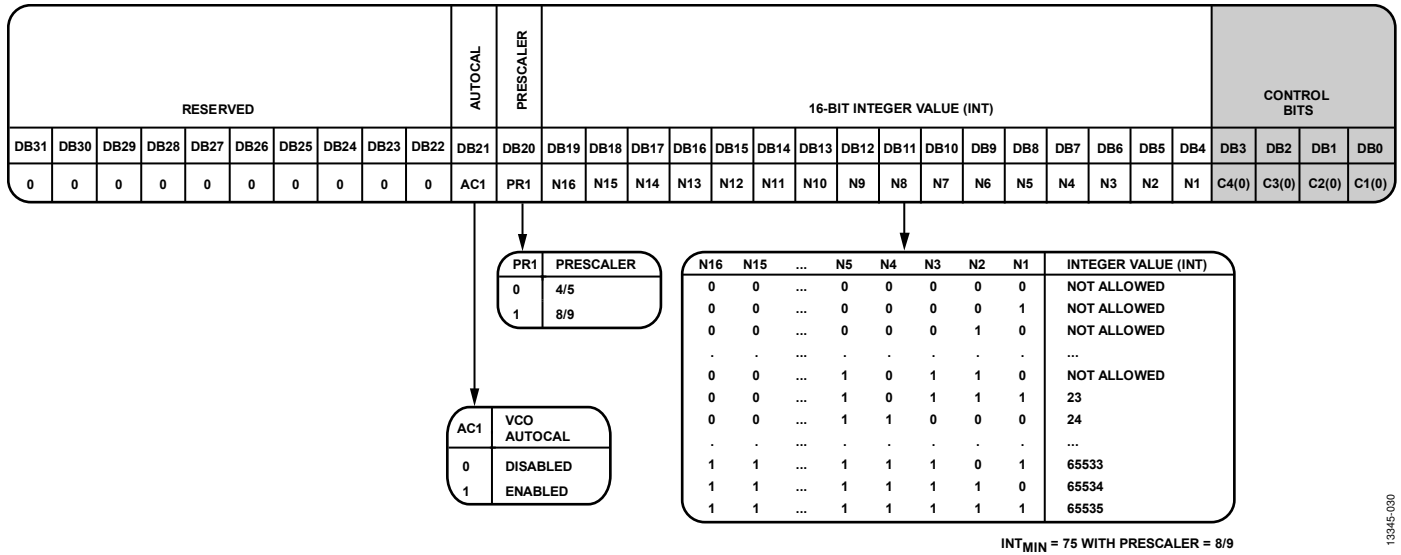


Figure 26. Register 0

REGISTER 0

Control Bits

With Bits[C4:C1] set to 0000, Register 0 is programmed. Figure 26 shows the input data format for programming this register.

Reserved

Bits[DB31:DB22] are reserved and must be set to 0.

Automatic Calibration (Autocal)

Write to Register 0 to enact (by default) the VCO automatic calibration, and to choose the appropriate VCO and VCO subband. Write 1 to the AC1 bit (Bit DB21) to enable the automatic calibration, which is the recommended mode of operation.

Set the AC1 bit to 0 to disable the automatic calibration, which leaves the ADF4355-3 in the same band it is already in when Register 0 is updated.

Disable the automatic calibration only for fixed frequency applications, phase adjust applications, or very small (<10 kHz) frequency jumps.

Prescaler Value

The dual modulus prescaler (P/P + 1), along with the INT, FRACx, and MODx counters, determines the overall division ratio from the VCO output to the PFD input. The PR1 bit (Bit DB20) in Register 0 sets the prescaler value.

Operating at CML levels, the prescaler takes the clock from the VCO output and divides it down for the counters. It is based on a synchronous 4/5 core. The prescaler limits the INT value; therefore, if P is 4/5, INT_{MIN} is 23, and if P is 8/9, INT_{MIN} is 75.

16-Bit Integer Value

The 16 INT bits (Bits[DB19:DB4]) set the INT value, which determines the integer part of the feedback division factor. The INT value is used in Equation 3 (see the RF Synthesizer—A Worked Example section). All integer values from 23 to 32,767 are allowed for the 4/5 prescaler. For the 8/9 prescaler, the minimum integer value is 75, and the maximum value is 65,535.

RESERVED				24-BIT MAIN FRACTIONAL VALUE (FRAC1)																	DBR ¹				CONTROL BITS						
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C4(0)	C3(0)	C2(0)	C1(1)

F24	F23	F2	F1	MAIN FRACTIONAL VALUE (FRAC1)
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
.
.
.
1	1	0	0	16777212
1	1	0	1	16777213
1	1	1	0	16777214
1	1	1	1	16777215

¹DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 27. Register 1

REGISTER 1

Control Bits

With Bits[C4:C1] set to 0001, Register 1 is programmed. Figure 27 shows the input data format for programming this register.

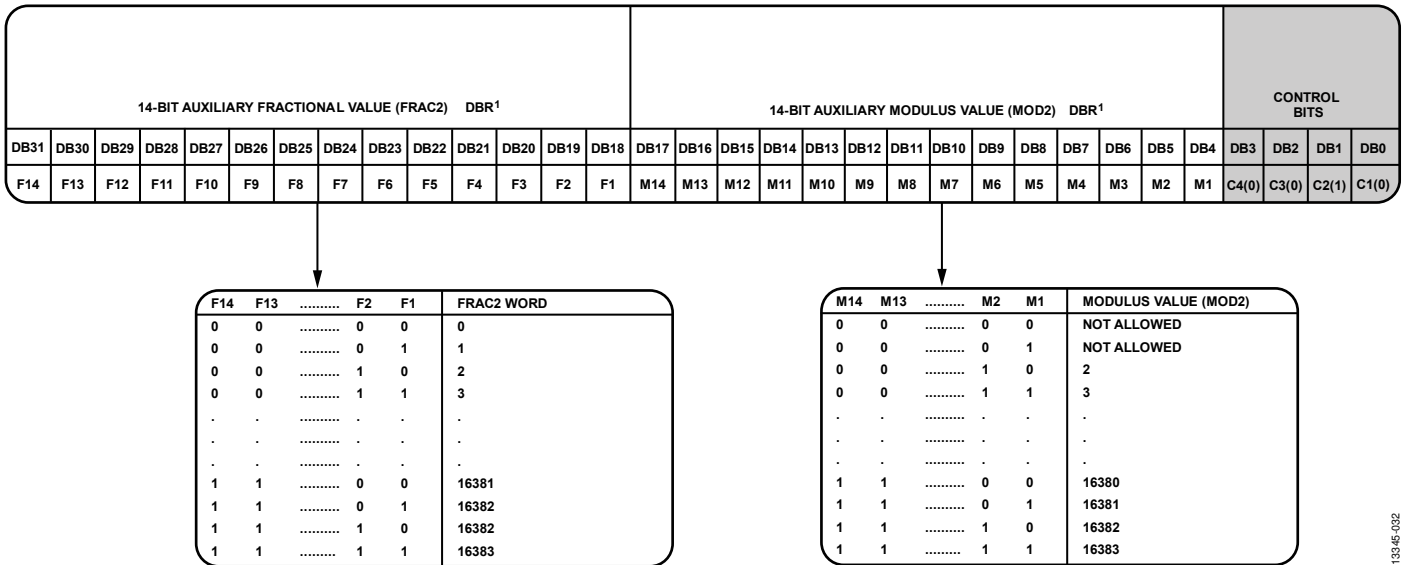
Reserved

Bits[DB31:DB28] are reserved and must be set to 0.

24-Bit Main Fractional Value

The 24 FRAC1 bits (Bits[DB27:DB4]) set the numerator of the fraction that is input to the Σ - Δ modulator. This fraction, along with the INT value, specifies the new frequency channel that the synthesizer locks to, as shown in the RF Synthesizer—A Worked Example section. FRAC1 values from 0 to (MOD1 – 1) cover channels over a frequency range equal to the PFD reference frequency.

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¹DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 28. Register 2

REGISTER 2

Control Bits

With Bits[C4:C1] set to 0010, Register 2 is programmed. Figure 28 shows the input data format for programming this register.

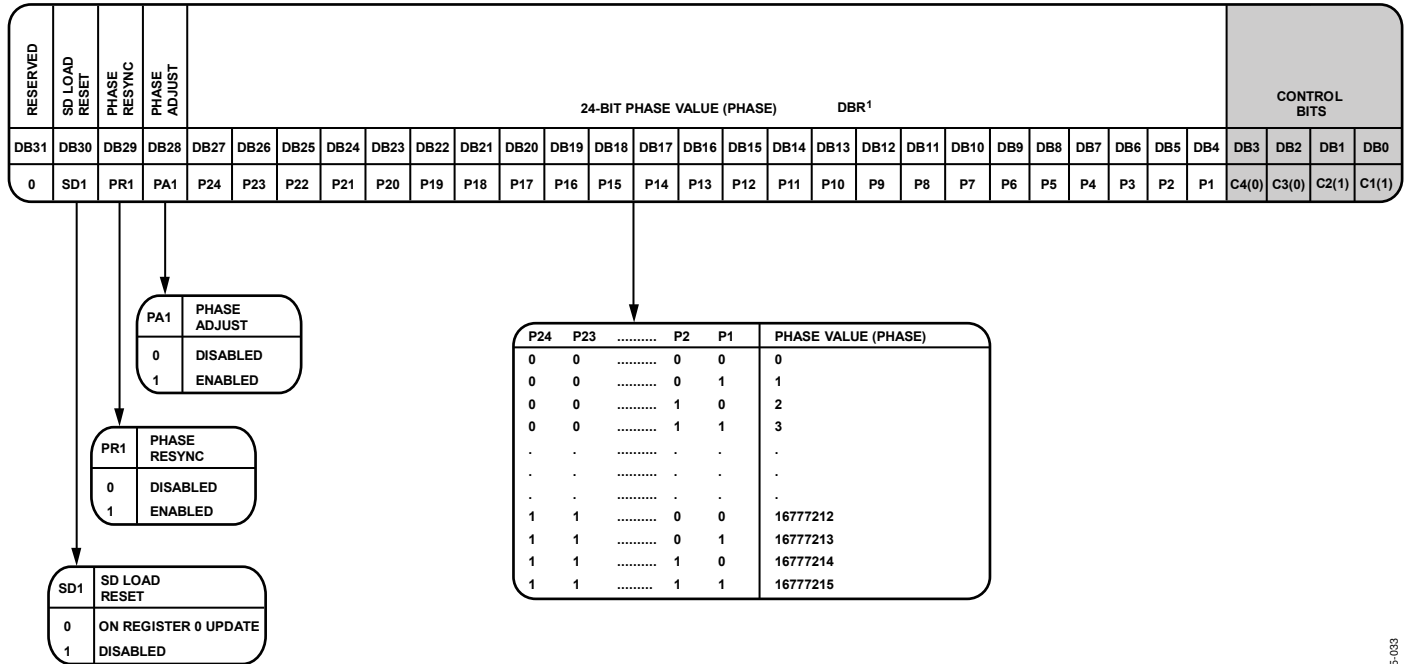
14-Bit Auxiliary Fractional Value (FRAC2)

The 14-bit auxiliary fractional value (Bits[DB31:DB18]) controls the auxiliary fractional word. FRAC2 must be less than the MOD2 value programmed in Register 2.

14-Bit Auxiliary Modulus Value (MOD2)

The 14-bit auxiliary modulus value (Bits[DB17:DB4]) sets the auxiliary fractional modulus. Use MOD2 to correct any residual error due to the main fractional modulus.

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¹DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 29. Register 3

REGISTER 3

Control Bits

With Bits[C4:C1] set to 0011, Register 3 is programmed. Figure 29 shows the input data format for programming this register.

Reserved

Bit DB31 is reserved and must be set to 0.

SD Load Reset

When writing to Register 0, the Σ-Δ (SD) modulator resets. For applications in which the phase is continually adjusted, this reset may not be desirable; therefore, in these cases, the Σ-Δ reset can be disabled by writing a 1 to the SD1 bit (Bit DB30).

Phase Resync

To use the phase resynchronization feature, the PR1 bit (Bit DB29) must be set to 1. If unused, the bit can be programmed to 0. The phase resync timer must also be used in Register 12 to ensure that the resynchronization feature is applied after the PLL settles to the final frequency. If the PLL has not settled to the final frequency, phase resync may not function correctly. Resynchronization is useful in phased array and beam forming applications. It ensures repeatability of output phase when programming the same frequency. In phase critical applications that use frequencies requiring the output divider (<3300 MHz), it is necessary to feed the N divider with the divided VCO frequency as distinct from the fundamental VCO frequency, which is achieved by

programming the D13 bit (Bit DB24) in Register 6 to 0, which ensures divided feedback to the N divider.

For resync applications, enable the Σ-Δ modulator load reset in Register 3 by setting DB30 to 0. Phase resync functions only when FRAC2 = 0.

Phase Adjustment

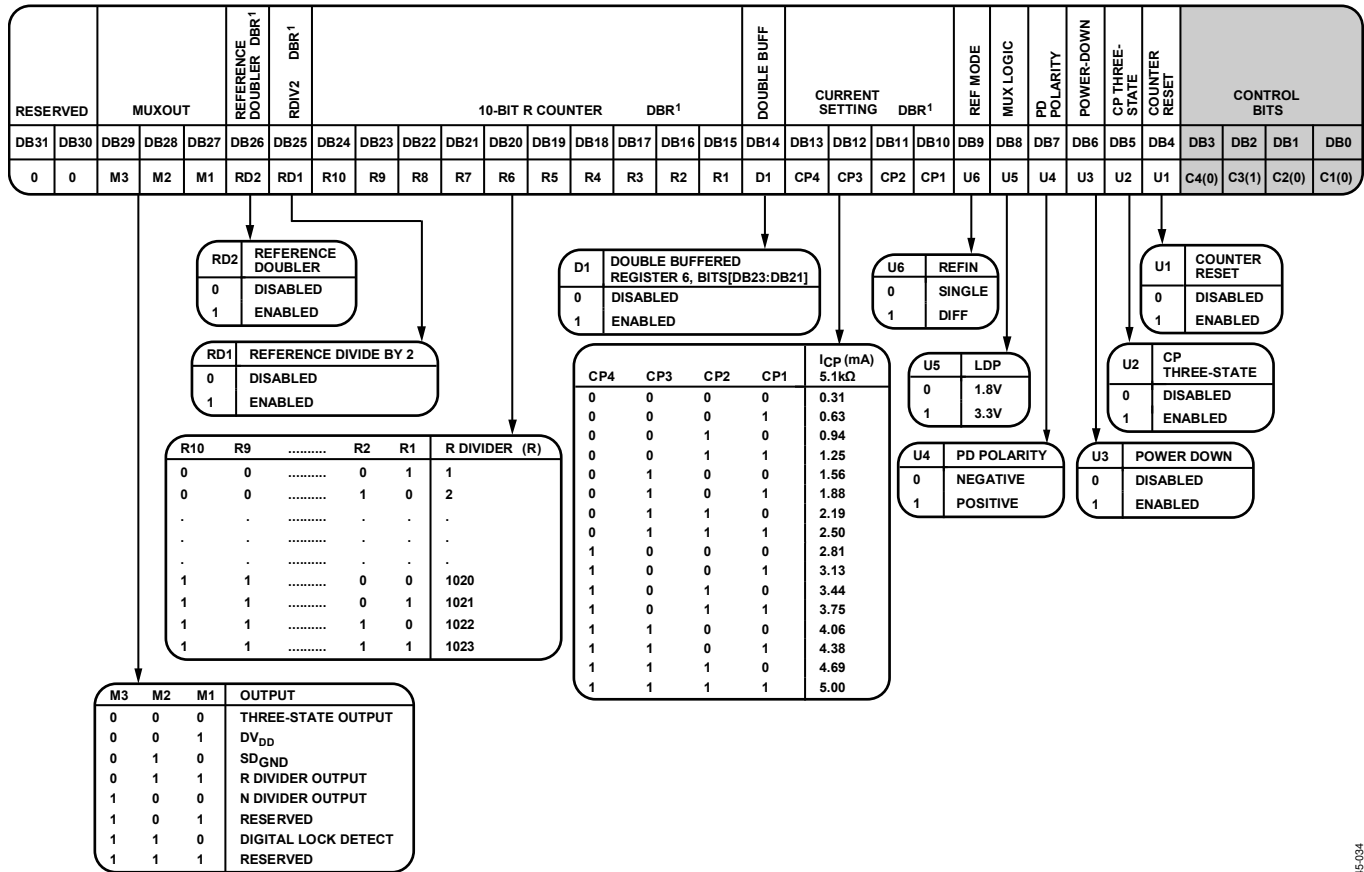
To adjust the relative output phase of the ADF4355-3 on each Register 0 update, set the PA1 bit (Bit DB28) to 1. This feature differs from the resynchronization feature in that it is useful when adjustments to phase are made continually in an application. For this function, disable the VCO automatic calibration by setting the AC1 bit (Bit DB21) in Register 0 to 1, and disable the SD load reset by setting the SD1 bit (Bit DB30) in Register 3 to 1. Note that phase resync and phase adjustment cannot be used simultaneously.

24-Bit Phase Value

The phase of the RF output frequency can be adjusted in 24-bit steps; from 0° (0) to 360° (2²⁴ - 1). For phase adjustment applications, the phase is set by

$$(Phase\ Value/16,777,216) \times 360^\circ \tag{7}$$

When the phase value is programmed to Register 3, each subsequent adjustment of Register 0 increments the phase by the value in this equation.



¹DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 30. Register 4

REGISTER 4

Control Bits

With Bits[C4:C1] set to 0100, Register 4 is programmed. Figure 30 shows the input data format for programming this register.

Reserved

Bits[DB31:DB30] are reserved and must be set to 0.

MUXOUT

The on-chip multiplexer (MUXOUT) is controlled by Bits[DB29:DB27]. For additional details, see Figure 30.

When changing frequency, that is, writing R0, MUXOUT must not be set to the N divider output or the R divider output. If needed, enable these functions after locking to the new frequency.

Reference Doubler

Setting the RD2 bit (Bit DB26) to 0 feeds the REF_{IN} signal directly to the 10-bit R counter, disabling the doubler. Setting this bit to 1 multiplies the reference frequency by a factor of 2 before feeding it into the 10-bit R counter. When the doubler is disabled, the REF_{IN} falling edge is the active edge at the PFD input to the fractional synthesizer. When the doubler is enabled, both the rising and falling edges of the reference frequency become active edges at the PFD input.

The maximum allowable reference frequency when the doubler is enabled is 100 MHz.

RDIV2

Setting the RDIV2 bit (Bit DB25) to 1 inserts a divide by 2 toggle flip-flop between the R counter and PFD, which halves the reference frequency to the PFD. This function provides a 50% duty cycle signal at the PFD input.

10-Bit R Counter

The 10-bit R counter divides the input reference frequency (REF_{IN}) to produce the reference clock to the PFD. Division ratios range from 1 to 1023.

Double Buffer

The D1 bit (Bit DB14) enables or disables double buffering of the RF divider select bits (Bits[DB23:DB21]) in Register 6. The Program Modes section explains double buffering further.

Charge Pump Current Setting

The CP4 to CP1 bits (Bits[DB13:DB10]) set the charge pump current. Set this value to the charge pump current that the loop filter is designed with (see Figure 30). For the lowest spurs, the 0.9 mA setting is recommended.

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Reference Mode

The ADF4355-3 permits the use of either differential or single-ended reference sources. For differential sources, set the reference mode bit (Bit DB9) to 1, and for single-ended sources, set it to 0. Single-ended mode results in lower integer boundary spurs. If only a differential signal is available, REF_{INB} can be left floating to get the integer boundary spur improvements (provided that the frequency and power meets the single-ended requirements shown in Table 1).

Level Select

To assist with logic compatibility, MUXOUT is programmable to two logic levels. Set the U5 bit (Bit DB8) to 0 to select 1.8 V logic, and set it to 1 to select 3.3 V logic.

Phase Detector Polarity

The U4 bit (Bit DB7) sets the phase detector polarity. Set DB7 to 1. Active filters are not supported.

Power-Down

The U3 bit (Bit DB6) sets the programmable power-down mode. Setting DB6 to 1 performs a power-down. Setting DB6 to 0 returns the synthesizer to normal operation. In software power-down mode, the ADF4355-3 retains all information in its registers. The register contents are lost only if the supply voltages are removed.

When power-down activates, the following events occur:

- The synthesizer counters are forced to their load state conditions.
- The VCO powers down.
- The charge pump is forced into three-state mode.
- The digital lock detect circuitry resets.
- The RF_{OUTA+}/RF_{OUTA-} and RF_{OUTB+}/RF_{OUTB-} output stages are disabled.
- The input registers remain active and capable of loading and latching data.

Charge Pump Three-State

Setting the U2 bit (Bit DB5) to 1 puts the charge pump into three-state mode. Set DB5 to 0 for normal operation.

Counter Reset

The U1 bit (Bit DB4) resets the R counter, N counter, and VCO band selection of the ADF4355-3. When DB4 is set to 1, the RF synthesizer N counter and R counter and the VCO band selection are reset. For normal operation, set DB4 to 0.

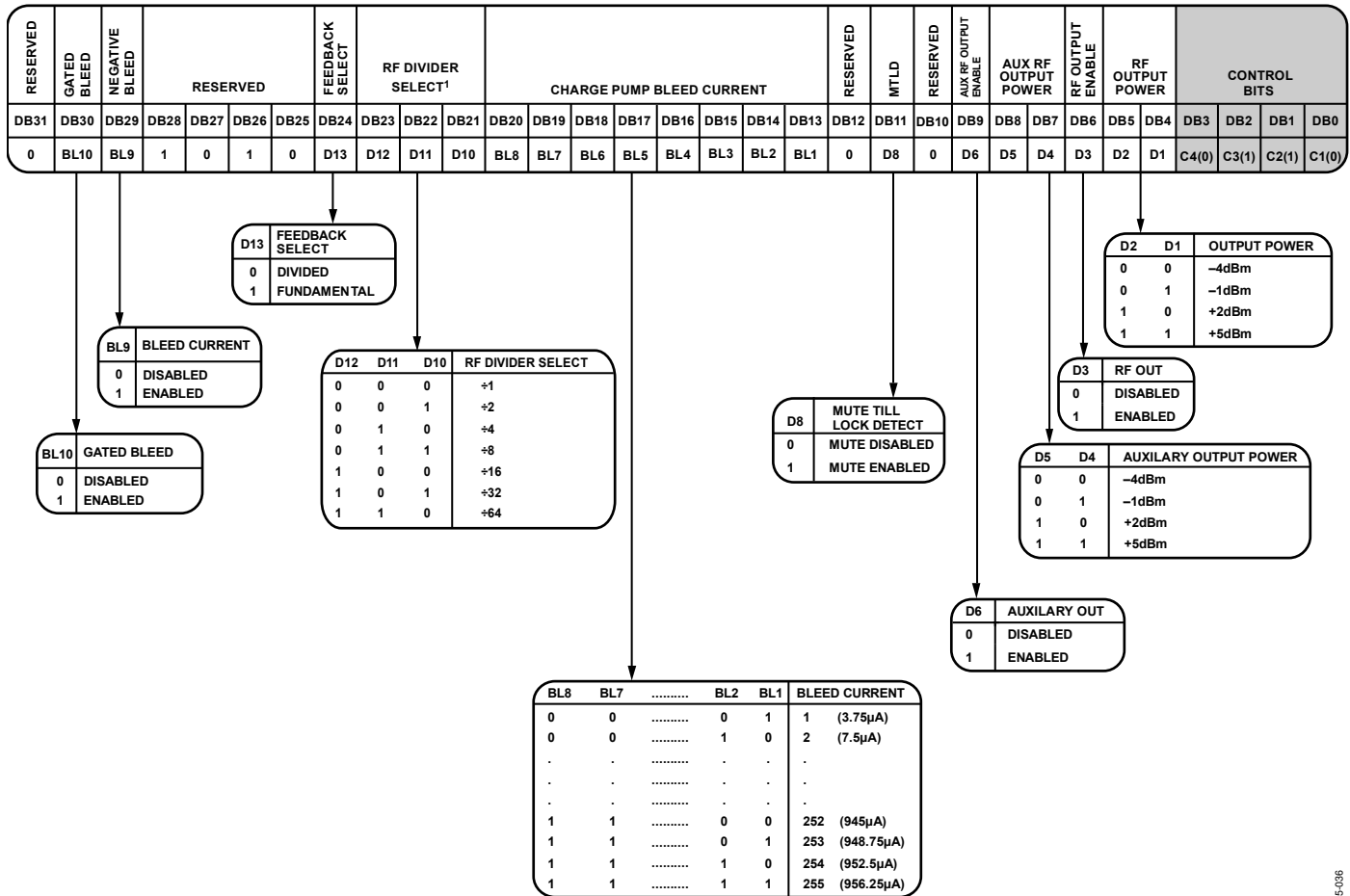
REGISTER 5

The bits in Register 5 are reserved and must be programmed as described in Figure 31, using a hexadecimal word of 0x00800005.

RESERVED																								CONTROL BITS							
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	C4(0)	C3(1)	C2(0)	C1(1)

Figure 31. Register 5 (0x00800005)

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¹BITS[DB23:DB21] ARE BUFFERED BY A WRITE TO REGISTER 0 WHEN THE DOUBLE BUFFER BIT IS ENABLED, BIT DB14 OF REGISTER 4.

Figure 32. Register 6

REGISTER 6

Control Bits

With Bits[C4:C1] set to 0110, Register 6 is programmed. Figure 32 shows the input data format for programming this register.

Reserved

Bit DB31 is reserved and must be set to 0.

Gated Bleed

Bleed currents can improve phase noise and spurs. However, due to a potential impact on lock time, the gated bleed bit, BL10 (Bit DB30), if set to 1, ensures bleed currents are not switched on until the digital lock detect asserts logic high. Note that this function requires digital lock detection to be enabled.

Negative Bleed

Use of constant negative bleed is recommended for most applications because it improves the linearity of the charge pump, leading to lower noise and spurious performance than leaving constant negative bleed off. To enable negative bleed, write 1 to BL9 (Bit DB29), and to disable negative bleed, write 0 to BL9 (Bit DB29). Use negative bleed only when operating in fractional-N mode, that is, FRAC1 or FRAC2 not equal to 0.

Reserved

Bits[DB28:DB25] are reserved and must be set to 1010.

Feedback Select

D13 (Bit DB24) selects the feedback from the output of the VCO to the N counter. When D13 is set to 1, the signal is taken directly from the VCO. When this bit is set to 0, the signal is taken from the output of the output dividers. The dividers enable coverage of the wide frequency band (51.5625 MHz to 6.6 GHz). When the divider is enabled and the feedback signal is taken from the output, the RF output signals of two separately configured PLLs are in phase. Divided feedback is useful in some applications where the positive interference of signals is required to increase the power.

Divider Select

D12 to D10 (Bits[DB23:DB21]) select the value of the RF output divider (see Figure 32). These bits are buffered by a write to Register 0 when Bit DB14 of Register 4 is high.