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Microwave Wideband Synthesizer with Integrated VCO

Data Sheet

ADF5355

FEATURES

- RF output frequency range: 54 MHz to 13,600 MHz
- Fractional-N synthesizer and integer-N synthesizer
- High resolution 38-bit modulus
- Phase frequency detector (PFD) operation to 125 MHz
- Reference frequency operation to 600 MHz
- Maintains frequency lock over −40°C to +85°C
- Low phase noise, voltage controlled oscillator (VCO)
- Programmable divide by 1, 2, 4, 8, 16, 32, or 64 output
- Analog and digital power supplies: 3.3 V
- Charge pump and VCO power supplies: 5.0 V, typical
- Logic compatibility: 1.8 V
- Programmable dual modulus prescaler of 4/5 or 8/9
- Programmable output power level
- RF output mute function
- Analog and digital lock detect
- Supported in the ADIsimPLL design tool

APPLICATIONS

- Wireless infrastructure (W-CDMA, TD-SCDMA, WiMAX, GSM, PCS, DCS, DECT)
- Point to point/point to multipoint microwave links
- Satellites/VSATs
- Test equipment/instrumentation
- Clock generation

GENERAL DESCRIPTION

The ADF5355 allows implementation of fractional-N or integer-N phase-locked loop (PLL) frequency synthesizers when used with an external loop filter and an external reference frequency. The wideband microwave VCO design permits frequency operation from 6.8 GHz to 13.6 GHz at one radio frequency (RF) output. A series of frequency dividers at another frequency output permits operation from 54 MHz to 6800 MHz.

The ADF5355 has an integrated VCO with a fundamental output frequency ranging from 3400 MHz to 6800 MHz. In addition, the VCO frequency is connected to divide by 1, 2, 4, 8, 16, 32, or 64 circuits that allow the user to generate RF output frequencies as low as 54 MHz. For applications that require isolation, the RF output stage can be muted. The mute function is both pin and software controllable.

Control of all on-chip registers is through a simple 3-wire interface. The ADF5355 operates with analog and digital power supplies ranging from 3.15 V to 3.45 V, with charge pump and VCO supplies from 4.75 V to 5.25 V. The ADF5355 also contains hardware and software power-down modes.

FUNCTIONAL BLOCK DIAGRAM

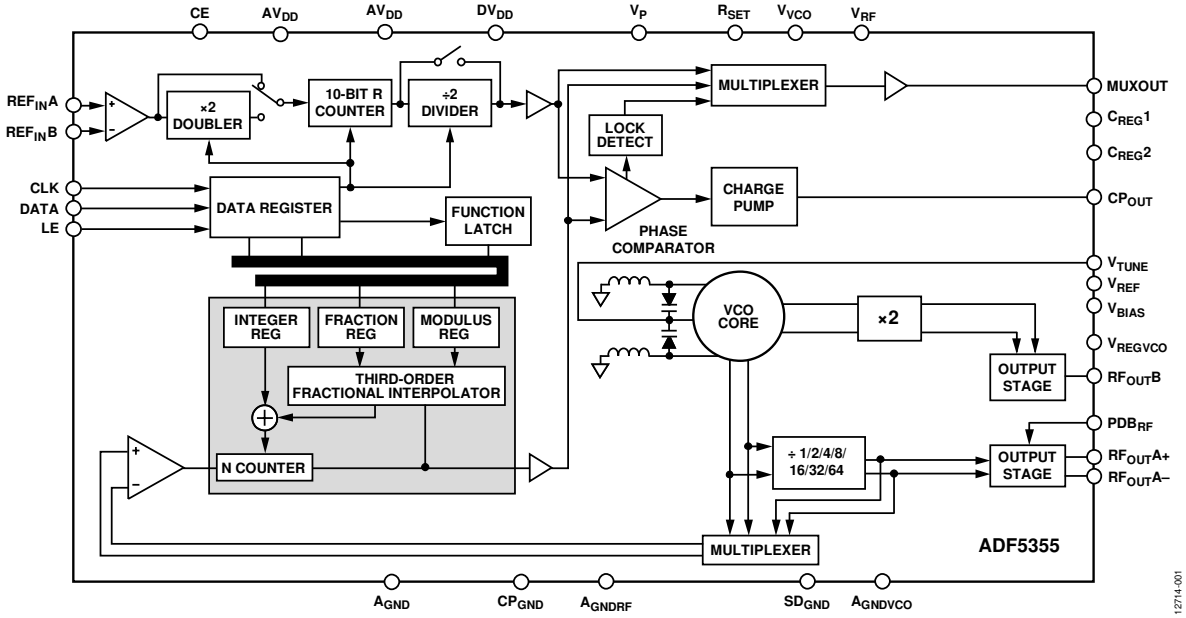

Figure 1.

Rev. C Document Feedback

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TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagram ... 1
Revision History ... 3
Specifications ... 4
Timing Characteristics ... 7
Absolute Maximum Ratings ... 8
Transistor Count ... 8
ESD Caution ... 8
Pin Configuration and Function Descriptions ... 9
Typical Performance Characteristics ... 11
Circuit Description ... 16
Reference Input ... 16
RF N Divider ... 16
Phase Frequency Detector (PFD) and Charge Pump ... 17
MUXOUT and Lock Detect ... 17
Input Shift Registers ... 17
Program Modes ... 18
VCO ... 18
Output Stage ... 18
Register Maps ... 20
Register 0 ... 22
Register 1 ... 23
Register 2 ... 24
Register 3 ... 25
Register 4 ... 26
Register 5 ... 27
Register 6 ... 28
Register 7 ... 30
Register 8 ... 31
Register 9 ... 31
Register 10 ... 32
Register 11 ... 32
Register 12 ... 33
Register Initialization Sequence ... 33
Frequency Update Sequence ... 33
RF Synthesizer—A Worked Example ... 34
Reference Doubler and Reference Divider ... 34
Spurious Optimization and Fast Lock ... 34
Optimizing Jitter ... 35
Spur Mechanisms ... 35
Lock Time ... 35
Applications Information ... 36
Power Supplies ... 36
Printed Circuit Board (PCB) Design Guidelines for a Chip-Scale Package ... 36
Output Matching ... 37
Outline Dimensions ... 38
Ordering Guide ... 38

REVISION HISTORY

4/2017—Rev. B to Rev C

Changes to Figure 55 and Power Supplies Section 36

1/2017—Rev. A to Rev B

Change to Features Section 1
Changes to Doubler Enabled Parameter and Endnote 3, Table 1 4
Changes to Table 2 7
Changes to Table 3 8
Changes to Table 4 9
Changes to Reference Input Section and Figure 32 Caption 16
Changes to Table 6 19
Changes to Phase Resync Section 25
Change to Reference Doubler Section 26
Changes to Power-Down Section 27
Changes to Negative Bleed Section 28
Changes to Loss of Lock (LOL) Mode Section 30
Changes to Register Initialization Sequence Section and Frequency Update Sequence Section 33
Changes to Power Supplies Section and Figure 55 36

2/2015—Rev. 0 to Rev. A

Changed Register 5, Bit DB5 Value from 0 to 1 ..... Throughout
Changed Register 5 Default Value from 0x00800005 to 0x00800025 ..... Throughout
Changed Register 8 Default Value from 0x102D4028 to 0x102D0428 ..... Throughout
Changes to Table 1 4
Changed Timing Diagram Section to Write Timing Diagram Section 7
Changes to Table 4 10
Changes to Figure 4 to Figure 6 11
Added Figure 7 to Figure 9; Renumbered Sequentially 11
Changes to Figure 10 to Figure 18 12
Changes to Figure 20 13
Changes to Figure 23 and Figure 27 14
Changes to Figure 28 to Figure 30 and Figure 31 Caption 15
Changes to Reference Input Section and INT, FRAC, MOD, and R Counter Relationship Section 16
Changes to Phase Frequency Detector (PFD) and Charge Pump Section 17
Changes to VCO Section and Output Stage Section 18
Changes to Automatic Calibration (AUTOCAL) Section 22
Changes to Figure 43 24
Changes to MUXOUT Section 26
Changes to Reference Mode Section and Counter Reset Section 27
Changes to Negative Bleed Section 28
Changes to Charge Pump Bleed Current Section 29
Changes to Register 9 Section, VCO Band Division Section, Timeout Section, Automatic Level Calibration Timeout Section, and Synthesizer Lock Timeout Section 31
Changes to ADC Conversion Clock (ADC_CLK_DIV) Section 32
Changes to Phase Resync Clock Divider Value Section and Frequency Update Sequence Section 33
Changes to RF Synthesizer—A Worked Example Section 34
Changes to Lock Time Section and Automatic Level Calibration Timeout Section 35
Added Lock Time—A Worked Example Section 35

10/2014—Revision 0: Initial Version

SPECIFICATIONS

AV_{DD} = DV_{DD} = V_{RF} = 3.3 V ± 5%, 4.75 V ≤ V_P = V_{VCO} ≤ 5.25 V, A_{GND} = CP_{GND} = A_{GNDVCO} = SD_{GND} = A_{GNDRF} = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
$REF_{IN}A$/$REF_{IN}B$ CHARACTERISTICS						
Input Frequency						For f < 10 MHz, ensure slew rate > 21 V/µs
Single-Ended Mode		10		250	MHz	
Differential Mode		10		600	MHz	
Doubler Enabled				100	MHz	Doubler is set in Register 4, Bit DB26
Input Sensitivity						
Single-Ended Mode		0.4		AV_{DD}	V p-p	$REF_{IN}A$ biased at AV_{DD}/2; ac coupling ensures AV_{DD}/2 bias
Differential Mode		0.4		1.8	V p-p	LVDS and LVPECL compatible, $REF_{IN}A$/$REF_{IN}B$ biased at 2.1 V; ac coupling ensures 2.1 V bias
Input Capacitance						
Single-Ended Mode			6.9		pF	
Differential Mode			1.4		pF	
Input Current				±60	µA	Single-ended reference programmed
				±250	µA	Differential reference programmed
Phase Detector Frequency				125	MHz	
CHARGE PUMP (CP)						
Charge Pump Current, Sink/Source	I_{CP}					R_{SET} = 5.1 kΩ
High Value			4.8		mA	
Low Value			0.3		mA	
R_{SET} Range			5.1		kΩ	Fixed
Current Matching			3		%	0.5 V ≤ V_{CP}[1] ≤ V_P − 0.5 V
I_{CP} vs. V_{CP}			3		%	0.5 V ≤ V_{CP}[1] ≤ V_P − 0.5 V
I_{CP} vs. Temperature			1.5		%	V_{CP}[1] = 2.5 V
LOGIC INPUTS						
Input High Voltage	V_{INH}	1.5			V	
Input Low Voltage	V_{INL}			0.6	V	
Input Current	I_{INH}/I_{INL}			±1	µA	
Input Capacitance	C_{IN}		3.0		pF	
LOGIC OUTPUTS						
Output High Voltage	V_{OH}	DV_{DD} − 0.4			V	
		1.5	1.8		V	1.8 V output selected
Output High Current	I_{OH}			500	µA	
Output Low Voltage	V_{OL}			0.4	V	I_{OL}[2] = 500 µA
POWER SUPPLIES						See Table 6
Analog Power	AV_{DD}	3.15		3.45	V	
Digital Power and RF Supply Voltage	DV_{DD}, V_{RF}		AV_{DD}			Voltages must equal AV_{DD}
Charge Pump and VCO Supply Voltage	V_P, V_{VCO}	4.75	5.0	5.25	V	V_P must equal V_{VCO}
Charge Pump Supply Power Current	I_P		8	9		
DI_{DD} + AI_{DD}[3]			62	69	mA	
Output Dividers			6 to 36		mA	Each output divide by 2 consumes 6 mA
Supply Current	I_{VCO}		70	85	mA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
$RF_{OUT}A\pm/RF_{OUT}B$ Supply Current	$I_{RF_{OUT}x\pm}$					$RF_{OUT}A\pm$ output stage is programmable; enabling $RF_{OUT}B$ draws negligible extra current
			16	20	mA	−4 dBm setting
			30	35	mA	−1 dBm setting
			42	50	mA	2 dBm setting
			55	70	mA	5 dBm setting
Low Power Sleep Mode			500		µA	Hardware power-down selected
			1000		µA	Software power-down selected
RF OUTPUT CHARACTERISTICS						
VCO Frequency Range		3400		6800	MHz	Fundamental VCO range
$RF_{OUT}B$ Output Frequency		6800		13600	MHz	2× VCO output ($RF_{OUT}B$)
$RF_{OUT}A+/RF_{OUT}A-$ Output Frequency		53.125		6800	MHz	
VCO Sensitivity	K_V		15		MHz/V	
Frequency Pushing (Open-Loop)			15		MHz/V	
Frequency Pulling (Open-Loop)			0.5		MHz	Voltage standing wave ratio (VSWR) = 2:1 $RF_{OUT}A+/RF_{OUT}A-$
			30		MHz	VSWR = 2:1 $RF_{OUT}B$
Harmonic Content						
Second			−27		dBc	Fundamental VCO output ($RF_{OUT}A+$)
			−22		dBc	Divided VCO output ($RF_{OUT}A+$)
Third			−20		dBc	Fundamental VCO output ($RF_{OUT}A+$)
			−12		dBc	Divided VCO output ($RF_{OUT}A+$)
Fundamental VCO Feedthrough			−8		dBm	$RF_{OUT}B$ = 10 GHz
			−55		dBc	$RF_{OUT}A+/RF_{OUT}A-$ = 1 GHz; VCO frequency = 4 GHz
RF Output Power[4]			+8		dBm	$RF_{OUT}A+$ = 1 GHz; 7.5 nH inductor to V_{RF}
			−3		dBm	$RF_{OUT}A+/RF_{OUT}A-$ = 6.8 GHz; 7.5 nH inductor to V_{RF}
			1		dBm	$RF_{OUT}B$ = 6.8 GHz
			−1		dBm	$RF_{OUT}B$ = 13.6 GHz
RF Output Power Variation			±1		dB	$RF_{OUT}A+/RF_{OUT}A-$ = 5 GHz
			±1		dB	$RF_{OUT}B$ = 10 GHz
RF Output Power Variation (over Frequency)			±6		dB	$RF_{OUT}A+/RF_{OUT}A-$ = 1 GHz to 6.8 GHz
			±4		dB	$RF_{OUT}B$ = 6.8 GHz to 13.6 GHz
Level of Signal with RF Output Disabled			−60		dBm	$RF_{OUT}A+/RF_{OUT}A-$ = 1 GHz
			−30		dBm	$RF_{OUT}A+/RF_{OUT}A-$ = 6.8 GHz
			−15		dBm	$RF_{OUT}B$ = 6.8 GHz
			−17		dBm	$RF_{OUT}B$ = 13.6 GHz
NOISE CHARACTERISTICS						
Fundamental VCO Phase Noise Performance						VCO noise in open-loop conditions
			−116		dBc/Hz	100 kHz offset from 3.4 GHz carrier
			−136		dBc/Hz	800 kHz offset from 3.4 GHz carrier
			−138		dBc/Hz	1 MHz offset from 3.4 GHz carrier
			−155		dBc/Hz	10 MHz offset from 3.4 GHz carrier
			−113		dBc/Hz	100 kHz offset from 5.0 GHz carrier
			−133		dBc/Hz	800 kHz offset from 5.0 GHz carrier
			−135		dBc/Hz	1 MHz offset from 5.0 GHz carrier
			−153		dBc/Hz	10 MHz offset from 5.0 GHz carrier
			−110		dBc/Hz	100 kHz offset from 6.8 GHz carrier
			−130		dBc/Hz	800 kHz offset from 6.8 GHz carrier
			−132		dBc/Hz	1 MHz offset from 6.8 GHz carrier
			−150		dBc/Hz	10 MHz offset from 6.8 GHz carrier

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
VCO 2× Phase Noise Performance						VCO noise in open-loop conditions
			−110		dBc/Hz	100 kHz offset from 6.8 GHz carrier
			−130		dBc/Hz	800 kHz offset from 6.8 GHz carrier
			−132		dBc/Hz	1 MHz offset from 6.8 GHz carrier
			−149		dBc/Hz	10 MHz offset from 6.8 GHz carrier
			−107		dBc/Hz	100 kHz offset from 10 GHz carrier
			−127		dBc/Hz	800 kHz offset from 10 GHz carrier
			−129		dBc/Hz	1 MHz offset from 10 GHz carrier
			−147		dBc/Hz	10 MHz offset from 10 GHz carrier
			−103		dBc/Hz	100 kHz offset from 13.6 GHz carrier
			−124		dBc/Hz	800 kHz offset from 13.6 GHz carrier
			−126		dBc/Hz	1 MHz offset from 13.6 GHz carrier
			−144		dBc/Hz	10 MHz offset from 13.6 GHz carrier
Normalized In-Band Phase Noise Floor						
Fractional Channel[5]			−221		dBc/Hz	
Integer Channel[6]			−223		dBc/Hz	
Normalized 1/f Noise, PN_{1_f}[7]			−116		dBc/Hz	10 kHz offset; normalized to 1 GHz
Integrated RMS Jitter			150		fs	
Spurious Signals due to PFD Frequency			−80		dBc	

[1] V_{CP} is the voltage at the CP_{OUT} pin.
[2] I_{OL} is the output low current.
[3] T_A = 25°C; AV_{DD} = DV_{DD} = V_{RF} = 3.3 V; V_{VCO} = V_P = 5.0 V; prescaler = 4/5; f_{REFIN} = 122.88 MHz; f_{PFD} = 61.44 MHz; and f_{RF} = 1650 MHz. For the nominal DI_{DD} + AI_{DD} (62 mA): DI_{DD} = 15 mA (typical), AI_{DD} (Pin 5) = 24 mA (typical), AI_{DD} (Pin 16) = 23 mA (typical).
[4] RF output power using the EV-ADF5355SD1Z evaluation board measured into a spectrum analyzer, with board and cable losses de-embedded. Unused RF output pins are terminated in 50 Ω.
[5] Use this value to calculate the phase noise for any application. To calculate in-band phase noise performance as seen at the VCO output, use the following formula: −221 + 10log(f_{PFD}) + 20logN. The value given is the lowest noise mode for the fractional channel.
[6] Use this value to calculate the phase noise for any application. To calculate in-band phase noise performance as seen at the VCO output, use the following formula: −223 + 10log(f_{PFD}) + 20logN. The value given is the lowest noise mode for the integer channel.
[7] The PLL phase noise is composed of 1/f (flicker) noise plus the normalized PLL noise floor. The formula for calculating the 1/f noise contribution at an RF frequency (f_{RF}) and at a frequency offset (f) is given by PN = P_{1_f} + 10log(10 kHz/f) + 20log(f_{RF}/1 GHz). Both the normalized phase noise floor and flicker noise are modeled in the ADIsimPLL design tool.

TIMING CHARACTERISTICS

AV_{DD} = DV_{DD} = V_{RF} = 3.3 V ± 5%, 4.75 V ≤ V_P = V_{VCO} ≤ 5.25 V, A_{GND} = CP_{GND} = A_{GNDVCO} = SD_{GND} = A_{GNDRF} = 0 V, R_{SET} = 5.1 kΩ, dBm referred to 50 Ω, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. Write Timing

Parameter	Limit	Unit	Description
f_{CLK}	50	MHz max	Serial peripheral interface CLK frequency
t_1	10	ns min	LE setup time
t_2	5	ns min	DATA to CLK setup time
t_3	5	ns min	DATA to CLK hold time
t_4	10	ns min	CLK high duration
t_5	10	ns min	CLK low duration
t_6	5	ns min	CLK to LE setup time
t_7	20 (or 2/f_{PFD}, whichever is longer)	ns min	LE pulse width

Write Timing Diagram

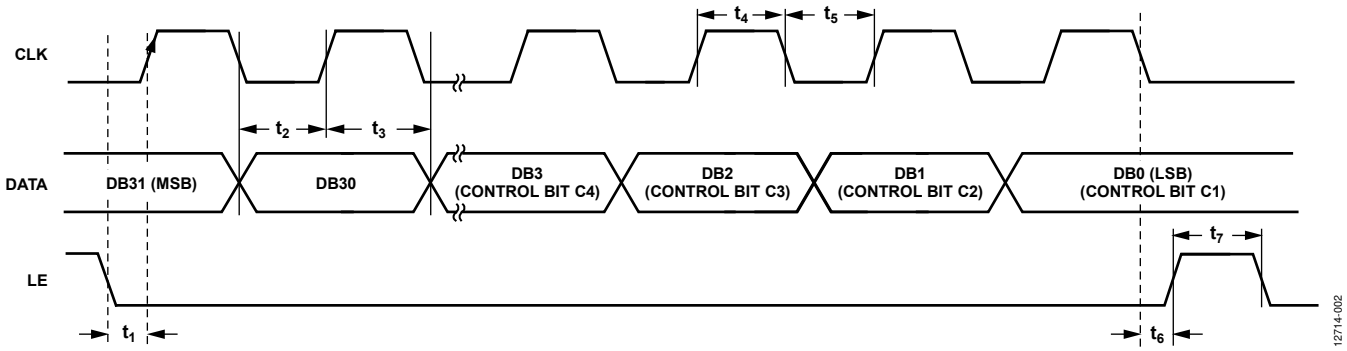


Figure 2. Write Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{RF}, DV_{DD}, AV_{DD} to GND[1, 2]	−0.3 V to +3.6 V
AV_{DD} to DV_{DD}	−0.3 V to +0.3 V
V_P, V_{VCO} to GND[1]	−0.3 V to +5.8 V
CP_{OUT} to GND[1]	−0.3 V to V_P + 0.3 V
Digital Input/Output Voltage to GND[1]	−0.3 V to DV_{DD} + 0.3 V
Analog Input/Output Voltage to GND[1]	−0.3 V to AV_{DD} + 0.3 V
$REF_{IN}A$, $REF_{IN}B$ to GND[1]	−0.3 V to AV_{DD} + 0.3 V
$REF_{IN}A$ to $REF_{IN}B$	±2.1 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
θ_{JA}, Thermal Impedance Paddle Soldered to GND[1]	27.3°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
Electrostatic Discharge (ESD)	
Charged Device Model	1000 V
Human Body Model	2500 V

[1] GND = A_{GND} = SD_{GND} = A_{GNDRF} = A_{GNDVCO} = CP_{GND} = 0 V.
[2] Do not connect V_{RF} to DV_{DD}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

The ADF5355 is a high performance RF integrated circuit with an ESD rating of 2.5 kV and is ESD sensitive. Take proper precautions for handling and assembly.

TRANSISTOR COUNT

The transistor count for the ADF5355 is 103,665 (CMOS) and 3214 (bipolar).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

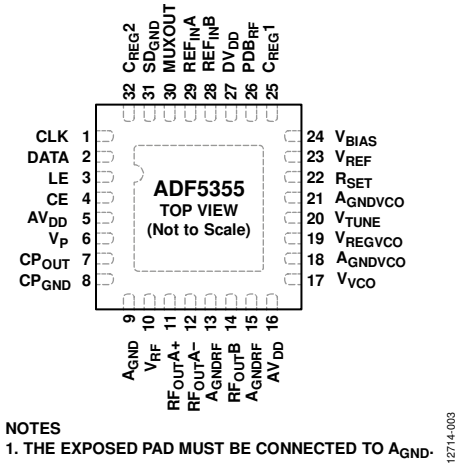


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CLK	Serial Clock Input. Data is clocked into the 32-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
2	DATA	Serial Data Input. The serial data is loaded most significant bit (MSB) first with the four least significant bits (LSBs) as the control bits. This input is a high impedance CMOS input.
3	LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift register is loaded into the register that is selected by the four LSBs.
4	CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump into three-state mode. A logic high (at levels equal to DV_{DD}) on this pin powers up the device, depending on the status of the power-down bits. Register contents are retained unless the supply voltages are removed.
5, 16	AV_{DD}	Analog Power Supply. This pin ranges from 3.15 V to 3.45 V. Connect decoupling capacitors to the analog ground plane as close to this pin as possible. AV_{DD} must have the same value as DV_{DD}.
6	V_P	Charge Pump Power Supply. V_P must have the same value as V_{VCO}. Connect decoupling capacitors to the ground plane as close to this pin as possible.
7	CP_{OUT}	Charge Pump Output. When enabled, this output provides $\pm I_{CP}$ to the external loop filter. The output of the loop filter is connected to V_{TUNE} to drive the internal VCO.
8	CP_{GND}	Charge Pump Ground. This output is the ground return pin for CP_{OUT}.
9	A_{GND}	Analog Ground. Ground return pin for AV_{DD}.
10	V_{RF}	Power Supply for the RF Output. Connect decoupling capacitors to the analog ground plane as close to this pin as possible. V_{RF} must have the same value as AV_{DD}. Do not connect V_{RF} to DV_{DD}.
11	$RF_{OUT}A+$	VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available. This pin can be left floating if $RF_{OUT}A$ is disabled in Register 6 or by the PDB_{RF} pin.
12	$RF_{OUT}A–$	Complementary VCO Output. The output level is programmable. The VCO fundamental output or a divided down version is available. This pin can be left floating if $RF_{OUT}A$ is disabled in Register 6 or by the PDB_{RF} pin.
13, 15	A_{GNDRF}	RF Output Stage Ground. Ground return pins for the RF output stage.
14	$RF_{OUT}B$	Auxiliary VCO Output. The 2× VCO output is available at this pin.
17	V_{VCO}	Power Supply for the VCO. The voltage on this pin ranges from 4.75 V to 5.25 V. Place decoupling capacitors to the analog ground plane as close to this pin as possible. For best performance, this supply must be clean and have low noise.
18, 21	A_{GNDVCO}	VCO Ground. Ground return path for the VCO.
19	V_{REGVCO}	VCO Compensation Node. Place decoupling capacitors to the ground plane as close to this pin as possible. Connect this pin directly to V_{VCO}.
20	V_{TUNE}	Control Input to the VCO. This voltage determines the output frequency and is derived from filtering the CP_{OUT} output voltage. The input capacitance of this pin is 9 pF.
22	R_{SET}	No Connection. Charge pump bias resistance is internal.

Pin No.	Mnemonic	Description
23	V_{REF}	Internal Compensation Node. DC biased at half the tuning range. Connect decoupling capacitors to the ground plane as close to this pin as possible.
24	V_{BIAS}	Reference Voltage. Connect a 100 nF decoupling capacitor to the ground plane as close to this pin as possible.
25, 32	$C_{REG}1$, $C_{REG}2$	Outputs from the LDO Regulator. Pin 25 and Pin 32 are the supply voltages to the digital circuits. Nominal voltage of 1.8 V. Decoupling capacitors of 100 nF connected to A_{GND} are required for these pins.
26	PDB_{RF}	$RF_{OUT}A$ Power-Down. A logic low on this pin powers down the $RF_{OUT}A\pm$ outputs only. This power-down function is also software controllable. Do not leave this pin floating.
27	DV_{DD}	Digital Power Supply. This pin must be at the same voltage as AV_{DD}. Do not connect to V_{RF}. Place decoupling capacitors to the ground plane as close to this pin as possible.
28	$REF_{IN}B$	Complementary Reference Input. If unused, ac couple this pin to A_{GND}.
29	$REF_{IN}A$	Reference Input.
30	MUXOUT	Multiplexer Output. The multiplexer output allows the digital lock detect, the analog lock detect, scaled RF, or the scaled reference frequency to be externally accessible.
31	SD_{GND}	Digital Σ-Δ Modulator Ground. Pin 31 is the ground return path for the Σ-Δ modulator.
	EPAD	Exposed Pad. The exposed pad must be connected to A_{GND}.

TYPICAL PERFORMANCE CHARACTERISTICS

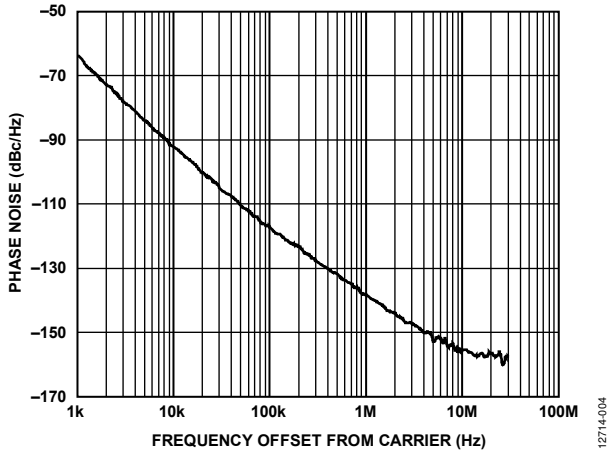


Figure 4. Open-Loop VCO Phase Noise, 3.4 GHz

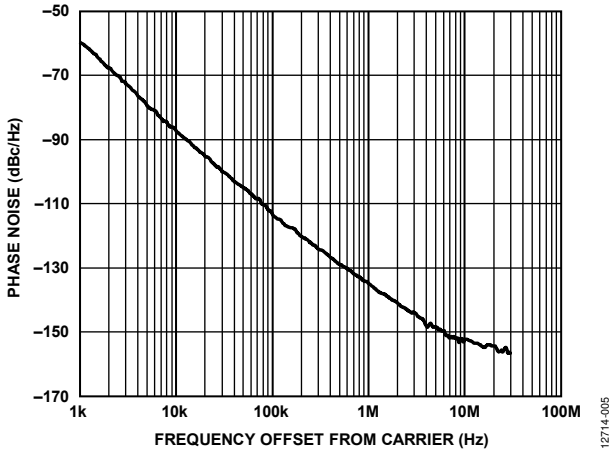


Figure 5. Open-Loop VCO Phase Noise, 5.0 GHz

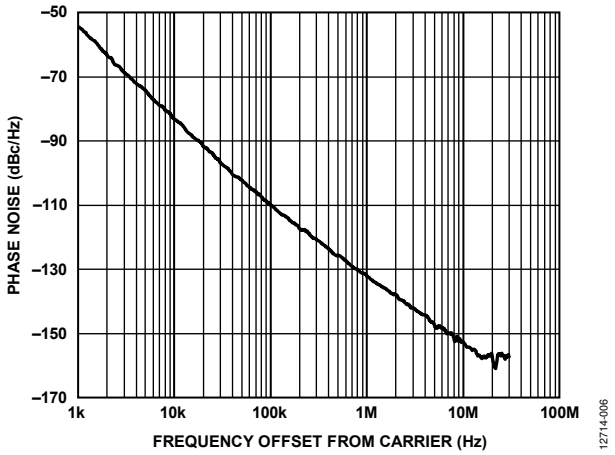


Figure 6. Open-Loop VCO Phase Noise, 6.8 GHz

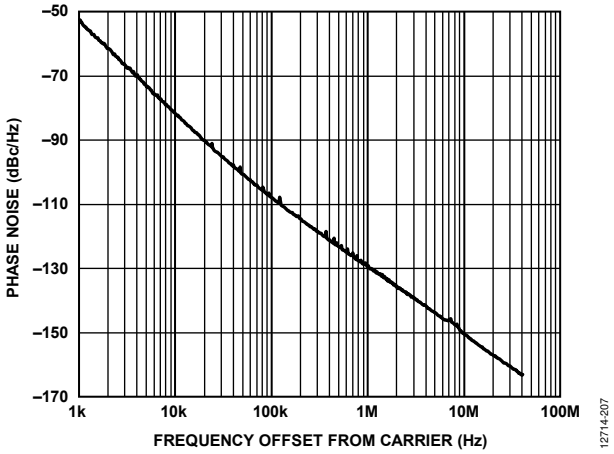


Figure 7. Open-Loop VCO Phase Noise, 8.0 GHz

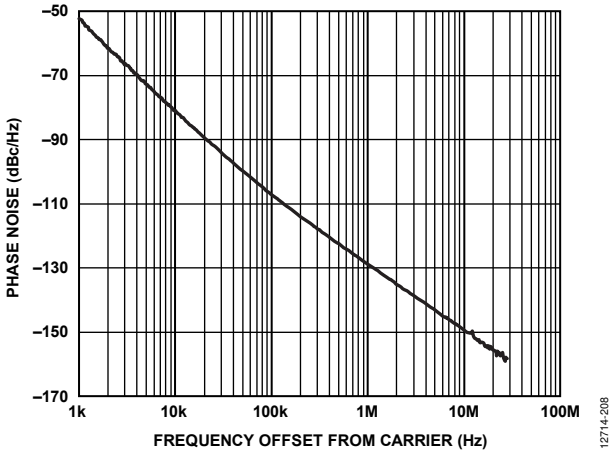


Figure 8. Open-Loop VCO Phase Noise, 10.0 GHz

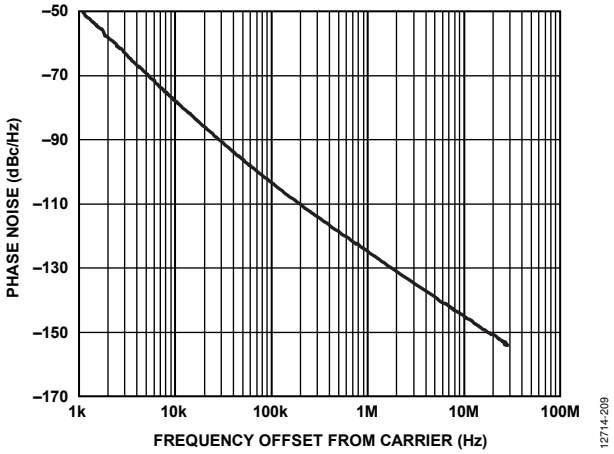


Figure 9. Open-Loop VCO Phase Noise, 13.6 GHz

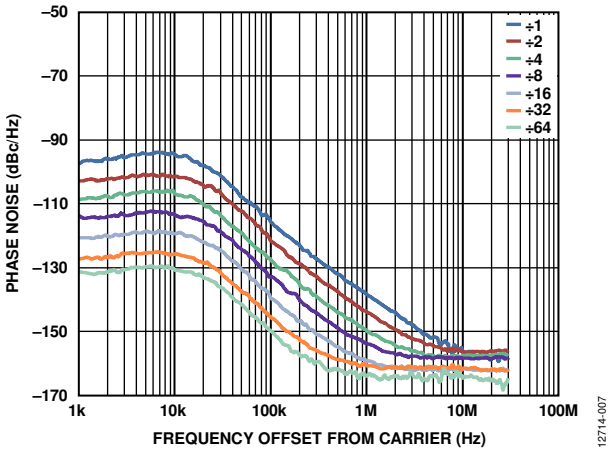


Figure 10. Closed-Loop Phase Noise, $RF_{OUT}A+$, Fundamental VCO and Dividers, VCO = 3.4 GHz, f_{PFD} = 61.44 MHz, Loop Bandwidth = 20 kHz

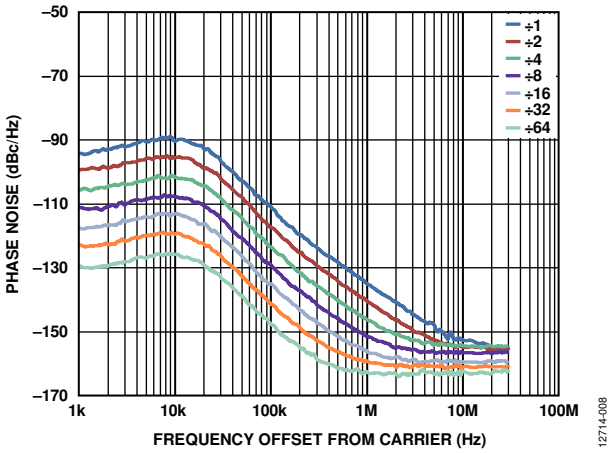


Figure 11. Closed-Loop Phase Noise, $RF_{OUT}A+$, Fundamental VCO and Dividers, VCO = 5.0 GHz, f_{PFD} = 61.44 MHz, Loop Bandwidth = 20 kHz

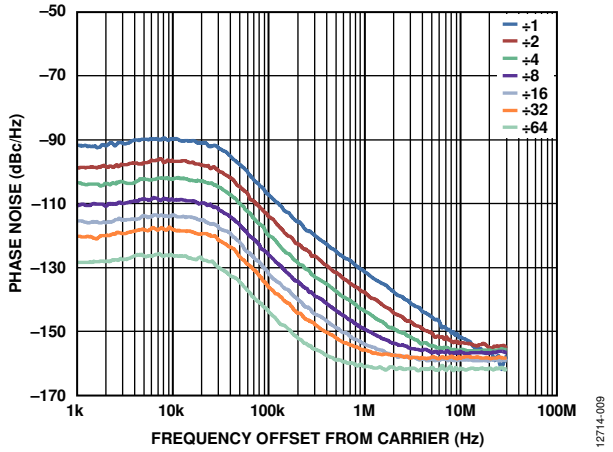


Figure 12. Closed-Loop Phase Noise, $RF_{OUT}A+$, Fundamental VCO and Dividers, VCO = 6.8 GHz, f_{PFD} = 61.44 MHz, Loop Bandwidth = 20 kHz

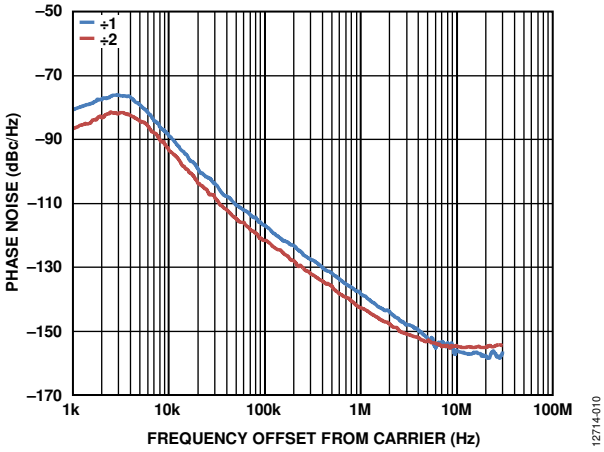


Figure 13. Closed-Loop Phase Noise, $RF_{OUT}A+$, Fundamental VCO and Divide by 2, VCO = 3.4 GHz, f_{PFD} = 61.44 MHz, Loop Bandwidth = 2 kHz

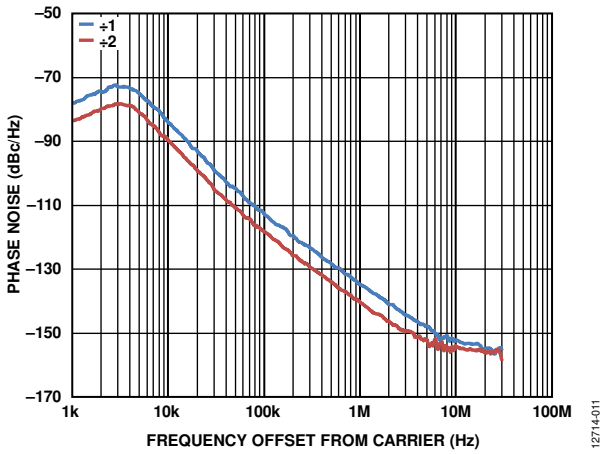


Figure 14. Closed-Loop Phase Noise, $RF_{OUT}A+$, Fundamental VCO and Divide by 2, VCO = 5.0 GHz, f_{PFD} = 61.44 MHz, Loop Bandwidth = 2 kHz

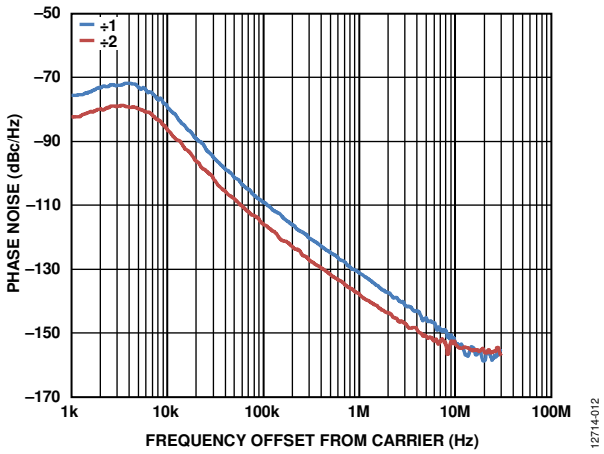


Figure 15. Closed-Loop Phase Noise, $RF_{OUT}A+$, Fundamental VCO and Divide by 2, VCO = 6.8 GHz, f_{PFD} = 61.44 MHz, Loop Bandwidth = 2 kHz

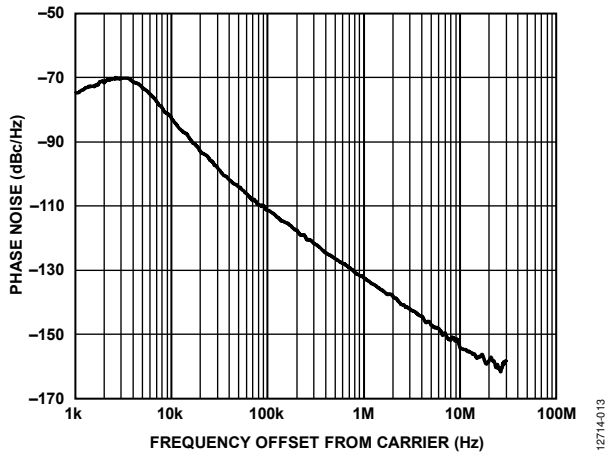


Figure 16. Closed-Loop Phase Noise, $RF_{OUT}B$ = 6.8 GHz, 2× VCO, VCO = 3.4 GHz, f_{PFD} = 61.44 MHz, Loop Bandwidth = 2 kHz

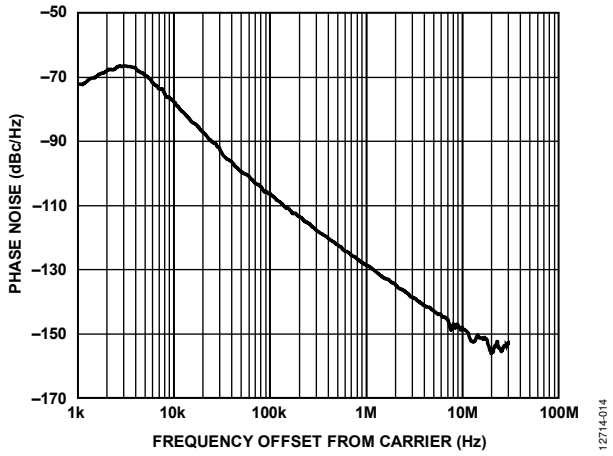


Figure 17. Closed-Loop Phase Noise, $RF_{OUT}B$ = 10 GHz, 2× VCO, VCO = 5.0 GHz, f_{PFD} = 61.44 MHz, Loop Bandwidth = 2 kHz

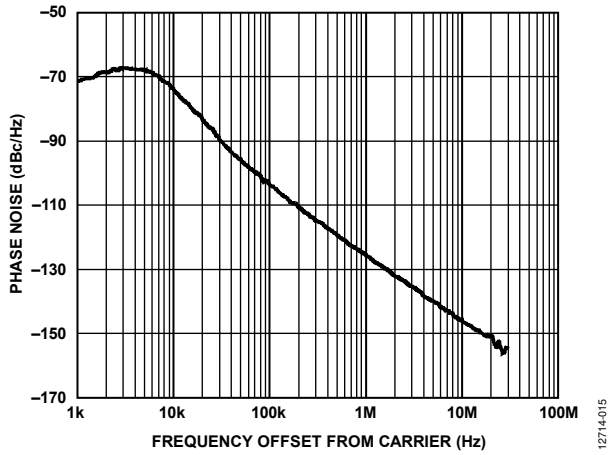


Figure 18. Closed-Loop Phase Noise, $RF_{OUT}B$ = 13.6 GHz, 2× VCO, VCO = 6.8 GHz, f_{PFD} = 61.44 MHz, Loop Bandwidth = 2 kHz

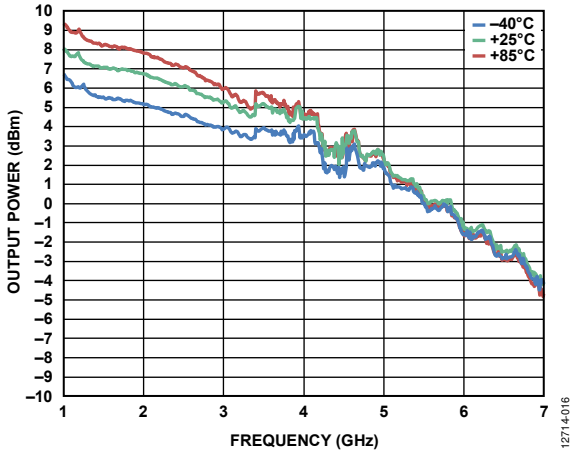


Figure 19. Output Power vs. Frequency, $RF_{OUT}A+/RF_{OUT}A-$ (7.5 nH Inductors, 10 pF Bypass Capacitors, Board Losses De-Embedded)

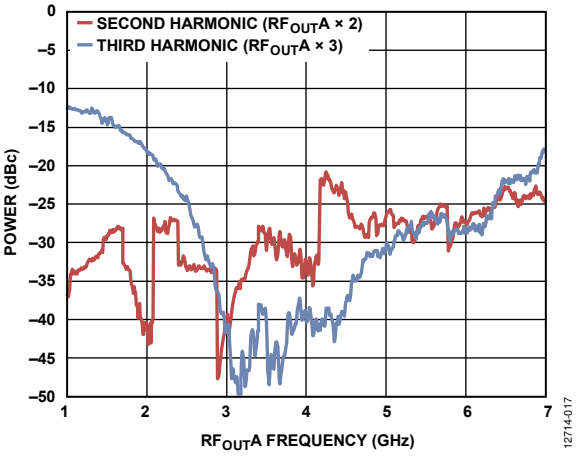


Figure 20. $RF_{OUT}A+/RF_{OUT}A-$ Harmonics vs. Frequency (7.5 nH Inductors, 10 pF Bypass Capacitors, Board Losses De-Embedded)

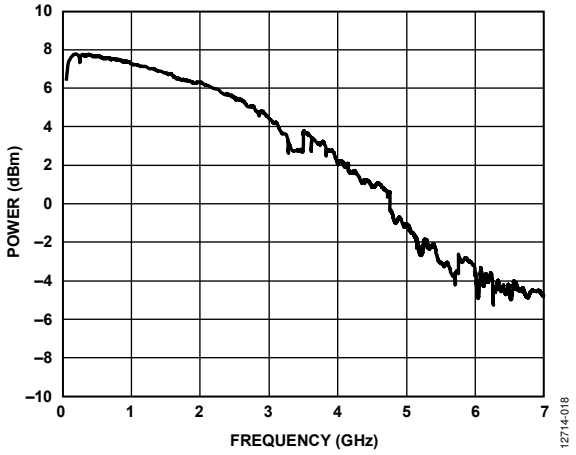


Figure 21. $RF_{OUT}A+/RF_{OUT}A-$ Power vs. Frequency (100 nH Inductors, 100 pF Bypass Capacitors, Board Measurement)

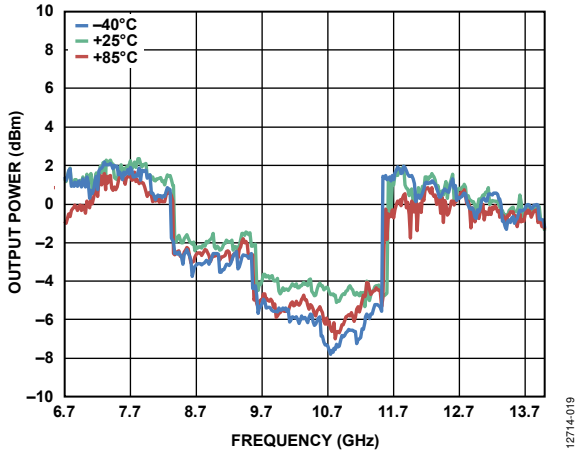


Figure 22. Output Power vs. Frequency, $RF_{OUT}B$ (10 pF Bypass Capacitor De-Embedded)

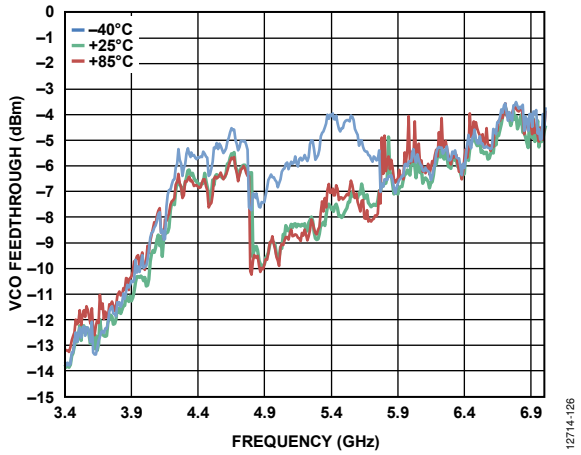


Figure 23. VCO Feedthrough at $RF_{OUT}B$ (De-Embedded) vs. Fundamental VCO Frequency

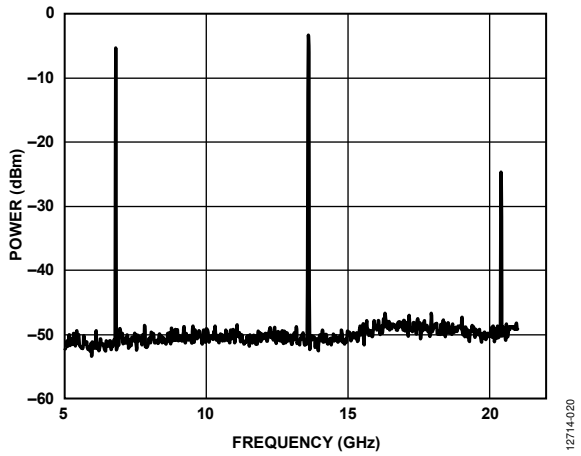


Figure 24. Wideband Spectrum, $RF_{OUT}B$, VCO = 6.8 GHz, $RF_{OUT}B$ Enabled, $RF_{OUT}A+/RF_{OUT}A–$ Disabled (Board Measurement)

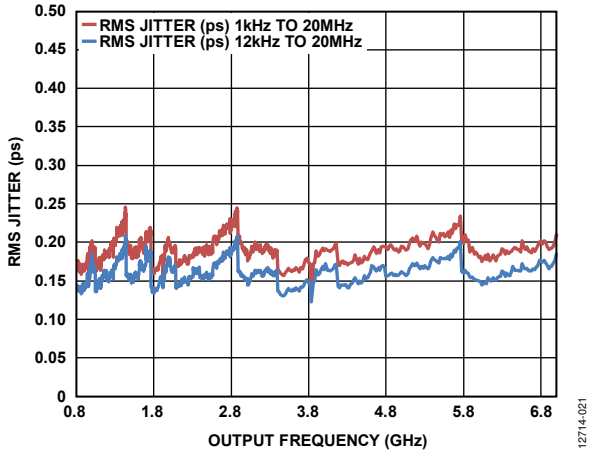


Figure 25. RMS Jitter vs. Output Frequency, f_{PFD} = 61.44 MHz, Loop Filter = 20 kHz

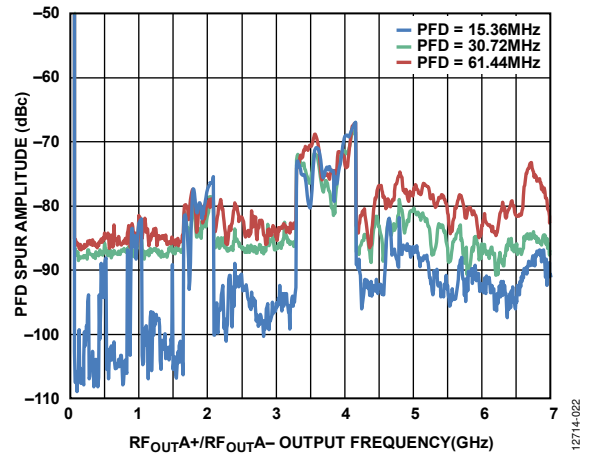


Figure 26. PFD Spur Amplitude vs. $RF_{OUT}A+/RF_{OUT}A–$ Output Frequency; f_{PFD} = 61.44 MHz, f_{PFD} = 30.72 MHz, and f_{PFD} = 15.36 MHz; Loop Filter = 20 kHz

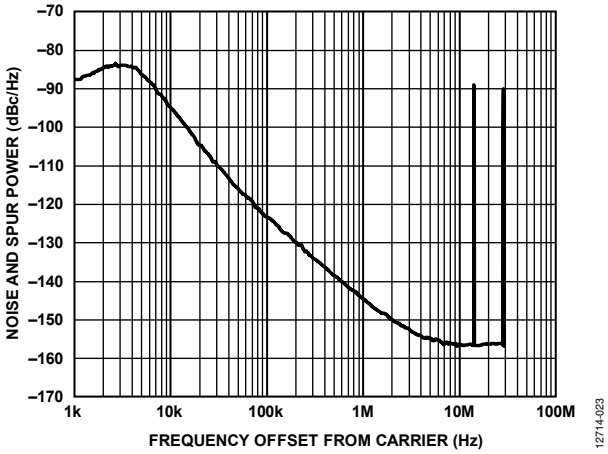


Figure 27. Fractional-N Spur Performance, GSM1800 Band, $RF_{OUT}A+$ = 1550.2 MHz, REF_{IN} = 122.88 MHz, f_{PFD} = 61.44 MHz, Output Divide by 4 Selected, Loop Filter Bandwidth = 2 kHz, Channel Spacing = 20 kHz

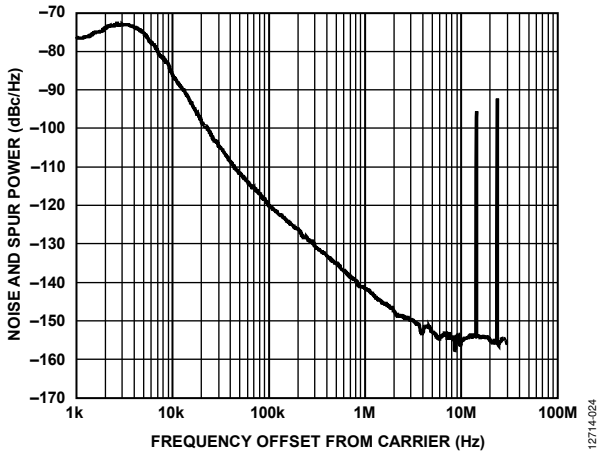


Figure 28. Fractional-N Spur Performance, W-CDMA Band, $RF_{OUT}A+$ = 2113.5 MHz, REF_{IN} = 122.88 MHz, f_{PFD} = 61.44 MHz, Output Divide by 2 Selected, Loop Filter Bandwidth = 2 kHz, Channel Spacing = 20 kHz

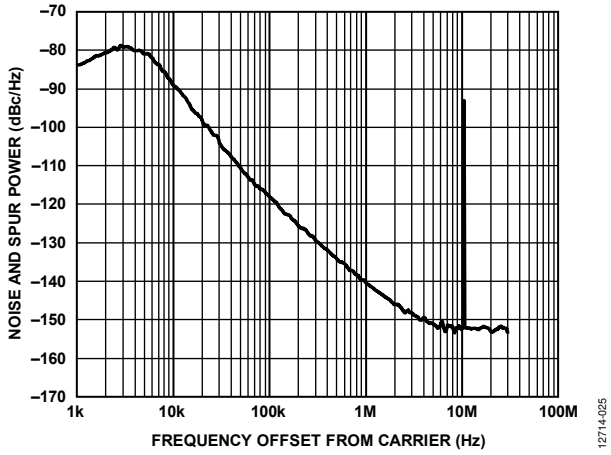


Figure 29. Fractional-N Spur Performance, $RF_{OUT}A+$ = 2.591 GHz, REF_{IN} = 122.88 MHz, f_{PFD} = 61.44 MHz, Output Divide by 2 Selected, Loop Filter Bandwidth = 2 kHz, Channel Spacing = 20 kHz

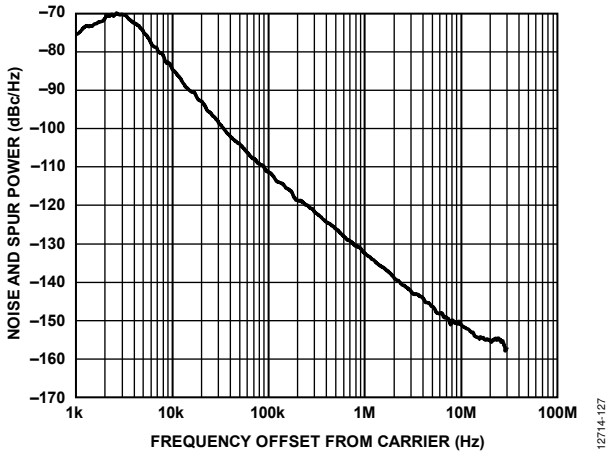


Figure 30. Fractional-N Spur Performance, $RF_{OUT}A+$ = 5.8 GHz, REF_{IN} = 122.88 MHz, f_{PFD} = 61.44 MHz, Output Divide by 2 Selected, Loop Filter Bandwidth = 2 kHz, Channel Spacing = 20 kHz

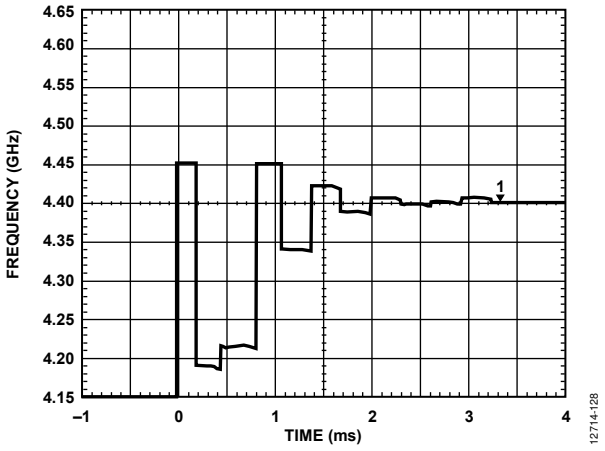


Figure 31. Lock Time for 250 MHz Jump from 4150 MHz to 4400 MHz, Loop Bandwidth = 20 kHz

CIRCUIT DESCRIPTION

REFERENCE INPUT

Figure 32 shows the reference input stage. The reference input can accept both single-ended and differential signals. Use the reference mode bit (Register 4, DB9) to select the signal. To use a differential signal on the reference input, program this bit high. In this case, SW1 and SW2 are open, SW3 and SW4 are closed, and the current source that drives the differential pair of transistors switches on (see Figure 32). The differential signal is buffered, and it is provided to an emitter coupled logic (ECL) to CMOS converter. When a single-ended signal is used as the reference, connect the reference signal to $REF_{IN}A$ and program Bit DB9 in Register 4 to 0. In this case, SW1 and SW2 are closed, SW3 and SW4 are open, and the current source that drives the differential pair of transistors switches off. Single-ended mode results in lower integer boundary spurs.

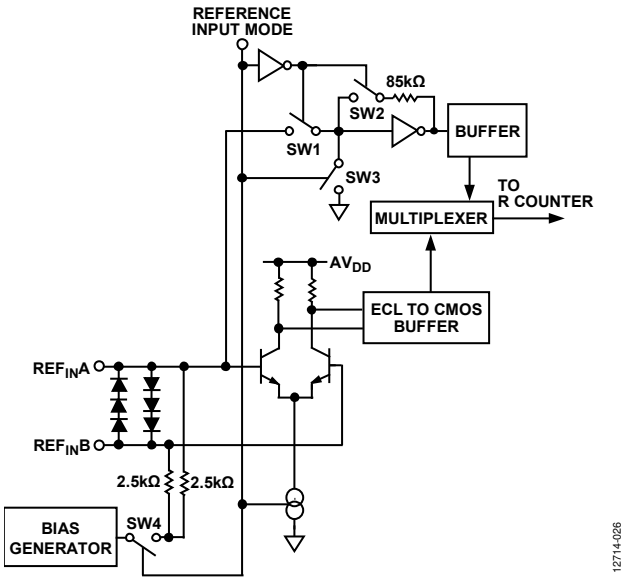


Figure 32. Reference Input Stage

RF N DIVIDER

The RF N divider allows a division ratio in the PLL feedback path. Determine the division ratio by the INT, FRAC1, FRAC2, and MOD2 values that this divider comprises.

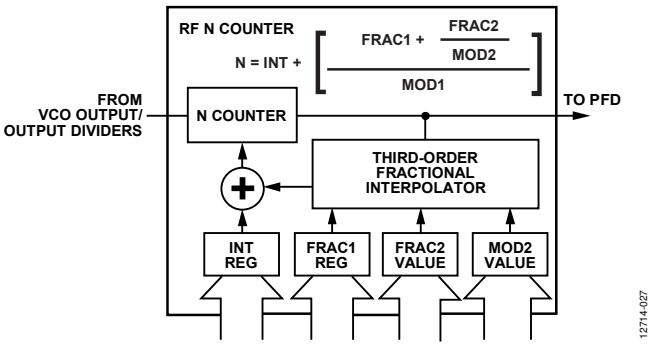


Figure 33. RF N Divider

INT, FRAC, MOD, and R Counter Relationship

The INT, FRAC1, FRAC2, MOD1, and MOD2 values, in conjunction with the R counter, make it possible to generate output frequencies that are spaced by fractions of the PFD frequency (f_{PFD}). For more information, see the RF Synthesizer—A Worked Example section.

Calculate the VCO output frequency (VCO_{OUT}) by

$$VCO_{OUT} = f_{PFD} \times N \quad (1)$$

where:
VCO_{OUT} is the output frequency of the external VCO voltage controlled oscillator (without using the output divider).
f_{PFD} is the frequency of the phase frequency detector.
N is the desired value of the feedback counter, N.

Calculate f_{PFD} by

$$f_{PFD} = REF_{IN} \times [(1 + D)/(R \times (1 + T))] \quad (2)$$

where:
REF_{IN} is the reference input frequency.
D is the REF_{IN} doubler bit.
R is the preset divide ratio of the binary 10-bit programmable reference counter (1 to 1023).
T is the REF_{IN} divide by 2 bit (0 or 1)

N comprises

$$N = INT + \frac{FRAC1 + \frac{FRAC2}{MOD2}}{MOD1} \quad (3)$$

where:
INT is the 16-bit integer value (23 to 32,767 for 4/5 prescaler, 75 to 65,535 for 8/9 prescaler).
FRAC1 is the numerator of the primary modulus (0 to 16,777,215).
FRAC2 is the numerator of the 14-bit auxiliary modulus (0 to 16,383).
MOD2 is the programmable, 14-bit auxiliary fractional modulus (2 to 16,383).
MOD1 is a 24-bit primary modulus with a fixed value of 2^{24} = 16,777,216.

This calculation results in a very fine frequency resolution with no residual frequency error. To apply this formula, take the following steps:

1. Calculate N by dividing VCO_{OUT}/f_{PFD}.
2. The integer value of this number forms INT.
3. Subtract this value from the full N value.
4. Multiply the remainder by 2^{24}.
5. The integer value of this number forms FRAC1.
6. Calculate MOD2 based on the channel spacing (f_{CHSP}) by

$$MOD2 = f_{PFD}/\text{GCD}(f_{PFD}, f_{CHSP}) \quad (4)$$

where:
f_{CHSP} is the desired channel spacing frequency.
GCD(f_{PFD}, f_{CHSP}) is the greatest common divisor of the PFD frequency and the channel spacing frequency.

7. Calculate FRAC2 by the following equation:

$$FRAC2 = [(N - INT) \times 2^{24} - FRAC1)] \times MOD2 \quad (5)$$

The FRAC2 and MOD2 fraction result in outputs with zero frequency error for channel spacings when

$$f_{PFD}/\text{GCD}(f_{PFD}, f_{CHSP}) = MOD2 < 16{,}383 \quad (6)$$

where:
f_{PFD} is the frequency of the phase frequency detector.
f_{CHSP} is the desired channel spacing.
GCD is a greatest common divisor function.

If zero frequency error is not required, the MOD1 and MOD2 denominators operate together to create a 38-bit resolution modulus.

INT N Mode

When FRAC1 and FRAC2 are 0, the synthesizer operates in integer-N mode.

R Counter

The 10-bit R counter allows the input reference frequency (REF_{IN}) to be divided down to produce the reference clock to the PFD. Division ratios from 1 to 1023 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 34 is a simplified schematic of the phase frequency detector. The PFD includes a fixed delay element (INT = 1.6 ns, FRAC = 2.6 ns) that sets the width of the anti-backlash pulse. This pulse ensures that there is no dead zone in the PFD transfer function and provides a consistent reference spur level. Set the phase detector polarity to positive on this device because of the positive tuning of the VCO.

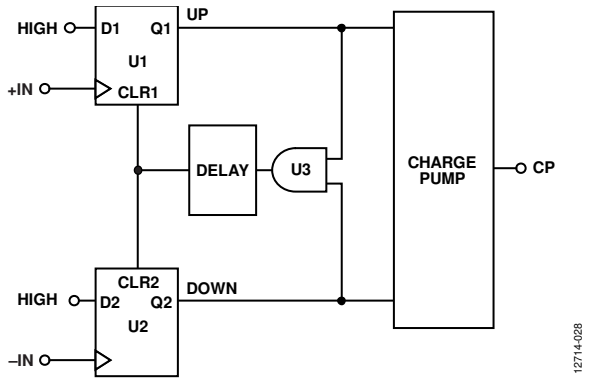


Figure 34. PFD Simplified Schematic

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF5355 allows the user to access various internal points on the chip. The M3, M2, and M1 bits in Register 4 control the state of MUXOUT. Figure 35 shows the MUXOUT section in block diagram form.

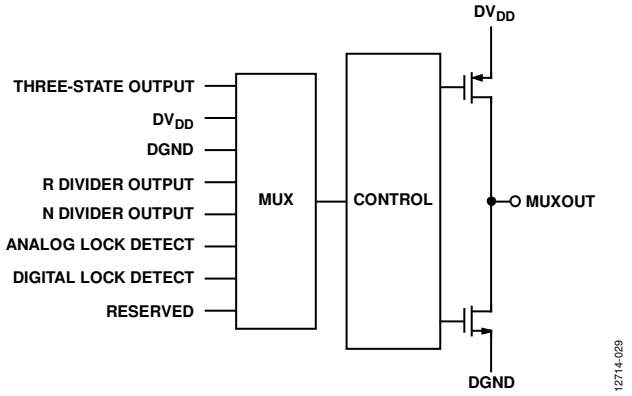


Figure 35. MUXOUT Schematic

INPUT SHIFT REGISTERS

The ADF5355 digital section includes a 10-bit R counter, a 16-bit RF integer-N counter, a 24-bit FRAC1 counter, a 14-bit auxiliary fractional counter, and a 14-bit auxiliary modulus counter. Data clocks into the 32-bit shift register on each rising edge of CLK. The data clocks in MSB first. Data transfers from the shift register to one of 13 latches on the rising edge of LE. The state of the four control bits (C4, C3, C2, and C1) in the shift register determines the destination latch. As shown in Figure 2, the four LSBs are DB3, DB2, DB1, and DB0. The truth table for these bits is shown in Table 5. Figure 39 and Figure 40 summarize the programming of the latches.

Table 5. Truth Table for the C4, C3, C2, and C1 Control Bits

Control Bits				
C4	**C3**	**C2**	**C1**	**Register**
0	0	0	0	Register 0
0	0	0	1	Register 1
0	0	1	0	Register 2
0	0	1	1	Register 3
0	1	0	0	Register 4
0	1	0	1	Register 5
0	1	1	0	Register 6
0	1	1	1	Register 7
1	0	0	0	Register 8
1	0	0	1	Register 9
1	0	1	0	Register 10
1	0	1	1	Register 11
1	1	0	0	Register 12

PROGRAM MODES

Table 5 and Figure 39 through Figure 53 show how the program modes must be set up in the ADF5355.

The following settings in the ADF5355 are double buffered: main fractional value (FRAC1), auxiliary modulus value (MOD2), auxiliary fractional value (FRAC2), reference doubler, reference divide by 2 (RDIV2), R counter value, and charge pump current setting. Two events must occur before the ADF5355 uses a new value for any of the double buffered settings. First, the new value must latch into the device by writing to the appropriate register, and second, a new write to Register 0 must be performed.

For example, to ensure that the modulus value loads correctly, every time that the modulus value updates, Register 0 must be written to. The RF divider select in Register 6 is also double buffered, but only if DB14 of Register 4 is high.

VCO

The VCO core in the ADF5355 consists of four separate VCOs, each of which uses 256 overlapping bands, which allows the device to cover a wide frequency range without large VCO sensitivity (K_V) and without resultant poor phase noise and spurious performance.

The correct VCO and band are chosen automatically by the VCO and band select logic whenever Register 0 is updated and automatic calibration is enabled. The VCO V_{TUNE} is disconnected from the output of the loop filter and is connected to an internal reference voltage.

The R counter output is used as the clock for the band select logic. After band selection, normal PLL action resumes. The nominal value of K_V is 15 MHz/V when the N divider is driven from the VCO output, or the K_V value is divided by D. D is the output divider value if the N divider is driven from the RF output divider (chosen by programming Bits[D23:D21] in Register 6).

The VCO shows variation of K_V as the tuning voltage, V_{TUNE}, varies within the band and from band to band. For wideband applications covering a wide frequency range (and changing output dividers), a value of 15 MHz/V provides the most accurate K_V, because this value is closest to the average value. Figure 36 shows how K_V varies with fundamental VCO frequency along with an average value for the frequency band. Users may prefer this figure when using narrow-band designs.

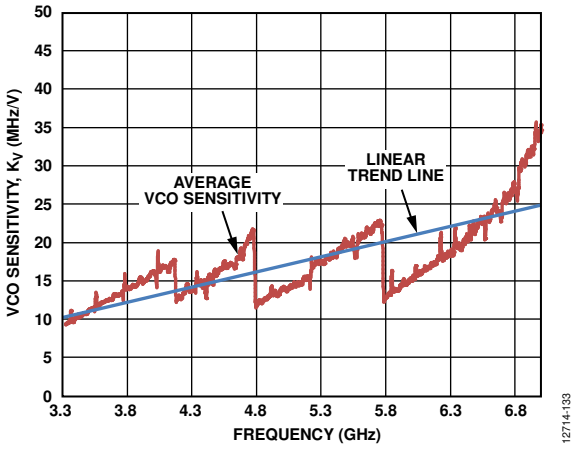


Figure 36. VCO Sensitivity, K_V vs. Frequency

OUTPUT STAGE

The $RF_{OUT}A+$ and $RF_{OUT}A-$ pins of the ADF5355 connect to the collectors of an NPN differential pair driven by buffered outputs of the VCO, as shown in Figure 37. In this scheme, the ADF5355 contains internal 50 Ω resistors connected to the V_{RF} pin. To optimize the power dissipation vs. the output power requirements, the tail current of the differential pair is programmable using Bits[D2:D1] in Register 6. Four current levels can be set. These levels give approximate output power levels of −4 dBm, −1 dBm, +2 dBm, and +5 dBm, respectively. Levels of −4 dBm, −1 dBm, +2 dBm can be achieved using a 50 Ω resistor to V_{RF} and ac coupling into a 50 Ω load. A +5 dBm level requires an external shunt inductor to V_{RF}. Note that an inductor has a narrower operating frequency than a 50 Ω resistor. For accurate power levels, refer to the Typical Performance Characteristics section. Add an external shunt inductor to provide higher power levels; however, this is less wideband than the internal bias only. Terminate the unused complementary output with a circuit similar to the used output.

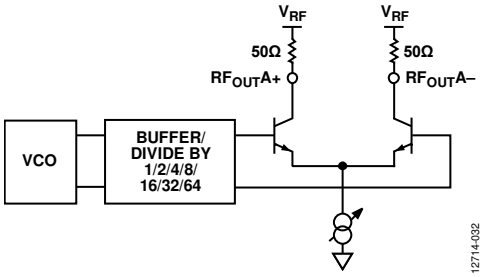


Figure 37. Output Stage

The doubled VCO output (6.8 GHz to 13.6 GHz) is available on the $RF_{OUT}B$ pin, which can be ac-coupled to the next circuit.

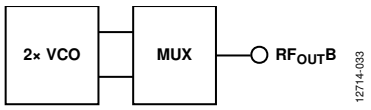


Figure 38. Output Stage

Another feature of the ADF5355 is that the supply current to the $RF_{OUT}A+/RF_{OUT}A-$ output stage can shut down until the ADF5355 achieves lock as measured by the digital lock detect circuitry. The mute till lock detect (MTLD) bit (Bit DB11) in Register 6 enables this function.

$RF_{OUT}B$ directly connects to the VCO, and it can be muted but only by using the $RF_{OUT}B$ bit (Bit DB10) in Register 6.

Table 6. Total I_{DD} ($RF_{OUT}A\pm$ Refers to $RF_{OUT}A+/RF_{OUT}A-$)

Divide By	$RF_{OUT}A\pm$ Off	$RF_{OUT}A\pm$ = −4 dBm	$RF_{OUT}A\pm$ = −1 dBm	$RF_{OUT}A\pm$ = +2 dBm	$RF_{OUT}A\pm$ = +5 dBm
5.0 V Supply (I_{VCO} and I_P)	78 mA	78 mA	78 mA	78 mA	78 mA
3.3 V Supply (AI_{DD}, DI_{DD}, I_{RF})[1]					
1	79.8 mA	101.3 mA	111.9 mA	122.7 mA	132.8 mA
2	87.8 mA	110.1 mA	120.6 mA	131.9 mA	141.9 mA
4	97.1 mA	119.3 mA	130.1 mA	141.6 mA	152.1 mA
8	104.9 mA	127.1 mA	137.8 mA	149.2 mA	159.7 mA
16	109.8 mA	131.8 mA	142.7 mA	154.1 mA	164.6 mA
32	113.6 mA	135.5 mA	146.5 mA	157.8 mA	168.4 mA
64	115.9 mA	137.8 mA	148.9 mA	160.1 mA	170.8 mA

[1] For DI_{DD} + AI_{DD} (nominal 62 mA): DI_{DD} = 15 mA (typical), AI_{DD} (Pin 5) = 24 mA (typical), AI_{DD} (Pin 16) = 23 mA (typical).

REGISTER MAPS

REGISTER 0

RESERVED										AUTOCAL	PRESCALER	16-BIT INTEGER VALUE (INT)														CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	0	AC1	PR1	N16	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	C4(0)	C3(0)	C2(0)	C1(0)

REGISTER 1

RESERVED				24-BIT MAIN FRACTIONAL VALUE (FRAC1) DBR[1]																						CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	F24	F23	F22	F21	F20	F19	F18	F17	F16	F15	F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	C4(0)	C3(0)	C2(0)	C1(1)

REGISTER 2

14-BIT AUXILIARY FRACTIONAL VALUE (FRAC2) DBR[1]														14-BIT AUXILIARY MODULUS VALUE (MOD2) DBR[1]												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
F14	F13	F12	F11	F10	F9	F8	F7	F6	F5	F4	F3	F2	F1	M14	M13	M12	M11	M10	M9	M8	M7	M6	M5	M4	M3	M2	M1	C4(0)	C3(0)	C2(1)	C1(0)

REGISTER 3

RESERVED	SD LOAD RESET	PHASE RESYNC	PHASE ADJUST	24-BIT PHASE VALUE (PHASE) DBR[1]																						CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	SD1	PR1	PA1	P24	P23	P22	P21	P20	P19	P18	P17	P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	C4(0)	C3(0)	C2(1)	C1(1)

REGISTER 4

RESERVED	MUXOUT			REFERENCE DOUBLER DBR[1]	RDIV2 DBR[1]	10-BIT R COUNTER DBR[1]										DOUBLE BUFF	CURRENT SETTING DBR[1]				REF MODE	MUX LOGIC	PD POLARITY	PD	CP THREE-STATE	COUNTER RESET	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	M3	M2	M1	RD2	RD1	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	D1	CP4	CP3	CP2	CP1	U6	U5	U4	U3	U2	U1	C4(0)	C3(1)	C2(0)	C1(0)

REGISTER 5

RESERVED																										CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	C4(0)	C3(1)	C2(0)	C1(1)

REGISTER 6

RESERVED	GATED BLEED	NEGATIVE BLEED	RESERVED				FEEDBACK SELECT	RF DIVIDER SELECT[2]			CHARGE PUMP BLEED CURRENT								RESERVED	MTLD	$RF_{OUT}B$	RESERVED			$RF_{OUT}A+/RF_{OUT}A-$	RF OUTPUT POWER	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	BL10	BL9	1	0	1	0	D13	D12	D11	D10	BL8	BL7	BL6	BL5	BL4	BL3	BL2	BL1	0	D8	D7	0	0	0	D3	D2	D1	C4(0)	C3(1)	C2(1)	C1(0)

[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.
[2]DBB = DOUBLE BUFFERED BITS—BUFFERED BY A WRITE TO REGISTER 0 WHEN BIT DB14 OF REGISTER 4 IS HIGH.

12714-034

Figure 39. Register Summary (Register 0 to Register 6)

REGISTER 7

RESERVED						LE SYNC	RESERVED														LD CYCLE COUNT		LOL MODE	FRAC-N LD PRECISION		LD MODE	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	LE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	LD5	LD4	LOL	LD3	LD2	LD1	C4(0)	C3(1)	C2(1)	C1(1)

REGISTER 8

RESERVED																												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	0	0	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	1	0	0	0	0	1	0	C4(1)	C3(0)	C2(0)	C1(0)

REGISTER 9

VCO BAND DIVISION								TIMEOUT										AUTOMATIC LEVEL TIMEOUT					SYNTHESIZER LOCK TIMEOUT					CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
VC8	VC7	VC6	VC5	VC4	VC3	VC2	VC1	TL10	TL9	TL8	TL7	TL6	TL5	TL4	TL3	TL2	TL1	AL5	AL4	AL3	AL2	AL1	SL5	SL4	SL3	SL2	SL1	C4(1)	C3(0)	C2(0)	C1(1)

REGISTER 10

RESERVED																		ADC CLOCK DIVIDER								ADC CONVERSION	ADC ENABLE	CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AE2	AE1	C4(1)	C3(0)	C2(1)	C1(0)

REGISTER 11

RESERVED																												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0	C4(1)	C3(0)	C2(1)	C1(1)

REGISTER 12

RESYNC CLOCK																RESERVED												CONTROL BITS			
DB31	DB30	DB29	DB28	DB27	DB26	DB25	DB24	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P16	P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	0	0	0	0	0	1	0	0	0	0	0	1	C4(1)	C3(1)	C2(0)	C1(0)

12714-035

Figure 40. Register Summary (Register 7 to Register 12)

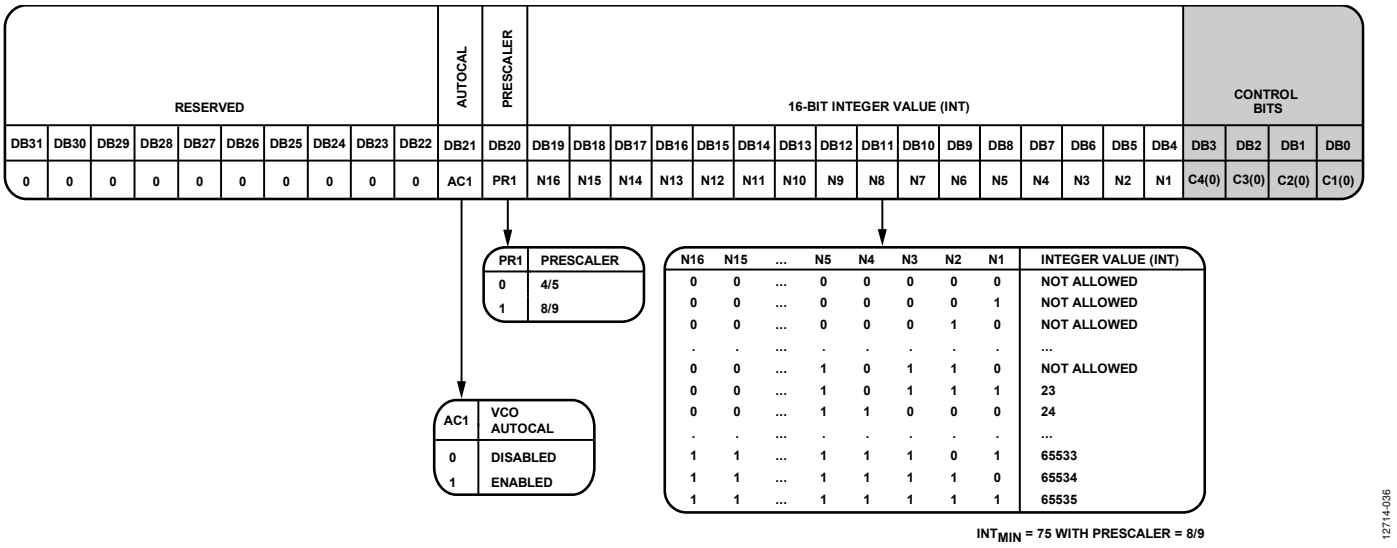


Figure 41. Register 0

REGISTER 0

Control Bits

With Bits[C4:C1] set to 0000, Register 0 is programmed. Figure 41 shows the input data format for programming this register.

Reserved

Bits[DB31:DB22] are reserved and must be set to 0.

Automatic Calibration (AUTOCAL)

Write to Register 0 to enact (by default) the VCO automatic calibration, and to choose the appropriate VCO and VCO subband. Write 1 to the AC1 bit (Bit DB21) to enable the automatic calibration, which is the recommended mode of operation.

Set the AC1 bit (Bit DB21) to 0 to disable the automatic calibration, which leaves the ADF5355 in the same band it was already in when Register 0 is updated.

Disable the automatic calibration only for fixed frequency applications, phase adjust applications, or very small (<10 kHz) frequency jumps.

Toggling automatic calibration (AUTOCAL) is also required when changing frequency. See the Frequency Update Sequence section for more information.

Prescaler Value

The dual modulus prescaler (P/P + 1), along with the INT, FRACx, and MODx counters, determines the overall division ratio from the VCO output to the PFD input. The PR1 bit (Bit DB20) in Register 0 sets the prescaler value.

Operating at CML levels, the prescaler takes the clock from the VCO output and divides it down for the counters. It is based on a synchronous 4/5 core. When the prescaler is set to 4/5, the maximum RF frequency allowed is 7 GHz. The prescaler limits the INT value; therefore, if P is 4/5, N_{MIN} is 23, and if P is 8/9, N_{MIN} is 75.

16-Bit Integer Value

The 16 INT bits (Bits[DB19:DB4]) set the INT value, which determines the integer part of the feedback division factor. The INT value is used in Equation 3 (see the INT, FRAC, MOD, and R Counter Relationship section). All integer values from 23 to 32,767 are allowed for the 4/5 prescaler. For the 8/9 prescaler, the minimum integer value is 75, and the maximum value is 65,535.

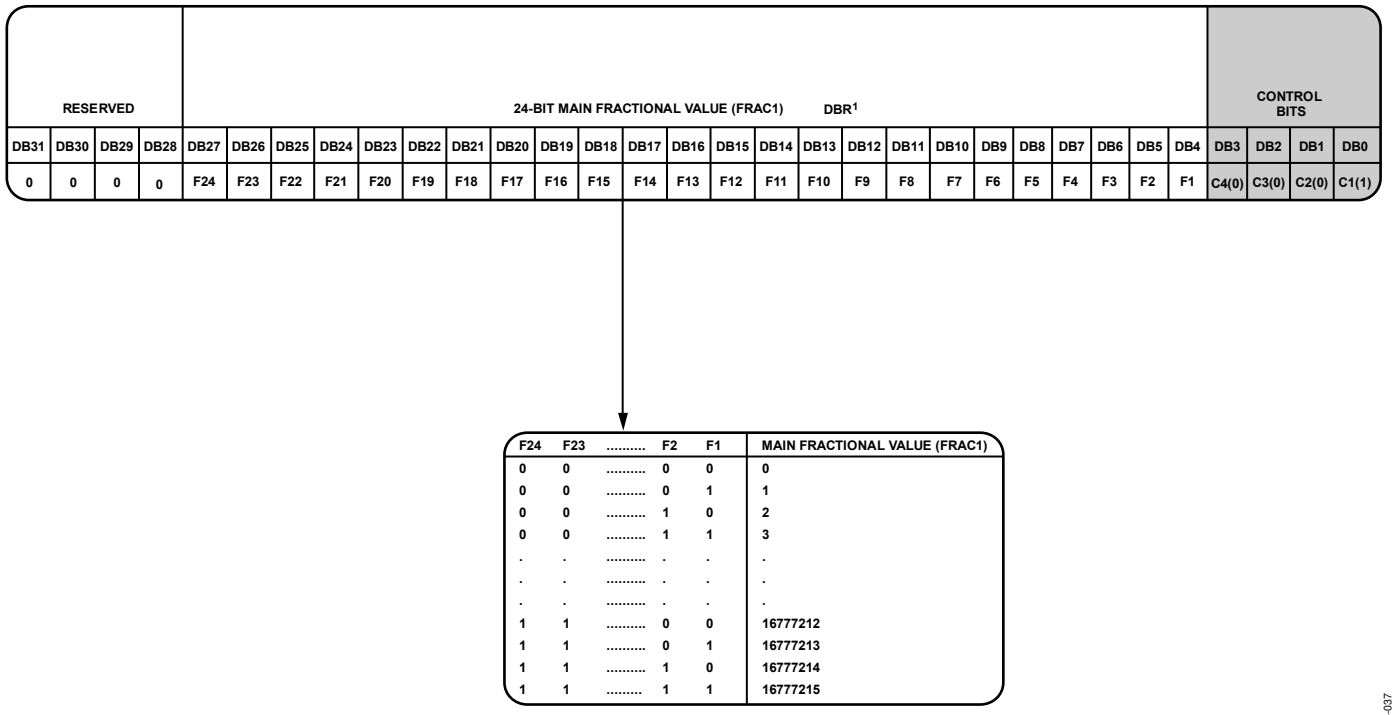


Figure 42. Register 1

REGISTER 1

Control Bits

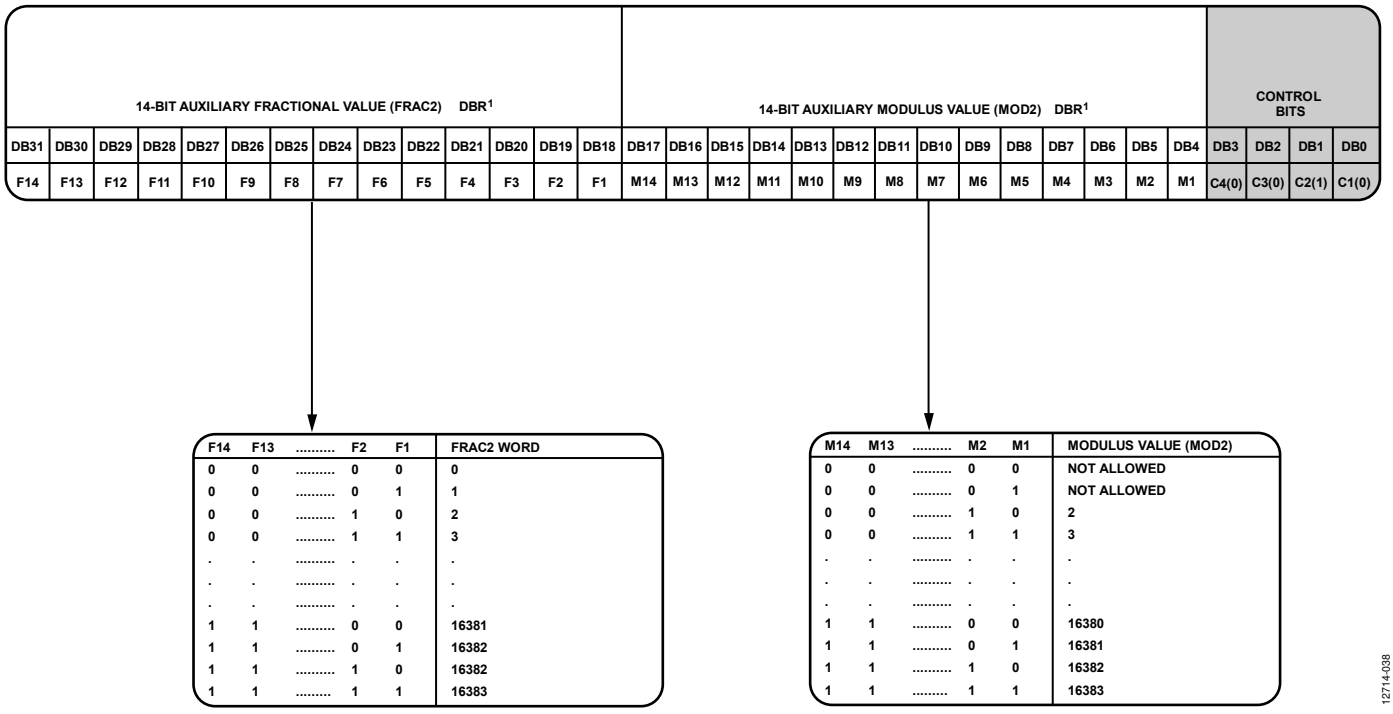
With Bits[C4:C1] set to 0001, Register 1 is programmed. Figure 42 shows the input data format for programming this register.

Reserved

Bits[DB31:DB28] are reserved and must be set to 0.

24-Bit Main Fractional Value

The 24 FRAC1 bits (Bits[DB27:DB4]) set the numerator of the fraction that is input to the Σ-Δ modulator. This fraction, along with the INT value, specifies the new frequency channel that the synthesizer locks to, as shown in the RF Synthesizer—A Worked Example section. FRAC1 values from 0 to (MOD1 − 1) cover channels over a frequency range equal to the PFD reference frequency.



1DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 43. Register 2

REGISTER 2

Control Bits

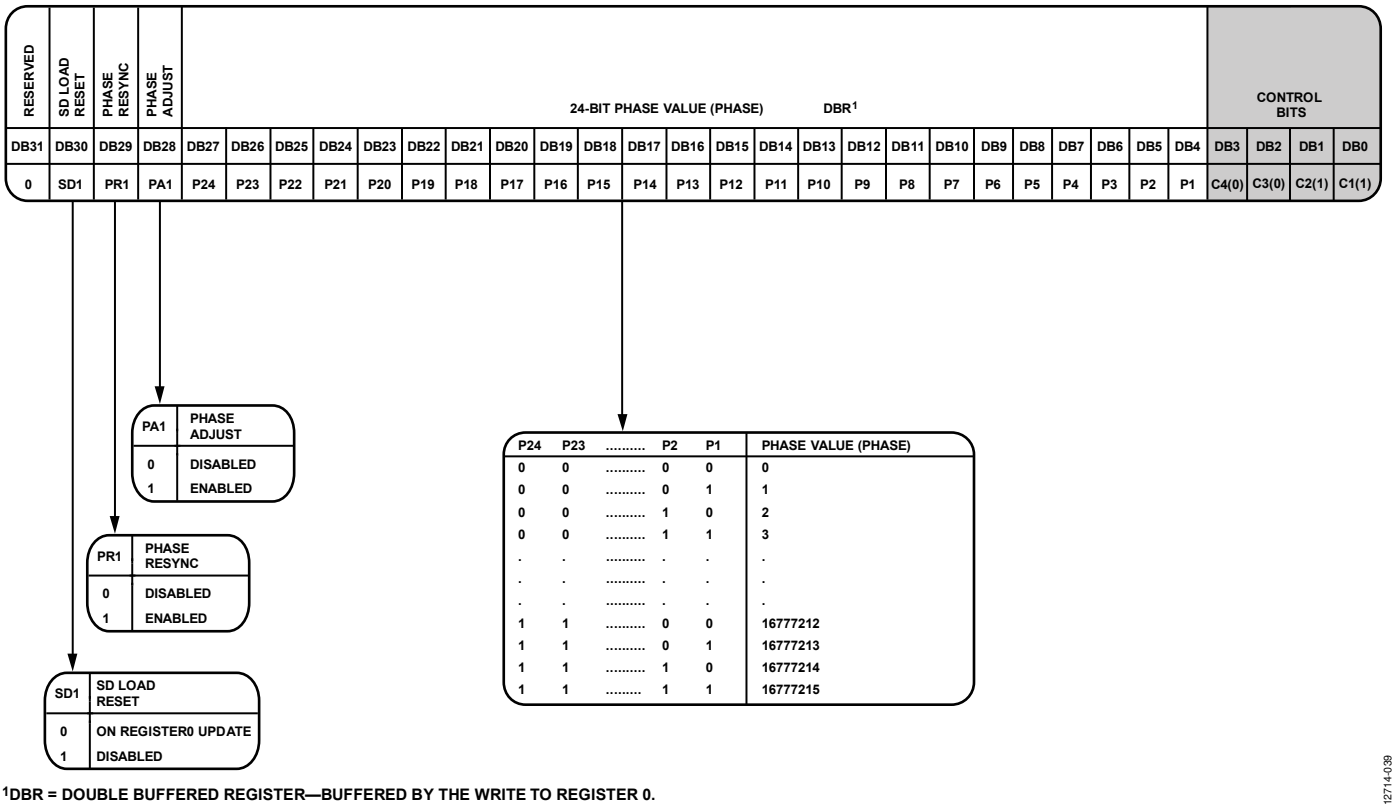
With Bits[C4:C1] set to 0010, Register 2 is programmed. Figure 43 shows the input data format for programming this register.

14-Bit Auxiliary Fractional Value (FRAC2)

The 14-bit auxiliary fractional value (Bits[DB31:DB18]) controls the auxiliary fractional word. FRAC2 must be less than the MOD2 value programmed in Register 2.

14-Bit Auxiliary Modulus Value (MOD2)

The 14-bit auxiliary modulus value (Bits[DB17:DB4]) sets the auxiliary fractional modulus. Use MOD2 to correct any residual error due to the main fractional modulus.



[1]DBR = DOUBLE BUFFERED REGISTER—BUFFERED BY THE WRITE TO REGISTER 0.

Figure 44. Register 3

REGISTER 3

Control Bits

With Bits[C4:C1] set to 0011, Register 3 is programmed. Figure 44 shows the input data format for programming this register.

Reserved

Bit DB31 is reserved and must be set to 0.

SD Load Reset

When writing to Register 0, the Σ-Δ modulator resets. For applications in which the phase is continually adjusted, this may not be desirable; therefore, in these cases, the Σ-Δ reset can be disabled by writing a 1 to the SD1 bit (Bit DB30).

Phase Resync

To use the phase resynchronization feature, the PR1 bit (Bit DB29) must be set to 1. If unused, the bit can be programmed to 0. The phase resync timer must also be used in Register 12 to ensure that the resynchronization feature is applied after PLL has settled to the final frequency. If the PLL has not settled to the final frequency, phase resync may not function correctly. Resynchronization is useful in phased array and beam forming applications. It ensures repeatability of output phase when programming the same frequency. In phase critical applications that use frequencies requiring the output divider (<3400 MHz), it is necessary to feed the N divider with the divided VCO frequency as distinct from the fundamental VCO frequency. This is achieved by programming the D13 bit (Bit DB24) in Register 6 to 0, which ensures divided feedback to the N divider.

Phase resynchronization operates only when FRAC2 = 0.

For resync applications, enable the SD load reset in Register 3 by setting DB30 to 0.

Phase Adjust

To adjust the relative output phase of the ADF5355 on each Register 0 update, set the PA1 bit (Bit DB28) to 1. This feature differs from the resynchronization feature in that it is useful when adjustments to phase are made continually in an application. For this function, disable the VCO automatic calibration by setting the AC1 bit (Bit DB21) in Register 0 to 0, and disable the SD load reset by setting the SD1 bit (Bit DB30) in Register 3 to 1. Note that phase resync and phase adjust cannot be used simultaneously.

24-Bit Phase Value

The phase of the RF output frequency can adjust in 24-bit steps, from 0° (0) to 360° ($2^{24} - 1$). For phase adjust applications, the phase is set by

$$(Phase\ Value/16{,}777{,}216) \times 360°$$

When the phase value is programmed to Register 3, each subsequent adjustment of Register 0 increments the phase by the value in this equation.