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FEATURES

Low power, low IF transceiver

Frequency bands

431 MHz to 478 MHz

862 MHz to 956 MHz

Data rates supported

0.15 kbps to 200 kbps, FSK

0.15 kbps to 64 kbps, ASK

2.3 V to 3.6 V power supply

Programmable output power

-16 dBm to +13 dBm in 0.3 dBm steps

Receiver sensitivity

-119 dBm at 1 kbps, FSK

-112 dBm at 9.6 kbps, FSK

-106.5 dBm at 9.6 kbps, ASK

Low power consumption

19 mA in receive mode

26.8 mA in transmit mode (10 dBm output)

-3 dBm IIP3 in high linearity mode

On-chip VCO and fractional-N PLL

On-chip 7-bit ADC and temperature sensor

Fully automatic frequency control loop (AFC) compensates for ± 25 ppm crystal at 862 MHz to 956 MHz or ± 50 ppm at 431 MHz to 478 MHz

Digital RSSI

Integrated Tx/Rx switch

Leakage current of $< 1 \mu\text{A}$ in power-down mode

APPLICATIONS

Low cost wireless data transfer

Remote control/security systems

Wireless metering

Keyless entry

Home automation

Process and building control

Wireless voice

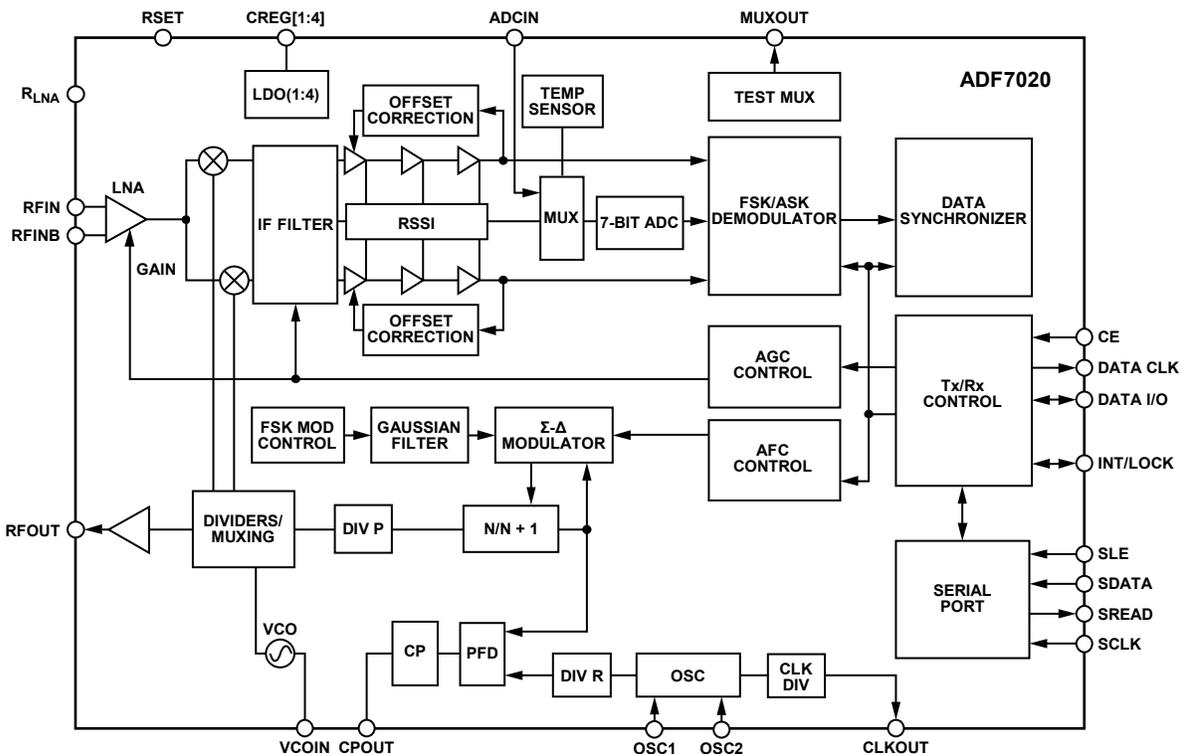
FUNCTIONAL BLOCK DIAGRAM


Figure 1.

06351-001

Rev. E

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ADF7020* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADF7020 Evaluation Boards

DOCUMENTATION

Application Notes

- AN-0987: Designing a Wireless Transceiver System to Meet the Wireless M-Bus Standard
- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-764: ADF7020 RF Port Impedance Values for Matching Purposes
- AN-771: ADSP-BF533 EZ-KIT Lite and ADF70xx Interface
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
- AN-852: Using the Test DAC on the ADF702x to Implement Functions Such as Analog FM DEMOD, SNR Measurement, FEC Decoding, and PSK/4FSK Demodulation
- AN-915: CDR Operation for ADF7020, ADF7020-1, ADF7021, and ADF7025
- AN-917: Using an LC Harmonic Filter at 868 MHz and 915 MHz with the EVAL-ADF7020 and EVAL-ADF7025 Evaluation Boards

Data Sheet

- ADF7020: High Performance, ISM Band, FSK/ASK Transceiver IC Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADF70xx Evaluation Software
- ADIsmLINK Development Platform

TOOLS AND SIMULATIONS

- ADIsimSRD Design Studio

REFERENCE DESIGNS

- CN0164

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Emerging Energy Applications Solutions Bulletin, Volume 10, Issue 4

Technical Articles

- Innovative Line Sensor Design with ADI Energy Harvesting and Low Power Signal Chain
- Low Power, Low Cost, Wireless ECG Holter Monitor
- RF Meets Power Lines: Designing Intelligent Smart Grid Systems that Promote Energy Efficiency
- Smart Metering Technology Promotes Energy Efficiency for a Greener World
- The Use of Short Range Wireless in a Multi-Metering System
- Understand Wireless Short-Range Devices for Global License-Free Systems
- Wireless Short Range Devices and Narrowband Communications
- Wireless Technologies for Smart Meters: Focus on Water Metering

DESIGN RESOURCES

- ADF7020 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADF7020 EngineerZone Discussions.

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6/2005—Revision 0: Initial Version

GENERAL DESCRIPTION

The [ADF7020](#) is a low power, highly integrated FSK/ASK/OOK transceiver designed for operation in the license-free ISM bands at 433 MHz, 868 MHz, and 915 MHz, as well as the proposed Japanese RFID band at 950 MHz. A Gaussian data filter option is available to allow either GFSK or G-ASK modulation, which provides a more spectrally efficient modulation. In addition to these modulation options, the [ADF7020](#) can also be used to perform both MSK and GMSK modulation, where MSK is a special case of FSK with a modulation index of 0.5. The modulation index is calculated as twice the deviation divided by the data rate. MSK is spectrally equivalent to O-QPSK modulation with half-sinusoidal Tx baseband shaping, so the [ADF7020](#) can also support this modulation option by setting up the device in MSK mode.

This device is suitable for circuit applications that meet the European ETSI-300-220, the North American FCC (Part 15), or the Chinese Short Range Device regulatory standards. A complete transceiver can be built using a small number of external discrete components, making the [ADF7020](#) very suitable for price-sensitive and area-sensitive applications.

The transmitter block on the [ADF7020](#) contains a VCO and low noise fractional-N PLL with an output resolution of <1 ppm. This frequency agile PLL allows the [ADF7020](#) to be used in frequency-hopping spread spectrum (FHSS) systems. The VCO operates at twice the fundamental frequency to reduce spurious emissions and frequency-pulling problems.

The transmitter output power is programmable in 0.3 dB steps from -16 dBm to +13 dBm. The transceiver RF frequency and modulation are programmable using a simple 3-wire interface. The device operates with a power supply range of 2.3 V to 3.6 V and can be powered down when not in use.

A low IF architecture is used in the receiver (200 kHz), minimizing power consumption and the external component count and avoiding interference problems at low frequencies. The [ADF7020](#) supports a wide variety of programmable features, including Rx linearity, sensitivity, and IF bandwidth, allowing the user to trade off receiver sensitivity and selectivity against current consumption, depending on the application. The receiver also features a patent-pending automatic frequency control (AFC) loop, allowing the PLL to track out the frequency error in the incoming signal.

An on-chip ADC provides readback of an integrated temperature sensor, an external analog input, the battery voltage, or the RSSI signal, which provides savings on an ADC in some applications. The temperature sensor is accurate to $\pm 10^{\circ}\text{C}$ over the full operating temperature range of -40°C to $+85^{\circ}\text{C}$. This accuracy can be improved by doing a 1-point calibration at room temperature and storing the result in memory.

SPECIFICATIONS

VDD = 2.3 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at VDD = 3 V, T_A = 25°C. All measurements are performed using the [EVAL-ADF7020DBZ1](#) through [EVAL-ADF7020DBZ3](#) using the PN9 data sequence, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
RF CHARACTERISTICS					
Frequency Ranges (Direct Output)	862		870	MHz	VCO adjust = 0, VCO bias = 10
	902		928	MHz	VCO adjust = 3, VCO bias = 10
	928		956	MHz	VCO adjust = 3, VCO bias = 12, VDD = 2.7 V to 3.6 V
Frequency Ranges (Divide-by-2 Mode)	431		440	MHz	VCO adjust = 0, VCO bias = 10
	440		478	MHz	VCO adjust = 3, VCO bias = 12
Phase Frequency Detector Frequency	RF/256		24	MHz	
TRANSMISSION PARAMETERS					
Data Rate					
FSK/GFSK	0.15		200	kbps	
OOK/ASK	0.15		64 ¹	kbps	
OOK/ASK	0.3		100	kbaud	Using Manchester encoding
Frequency Shift Keying					
GFSK/FSK Frequency Deviation ^{2,3}	1		110	kHz	PFD = 3.625 MHz
	4.88		620	kHz	PFD = 20 MHz
Deviation Frequency Resolution	100			Hz	PFD = 3.625 MHz
Gaussian Filter BT		0.5			
Amplitude Shift Keying					
ASK Modulation Depth			30	dB	
PA Off Feedthrough in OOK Mode		-50		dBm	
Transmit Power ⁴	-20		+13	dBm	VDD = 3.0 V, T _A = 25°C
Transmit Power Variation vs. Temperature		±1		dB	From -40°C to +85°C
Transmit Power Variation vs. VDD		±1		dB	From 2.3 V to 3.6 V at 915 MHz, T _A = 25°C
Transmit Power Flatness		±1		dB	From 902 MHz to 928 MHz, 3 V, T _A = 25°C
Programmable Step Size					
-20 dBm to +13 dBm		0.3125		dB	
Integer Boundary Reference		-55		dBc	50 kHz loop BW
		-65		dBc	
Harmonics					
Second Harmonic		-27		dBc	Unfiltered conductive
Third Harmonic		-21		dBc	
All Other Harmonics		-35		dBc	
VCO Frequency Pulling, OOK Mode		30		kHz rms	DR = 9.6 kbps
Optimum PA Load Impedance ⁵		39 + j61		Ω	FRF = 915 MHz
		48 + j54		Ω	FRF = 868 MHz
		54 + j94		Ω	FRF = 433 MHz
RECEIVER PARAMETERS					
FSK/GFSK Input Sensitivity					At BER = 1E - 3, FRF = 915 MHz, LNA and PA matched separately ⁶
Sensitivity at 1 kbps		-119.2		dBm	FDEV = 5 kHz, high sensitivity mode ⁷
Sensitivity at 9.6 kbps		-112.8		dBm	FDEV = 10 kHz, high sensitivity mode
Sensitivity at 200 kbps		-100		dBm	FDEV = 50 kHz, high sensitivity mode
OOK Input Sensitivity					At BER = 1E - 3, FRF = 915 MHz
Sensitivity at 1 kbps		-116		dBm	High sensitivity mode
Sensitivity at 9.6 kbps		-106.5		dBm	High sensitivity mode

Parameter	Min	Typ	Max	Unit	Test Conditions
LNA and Mixer, Input IP3 ⁷					
Enhanced Linearity Mode		-3		dBm	Pin = -20 dBm, 2 CW interferers FRF = 915 MHz, F1 = FRF + 3 MHz F2 = FRF + 6 MHz, maximum gain <1 GHz at antenna input >1 GHz at antenna input
Low Current Mode		-5		dBm	
High Sensitivity Mode		-24		dBm	
Rx Spurious Emissions ⁸			-57	dBm	
			-47	dBm	
AFC					
Pull-In Range at 868 MHz/915 MHz		±50		kHz	IF_BW = 200 kHz
Pull-In Range at 433 MHz		±25		kHz	IF_BW = 200 kHz
Response Time		48		Bits	Modulation index = 0.875
Accuracy		1		kHz	
CHANNEL FILTERING					Desired signal 3 dB above the input sensitivity level, CW interferer power level increased until BER = 10 ⁻³ , image channel excluded
Adjacent Channel Rejection (Offset = ±1 × IF Filter BW Setting)		27		dB	IF filter BW settings = 100 kHz, 150 kHz, 200 kHz
Second Adjacent Channel Rejection (Offset = ±2 × IF Filter BW Setting)		50		dB	IF filter BW settings = 100 kHz, 150 kHz, 200 kHz
Third Adjacent Channel Rejection (Offset = ±3 × IF Filter BW Setting)		55		dB	IF filter BW settings = 100 kHz, 150 kHz, 200 kHz
Image Channel Rejection (Uncalibrated)		30		dB	Image at FRF = 400 kHz
Image Channel Rejection (Calibrated)		50		dB	Image at FRF = 400 kHz
CO-CHANNEL REJECTION		-2		dB	
Wideband Interference Rejection		70		dB	Swept from 100 MHz to 2 GHz, measured as channel rejection
BLOCKING					Desired signal 3 dB above the input sensitivity level, CW interferer power level increased until BER = 10 ⁻²
±1 MHz		60		dB	FSK mode, BER = 10 ⁻³ FRF = 915 MHz, RFIN to GND FRF = 868 MHz FRF = 433 MHz
±5 MHz		68		dB	
±10 MHz		65		dB	
±10 MHz (High Linearity Mode)		72		dB	
Saturation (Maximum Input Level)		12		dBm	
LNA Input Impedance		24 - j60		Ω	
		26 - j63		Ω	
		71 - j128		Ω	
RSSI					
Range at Input		-110 to -24		dBm	
Linearity		±2		dB	
Absolute Accuracy		±3		dB	
Response Time		150		μs	See the RSSI/AGC section
PHASE-LOCKED LOOP					
VCO Gain		65		MHz/V	902 MHz to 928 MHz band, VCO adjust = 0, VCO_BIAS_SETTING = 10
		130		MHz/V	860 MHz to 870 MHz band, VCO adjust = 0
		65		MHz/V	433 MHz, VCO adjust = 0
Phase Noise (In-Band)		-89		dBc/Hz	PA = 0 dBm, VDD = 3.0 V, PFD = 10 MHz, FRF = 915 MHz, VCO_BIAS_SETTING = 10
Phase Noise (Out-of-Band)		-110		dBc/Hz	1 MHz offset
Residual FM		128		Hz	From 200 Hz to 20 kHz, FRF = 868 MHz
PLL Settling		40		μs	Measured for a 10 MHz frequency step to within 5 ppm accuracy, PFD = 20 MHz, LBW = 50 kHz

Parameter	Min	Typ	Max	Unit	Test Conditions
REFERENCE INPUT					
Crystal Reference	3.625		24	MHz	See crystal manufacturer's specification sheet 11.0592 MHz crystal, using 33 pF load capacitors Using 16 pF load capacitors See the Reference Input section
External Oscillator	3.625		24	MHz	
Load Capacitance		33		pF	
Crystal Start-Up Time		2.1		ms	
Input Level		1.0		ms	
				CMOS levels	See the Reference Input section
ADC PARAMETERS					
INL		±1		LSB	From 2.3 V to 3.6 V, T _A = 25°C
DNL		±1		LSB	From 2.3 V to 3.6 V, T _A = 25°C
TIMING INFORMATION					
Chip Enabled to Regulator Ready		10		μs	C _{REG} = 100 nF
Chip Enabled to RSSI Ready		3.0		ms	See Table 11 for more details
Tx to Rx Turnaround Time		150 μs + (5 × T _{BIT})			Time to synchronized data out, includes AGC settling; see the AGC Information and Timing section
LOGIC INPUTS					
Input High Voltage, V _{INH}	0.7 × VDD			V	
Input Low Voltage, V _{INL}			0.2 × VDD	V	
Input Current, I _{INH} /I _{INL}			±1	μA	
Input Capacitance, C _{IN}			10	pF	
Control Clock Input			50	MHz	
LOGIC OUTPUTS					
Output High Voltage, V _{OH}	DVDD – 0.4			V	I _{OH} = 500 μA
Output Low Voltage, V _{OL}			0.4	V	I _{OL} = 500 μA
CLK _{OUT} Rise/Fall			5	ns	
CLK _{OUT} Load			10	pF	
TEMPERATURE RANGE, T _A	–40		+85	°C	
POWER SUPPLIES					
Voltage Supply VDD	2.3		3.6	V	All VDD pins must be tied together
Transmit Current Consumption					FRF = 915 MHz, VDD = 3.0 V, PA is matched to 50 Ω
–20 dBm		14.8		mA	Combined PA and LNA matching network as on EVAL-ADF7020DBZ1 through EVAL-ADF7020DBZ3 boards, VCO_BIAS_SETTING = 12
–10 dBm		15.9		mA	
0 dBm		19.1		mA	
10 dBm		28.5		mA	
10 dBm		26.8		mA	
Receive Current Consumption					PA matched separately with external antenna switch, VCO_BIAS_SETTING = 12
Low Current Mode		19		mA	
High Sensitivity Mode		21		mA	
Power-Down Mode					
Low Power Sleep Mode		0.1	1	μA	

¹ Higher data rates are achievable, depending on local regulations.

² For the definition of frequency deviation, see the Register 2—Transmit Modulation Register (FSK Mode) section.

³ For the definition of GFSK frequency deviation, see the Register 2—Transmit Modulation Register (GFSK/GOOK Mode) section.

⁴ Measured as maximum unmodulated power. Output power varies with both supply and temperature.

⁵ For matching details, see the LNA/PA Matching section and the [AN-764 Application Note](#).

⁶ Sensitivity for combined matching network case is typically 2 dB less than separate matching networks.

⁷ See Table 5 for a description of different receiver modes.

⁸ Follow the matching and layout guidelines to achieve the relevant FCC/ETSI specifications.

TIMING CHARACTERISTICS

VDD = 3 V ± 10%, VGND = 0 V, TA = 25°C, unless otherwise noted. Guaranteed by design, not production tested.

Table 2.

Parameter	Limit at T _{MIN} to T _{MAX}	Unit	Test Conditions/Comments
t ₁	>10	ns	SDATA to SCLK setup time
t ₂	>10	ns	SDATA to SCLK hold time
t ₃	>25	ns	SCLK high duration
t ₄	>25	ns	SCLK low duration
t ₅	>10	ns	SCLK to SLE setup time
t ₆	>20	ns	SLE pulse width
t ₈	<25	ns	SCLK to SREAD data valid, readback
t ₉	<25	ns	SREAD hold time after SCLK, readback
t ₁₀	>10	ns	SCLK to SLE disable time, readback

TIMING DIAGRAMS

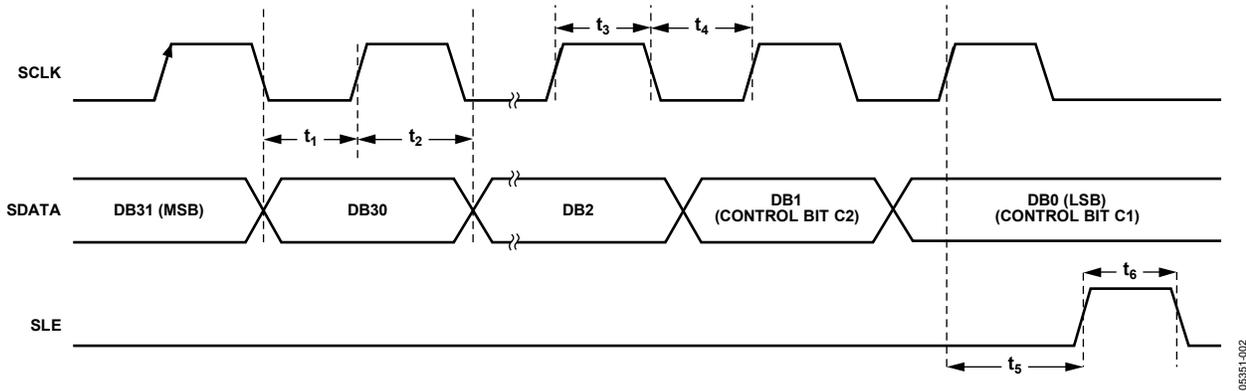


Figure 2. Serial Interface Timing Diagram

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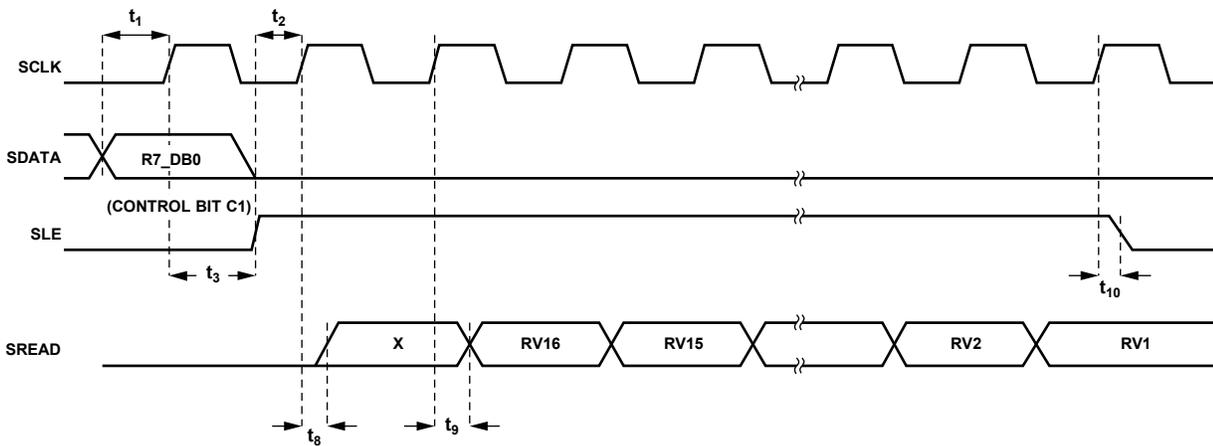


Figure 3. Readback Timing Diagram

05351-003

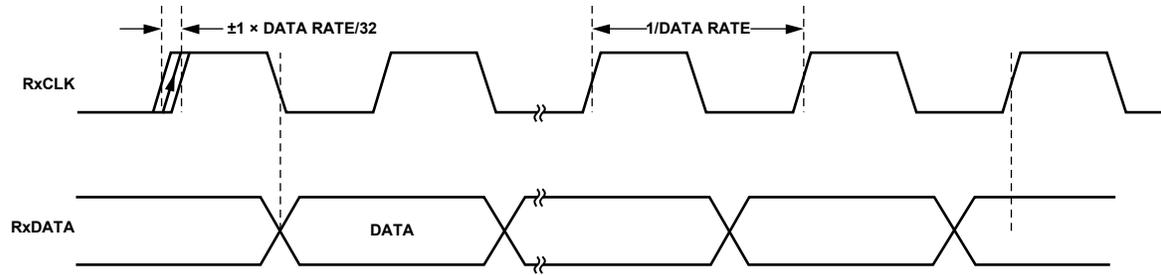
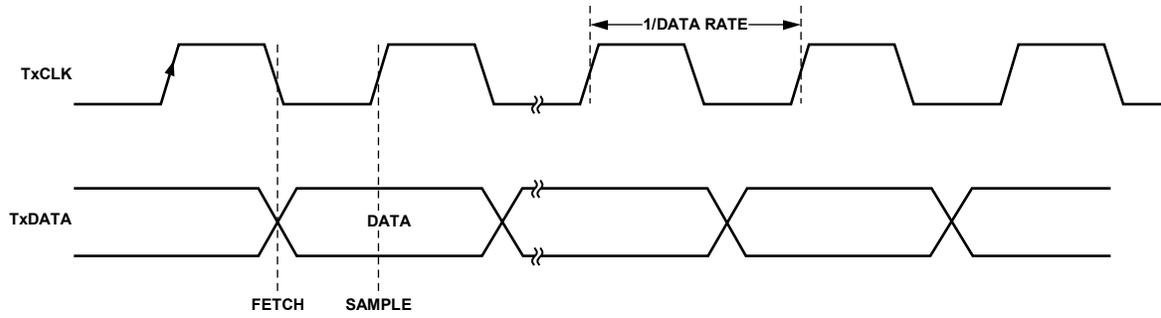


Figure 4. RxData/RxCLK Timing Diagram

05351-004



NOTES
1. TxCLK ONLY AVAILABLE IN GFSK MODE.

Figure 5. TxData/TxCLK Timing Diagram

05351-005

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 3.

Parameter	Rating
VDD to GND ¹	-0.3 V to +5 V
Analog I/O Voltage to GND	-0.3 V to AVDD + 0.3 V
Digital I/O Voltage to GND	-0.3 V to DVDD + 0.3 V
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Storage Temperature Range	-65°C to +125°C
Maximum Junction Temperature	150°C
MLF θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

¹ GND = GND1 = RFGND = GND4 = VCO GND = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

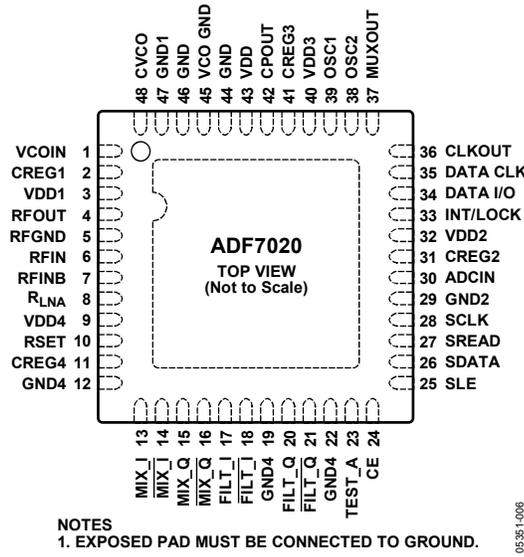
This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD MUST BE CONNECTED TO GROUND.

Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCOIN	The tuning voltage on this pin determines the output frequency of the voltage-controlled oscillator (VCO). The higher the tuning voltage, the higher the output frequency.
2	CREG1	Regulator Voltage for PA Block. A 100 nF in parallel with a 5.1 pF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
3	VDD1	Voltage Supply for PA Block. Decoupling capacitors of 0.1 μF and 10 pF should be placed as close as possible to this pin. All VDD pins should be tied together.
4	RFOUT	The modulated signal is available at this pin. Output power levels are from -20 dBm to +13 dBm. The output should be impedance matched to the desired load using suitable components. See the Transmitter section.
5	RFGND	Ground for Output Stage of Transmitter. All GND pins should be tied together.
6	RFIN	LNA Input for Receiver Section. Input matching is required between the antenna and the differential LNA input to ensure maximum power transfer. See the LNA/PA Matching section.
7	RFINB	Complementary LNA Input. See the LNA/PA Matching section.
8	RLNA	External bias resistor for LNA. Optimum resistor is 1.1 kΩ with 5% tolerance.
9	VDD4	Voltage Supply for LNA/MIXER Block. This pin should be decoupled to ground with a 10 nF capacitor.
10	RSET	External Resistor to Set Charge Pump Current and Some Internal Bias Currents. Use 3.6 kΩ with 5% tolerance.
11	CREG4	Regulator Voltage for LNA/MIXER Block. A 100 nF capacitor should be placed between this pin and GND for regulator stability and noise rejection.
12	GND4	Ground for LNA/MIXER Block.
13 to 18	MIX_I, MIX_I, MIX_Q, MIX_Q, FILT_I, FILT_I	Signal Chain Test Pins. These pins are high impedance under normal conditions and should be left unconnected.
19, 22	GND4	Ground for LNA/MIXER Block.
20, 21, 23	FILT_Q, FILT_Q, TEST_A	Signal Chain Test Pins. These pins are high impedance under normal conditions and should be left unconnected.
24	CE	Chip Enable. Bringing CE low puts the ADF7020 into complete power-down. Register values are lost when CE is low, and the part must be reprogrammed once CE is brought high.
25	SLE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the fourteen latches. A latch is selected using the control bits.
26	SDATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs as the control bits. This pin is a high impedance CMOS input.

Pin No.	Mnemonic	Description
27	SREAD	Serial Data Output. This pin is used to feed readback data from the ADF7020 to the microcontroller. The SCLK input is used to clock each readback bit (AFC, ADC readback) from the SREAD pin.
28	SCLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This pin is a digital CMOS input.
29	GND2	Ground for Digital Section.
30	ADCIN	Analog-to-Digital Converter Input. The internal 7-bit ADC can be accessed through this pin. Full scale is 0 V to 1.9 V. Readback is made using the SREAD pin.
31	CREG2	Regulator Voltage for Digital Block. A 100 nF in parallel with a 5.1 pF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
32	VDD2	Voltage Supply for Digital Block. A decoupling capacitor of 10 nF should be placed as close as possible to this pin.
33	INT/LOCK	Bidirectional Pin. In output mode (interrupt mode), the ADF7020 asserts the INT/ LOCK pin when it has found a match for the preamble sequence. In input mode (lock mode), the microcontroller can be used to lock the demodulator threshold when a valid preamble has been detected. Once the threshold is locked, NRZ data can be reliably received. In this mode, a demodulation lock can be asserted with minimum delay.
34	DATA I/O	Transmit Data Input/Received Data Output. This is a digital pin, and normal CMOS levels apply.
35	DATA CLK	In receive mode, the pin outputs the synchronized data clock. The positive clock edge is matched to the center of the received data. In GFSK transmit mode, the pin outputs an accurate clock to latch the data from the microcontroller into the transmit section at the exact required data rate. See the Gaussian Frequency Shift Keying (GFSK) section.
36	CLKOUT	A Divided-Down Version of the Crystal Reference with Output Driver. The digital clock output can be used to drive several other CMOS inputs, such as a microcontroller clock. The output has a 50:50 mark-space ratio.
37	MUXOUT	This pin provides the LOCK_DETECT signal, which is used to determine if the PLL is locked to the correct frequency. Other signals include REGULATOR_READY, which is an indicator of the status of the serial interface regulator.
38	OSC2	The reference crystal should be connected between this pin and OSC1. A TCXO reference can be used by driving this pin with CMOS levels and disabling the crystal oscillator.
39	OSC1	The reference crystal should be connected between this pin and OSC2.
40	VDD3	Voltage Supply for the Charge Pump and PLL Dividers. This pin should be decoupled to ground with a 0.01 μ F capacitor.
41	CREG3	Regulator Voltage for Charge Pump and PLL Dividers. A 100 nF in parallel with a 5.1 pF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
42	CPOUT	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
43	VDD	Voltage Supply for VCO Tank Circuit. This pin should be decoupled to ground with a 0.01 μ F capacitor.
44 to 47	GND, GND1, VCO GND	Grounds for VCO Block.
48	CVCO	A 22 nF capacitor should be placed between this pin and CREG1 to reduce VCO noise.
	EP	Exposed Pad. The exposed pad must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

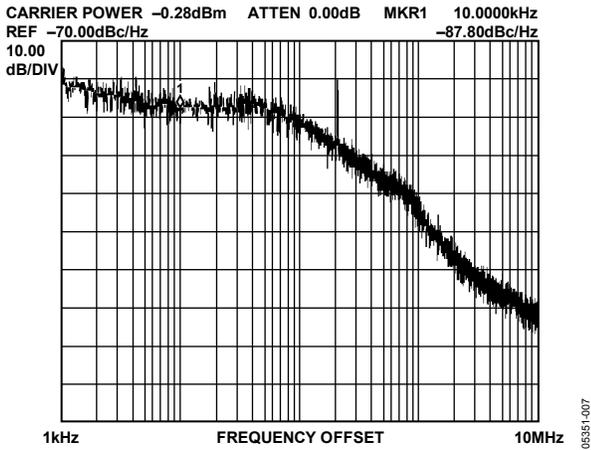


Figure 7. Phase Noise Response at 868.3 MHz, VDD = 3.0 V, ICP = 1.5 mA

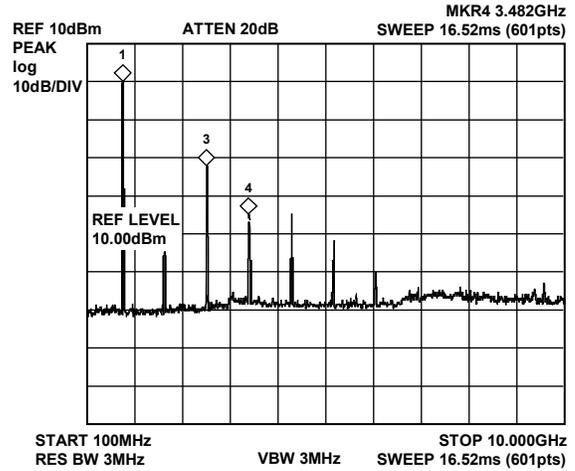


Figure 10. Harmonic Response, R_{FOUT} Matched to 50 Ω , No Filter

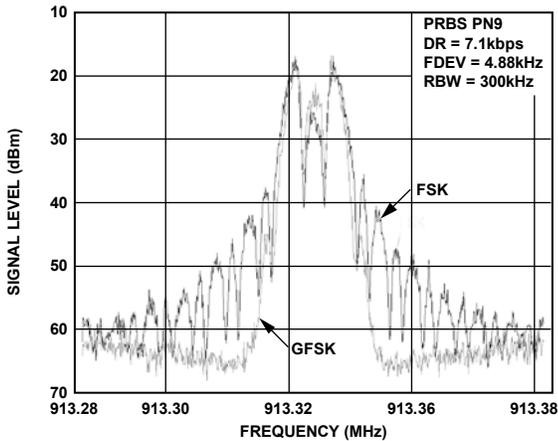


Figure 8. Output Spectrum in FSK and GFSK Modulation

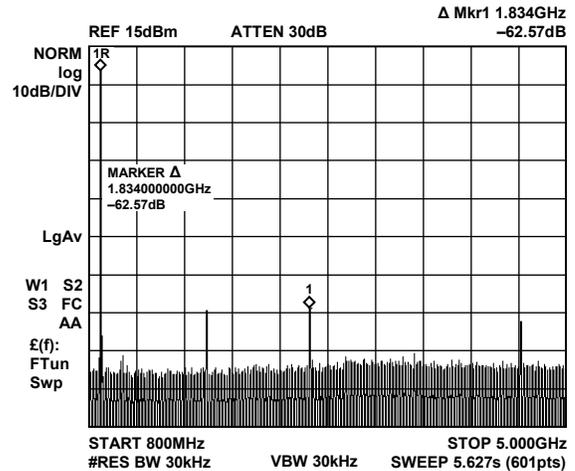


Figure 11. Harmonic Response, Murata Dielectric Filter

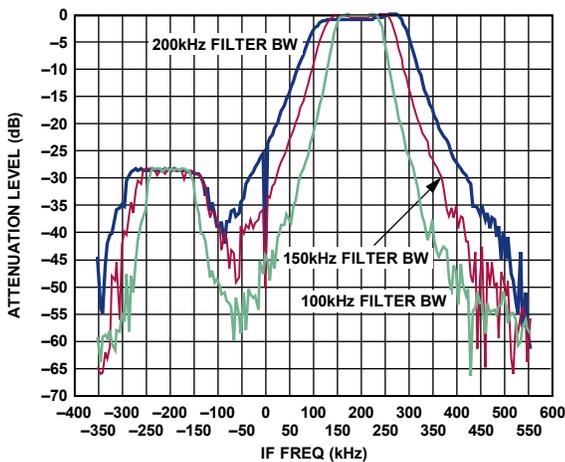


Figure 9. IF Filter Response

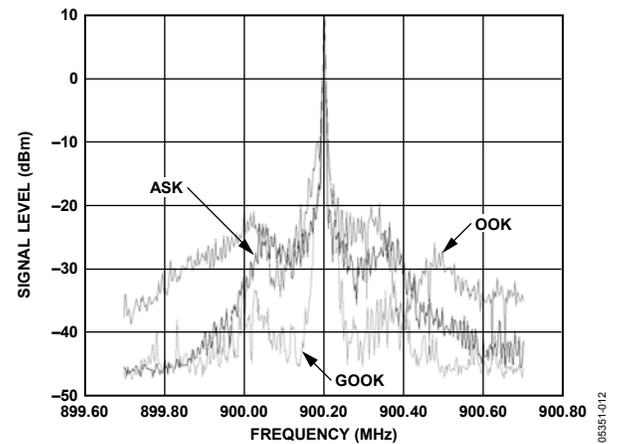


Figure 12. Output Spectrum in ASK, OOK, and GOOK Modes, DR = 10 kbps

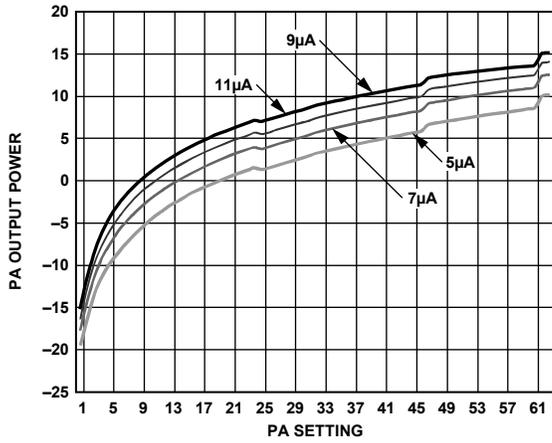


Figure 13. PA Output Power vs. Setting

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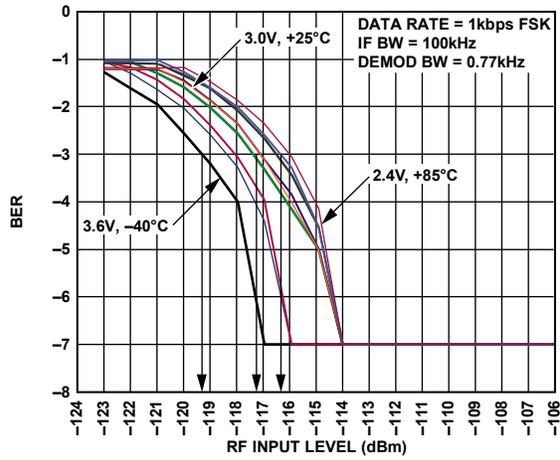


Figure 16. BER vs. VDD and Temperature

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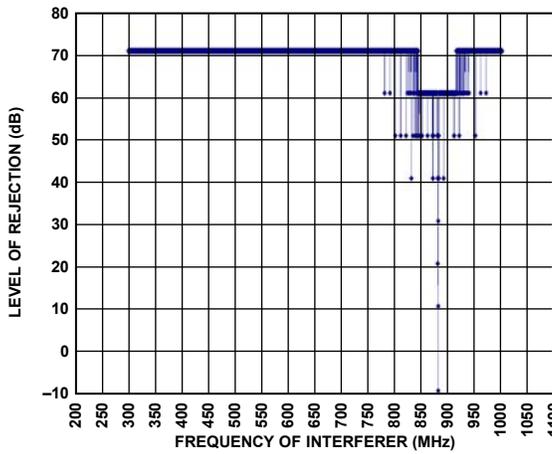


Figure 14. Wideband Interference Rejection; Wanted Signal (880 MHz) at 3 dB above Sensitivity Point Interferer = FM Jammer (9.76 kbps, 10 kHz Deviation)

05351-014

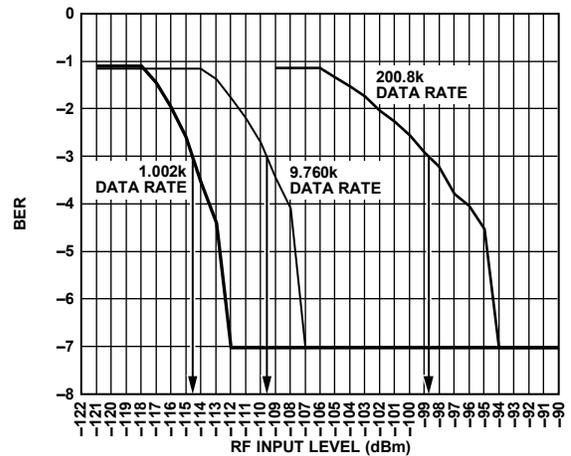


Figure 17. BER vs. Data Rate (Combined Matching Network) Separate LNA and PA Matching Paths Typically Improve Performance by 2 dB

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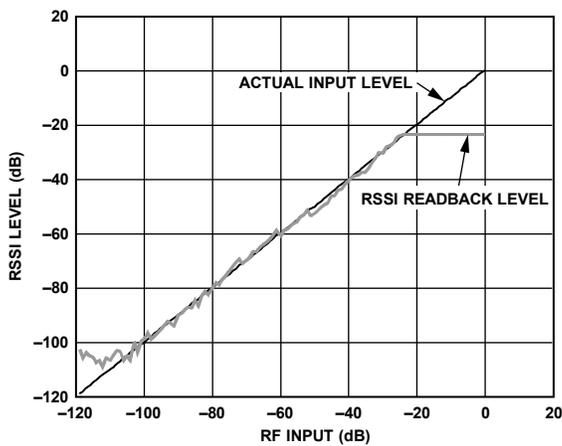


Figure 15. Digital RSSI Readback Linearity

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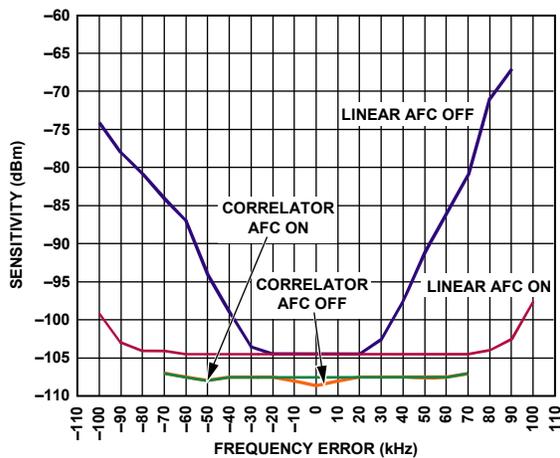


Figure 18. Sensitivity vs. Frequency Error with AFC On/Off

05351-018

FREQUENCY SYNTHESIZER

REFERENCE INPUT

The on-board crystal oscillator circuitry (see Figure 19) can use an inexpensive quartz crystal as the PLL reference. The oscillator circuit is enabled by setting R1_DB12 high. It is enabled by default on power-up and is disabled by bringing CE low. Errors in the crystal can be corrected using the automatic frequency control (see the AFC section) feature or by adjusting the fractional-N value (see the N Counter section). A single-ended reference (TCXO, CXO) can also be used. The CMOS levels should be applied to OSC2 with R1_DB12 set low.

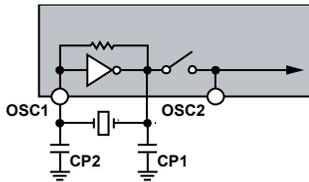


Figure 19. Oscillator Circuit on the ADF7020

Two parallel resonant capacitors are required for oscillation at the correct frequency; their values are dependent on the crystal specification. They should be chosen so that the series value of capacitance added to the PCB track capacitance adds up to the load capacitance of the crystal, usually 20 pF. PCB track capacitance values might vary from 2 pF to 5 pF, depending on board layout. Thus, calculate CP1 and CP2 using:

$$C_L = \frac{1}{\frac{1}{C_{P1}} + \frac{1}{C_{P2}}} + C_{PCB}$$

Where possible, choose capacitors that have a low temperature coefficient to ensure stable frequency operation over all conditions.

CLKOUT Divider and Buffer

The CLKOUT circuit takes the reference clock signal from the oscillator section, shown in Figure 20, and supplies a divided down 50:50 mark-space signal to the CLKOUT pin. An even divide from 2 to 30 is available. This divide number is set in R1_DB[8:11]. On power-up, the CLKOUT defaults to divide-by-8.

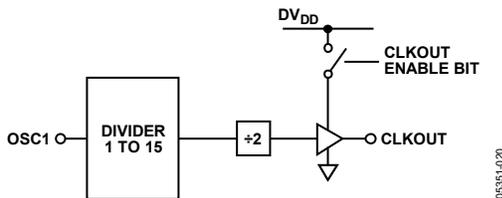


Figure 20. CLKOUT Stage

To disable CLKOUT, set the divide number to 0. The output buffer can drive up to a 20 pF load with a 10% rise time at 4.8 MHz. Faster edges can result in some spurious feedthrough to the output. A small series resistor (50 Ω) can be used to slow the clock edges to reduce these spurs at f_{CLK}.

R Counter

The 3-bit R counter divides the reference input frequency by an integer ranging from 1 to 7. The divided-down signal is presented as the reference clock to the phase frequency detector (PFD). The divide ratio is set in Register 1. Maximizing the PFD frequency reduces the N value. Every doubling of the PFD gives a 3 dB benefit in phase noise, as well as reducing occurrences of spurious components. The R register defaults to R = 1 on power-up.

$$PFD [Hz] = XTAL/R$$

MUXOUT and Lock Detect

The MUXOUT pin allows the user to access various digital points in the ADF7020. The state of MUXOUT is controlled by Bits R0_DB[29:31].

Regulator Ready

Regulator ready is the default setting on MUXOUT after the transceiver has been powered up. The power-up time of the regulator is typically 50 μs. Because the serial interface is powered from the regulator, the regulator must be at its nominal voltage before the ADF7020 can be programmed. The status of the regulator can be monitored at MUXOUT. When the regulator ready signal on MUXOUT is high, programming of the ADF7020 can begin.

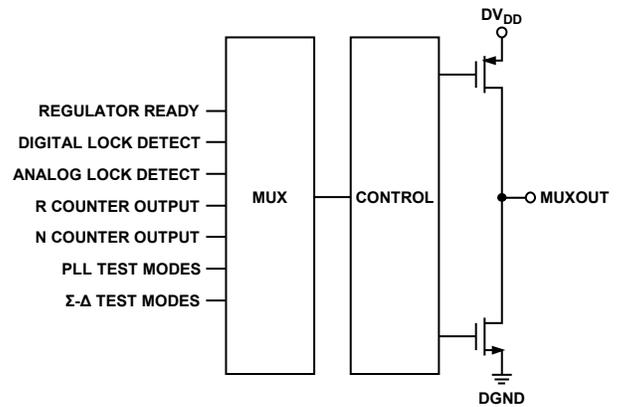


Figure 21. MUXOUT Circuit

Digital Lock Detect

Digital lock detect is active high. The lock detect circuit is located at the PFD. When the phase error on five consecutive cycles is less than 15 ns, lock detect is set high. Lock detect remains high until 25 ns phase error is detected at the PFD. Because no external components are needed for digital lock detect, it is more widely used than analog lock detect.

Analog Lock Detect

This N-channel open-drain lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When a lock has been detected, this output is high with narrow low going pulses.

Voltage Regulators

The ADF7020 contains four regulators to supply stable voltages to the part. The nominal regulator voltage is 2.3 V. Each regulator should have a 100 nF capacitor connected between CREGx and GND. When CE is high, the regulators and other associated circuitry are powered on, drawing a total supply current of 2 mA. Bringing the chip-enable pin low disables the regulators, reduces the supply current to less than 1 μA, and erases all values held in the registers. The serial interface operates off a regulator supply; therefore, to write to the part, the user must have CE high and the regulator voltage must be stabilized. Regulator status (CREG4) can be monitored using the regulator ready signal from MUXOUT.

Loop Filter

The loop filter integrates the current pulses from the charge pump to form a voltage that tunes the output of the VCO to the desired frequency. It also attenuates spurious levels generated by the PLL. A typical loop filter design is shown in Figure 22.

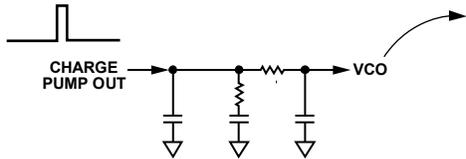


Figure 22. Typical Loop Filter Configuration

In FSK, the loop should be designed so that the loop bandwidth (LBW) is approximately one and a half times the data rate. Widening the LBW excessively reduces the time spent jumping between frequencies, but it can cause insufficient spurious attenuation.

For ASK systems, a wider LBW is recommended. The sudden large transition between two power levels can result in VCO pulling and can cause a wider output spectrum than is desired. By widening the LBW to more than 10 times the data rate, the amount of VCO pulling is reduced, because the loop settles quickly back to the correct frequency. The wider LBW can restrict the output power and data rate of ASK-based systems compared with FSK-based systems.

Narrow-loop bandwidths can result in the loop taking long periods of time to attain lock. Careful design of the loop filter is critical to obtaining accurate FSK/GFSK modulation.

For GFSK, it is recommended that an LBW of 1.0 to 1.5 times the data rate be used to ensure that sufficient samples are taken of the input data while filtering system noise. The free design tool ADIsimSRD Design Studio™ can be used to design loop filters for the ADF7020. It can also be used to view the effect of loop filter bandwidth on the spectrum of the transmitted signal for different combinations of modulation type, data rates, and modulation indices.

N Counter

The feedback divider in the ADF7020 PLL consists of an 8-bit integer counter and a 15-bit Σ-Δ fractional-N divider. The integer counter is the standard pulse-swallow type common in PLLs. This sets the minimum integer divide value to 31. The fractional divide value gives very fine resolution at the output, where the output frequency of the PLL is calculated as

$$f_{OUT} = PFD \times \left(INTEGER_N + \frac{FRACTIONAL_N}{2^{15}} \right)$$

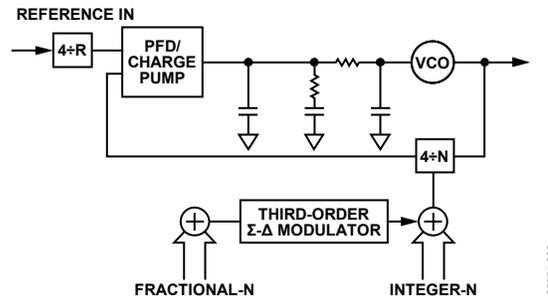


Figure 23. Fractional-N PLL

The maximum N divide value is the combination of the INTEGER_N (maximum = 255) and the FRACTIONAL_N (maximum = 32767/32768) and puts a lower limit on the minimum usable PFD.

$$PFD_{MIN} [Hz] = \text{Maximum Required Output Frequency} / (255 + 1)$$

For example, when operating in the European 868 MHz to 870 MHz band, PFD_{MIN} equals 3.4 MHz. In the majority of cases, it is advisable to use as high a value of PFD as possible to obtain best phase noise performance.

Voltage Controlled Oscillator (VCO)

To minimize spurious emissions, the on-chip VCO operates from 1724 MHz to 1912 MHz. The VCO signal is then divided by 2 to give the required frequency for the transmitter and the required LO frequency for the receiver.

The VCO should be recentered, depending on the required frequency of operation, by programming the VCO Adjust Bits R1_DB[20:21].

The VCO is enabled as part of the PLL by the PLL Enable bit, R0_DB28.

A further frequency divide-by-2 block is included to allow operation in the lower 433 MHz and 460 MHz bands. To enable operation in these bands, R1_DB13 should be set to 1. The VCO needs an external 22 nF between the VCO and the regulator to reduce internal noise.

VCO Bias Current

VCO bias current can be adjusted using Bit R1_DB19 to Bit R1_DB16. To ensure VCO oscillation, the minimum bias current setting under all conditions is 0xA.

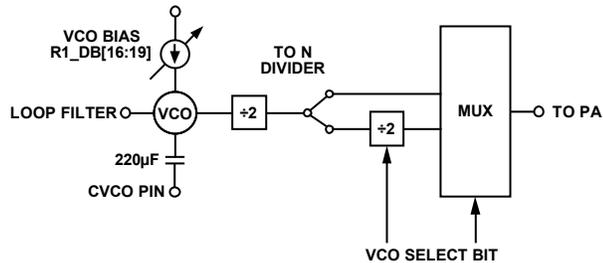


Figure 24. Voltage-Controlled Oscillator (VCO)

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CHOOSING CHANNELS FOR BEST SYSTEM PERFORMANCE

The fractional-N PLL allows the selection of any channel within 868 MHz to 956 MHz (and 433 MHz using divide-by-2) to a resolution of <300 Hz. This also facilitates frequency-hopping systems.

Careful selection of the XTAL frequency is important to achieve best spurious and blocking performance. The architecture of fractional-N causes some level of the nearest integer channel to couple directly to the RF output. This phenomenon is often referred to as integer boundary spurious. If the desired RF channel and the nearest integer channel are separated by a frequency of less than the PLL loop bandwidth (LBW), the integer boundary spurs are not attenuated by the loop.

Integer boundary spurs can be significantly reduced in amplitude by choosing XTAL values that place the wanted RF channel away from integer multiples of the PFD.

TRANSMITTER

RF OUTPUT STAGE

The PA of the ADF7020 is based on a single-ended, controlled current, open-drain amplifier that has been designed to deliver up to 13 dBm into a 50 Ω load at a maximum frequency of 956 MHz.

The PA output current and, consequently, the output power are programmable over a wide range. The PA configurations in FSK/GFSK and ASK/OOK modulation modes are shown in Figure 25 and Figure 26, respectively. In FSK/GFSK modulation mode, the output power is independent of the state of the DATA I/O pin. In ASK/OOK modulation mode, it is dependent on the state of the DATA I/O pin and Bit R2_DB29, which selects the polarity of the TxData input. For each transmission mode, the output power can be adjusted as follows:

- FSK/GFSK
The output power is set using Bits R2_DB[9:14].
- ASK
The output power for the inactive state of the TxData input is set by Bits R2_DB[15:20]. The output power for the active state of the TxData input is set by Bits R2_DB[9:14].
- OOK
The output power for the active state of the TxData input is set by Bits R2_DB[9:14]. The PA is muted when the TxData input is inactive.

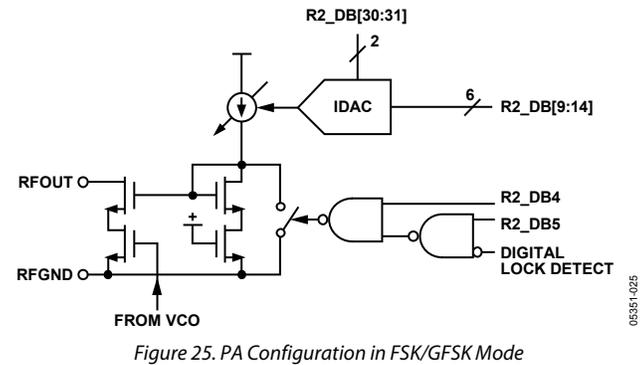


Figure 25. PA Configuration in FSK/GFSK Mode

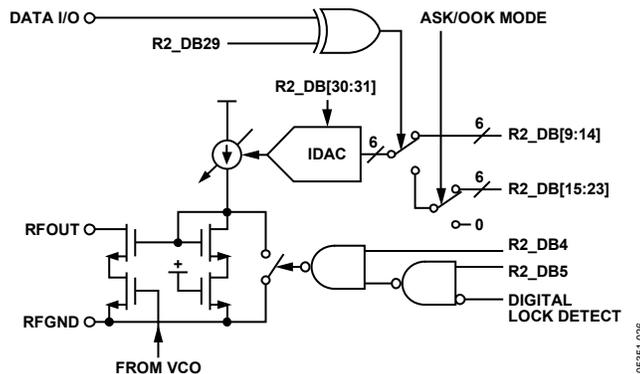


Figure 26. PA Configuration in ASK/OOK Mode

The PA is equipped with overvoltage protection, which makes it robust in severe mismatch conditions. Depending on the application, one can design a matching network for the PA to exhibit optimum efficiency at the desired radiated output power level for a wide range of different antennas, such as loop or monopole antennas. See the LNA/PA Matching section for details.

PA Bias Currents

Control Bits R2_DB[30:31] facilitate an adjustment of the PA bias current to further extend the output power control range, if necessary. If this feature is not required, the default value of 7 μA is recommended. The output stage is powered down by resetting Bit R2_DB4. To reduce the level of undesired spurious emissions, the PA can be muted during the PLL lock phase by toggling this bit.

MODULATION SCHEMES

Frequency Shift Keying (FSK)

Frequency shift keying is implemented by setting the N value for the center frequency and then toggling this with the TxData line. The deviation from the center frequency is set using Bits R2_DB[15:23]. The deviation from the center frequency in Hz is

$$FSK_{DEVIATION} [Hz] = \frac{PFD \times Modulation\ Number}{2^{14}}$$

where *Modulation Number* is a number from 1 to 511 (R2_DB[15:23]).

Select FSK using Bits R2_DB[6:8].

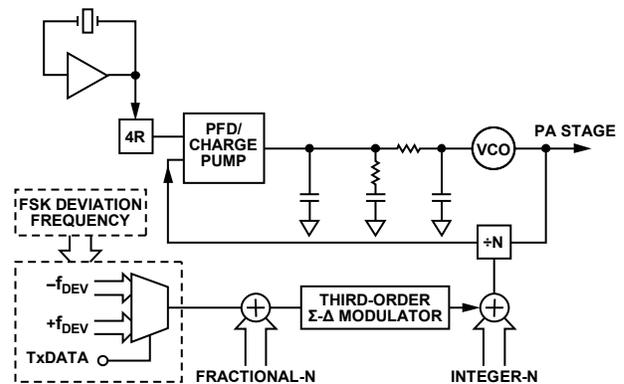


Figure 27. FSK Implementation

Gaussian Frequency Shift Keying (GFSK)

Gaussian frequency shift keying reduces the bandwidth occupied by the transmitted spectrum by digitally prefiltering the TxData. A TxCLK output line is provided from the ADF7020 for synchronization of TxData from the microcontroller. The TxCLK line can be connected to the clock input of a shift register that clocks data to the transmitter at the exact data rate.

Setting Up the ADF7020 for GFSK

To set up the frequency deviation, set the PFD and the modulation control bits.

$$GFSK_{DEVIATION}[\text{Hz}] = \frac{PFD \times 2^m}{2^{12}}$$

where m is GFSK_MOD_CONTROL, set using R2_DB[24:26].

To set up the GFSK data rate,

$$DR[\text{bps}] = \frac{PFD}{DIVIDER_FACTOR \times INDEX_COUNTER}$$

The INDEX_COUNTER variable controls the number of intermediate frequency steps between the low and high frequency. It is usually possible to achieve a given data rate with various combinations of DIVIDER_FACTOR and INDEX_COUNTER. Choosing a higher INDEX_COUNTER can help in improving the spectral performance.

Amplitude Shift Keying (ASK)

Amplitude shift keying is implemented by switching the output stage between two discrete power levels. This is accomplished by toggling the DAC, which controls the output level between two 6-bit values set up in Register 2. A 0 TxData bit sends Bits R2_DB[15:20] to the DAC. A high TxData bit sends Bits R2_DB[9:14] to the DAC. A maximum modulation depth of 30 dB is possible.

On-Off Keying (OOK)

On-off keying is implemented by switching the output stage to a certain power level for a high TxData bit and switching the output stage off for a zero. For OOK, the transmitted power for a high input is programmed using Bits R2_DB[9:14].

Gaussian On-Off Keying (GOOK)

Gaussian on-off keying represents a prefiltered form of OOK modulation. The usually sharp symbol transitions are replaced with smooth Gaussian filtered transitions, the result being a reduction in frequency pulling of the VCO. Frequency pulling of the VCO in OOK mode can lead to a wider than desired BW, especially if it is not possible to increase the loop filter BW > 300 kHz. The GOOK sampling clock samples data at the data rate (see the Setting Up the ADF7020 for GFSK section).

RECEIVER

RF FRONT END

The ADF7020 is based on a fully integrated, low IF receiver architecture. The low IF architecture facilitates a very low external component count and does not suffer from power line-induced interference problems.

Figure 28 shows the structure of the receiver front end. The many programming options allow users to trade off sensitivity, linearity, and current consumption against each other in the way best suitable for their applications. To achieve a high level of resilience against spurious reception, the LNA features a differential input. Switch SW2 shorts the LNA input when transmit mode is selected (R0_DB27 = 0). This feature facilitates the design of a combined LNA/PA matching network, avoiding the need for an external Rx/Tx switch. See the LNA/PA Matching section for details on the design of the matching network.

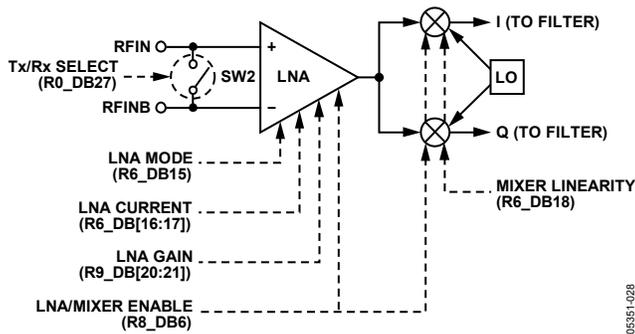


Figure 28. ADF7020 RF Front End

The LNA is followed by a quadrature down conversion mixer, that converts the RF signal to the IF frequency of 200 kHz. It is important to consider that the output frequency of the synthesizer must be programmed to a value 200 kHz below the center frequency of the received channel.

The LNA has two basic operating modes: high gain/low noise mode and low gain/low power mode. To switch between these two modes, use the LNA_MODE bit, R6_DB15. The mixer is also configurable between a low current and an enhanced linearity mode using the MIXER_LINEARITY bit, R6_DB18.

Based on the specific sensitivity and linearity requirements of the application, it is recommended to adjust control bits LNA_MODE (R6_DB15) and MIXER_LINEARITY (R6_DB18), as outlined in Table 5.

The gain of the LNA is configured by the LNA_GAIN field, R9_DB[20:21], and can be set by either the user or the automatic gain control (AGC) logic.

IF Filter Settings/Calibration

Out-of-band interference is rejected by means of a fourth-order Butterworth polyphase IF filter centered around a frequency of 200 kHz. The bandwidth of the IF filter can be programmed between 100 kHz and 200 kHz by using Control Bits R1_DB[22:23] and should be chosen as a compromise between interference rejection, attenuation of the desired signal, and the AFC pull-in range.

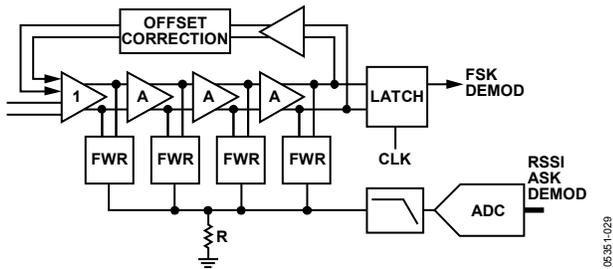
To compensate for manufacturing tolerances, the IF filter should be calibrated once after power-up. The IF filter calibration logic requires that the IF filter divider in Bits R6_DB[20:28] be set as dependent on the crystal frequency. Once initiated by setting Bit R6_DB19, the calibration is performed automatically without any user intervention. The calibration time is 200 μs, during which the ADF7020 should not be accessed. It is important not to initiate the calibration cycle before the crystal oscillator has fully settled. If the AGC loop is disabled, the gain of IF filter can be set to three levels using the FILTER_GAIN field, R9_DB[20:21]. The filter gain is adjusted automatically, if the AGC loop is enabled.

Table 5. LNA/Mixer Modes

Receiver Mode	LNA Mode (R6_DB15)	LNA Gain Value (R9_DB[20:21])	Mixer Linearity (R6_DB18)	Sensitivity (DR = 9.6 kbps, f _{DEV} = 10 kHz)	Rx Current Consumption (mA)	Input IP3 (dBm)
High Sensitivity Mode (Default)	0	30	0	-110.5	21	-24
RxMode2	1	10	0	-104	20	-13.5
Low Current Mode	1	3	0	-94	19	-5
Enhanced Linearity Mode	1	3	1	-88	19	-3
RxMode5	1	10	1	-98	20	-10
RxMode6	0	30	1	-107	21	-20

RSSI/AGC

The RSSI is implemented as a successive compression log amp following the baseband channel filtering. The log amp achieves ±3 dB log linearity. It also doubles as a limiter to convert the signal-to-digital levels for the FSK demodulator. The RSSI itself is used for amplitude shift keying (ASK) demodulation. In ASK mode, extra digital filtering is performed on the RSSI value. Offset correction is achieved using a switched capacitor integrator in feedback around the log amp. This uses the baseband offset clock divide. The RSSI level is converted for user readback and digitally controlled AGC by an 80-level (7-bit) flash ADC. This level can be converted to input power in dBm.



NOTES
1. FWR = FULL WAVE RECTIFIER

Figure 29. RSSI Block Diagram

RSSI Thresholds

When the RSSI is above AGC_HIGH_THRESHOLD, the gain is reduced. When the RSSI is below AGC_LOW_THRESHOLD, the gain is increased. A delay (AGC_DELAY) is programmed to allow for settling of the loop. The user programs the two threshold values (recommended defaults of 30 and 70) and the delay (default of 10). The default AGC setup values should be adequate for most applications. The threshold values must be chosen to be more than 30 apart for the AGC to operate correctly.

Offset Correction Clock

In Register 3, the user should set the BB offset clock divide bits R3_DB[4:5] to give an offset clock between 1 MHz and 2 MHz.

$$BBOS_CLK\ (Hz) = XTAL / (BBOS_CLK_DIVIDE)$$

where BBOS_CLK_DIVIDE can be set to 4, 8, or 16.

AGC Information and Timing

AGC is selected by default, and operates by selecting the appropriate LNA and filter gain settings for the measured RSSI level. It is possible to disable AGC by writing to Register 9 if entering one of the modes listed in Table 5 is desired, for example. The time for the AGC circuit to settle and, therefore, the time to take an accurate RSSI measurement is typically 150 μs, although this depends on how many gain settings the AGC circuit has to cycle through. After each gain change, the AGC loop waits for a programmed time to allow transients to settle.

This wait time can be adjusted to speed up this settling by adjusting the appropriate parameters.

$$AGC_WAIT_TIME = \frac{AGC_DELAY \times SEQ_CLK}{XTAL}$$

$$AGC\ Settling = AGC_WAIT_TIME \times Number\ of\ Gain\ Changes$$

Thus, in the worst case, if the AGC loop has to go through all 5 gain changes, AGC_DELAY = 10, SEQ_CLK = 200 kHz, AGC Settling = 10 × 5 μs × 5 = 250 μs. Minimum AGC_WAIT_TIME needs to be at least 25 μs.

RSSI Formula (Converting to dBm)

$$INPUT_POWER\ [dBm] = -120\ dBm + (READBACK_CODE + GAIN_MODE_CORRECTION) \times 0.5$$

where:

READBACK_CODE is given by Bit RV7 to Bit RV1 in the readback register (see the Readback Format section). GAIN_MODE_CORRECTION is given by the values in Table 6.

LNA gain and filter gain (LG2/LG1, FG2/FG1) are also obtained from the readback register.

Table 6. Gain Mode Correction

LNA Gain (LG2, LG1)	Filter Gain (FG2, FG1)	Gain Mode Correction
H (1,1)	H (1,0)	0
M (1,0)	H (1,0)	24
M (1,0)	M (0,1)	45
M (1,0)	L (0,0)	63
L (0,1)	L (0,0)	90
EL (0,0)	L (0,0)	105

An additional factor should be introduced to account for losses in the front-end matching network/antenna.

FSK DEMODULATORS ON THE ADF7020

The two FSK demodulators on the ADF7020 are

- FSK correlator/demodulator
- Linear demodulator

Select these using the demodulator select bits, R4_DB[4:5].

FSK CORRELATOR/DEMODULATOR

The quadrature outputs of the IF filter are first limited and then fed to a pair of digital frequency correlators that perform band-pass filtering of the binary FSK frequencies at (IF + f_{DEV}) and (IF - f_{DEV}). Data is recovered by comparing the output levels from each of the two correlators. The performance of this frequency discriminator approximates that of a matched filter detector, which is known to provide optimum detection in the presence of additive white Gaussian noise (AWGN).

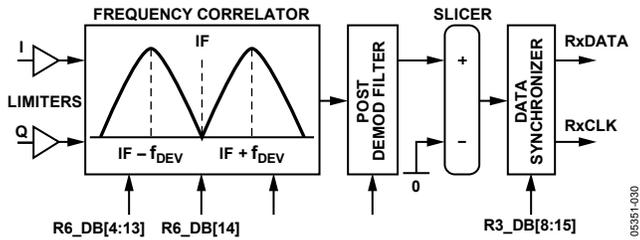


Figure 30. FSK Correlator/Demodulator Block Diagram

Postdemodulator Filter

A second-order, digital low-pass filter removes excess noise from the demodulated bit stream at the output of the discriminator. The bandwidth of this postdemodulator filter is programmable and must be optimized for the user’s data rate. If the bandwidth is set too narrow, performance is degraded due to intersymbol interference (ISI). If the bandwidth is set too wide, excess noise degrades the receiver’s performance. Typically, the 3 dB bandwidth of this filter is set at approximately 0.75 times the user’s data rate, using Bits R4_DB[6:15].

Bit Slicer

The received data is recovered by the threshold detecting the output of the postdemodulator low-pass filter. In the correlator/demodulator, the binary output signal levels of the frequency discriminator are always centered on 0. Therefore, the slicer threshold level can be fixed at 0, and the demodulator performance is independent of the run-length constraints of the transmit data bit stream. This results in robust data recovery, which does not suffer from the classic baseline wander problems that exist in the more traditional FSK demodulators.

Frequency errors are removed by an internal AFC loop that measures the average IF frequency at the limiter output and applies a frequency correction value to the fractional-N synthesizer. This loop should be activated when the frequency errors are greater than approximately 40% of the transmit frequency deviation (see the AFC section).

Data Synchronizer

An oversampled digital PLL is used to resynchronize the received bit stream to a local clock. The oversampled clock rate of the PLL (CDR_CLK) must be set at 32 times the data rate. See the Register 3—Receiver Clock Register Comments section for a definition of how to program. The clock recovery PLL can accommodate frequency errors of up to ±2%.

FSK Correlator Register Settings

To enable the FSK correlator/demodulator, Bits R4_DB[5:4] should be set to 01. To achieve best performance, the bandwidth of the FSK correlator must be optimized for the specific deviation frequency that is used by the FSK transmitter.

The discriminator BW is controlled in Register 6 by Bit R6_DB[4:13] and is defined as

$$DISCRIMINATOR_BW = \frac{DEMOD_CLK \times K}{800 \times 10^3}$$

where:

DEMOD_CLK is as defined in the Register 3—Receiver Clock Register section, second comment.

$K = \text{Round}(200 \times 10^3 / \text{FSK Deviation})$

To optimize the coefficients of the FSK correlator, two additional bits, R6_DB14 and R6_DB29, must be assigned. The value of these bits depends on whether K (as defined above) is odd or even. These bits are assigned according to Table 7 and Table 8.

Table 7. When K Is Even

K	K/2	R6_DB14	R6_DB29
Even	Even	0	0
Even	Odd	0	1

Table 8. When K Is Odd

K	(K + 1)/2	R6_DB14	R6_DB29
Odd	Even	1	0
Odd	Odd	1	1

Postdemodulator Bandwidth Register Settings

The 3 dB bandwidth of the postdemodulator filter is controlled by Bits R4_DB[6:15] and is given by

$$POSTDEMOD_BW_SETTING = \frac{2^{10} \times 2\pi \times f_{CUTOFF}}{DEMOD_CLK}$$

where f_{CUTOFF} is the target 3 dB bandwidth in Hz of the post-demodulator filter. This should typically be set to 0.75 times the data rate (DR).

Some sample settings for the FSK correlator/demodulator are

$$\begin{aligned} DEMOD_CLK &= 5 \text{ MHz} \\ DR &= 9.6 \text{ kbps} \\ f_{DEV} &= 20 \text{ kHz} \end{aligned}$$

Therefore,

$$\begin{aligned} f_{CUTOFF} &= 0.75 \times 9.6 \times 10^3 \text{ Hz} \\ POSTDEMOD_BW_SETTING &= 2^{11} \pi 7.2 \times 10^3 \text{ Hz} / (5 \text{ MHz}) \\ POSTDEMOD_BW_SETTING &= \text{Round}(9.26) = 9 \end{aligned}$$

and

$$\begin{aligned} K &= \text{Round}(200 \text{ kHz}) / 20 \text{ kHz} = 10 \\ DISCRIMINATOR_BW &= (5 \text{ MHz} \times 10) / (800 \times 10^3) = 62.5 = 63 \text{ (rounded to the nearest integer)} \end{aligned}$$

Table 9. Register Settings¹

Setting Name	Register Address	Value
POSTDEMOD_BW_SETTING	R4_DB[6:15]	0x09
DISCRIMINATOR_BW	R6_DB[4:13]	0x3F
DOT_PRODUCT	R6_DB14	0
RXDATA_INVERT	R6_DB29	1

¹ The latest version of the [ADF7020](#) configuration software can aid in calculating register settings.

LINEAR FSK DEMODULATOR

Figure 31 shows a block diagram of the linear FSK demodulator.

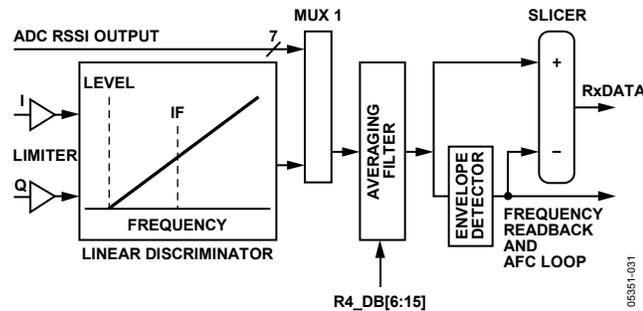


Figure 31. Block Diagram of Frequency Measurement System and ASK/OOK/Linear FSK Demodulator

This method of frequency demodulation is useful when very short preamble length is required, and the system protocol cannot support the overhead of the settling time of the internal feedback AFC loop settling.

A digital frequency discriminator provides an output signal that is linearly proportional to the frequency of the limiter outputs. The discriminator output is then filtered and averaged using a combined averaging filter and envelope detector. The demodulated FSK data is recovered by threshold-detecting the output of the averaging filter, (see Figure 31). In this mode, the slicer output shown in Figure 31 is routed to the data synchronizer PLL for clock synchronization. To enable the linear FSK demodulator, set Bits R4_DB[4:5] to 00.

The 3 dB bandwidth of the postdemodulation filter is set in the same way as the FSK correlator/demodulator, which is set in R4_DB[6:15] and is defined as

$$POSTDEMOD_BW_SETTING = \frac{2^{10} \times 2\pi \times f_{CUTOFF}}{DEMOM_CLK}$$

where f_{CUTOFF} is the target 3 dB bandwidth in Hz of the postdemodulator filter. DEMOD_CLK is as defined in the Register 3—Receiver Clock Register section, second comment.

ASK/OOK Operation

ASK/OOK demodulation is activated by setting Bits R4_DB[4:5] to 10.

Digital filtering and envelope detecting the digitized RSSI input via MUX 1, as shown in Figure 31, performs ASK/OOK demodulation. The bandwidth of the digital filter must be optimized to remove any excess noise without causing ISI in the received ASK/OOK signal.

The 3 dB bandwidth of this filter is typically set at approximately 0.75 times the user data rate and is assigned by R4_DB[6:15] as

$$POSTDEMOD_BW_SETTING = \frac{2^{10} \times 2\pi \times f_{CUTOFF}}{DEMOM_CLK}$$

where f_{CUTOFF} is the target 3 dB bandwidth in Hz of the postdemodulator filter.

It is also recommended to adjust the peak response factor to 6 in Register 10 for robust operation over the full input range. This improves the receiver's AM immunity performance.

AFC

The [ADF7020](#) supports a real-time AFC loop, which is used to remove frequency errors that can arise due to mismatches between the transmit and receive crystals. This uses the frequency discriminator block, as described in the Linear FSK Demodulator section (see Figure 31). The discriminator output is filtered and averaged to remove the FSK frequency modulation, using a combined averaging filter and envelope detector. In FSK mode, the output of the envelope detector provides an estimate of the average IF frequency.

Two methods of AFC, external and internal, are supported on the [ADF7020](#) (in FSK mode only).

External AFC

The user reads back the frequency information through the [ADF7020](#) serial port and applies a frequency correction value to the fractional-N synthesizer's N divider.

The frequency information is obtained by reading the 16-bit signed AFC_READBACK, as described in the Readback Format section, and applying the following formula:

$$FREQ_RB \text{ [Hz]} = (AFC_READBACK \times DEMOD_CLK) / 2^{15}$$

Note that while the AFC_READBACK value is a signed number, under normal operating conditions, it is positive. The frequency error can be calculated from

$$FREQ_ERROR \text{ [Hz]} = FREQ_RB \text{ (Hz)} - 200 \text{ kHz}$$

Thus, in the absence of frequency errors, the FREQ_RB value is equal to the IF frequency of 200 kHz.

Internal AFC

The ADF7020 supports a real-time internal automatic frequency control loop. In this mode, an internal control loop automatically monitors the frequency error and adjusts the synthesizer N divider using an internal PI control loop.

The internal AFC control loop parameters are controlled in Register 11. The internal AFC loop is activated by setting R11_DB20 to 1. A scaling coefficient must also be entered, based on the crystal frequency in use. This is set up in Bits R11_DB[4:19] and should be calculated using

$$AFC_SCALING_COEFFICIENT = (500 \times 2^{24})/XTAL$$

Therefore, using a 10 MHz XTAL yields an AFC scaling coefficient of 839.

AFC Performance

The improved sensitivity performance of the Rx when AFC is enabled and in the presence of frequency errors is shown in Figure 18. The maximum AFC frequency range is ± 50 kHz, which corresponds to ± 58 ppm at 868 MHz. This is the total error tolerance allowed in the link. For example, in a point-to-point system, AFC can compensate for two ± 29 ppm crystals or one ± 50 ppm crystal and one ± 8 ppm TCXO.

AFC settling typically takes 48 bits to settle within ± 1 kHz. This can be improved by increasing the postdemodulator bandwidth in Register 4 at the expense of Rx sensitivity.

When AFC errors have been removed using either the internal or external AFC, further improvement in the receiver's sensitivity can be obtained by reducing the IF filter bandwidth using Bits R1_DB[22:23].

AUTOMATIC SYNC WORD RECOGNITION

The ADF7020 also supports automatic detection of the sync or ID fields. To activate this mode, the sync (or ID) word must be preprogrammed into the ADF7020. In receive mode, this preprogrammed word is compared to the received bit stream and, when a valid match is identified, the external pin INT/LOCK is asserted by the ADF7020.

This feature can be used to alert the microprocessor that a valid channel has been detected. It relaxes the computational requirements of the microprocessor and reduces the overall power consumption. The INT/LOCK is automatically deasserted again after nine data clock cycles.

The automatic sync/ID word detection feature is enabled by selecting Demodulator Mode 2 or Demodulator Mode 3 in the demodulator setup register. Do this by setting Bits R4_DB[25:23] = 010 or 011. Bits R5_DB[4:5] are used to set the length of the sync/ID word, which can be 12, 16, 20, or 24 bits long. The transmitter must transmit the MSB of the sync byte first and the LSB last to ensure proper alignment in the receiver sync byte detection hardware.

For systems using forward error correction (FEC), an error tolerance parameter can also be programmed that accepts a valid match when up to three bits of the word are incorrect. The error tolerance value is assigned in Bits R5_DB[6:7].