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High Performance, Narrow-Band Transceiver IC

Data Sheet

ADF7021-V

FEATURES

- High performance, low power, narrow-band transceiver
- Enhanced performance ADF7021-N with external VCO
- Frequency bands using external VCO: 80 MHz to 960 MHz
- Improved adjacent channel power (ACP) and adjacent channel rejection (ACR) compared with the ADF7021-N
- Programmable IF filter bandwidths: 9 kHz, 13.5 kHz, and 18.5 kHz
- Modulation schemes: 2FSK, 3FSK, 4FSK, MSK
- Spectral shaping: Gaussian and raised cosine filtering
- Data rates: 0.05 kbps to 24 kbps
- Power supply: 2.3 V to 3.6 V
- Programmable output power: −16 dBm to +13 dBm in 63 steps
- Automatic power amplifier (PA) ramp control
- Receiver sensitivity
  - −125 dBm at 250 bps, 2FSK
  - −122 dBm at 1 kbps, 2FSK
- Patent pending, on-chip image rejection calibration
- On-chip fractional-N PLL
- On-chip, 7-bit ADC and temperature sensor
- Fully automatic frequency control (AFC) loop
- Digital received signal strength indication (RSSI)
- Integrated Tx/Rx switch
- Leakage current in power-down mode: 0.1 µA

APPLICATIONS

- Narrow-band, short-range device (SRD) standards
  - ETSI EN 300 220
    - 500 mW output power capability in 869 MHz g3 subband with external PA
    - High performance receiver rejection, blocking, and adjacent channel power (ACP)
  - FCC Part 90 (meets Emission Mask D requirements)
  - FCC Part 95
  - ARIB STD-T67
- Wireless metering
- Narrow-band wireless telemetry

FUNCTIONAL BLOCK DIAGRAM

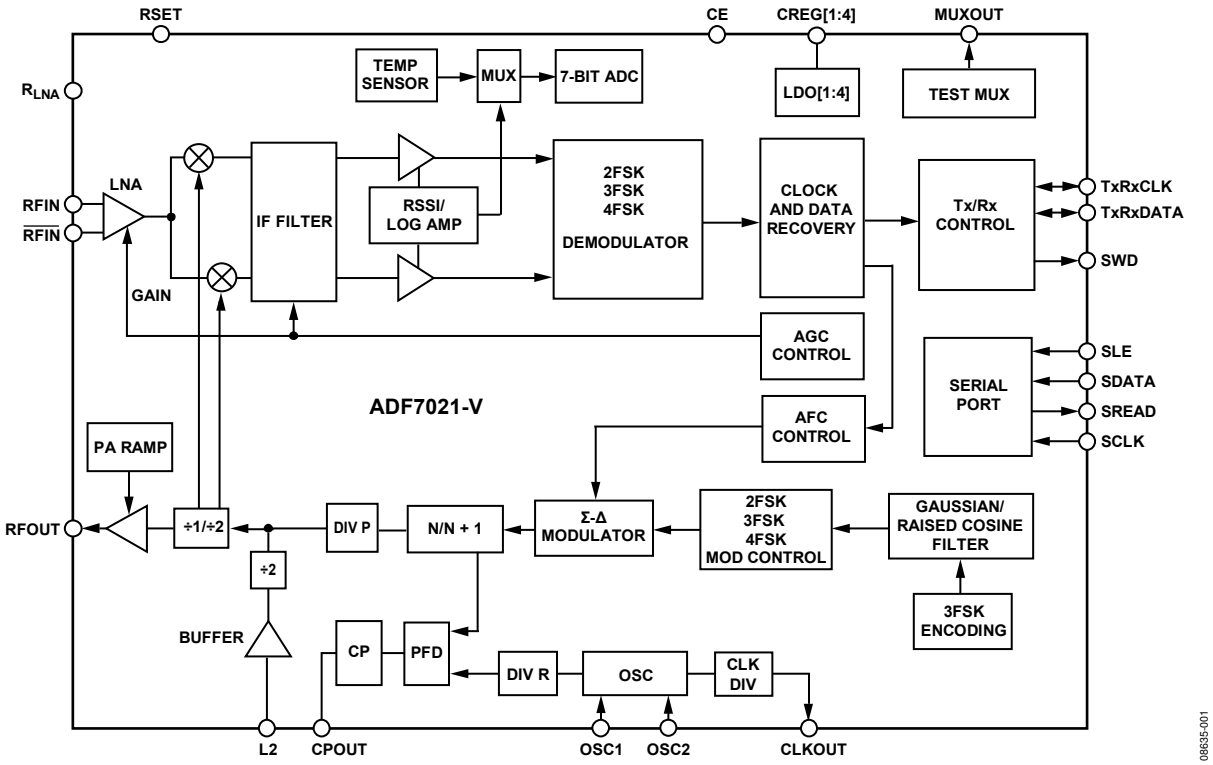

Figure 1.

Rev. B

Document Feedback

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ADF7021-V* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADF7021-V Evaluation Boards

DOCUMENTATION

Application Notes

- AN-0987: Designing a Wireless Transceiver System to Meet the Wireless M-Bus Standard
- AN-1182: Understanding and Optimizing the AFC Loop on the ADF7021 for Minimum Preamble
- AN-1258: Image Rejection Calibration on the ADF7021, ADF7021-N, and ADF7021-V
- AN-1285: ADF7021-N Radio Performance for Wireless Meter-Bus (WM-Bus), Mode N
- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-771: ADSP-BF533 EZ-KIT Lite and ADF70xx Interface
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
- AN-852: Using the Test DAC on the ADF702x to Implement Functions Such as Analog FM DEMOD, SNR Measurement, FEC Decoding, and PSK/4FSK Demodulation
- AN-859: RF Port Impedance Data, Matching, and External Component Selection for the ADF7020-1, ADF7021, and ADF7021-N
- AN-915: CDR Operation for ADF7020, ADF7020-1, ADF7021, and ADF7025

Data Sheet

- ADF7021-V: High Performance,Narrow-Band Transceiver IC Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADF70xx Evaluation Software
- ADIismLINK Development Platform

TOOLS AND SIMULATIONS

- ADIsimSRD Design Studio

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Emerging Energy Applications Solutions Bulletin, Volume 10, Issue 4

Technical Articles

- Low Power, Low Cost, Wireless ECG Holter Monitor
- RF Meets Power Lines: Designing Intelligent Smart Grid Systems that Promote Energy Efficiency
- Smart Metering Technology Promotes Energy Efficiency for a Greener World
- The Use of Short Range Wireless in a Multi-Metering System
- Understand Wireless Short-Range Devices for Global License-Free Systems
- Wireless Short Range Devices and Narrowband Communications
- Wireless Technologies for Smart Meters: Focus on Water Metering

DESIGN RESOURCES

- ADF7021-V Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADF7021-V EngineerZone Discussions.

SAMPLE AND BUY

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TABLE OF CONTENTS

REVISION HISTORY

9/14—Rev. A to Rev. B

Changes to Table 8 16
Change to RSSI Formula (Converting to dBm) Section 30
Change to Postdemodulator Filter Setup Section 33
Change to When to Use Fine Calibration Section 38
Change to Battery Voltage/ADCIN/Temperature Sensor Readback Section 44
Change to Register 4—Demodulator Setup Register Section 50
Change to Register 7—Readback Setup Register Section 53
Change to Register 4—AFC Register Section 56

8/12—Rev. 0 to Rev. A

Changes to Figure 6 15
Updated Outline Dimensions 60
Changes to Ordering Guide 60

4/10—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADF7021-V is a high performance, low power, narrow-band RF transceiver based on the ADF7021-N. The architecture of the ADF7021-V transceiver is similar to that of the ADF7021-N except that an external VCO is used by the on-chip RF synthesizer for applications that require improved phase noise performance.

The ADF7021-V is designed to operate in both the license-free ISM bands and in the licensed bands from 80 MHz to 960 MHz.

To minimize RF feedthrough and spurious emissions, the external VCO operates at 2× or 4× the desired RF frequency; the ADF7021-V supports a maximum VCO frequency operation of 1920 MHz. The 4× VCO operation is programmable by enabling an additional on-chip divide-by-2 outside the RF synthesizer loop and offers improved phase noise performance.

As with the ADF7021-N receiver, the IF filter bandwidths of 9 kHz, 13.5 kHz, and 18.5 kHz are supported, making the ADF7021-V ideally suited to worldwide narrow-band telemetry applications.

The part has both Gaussian and raised cosine transmit data filtering options to improve spectral efficiency for narrow-band applications. It is suitable for circuit applications targeted at the following:

- European ETSI EN 300 220
- North American FCC Part 15, Part 90, and Part 95
- Japanese ARIB STD-T67
- Korean short-range device regulations
- Chinese short-range device regulations

A complete transceiver can be built using a small number of discrete external components, making the ADF7021-V very suitable for area-sensitive, high performance driven applications.

The range of on-chip FSK modulation and data filtering options allows users greater flexibility in their choice of modulation schemes while meeting the tight spectral efficiency requirements. The ADF7021-V also supports protocols that dynamically switch among 2FSK, 3FSK, and 4FSK to maximize communication range and data throughput.

The transmit section contains a low noise fractional-N PLL with an output resolution of <1 ppm. The frequency-agile PLL allows the ADF7021-V to be used in frequency-hopping spread spectrum (FHSS) systems. The VCO is external, which provides better phase noise and thus lower adjacent channel power (ACP) and adjacent channel rejection (ACR) compared with the ADF7021-N. The VCO tuning range extends from 0.2 V to 2 V; take this range into account when choosing the external VCO.

The transmitter output power is programmable in 63 steps from −16 dBm to +13 dBm and has an automatic power amplifier ramp control to prevent spectral splatter and help meet regulatory standards. The transceiver RF frequency, channel spacing, and modulation are programmable using a simple 3-wire interface. The device operates with a power supply range of 2.3 V to 3.6 V and can be powered down when not in use.

A low IF architecture is used in the receiver (100 kHz), which minimizes power consumption and the external component count yet avoids dc offset and flicker noise at low frequencies. The IF filter has programmable bandwidths of 9 kHz, 13.5 kHz, and 18.5 kHz. The ADF7021-V supports a wide variety of programmable features, including Rx linearity, sensitivity, and IF bandwidth, allowing the user to trade off receiver sensitivity and selectivity against current consumption, depending on the application. The receiver also features a patented automatic frequency control (AFC) loop with programmable pull-in range that allows the PLL to remove the frequency error in the incoming signal.

The receiver achieves an image rejection performance of 50 dB using a patent-pending IR calibration scheme that does not require the use of an external RF source.

An on-chip ADC provides readback of the integrated temperature sensor, external analog input, battery voltage, and RSSI signal, which can eliminate the need for an external ADC in some applications. The temperature sensor is accurate to ±10°C over the full operating temperature range of −40°C to +85°C. This accuracy can be improved by performing a one-point calibration at room temperature and storing the result in memory.

SPECIFICATIONS

V_{DD} = 2.3 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C. All measurements are performed with the EVAL-ADF7021-VDBxZ using the PN9 data sequence, unless otherwise noted. The version number of ETSI EN 300 200-1 is V2.3.1. LBW = loop bandwidth and IFBW = IF filter bandwidth.

RF AND PLL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF CHARACTERISTICS					
Phase Frequency Detector (PFD) Frequency	RF/256		24	MHz	Maximum usable PFD at a particular RF frequency is limited by the minimum N divider value
PHASE-LOCKED LOOP (PLL)					
Normalized In-Band Phase Noise Floor[1]		−203		dBc/Hz	
PLL Settling		155		µs	Measured for a 100 kHz frequency step to within 5 ppm accuracy, PFD = 19.68 MHz, LBW = 8 kHz
EXTERNAL VCO					
Tuning Range	0.2		2	V	
Pin L2 Input Sensitivity	0			dBm	VCO frequency < 1920 MHz
REFERENCE INPUT					
Crystal Reference[2]	3.625		24	MHz	
External Oscillator[2, 3]	3.625		24	MHz	
Crystal Start-Up Time[4]					10 MHz XTAL, 33 pF load capacitors, V_{DD} = 3.0 V
XTAL Bias = 20 µA		0.930		ms	
XTAL Bias = 35 µA		0.438		ms	
Input Level for External Oscillator					
OSC1 Pin		0.8		V p-p	Clipped sine wave
OSC2 Pin		CMOS levels		V	
ADC PARAMETERS					V_{DD} = 2.3 V to 3.6 V, T_A = 25°C
Integral Nonlinearity (INL)		±0.4		LSB	
Differential Nonlinearity (DNL)		±0.4		LSB	

[1] This value can be used to calculate the in-band phase noise for any operating frequency. Use the following equation to calculate the in-band phase noise performance as seen at the power amplifier (PA) output: −203 + 10 log(f_{PFD}) + 20 log$N$.
[2] Guaranteed by design. Sample tested to ensure compliance.
[3] A TCXO, VCXO, or OCXO can be used as an external oscillator.
[4] Crystal start-up time is the time from chip enable (CE) being asserted to correct clock frequency on the CLKOUT pin.

TRANSMISSION SPECIFICATIONS

LBW = loop bandwidth.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DATA RATE					Limited by the loop bandwidth
2FSK	0.05		18.5	kbps	LBW must be ≥1.25 × data rate for correct operation
3FSK	0.05		18.5	kbps	LBW = 18.5 kHz
4FSK	0.05		24	kbps	LBW = 18.5 kHz
MODULATION					
Frequency Deviation (f_{DEV})	0.056		28.26	kHz	PFD = 3.625 MHz
	0.306		156	kHz	PFD = 20 MHz
Frequency Deviation Resolution	56			Hz	PFD = 3.625 MHz
Gaussian Filter Bandwidth Time (BT)		0.5			
Raised Cosine Filter Alpha		0.5/0.7			Programmable
TRANSMIT POWER					
Maximum Transmit Power[1]		13		dBm	V_{DD} = 3.0 V, T_A = 25°C
Transmit Power Variation vs. Temperature		±1		dB	T_A = −40°C to +85°C
Transmit Power Variation vs. V_{DD}		±1		dB	V_{DD} = 2.3 V to 3.6 V at 915 MHz, T_A = 25°C
Transmit Power Flatness		±1		dB	902 MHz to 928 MHz, V_{DD} = 3 V, T_A = 25°C
Programmable Step Size		0.3125		dB	−16 dBm to +13 dBm
ADJACENT CHANNEL POWER (ACP)					Gaussian 2FSK modulation, 13 dBm output power, PFD = 19.68 MHz, LBW = 6 kHz
460 MHz					
12.5 kHz Channel Spacing		−47		dBm	Measured in a ±8.5 kHz bandwidth at ±12.5 kHz offset, 2.4 kbps PN9 data, f_{DEV} = 1.2 kHz
25 kHz Channel Spacing		−53		dBm	Measured in a ±16 kHz bandwidth at ±25 kHz offset, 4.8 kbps PN9 data, f_{DEV} = 2.4 kHz
868 MHz					Compliant with ETSI EN 300 220
12.5 kHz Channel Spacing		−44		dBm	Measured in a ±8.5 kHz bandwidth at ±12.5 kHz offset, 2.4 kbps PN9 data, f_{DEV} = 1.2 kHz
25 kHz Channel Spacing		−49		dBm	Measured in a ±16 kHz bandwidth at ±25 kHz offset, 4.8 kbps PN9 data, f_{DEV} = 2.4 kHz
MODULATION BANDWIDTH					869.525 MHz, Gaussian 2FSK modulation, 4.8 kbps, f_{DEV} = 2.4 kHz, 10 dBm output power,[2] compliant with ETSI EN 300 220, LBW = 6 kHz
125 kHz Offset		−74.5		dBm/1 kHz	
125 kHz + 200 kHz		−79		dBm/1 kHz	
125 kHz + 400 kHz		−69.5		dBm/10 kHz	
125 kHz + 1 MHz		−62		dBm/100 kHz	
EMISSION MASK					FCC Part 90 Emission Mask D, 100 Hz resolution bandwidth, Gaussian 2FSK modulation, LBW = 6 kHz, 10 dBm output power, 2.4 kbps PN9 data, f_{DEV} = 1.2 kHz
12.5 kHz Offset					
460 MHz		−77		dBc	
OCCUPIED BANDWIDTH					99.0% of total mean power, LBW = 6 kHz, 10 dBm output power
2FSK, Gaussian Data Filtering					
12.5 kHz Channel Spacing		4.0		kHz	2.4 kbps PN9 data, f_{DEV} = 1.2 kHz
25 kHz Channel Spacing		8.5		kHz	4.8 kbps PN9 data, f_{DEV} = 2.4 kHz
2FSK, Raised Cosine Data Filtering					
12.5 kHz Channel Spacing		4.5		kHz	2.4 kbps PN9 data, f_{DEV} = 1.2 kHz
25 kHz Channel Spacing		9.6		kHz	4.8 kbps PN9 data, f_{DEV} = 2.4 kHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
3FSK, Raised Cosine Filtering					
12.5 kHz Channel Spacing		4.3		kHz	2.4 kbps PN9 data, f_{DEV} = 1.2 kHz
25 kHz Channel Spacing		8.5		kHz	4.8 kbps PN9 data, f_{DEV} = 2.4 kHz
4FSK, Raised Cosine Filtering					
25 kHz Channel Spacing		11.3		kHz	9.6 kbps PN9 data, f_{DEV} = 1.2 kHz
SPURIOUS EMISSIONS					
Reference Spurs		−65		dBc	LBW = 8 kHz
HARMONICS[3]					13 dBm output power
Second Harmonic		−35/−52		dBc	Unfiltered conductive/filtered conductive
Third Harmonic		−43/−60		dBc	Unfiltered conductive/filtered conductive
All Other Harmonics		−36/−65		dBc	Unfiltered conductive/filtered conductive
OPTIMUM PA LOAD IMPEDANCE					
f_{RF} = 915 MHz		39 + j61		Ω	
f_{RF} = 868 MHz		48 + j54		Ω	
f_{RF} = 470 MHz		97.5 + j64.4		Ω	
f_{RF} = 450 MHz		98 + j65		Ω	
f_{RF} = 426 MHz		100 + j65		Ω	
f_{RF} = 315 MHz		129 + j63		Ω	
f_{RF} = 175 MHz		173 + j49		Ω	
f_{RF} = 169 MHz		74.5 + j48.5		Ω	

[1] Measured as maximum unmodulated power.
[2] Suitable for ETSI 500 mW Tx requirements.
[3] Conductive filtered harmonic emissions measured on the EVAL-ADF7021-VDBxZ, which includes a T-stage harmonic filter (two inductors and one capacitor).

RECEIVER SPECIFICATIONS

LBW = loop bandwidth and IFBW = IF filter bandwidth.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DATA RATE					Limited by the IF filter bandwidth[1]
2FSK	0.05		9.0	kbps	IFBW = 9 kHz
	0.05		13.5	kbps	IFBW = 13.5 kHz
	0.05		18.5	kbps	IFBW = 18.5 kHz
3FSK	0.05		18.5	kbps	IFBW = 18.5 kHz
4FSK	0.05		24	kbps	IFBW = 18.5 kHz
SENSITIVITY					Bit error rate (BER) = 10^{-3}
2FSK					
Sensitivity at 0.25 kbps		−125		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IFBW = 9.0 kHz
Sensitivity at 1 kbps		−122		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IFBW = 9.0 kHz
Sensitivity at 2.4 kbps		−119		dBm	f_{DEV} = 1.2 kHz, high sensitivity mode, IFBW = 9.0 kHz
Sensitivity at 4.8 kbps		−116		dBm	f_{DEV} = 2.4 kHz, high sensitivity mode, IFBW = 9.0 kHz
Sensitivity at 9.6 kbps		−114		dBm	f_{DEV} = 4.8 kHz, high sensitivity mode, IFBW = 18.5 kHz
Gaussian 2FSK					
Sensitivity at 0.25 kbps		−125		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IFBW = 9.0 kHz
Sensitivity at 1 kbps		−122		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IFBW = 9.0 kHz
Sensitivity at 2.4 kbps		−120		dBm	f_{DEV} = 1.2 kHz, high sensitivity mode, IFBW = 9.0 kHz
Sensitivity at 4.8 kbps		−117		dBm	f_{DEV} = 2.4 kHz, high sensitivity mode, IFBW = 9.0 kHz
Sensitivity at 9.6 kbps		−114		dBm	f_{DEV} = 4.8 kHz, high sensitivity mode, IFBW = 18.5 kHz
GMSK					
Sensitivity at 4.8 kbps		−114.5		dBm	f_{DEV} = 1.2 kHz, high sensitivity mode, IFBW = 9.0 kHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Raised Cosine 2FSK					
Sensitivity at 0.25 kbps		−125		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IFBW = 9.0 kHz
Sensitivity at 1 kbps		−121		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IFBW = 9.0 kHz
Sensitivity at 2.4 kbps		−120		dBm	f_{DEV} = 1.2 kHz, high sensitivity mode, IFBW = 9.0 kHz
Sensitivity at 4.8 kbps		−115		dBm	f_{DEV} = 2.4 kHz, high sensitivity mode, IFBW = 9.0 kHz
Sensitivity at 9.6 kbps		−114		dBm	f_{DEV} = 4.8 kHz, high sensitivity mode, IFBW = 18.5 kHz
3FSK					
Sensitivity at 4.8 kbps		−110		dBm	f_{DEV} = 2.4 kHz, high sensitivity mode, IFBW = 18.5 kHz, Viterbi detection on
Raised Cosine 3FSK					
Sensitivity at 4.8 kbps		−110		dBm	f_{DEV} = 2.4 kHz, high sensitivity mode, IFBW = 13.5 kHz, alpha = 0.5, Viterbi detection on
4FSK					
Sensitivity at 4.8 kbps		−112		dBm	f_{DEV} (inner)^2 = 1.2 kHz, high sensitivity mode, IFBW = 13.5 kHz
Raised Cosine 4FSK					
Sensitivity at 4.8 kbps		−109		dBm	f_{DEV} (inner)^2 = 1.2 kHz, high sensitivity mode, IFBW = 13.5 kHz, alpha = 0.5
INPUT IP3					Two-tone test, f_{LO} = 860 MHz, f1 = f_{LO} + 100 kHz, f2 = f_{LO} − 800 kHz
Low Gain, Enhanced Linearity Mode		−3		dBm	LNA_GAIN = 3, MIXER_LINEARITY = 1
Medium Gain Mode		−13.5		dBm	LNA_GAIN = 10, MIXER_LINEARITY = 0
High Sensitivity Mode		−24		dBm	LNA_GAIN = 30, MIXER_LINEARITY = 0
ADJACENT CHANNEL REJECTION (ACR)					
868 MHz					Desired signal is 3 dB above the sensitivity point of −109.5 dBm as per EN 300 220; rejection is measured as the level of an unmodulated interferer to cause a BER of 10^{-2} for the desired signal
12.5 kHz Channel Spacing		−60		dBm	IFBW = 9 kHz, data rate = 0.25 kbps, f_{DEV} = 1 kHz, LBW = 6 kHz
25 kHz Channel Spacing		−39		dBm	IFBW = 9 kHz, data rate = 0.25 kbps, f_{DEV} = 1 kHz, LBW = 6 kHz
12.5 kHz Channel Spacing		−60		dBm	IFBW = 9 kHz, data rate = 1 kbps, f_{DEV} = 1 kHz, LBW = 6 kHz
25 kHz Channel Spacing		−40		dBm	IFBW = 9 kHz, data rate = 1 kbps, f_{DEV} = 1 kHz, LBW = 6 kHz
12.5 kHz Channel Spacing		−59.5		dBm	IFBW = 9 kHz, data rate = 2.4 kbps, f_{DEV} = 1.2 kHz, LBW = 6 kHz
25 kHz Channel Spacing		−42		dBm	IFBW = 9 kHz, data rate = 2.4 kbps, f_{DEV} = 1.2 kHz, LBW = 6 kHz
12.5 kHz Channel Spacing		−63		dBm	IFBW = 9 kHz, data rate = 4.8 kbps, f_{DEV} = 2.4 kHz, LBW = 6 kHz
25 kHz Channel Spacing		−45		dBm	IFBW = 9 kHz, data rate = 4.8 kbps, f_{DEV} = 2.4 kHz, LBW = 6 kHz
25 kHz Channel Spacing		−57		dBm	IFBW = 18.5 kHz, data rate = 9.6 kbps, f_{DEV} = 4.8 kHz, LBW = 6 kHz
460 MHz					Desired signal is at −106.5 dBm; rejection is measured as the level of an unmodulated interferer to cause a BER of 10^{-2} for the desired signal
12.5 kHz Channel Spacing		−59.5		dBm	IFBW = 9 kHz, data rate = 0.25 kbps, f_{DEV} = 1 kHz, LBW = 6 kHz
25 kHz Channel Spacing		−37.5		dBm	IFBW = 9 kHz, data rate = 0.25 kbps, f_{DEV} = 1 kHz, LBW = 6 kHz
12.5 kHz Channel Spacing		−60		dBm	IFBW = 9 kHz, data rate = 1 kbps, f_{DEV} = 1 kHz, LBW = 6 kHz
25 kHz Channel Spacing		−41		dBm	IFBW = 9 kHz, data rate = 1 kbps, f_{DEV} = 1 kHz, LBW = 6 kHz
12.5 kHz Channel Spacing		−62		dBm	IFBW = 9 kHz, data rate = 2.4 kbps, f_{DEV} = 1.2 kHz, LBW = 6 kHz
25 kHz Channel Spacing		−43		dBm	IFBW = 9 kHz, data rate = 2.4 kbps, f_{DEV} = 1.2 kHz, LBW = 6 kHz
12.5 kHz Channel Spacing		−61.5		dBm	IFBW = 9 kHz, data rate = 4.8 kbps, f_{DEV} = 2.4 kHz, LBW = 6 kHz
25 kHz Channel Spacing		−44.5		dBm	IFBW = 9 kHz, data rate = 4.8 kbps, f_{DEV} = 2.4 kHz, LBW = 6 kHz
25 kHz Channel Spacing		−56		dBm	IFBW = 18.5 kHz, data rate = 9.6 kbps, f_{DEV} = 4.8 kHz, LBW = 6 kHz
COCHANNEL REJECTION					Desired signal is 3 dB above the sensitivity point of −109.5 dBm; rejection is measured as the level of an interferer to cause a BER of 10^{-2} for the desired signal
868 MHz		−5		dB	IFBW = 9 kHz, data rate = 4.8 kbps, f_{DEV} = 2.4 kHz, LBW = 6 kHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
IMAGE CHANNEL REJECTION					Desired signal (2FSK, 9.6 kbps, ±4 kHz deviation) is 3 dB above the sensitivity point (BER = 10^{-2}); modulated interferer (2FSK, 9.6 kbps, ±4 kHz deviation) is placed at the image frequency of f_{RF} − 200 kHz; the interferer level is increased until BER = 10^{-2}
868 MHz		26/39		dB	Uncalibrated/calibrated,[3] V_{DD} = 3.0 V, T_A = 25°C
460 MHz		29/50		dB	Uncalibrated/calibrated,[3] V_{DD} = 3.0 V, T_A = 25°C
BLOCKING					Desired signal is 3 dB above the sensitivity point of −109.5 dBm; rejection is measured as the level of an unmodulated interferer to cause a BER of 10^{-2} for the desired signal; as per ETSI EN 300 220-1
±1 MHz		−29.5		dBm	
±2 MHz		−26.5		dBm	
±5 MHz		−26		dBm	
±10 MHz		−25.5		dBm	
SATURATION (MAXIMUM INPUT LEVEL)		12		dBm	2FSK mode, BER = 10^{-3}
RECEIVED SIGNAL STRENGTH INDICATION (RSSI)					
Input Power Range[4]		−120 to −47		dBm	
Linearity		±2		dB	Input power range = −100 dBm to −47 dBm
Absolute Accuracy		±3		dB	Input power range = −100 dBm to −47 dBm
Response Time		333		µs	As per AGC gain stage, AGC clock = 3 kHz
AUTOMATIC FREQUENCY LOOP (AFC)					
Pull-In Range, Minimum		0.5		kHz	Range is programmable in Register 10 (Bits[DB31:DB24])
Pull-In Range, Maximum		1.5 × IF_ FILTER_BW		kHz	Range is programmable in Register 10 (Bits[DB31:DB24])
Response Time		96		Bits	Dependent on modulation index
Accuracy		0.5		kHz	Input power range = −100 dBm to +12 dBm
Rx SPURIOUS EMISSIONS[5]					
External 920 MHz VCO		−54/−88		dBm	<1 GHz at antenna input, unfiltered conductive/filtered conductive
External 920 MHz VCO		−45/−66		dBm	>1 GHz at antenna input, unfiltered conductive/filtered conductive
External 1738 MHz VCO		−85/−85		dBm	<1 GHz at antenna input, unfiltered conductive/filtered conductive
External 1738 MHz VCO		−39/−52		dBm	>1 GHz at antenna input, unfiltered conductive/filtered conductive
LNA INPUT IMPEDANCE					RFIN to RFGND; refer to the AN-859 Application Note for other frequencies
f_{RF} = 915 MHz		24 − j60		Ω	
f_{RF} = 868 MHz		26 − j63		Ω	
f_{RF} = 470 MHz		58 − j124		Ω	
f_{RF} = 450 MHz		63 − j129		Ω	
f_{RF} = 426 MHz		68 − j134		Ω	
f_{RF} = 315 MHz		96 − j160		Ω	
f_{RF} = 175 MHz		178 − j190		Ω	
f_{RF} = 169 MHz		182.5 − j194		Ω	

[1] Using Gaussian or raised cosine filtering. Choose the frequency deviation to ensure that the transmit-occupied signal bandwidth is within the receiver IF filter bandwidth.
[2] 4FSK f_{DEV} is defined as the frequency spacing from the RF carrier to $+f_{DEV}$ or $-f_{DEV}$. It is also equal to half the frequency spacing between adjacent symbols.
[3] Calibration of the image rejection used an external RF source.
[4] For received signal levels < −100 dBm, it is recommended that the RSSI readback value be averaged over a number of samples to improve RSSI accuracy at low input power.
[5] Filtered conductive receive spurious emissions are measured on the EVAL-ADF7021-VDBxZ, which includes a T-stage harmonic filter (two inductors and one capacitor).

DIGITAL SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIMING INFORMATION					
Chip Enabled to Regulator Ready		50		µs	CREG[1:4] = 100 nF
Chip Enabled to Tx Mode					32-bit register write time = 50 µs
TCXO Reference		1		ms	Depends on VCO settling
XTAL		2		ms	Depends on VCO settling
Chip Enabled to Rx Mode					32-bit register write time = 50 µs, IF filter coarse calibration only
TCXO Reference		1.2		ms	Depends on VCO settling
XTAL		2.2		ms	Depends on VCO settling
Tx-to-Rx Turnaround Time		AGC settling + ($5 \times t_{BIT}$)		ms	Time to synchronized data output; includes AGC settling (three AGC levels) and CDR synchronization; t_{BIT} = data bit period; AFC settling not included
LOGIC INPUTS					
Input High Voltage, V_{INH}	$0.7 \times V_{DD}$			V	
Input Low Voltage, V_{INL}			$0.2 \times V_{DD}$	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
Control Clock Input			50	MHz	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	VDD2 − 0.4			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
CLKOUT Rise/Fall Time			5	ns	
CLKOUT Load			10	pF	

GENERAL SPECIFICATIONS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE RANGE (T_A)	−40		+85	°C	
POWER SUPPLIES					
Voltage Supply, V_{DD}	2.3		3.6	V	All VDDx pins must be tied together
TRANSMIT CURRENT CONSUMPTION[1, 2]					V_{DD} = 3.0 V, PA is matched into 50 Ω
868 MHz					
0 dBm		17.6		mA	
5 dBm		20.8		mA	
10 dBm		27.1		mA	
460 MHz					
0 dBm		13.8		mA	
5 dBm		17		mA	
10 dBm		23		mA	
RECEIVE CURRENT CONSUMPTION[2]					V_{DD} = 3.0 V
868 MHz					
Low Current Mode		19.3		mA	
High Sensitivity Mode		21.7		mA	
460 MHz					
Low Current Mode		16.3		mA	
High Sensitivity Mode		18.3		mA	
POWER-DOWN CURRENT CONSUMPTION[2]					
Low Power Sleep Mode		0.1	1	µA	CE low

[1] The transmit current consumption tests used the same combined PA and LNA matching network as that used on the EVAL-ADF7021-VDBxZ evaluation boards. Improved PA efficiency is achieved by using a separate PA matching network.
[2] Device current only. VCO and TCXO currents are excluded.

TIMING CHARACTERISTICS

V_{DD} = 3 V ± 10%, GND = 0 V, T_A = 25°C, unless otherwise noted. Guaranteed by design but not production tested.

Table 6.

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Description
t_1	>10	ns	SDATA to SCLK setup time
t_2	>10	ns	SDATA to SCLK hold time
t_3	>25	ns	SCLK high duration
t_4	>25	ns	SCLK low duration
t_5	>10	ns	SCLK to SLE setup time
t_6	>20	ns	SLE pulse width
t_8	<25	ns	SCLK to SREAD data valid, readback
t_9	<25	ns	SREAD hold time after SCLK, readback
t_{10}	>10	ns	SCLK to SLE disable time, readback
t_{11}	$5 < t_{11} < (¼ \times t_{BIT})$	ns	TxRxCLK negative edge to SLE
t_{12}	>5	ns	TxRxDATA to TxRxCLK setup time (Tx mode)
t_{13}	>5	ns	TxRxCLK to TxRxDATA hold time (Tx mode)
t_{14}	$5 < t_{14} < (¼ \times t_{BIT})$	µs	TxRxCLK negative edge to SLE
t_{15}	$>¼ \times t_{BIT}$	µs	SLE positive edge to positive edge of TxRxCLK (Rx mode)

TIMING DIAGRAMS

Serial Interface

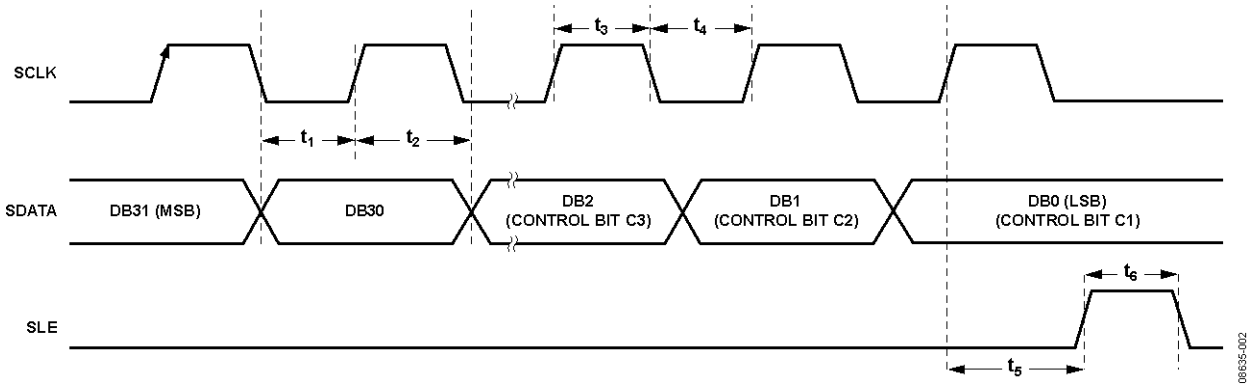

Figure 2. Serial Interface Timing Diagram

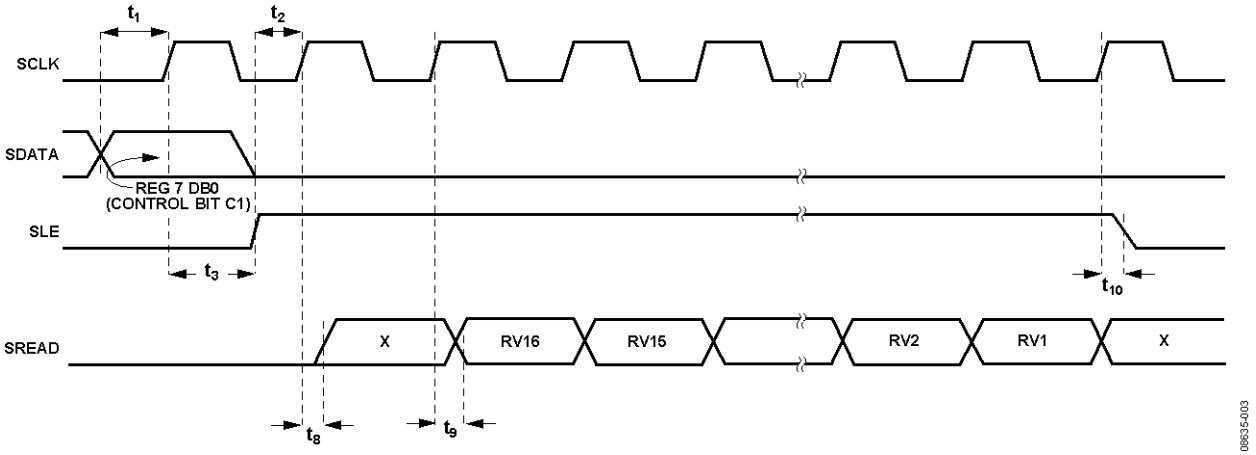

Figure 3. Serial Interface Readback Timing Diagram

2FSK/3FSK Timing

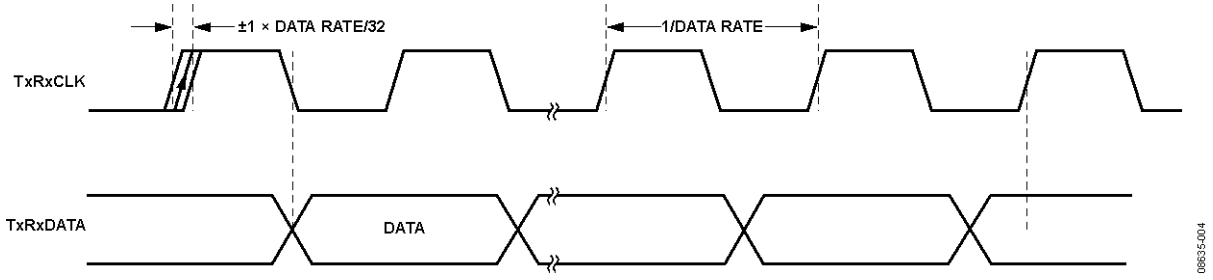

Figure 4. TxRxDATA/TxRxCLK Timing Diagram in Receive Mode

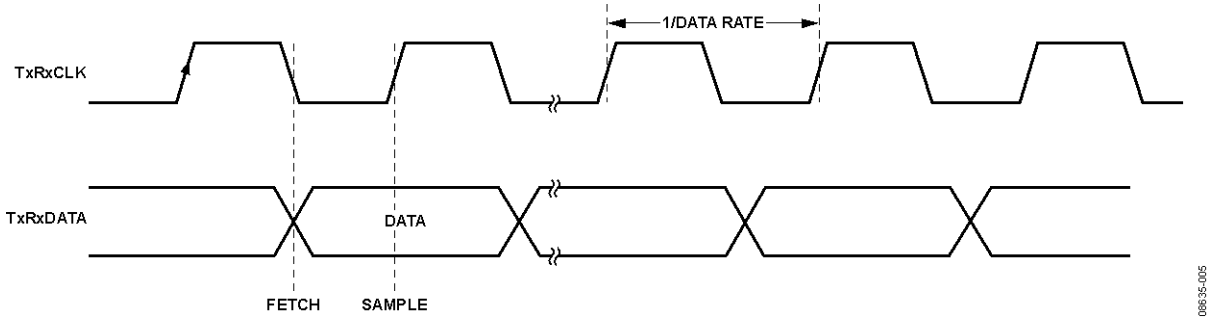

Figure 5. TxRxDATA/TxRxCLK Timing Diagram in Transmit Mode

4FSK Timing

In 4FSK receive mode, MSB/LSB synchronization is guaranteed by detection of the SWD pin in the receive bit stream.

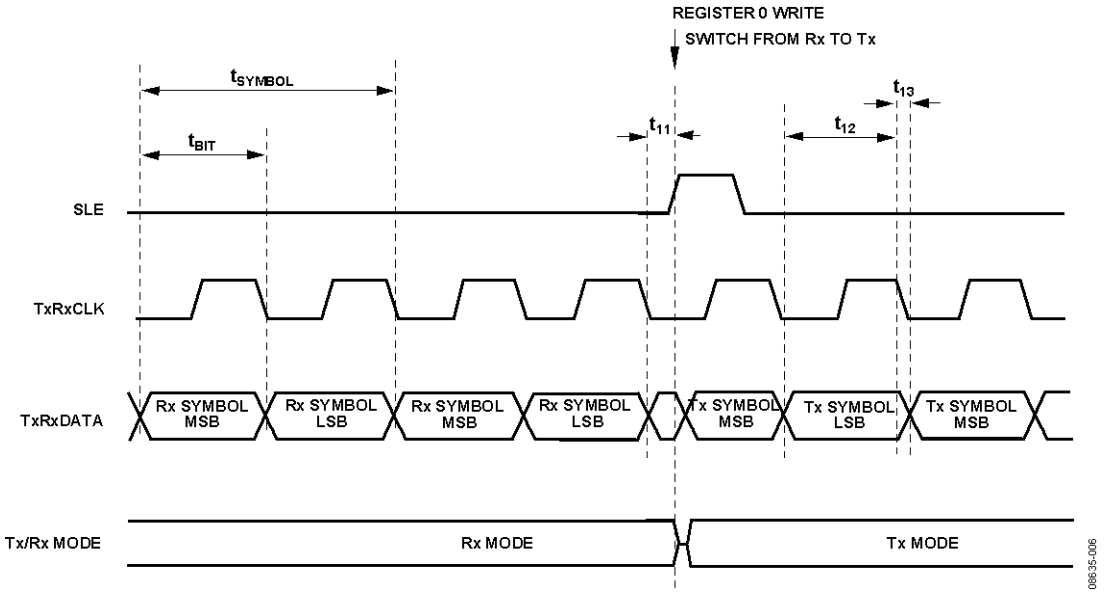

Figure 6. Receive-to-Transmit Timing Diagram in 4FSK Mode

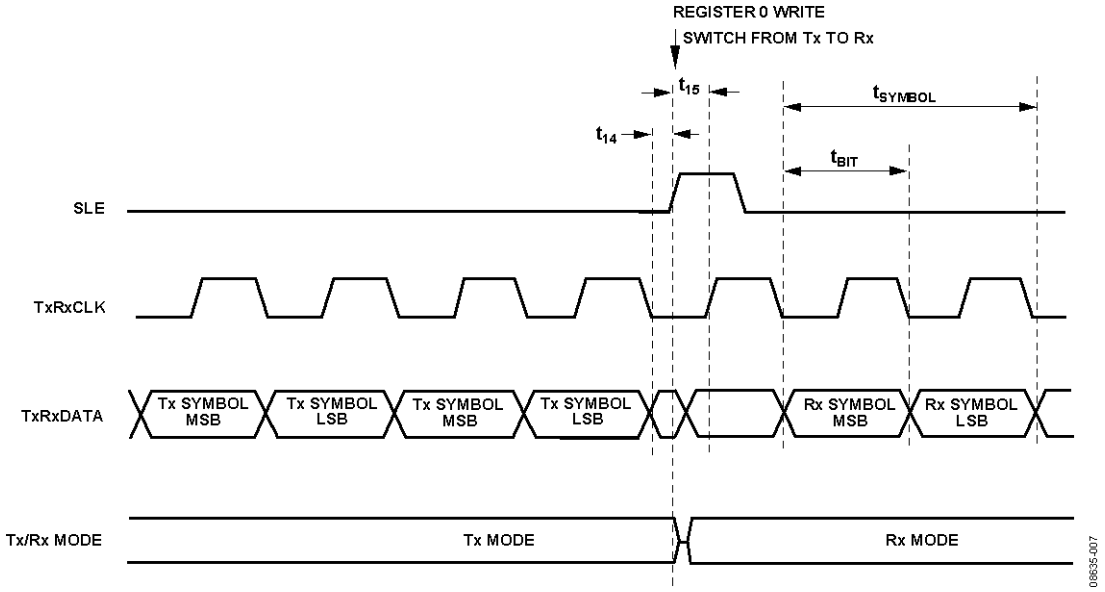

Figure 7. Transmit-to-Receive Timing Diagram in 4FSK Mode

UART/SPI Mode

UART mode is enabled by setting Register 0, Bit DB28 to 1. SPI mode is enabled by setting Register 0, Bit DB28 to 1 and setting Register 15, Bits[DB19:DB17] to 0x7. The transmit/receive data clock is available on the CLKOUT pin.

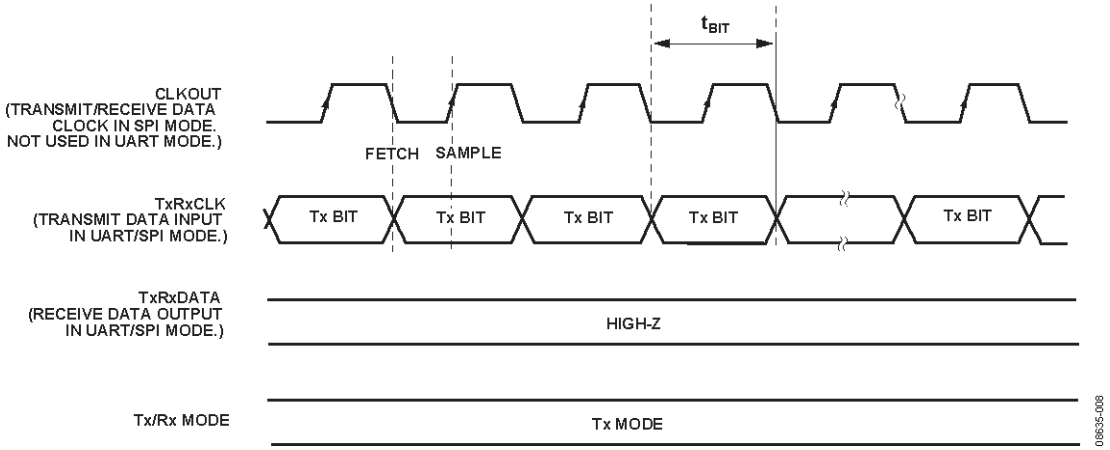

Figure 8. Transmit Timing Diagram in UART/SPI Mode

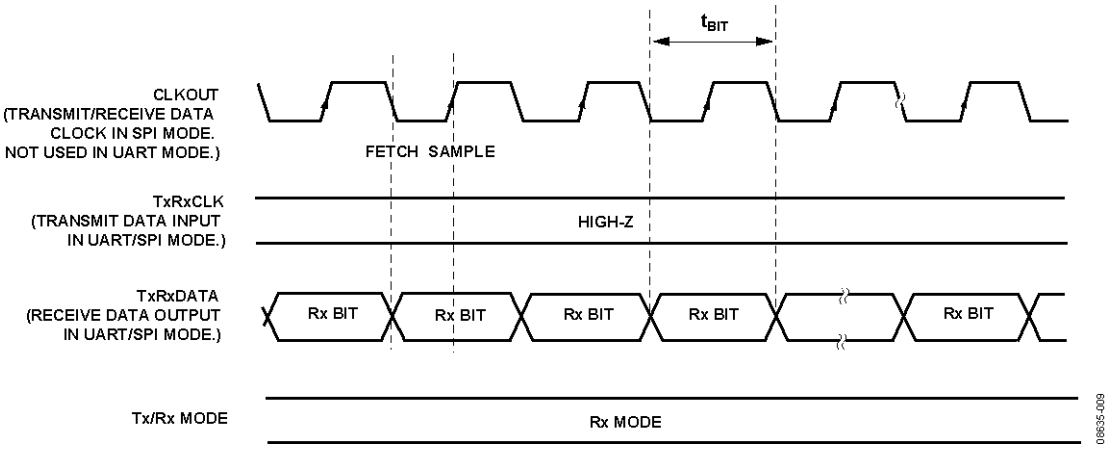

Figure 9. Receive Timing Diagram in UART/SPI Mode

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to GND[1]	−0.3 V to +5 V
Analog I/O Voltage to GND[1]	−0.3 V to VDDx + 0.3 V
Digital I/O Voltage to GND[1]	−0.3 V to VDDx + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
MLF θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

[1] GND = GND1 = GND2 = GND4 = RFGND = 0 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Take proper precautions for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

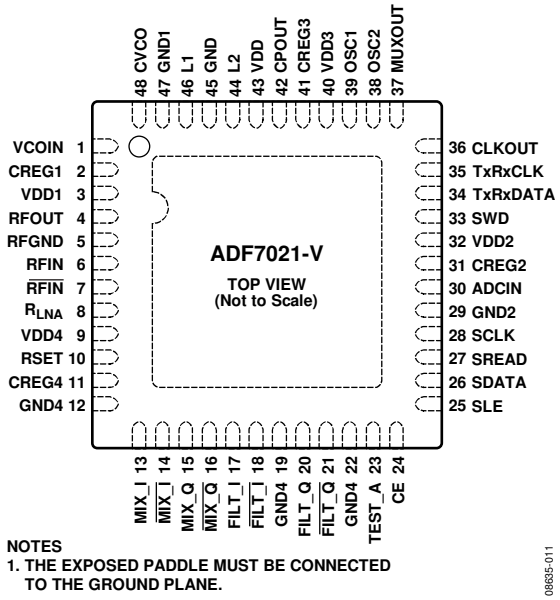

Figure 10. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCOIN	Do not connect.
2	CREG1	Regulator Voltage for PA Block. Place a series 3.9 Ω resistor and a 100 nF capacitor between this pin and ground for regulator stability and noise rejection.
3	VDD1	Voltage Supply for PA Block and VCO Cores. Place decoupling capacitors of 0.1 µF and 100 pF as close as possible to this pin. Tie all VDDx pins together.
4	RFOUT	The modulated signal is available at this pin. Output power levels are from −16 dBm to +13 dBm. Impedance match the output to the desired load using suitable components.
5	RFGND	Ground for Output Stage of Transmitter. Tie all GND pins together.
6	RFIN	LNA Input for Receiver Section. Input matching is required between the antenna and the differential LNA input to ensure maximum power transfer.
7	$\overline{\text{RFIN}}$	Complementary LNA Input.
8	R_{LNA}	External Bias Resistor for LNA. Optimum resistor is 1.1 kΩ with 5% tolerance.
9	VDD4	Voltage Supply for LNA/Mixer Block. Decouple this pin to ground with a 10 nF capacitor. Tie all VDDx pins together.
10	RSET	External Resistor. Sets charge pump current and some internal bias currents. Use a 3.6 kΩ resistor with 5% tolerance.
11	CREG4	Regulator Voltage for LNA/Mixer Block. Place a 100 nF capacitor between this pin and ground for regulator stability and noise rejection.
12, 19, 22	GND4	Ground for LNA/Mixer Block. Tie all GND pins together.
13 to 16	MIX_I, $\overline{\text{MIX\_I}}$, MIX_Q, $\overline{\text{MIX\_Q}}$	Signal Chain Test Pins. These pins are high impedance under normal conditions; leave the pins unconnected.
17, 18, 20, 21	FILT_I, $\overline{\text{FILT\_I}}$, FILT_Q, $\overline{\text{FILT\_Q}}$,	Signal Chain Test Pins. These pins are high impedance under normal conditions; leave the pins unconnected.
23	TEST_A	Signal Chain Test Pin. This pin is high impedance under normal conditions; leave the pins unconnected.
24	CE	Chip Enable. Bringing CE low puts the ADF7021-V into complete power-down. Register values are lost when CE is low, and the part must be reprogrammed after CE is brought high.
25	SLE	Load Enable, CMOS Input. When SLE goes high, the data stored in the shift registers is loaded into one of the 16 latches. A latch is selected using the control bits.
26	SDATA	Serial Data Input. The serial data is loaded MSB first with the four LSBs as the control bits. This pin is a high impedance CMOS input.

Pin No.	Mnemonic	Description
27	SREAD	Serial Data Output. This pin is used to feed readback data from the ADF7021-V to the microcontroller. The SCLK input is used to clock each readback bit (for example, AFC or ADC) from the SREAD pin.
28	SCLK	Serial Clock Input. The serial clock is used to clock in the serial data to the registers. The data is latched into the 32-bit shift register on the SCLK rising edge. This pin is a digital CMOS input.
29	GND2	Ground for Digital Block. Tie all GND pins together.
30	ADCIN	Analog-to-Digital Converter Input. The internal 7-bit ADC can be accessed through this pin. Full scale is 0 V to 1.9 V. Readback is through the SREAD pin.
31	CREG2	Regulator Voltage for Digital Block. Place a 100 nF capacitor between this pin and ground for regulator stability and noise rejection.
32	VDD2	Voltage Supply for Digital Block. Place a decoupling capacitor of 10 nF as close as possible to this pin. Tie all VDDx pins together.
33	SWD	Sync Word Detect. The ADF7021-V asserts this pin when it finds a match for the sync word sequence. This provides an interrupt for an external microcontroller, indicating that valid data is being received.
34	TxRxDATA	Transmit Data Input/Received Data Output. This is a digital pin, and normal CMOS levels apply. In UART/SPI receive mode, this pin provides an output for the received data. In UART/SPI transmit mode, this pin is high impedance.
35	TxRxCLK	Outputs the data clock in both receive and transmit modes. This is a digital pin, and normal CMOS levels apply. The positive clock edge is matched to the center of the received data. In standard transmit mode, this pin outputs an accurate clock to latch the data from the microcontroller into the transmit section at the exact required data rate. In UART/SPI transmit mode, this pin is used to input the transmit data. In UART/SPI receive mode, this pin is high impedance.
36	CLKOUT	Divided-Down Version of the Crystal Reference with Output Driver. The digital clock output can be used to drive several other CMOS inputs, such as a microcontroller clock. The output has a 50:50 mark/space ratio and is inverted with respect to the reference. Place a series 1 kΩ resistor as close as possible to the pin in applications where the CLKOUT feature is used.
37	MUXOUT	Provides the DIGITAL_LOCK_DETECT signal. This signal is used to determine whether the PLL is locked to the correct frequency. It also provides other signals such as REGULATOR_READY, which is an indicator of the status of the serial interface regulator.
38	OSC2	Connect the reference crystal between this pin and OSC1. A TCXO reference can be used by driving this pin with CMOS levels and disabling the internal crystal oscillator.
39	OSC1	Connect the reference crystal between this pin and OSC2. A TCXO reference can be used by driving this pin with ac-coupled 0.8 V p-p levels and by enabling the internal crystal oscillator.
40	VDD3	Voltage Supply for Charge Pump and PLL Dividers. Decouple this pin to ground with a 10 nF capacitor. Tie all VDDx pins together.
41	CREG3	Regulator Voltage for Charge Pump and PLL Dividers. Place a 100 nF capacitor between this pin and ground for regulator stability and noise rejection.
42	CPOUT	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
43	VDD	Voltage Supply for RF Circuitry. Place a decoupling capacitor of 10 nF as close as possible to this pin. Tie all VDDx pins together.
44	L2	VCO Buffer Input.
45	GND	Ground. Tie all GND pins together.
46	L1	Do not connect.
47	GND1	Ground. Tie all GND pins together.
48	CVCO	Do not connect.
EP	Exposed Paddle	The exposed paddle must be connected to the ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

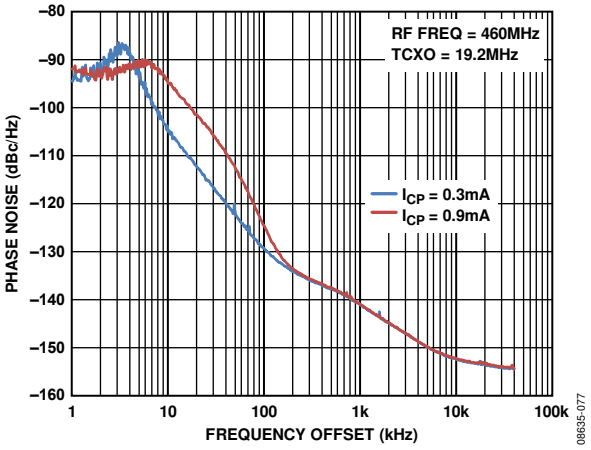

Figure 11. Phase Noise Response at 460 MHz, V_{DD} = 3 V

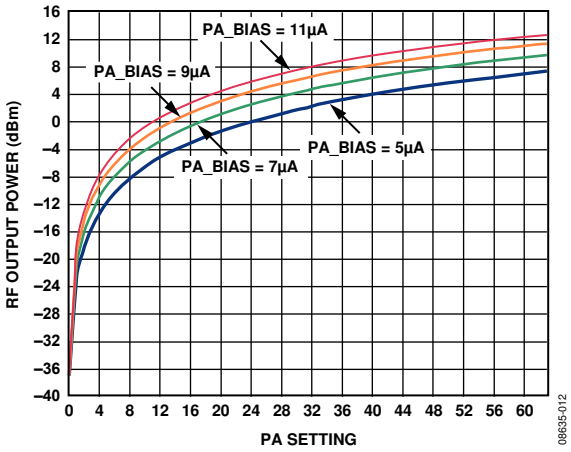

Figure 14. RF Output Power vs. PA Setting

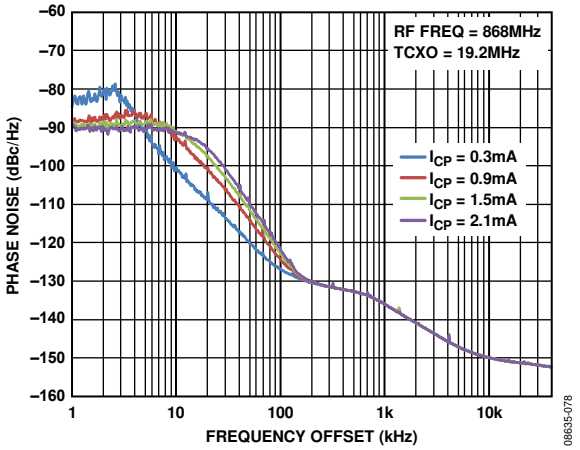

Figure 12. Phase Noise Response at 868 MHz, V_{DD} = 2.3 V

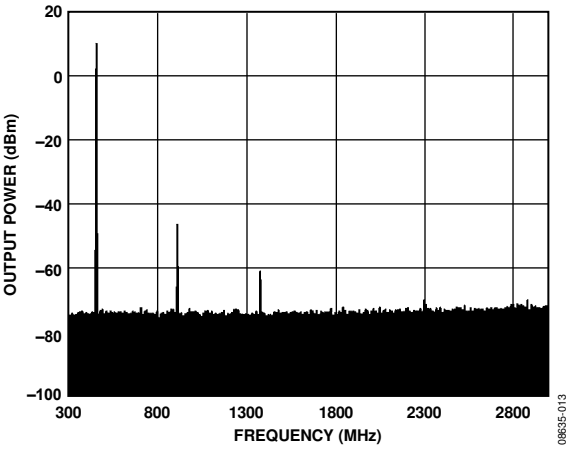

Figure 15. PA Output Harmonic Response with T-Stage LC Filter

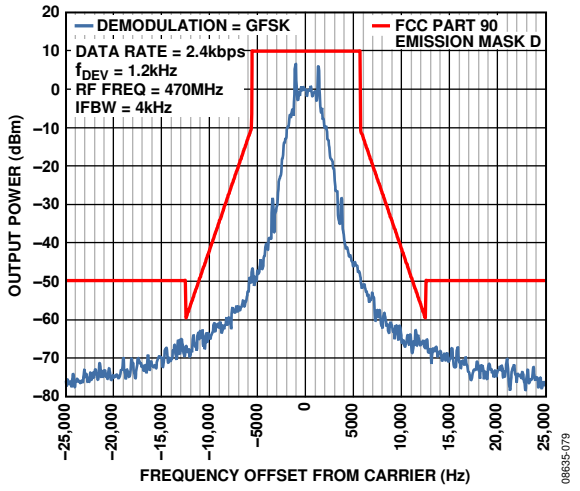

Figure 13. Output Spectrum in FCC Part 90 Emission Mask D and GFSK Modes

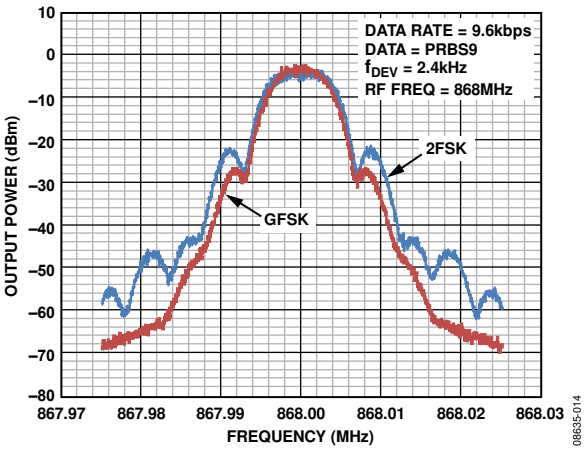

Figure 16. Output Spectrum in 2FSK and GFSK Modes

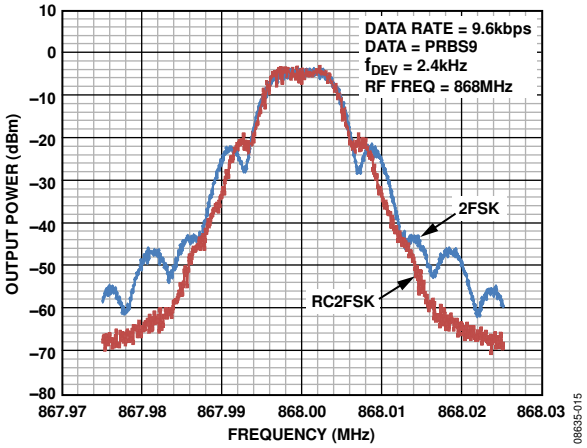

Figure 17. Output Spectrum in 2FSK and Raised Cosine 2FSK Modes

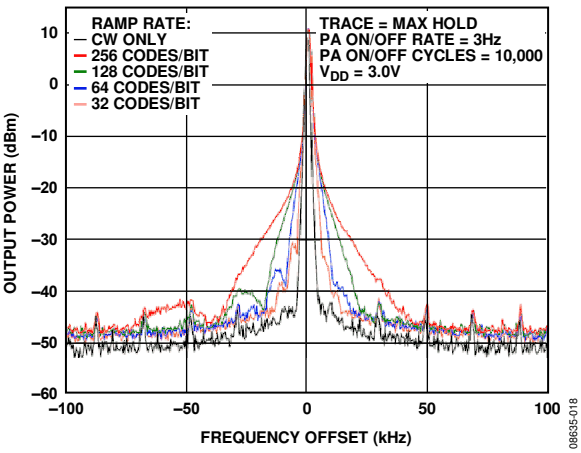

Figure 20. Output Spectrum in Maximum Hold for Various PA Ramp Rate Options

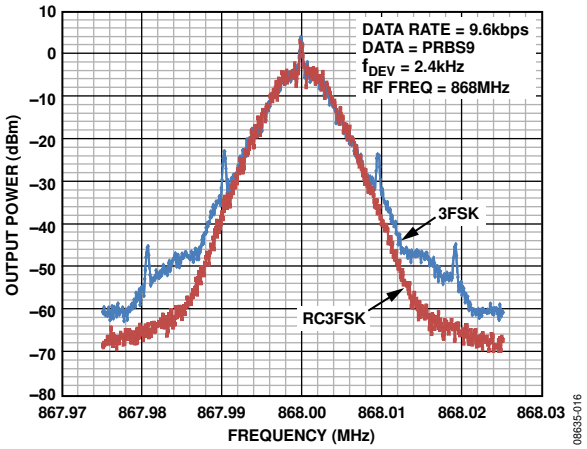

Figure 18. Output Spectrum in 3FSK and Raised Cosine 3FSK Modes

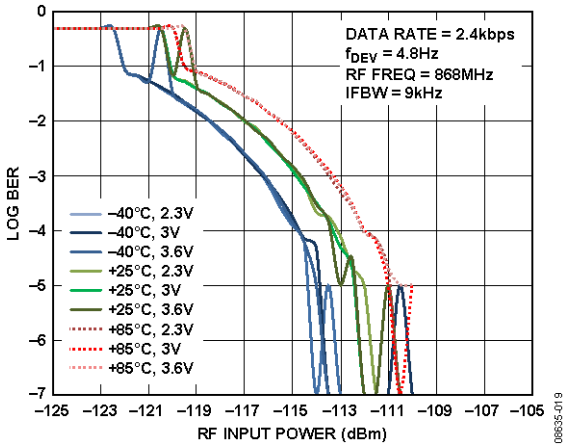

Figure 21. 2FSK Sensitivity vs. V_{DD} and Temperature at 868 MHz

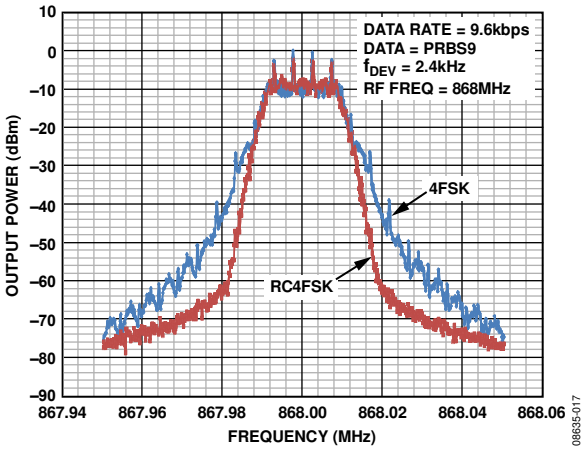

Figure 19. Output Spectrum in 4FSK and Raised Cosine 4FSK Modes

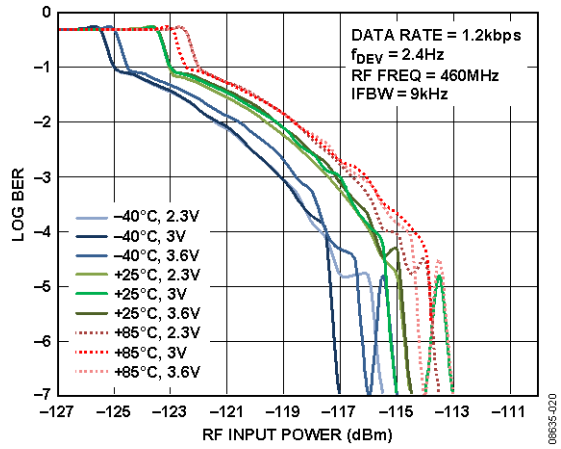

Figure 22. 2FSK Sensitivity vs. V_{DD} and Temperature at 460 MHz

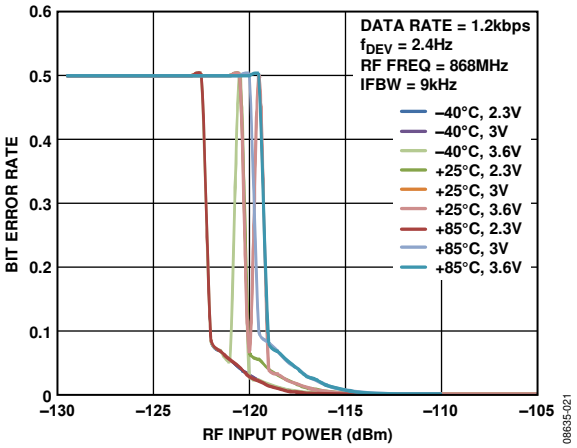

Figure 23. 2FSK Sensitivity vs. V_{DD} and Temperature at 868 MHz

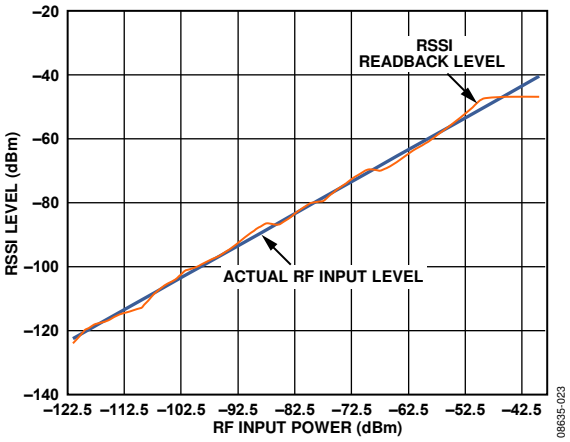

Figure 26. Digital RSSI Readback Linearity

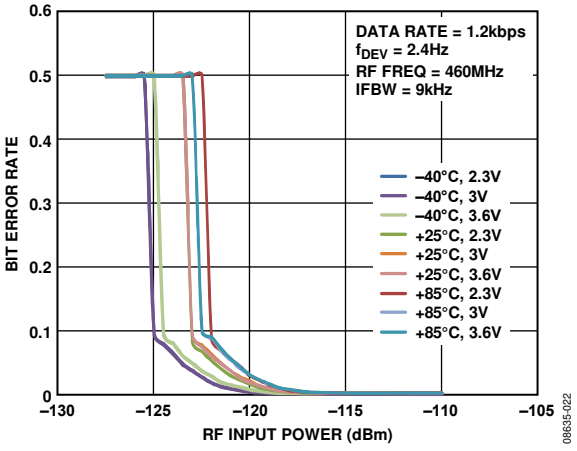

Figure 24. 2FSK Sensitivity vs. V_{DD} and Temperature at 460 MHz

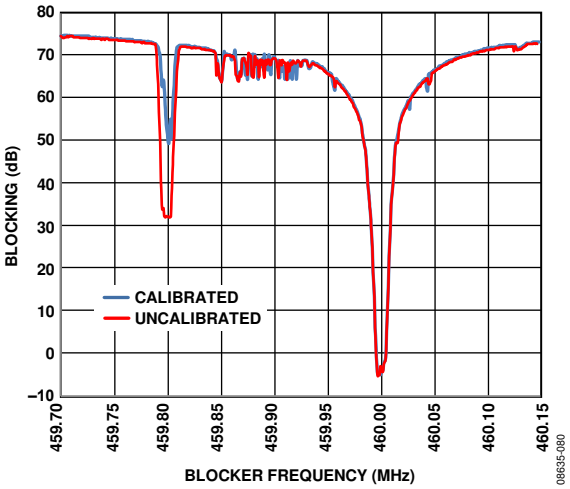

Figure 27. Image Rejection, Uncalibrated vs. Calibrated

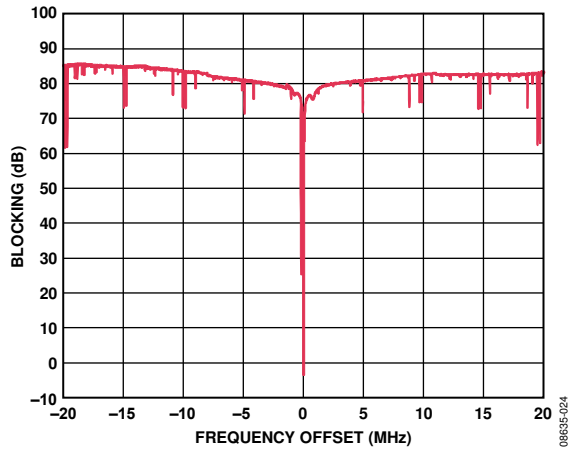

Figure 25. Wideband Interference Rejection (Modulated Carrier Is Swept 20 MHz Either Side of an 868 MHz Modulated GFSK 2.4 kHz/4.8 kbps Wanted Signal at the Sensitivity Point (−106.5 dBm); the Power Level of the Blocker Is Adjusted to Give a BER of 10^{-2}; Interferer Is a GFSK PRBS15 4.8 kHz/2.4 kHz Signal)

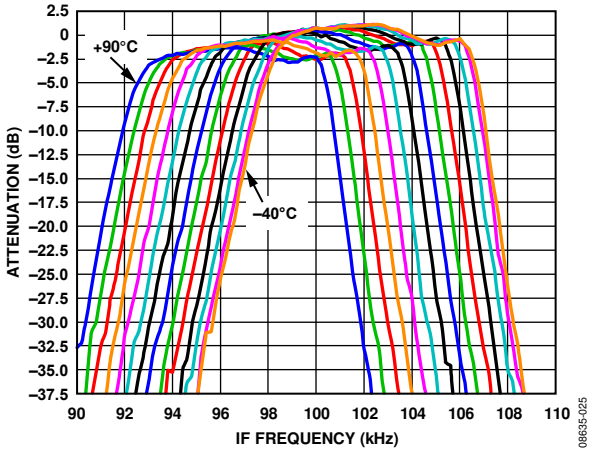

Figure 28. Variation of IF Filter Response with Temperature (IF_FILTER_BW = 9 kHz, Temperature Range Is −40°C to +90°C in 10° Steps)

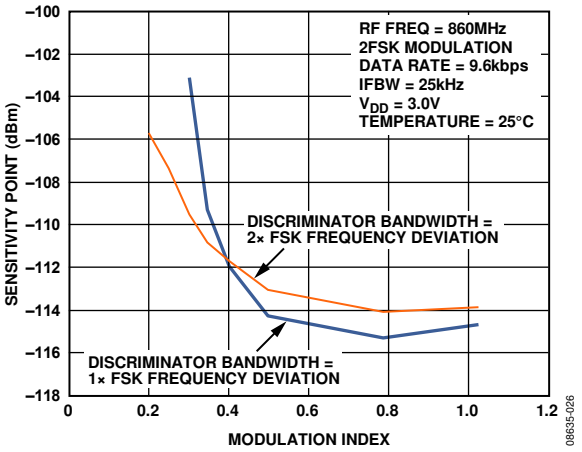

Figure 29. 2FSK Sensitivity vs. Modulation Index and Correlator Discriminator Bandwidth

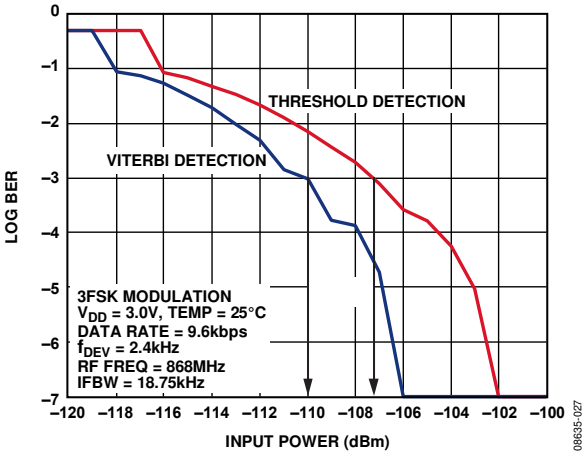

Figure 30. 3FSK Receiver Sensitivity Using Viterbi Detection and Threshold Detection

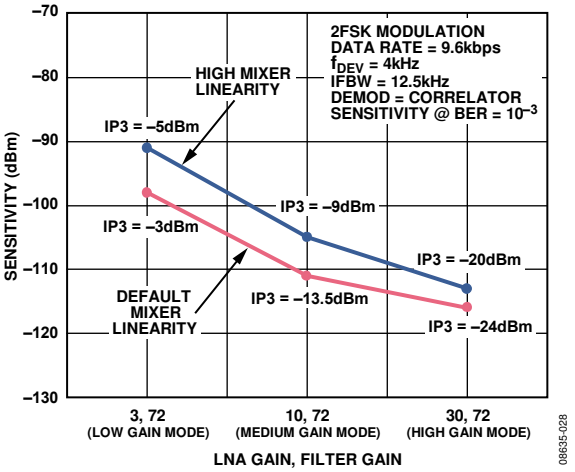

Figure 31. 2FSK Receiver Sensitivity vs. LNA Gain/IF Filter Gain and Mixer Linearity Settings (Input IP3 at Each Setting Also Shown)

FREQUENCY SYNTHESIZER

REFERENCE INPUT

The on-board crystal oscillator circuitry (see Figure 32) can use a quartz crystal as the PLL reference. A quartz crystal with a frequency tolerance of ≤10 ppm for narrow-band applications is recommended. It is possible to use a quartz crystal with >10 ppm tolerance, but compensation for the frequency error of the crystal is necessary to comply with the absolute frequency error specifications of narrow-band regulations (for example, ARIB STD-T67 and ETSI EN 300 220).

The oscillator circuit is enabled by setting Bit DB12 in Register 1 high. It is enabled by default on power-up and is disabled by bringing CE low. Errors in the crystal can be corrected using the automatic frequency control (AFC) feature or by adjusting the fractional-N value (see the N Counter section).

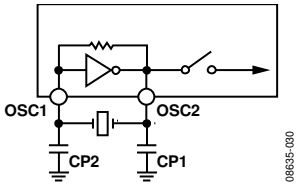

Figure 32. Crystal Oscillator Circuit on the ADF7021-V

Two parallel resonant capacitors are required for oscillation at the correct frequency. Their values are dependent on the crystal specification. Select the resonant capacitors to ensure that the series value of capacitance added to the PCB track capacitance adds up to the specified load capacitance of the crystal, usually 12 pF to 20 pF. Track capacitance values vary from 2 pF to 5 pF, depending on board layout. When possible, choose capacitors that have a very low temperature coefficient to ensure stable frequency operation over all conditions.

Using a TCXO Reference

A single-ended reference (TCXO, VCXO, or OCXO) can also be used with the ADF7021-V. This is recommended for applications that have absolute frequency accuracy requirements of <10 ppm, such as applications requiring compliance with ARIB STD-T67 or ETSI EN 300 220. The following are two options for interfacing the ADF7021-V to an external reference oscillator.

- An oscillator with CMOS output levels can be applied to OSC2. Disable the internal oscillator circuit by setting Bit DB12 in Register 1 low.
- An oscillator with 0.8 V p-p levels can be ac-coupled through a 22 pF capacitor into OSC1. Enable the internal oscillator circuit by setting Bit DB12 in Register 1 high.

Programmable Crystal Bias Current

Bias current in the oscillator circuit can be configured from 20 µA to 35 µA by writing to the XTAL_BIAS bits (Register 1, Bits[DB14:DB13]). Increasing the bias current allows the crystal oscillator to power up faster.

CLKOUT Divider and Buffer

The CLKOUT circuit takes the reference clock signal from the oscillator section, shown in Figure 32, and supplies a divided-down, 50:50 mark/space signal to the CLKOUT pin. The CLKOUT signal is inverted with respect to the reference clock. An even divide from 2 to 30 is available; this divide number is set in Register 1, Bits[DB10:DB7]. On power-up, the CLKOUT defaults to divide-by-8.

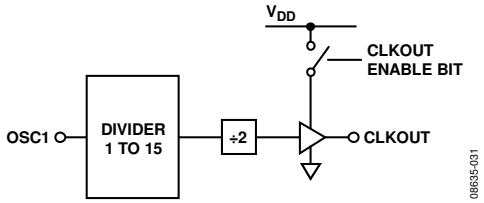

Figure 33. CLKOUT Stage

To disable CLKOUT, set the divide number to 0. The output buffer can drive a load of up to 20 pF with a 10% rise time at 4.8 MHz. Faster edges can result in some spurious feedthrough to the output. A series resistor (1 kΩ) can be used to slow the clock edges to reduce these spurs at the CLKOUT frequency.

R Counter

The 3-bit R counter divides the reference input frequency by an integer from 1 to 7. The divided-down signal is presented as the reference clock to the phase frequency detector (PFD). The divide ratio is set in Register 1, Bits[DB6:DB4]. Maximizing the PFD frequency reduces the N value. This reduces the noise multiplied at a rate of 20 log(N) to the output and reduces occurrences of spurious components.

Register 1 defaults to R = 1 on power-up.

$$PFD\ (\text{Hz}) = XTAL/R$$

Loop Filter

The loop filter integrates the current pulses from the charge pump to form a voltage that tunes the output of the VCO to the desired frequency. It also attenuates spurious levels generated by the PLL. A typical loop filter design is shown in Figure 34.

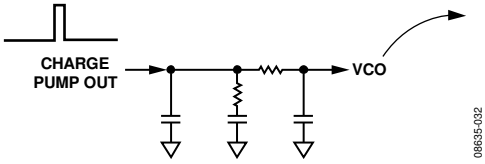

Figure 34. Typical Loop Filter Configuration

Design the loop so that the loop bandwidth (LBW) is approximately 6 kHz. This provides a good compromise between in-band phase noise and out-of-band spurious rejection. Widening the LBW excessively reduces the time spent jumping between frequencies, but it can cause insufficient spurious attenuation. Use the loop filter design on the EVAL-ADF7021-VDBxZ for optimum performance.

The free design tool ADIsimSRD™ Design Studio can also be used to design loop filters for the ADF7021-V. See the ADIsimSRD Design Studio website (www.analog.com/adisimsrd) for details).

N Counter

The feedback divider in the ADF7021-V PLL consists of an 8-bit integer counter (set using Register 0, Bits[DB26:DB19]) and a 15-bit, Σ-Δ fractional-N divider (set using Register 0, Bits[DB18:DB4]). The integer counter is the standard pulse-swallow type that is common in PLLs. It sets the minimum integer divide value to 23. The fractional divide value provides very fine resolution at the output, where the output frequency of the PLL is calculated as

$$f_{OUT} = \frac{XTAL}{R} \times \left(INTEGER\_N + \frac{FRACTIONAL\_N}{2^{15}} \right)$$

When RF_DIVIDE_BY_2 is enabled (see the Voltage Controlled Oscillator (VCO) section), this formula becomes

$$f_{OUT} = \frac{XTAL}{R} \times 0.5 \times \left(INTEGER\_N + \frac{FRACTIONAL\_N}{2^{15}} \right)$$

The combination of INTEGER_N (maximum = 255) and FRACTIONAL_N (maximum = 32,768/32,768) gives a maximum N divider of 255 + 1. Therefore, the minimum usable PFD is

$$PFD_{MIN}\ (\text{Hz}) = \frac{Maximum Required Output\ Frequency}{(255+1)}$$

For example, when operating in the European 868 MHz to 870 MHz band, PFD_{MIN} = 3.4 MHz.

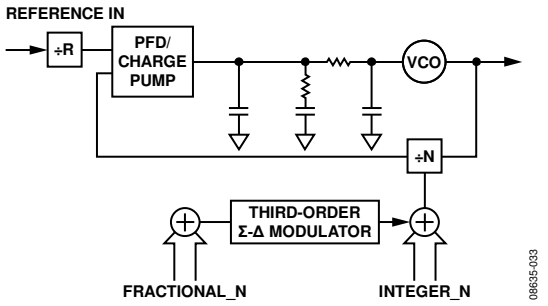

Figure 35. Fractional-N PLL

Voltage Regulators

The ADF7021-V contains four regulators to supply stable voltages to the part. The nominal regulator voltage is 2.3 V. Regulator 1 requires a 3.9 Ω resistor and a 100 nF capacitor in series between CREG1 and ground, whereas the other regulators require a 100 nF capacitor connected between CREGx and ground. When CE is high, the regulators and other associated circuitry are powered on, drawing a total supply current of 2 mA. Bringing the CE pin low disables the regulators, reduces the supply current to less than 1 µA, and erases all values held in the registers.

The serial interface operates from a regulator supply. Therefore, to write to the part, CE must be high and the regulator voltage must be stabilized. Regulator status (CREG4) can be monitored using the REGULATOR_READY signal from the MUXOUT pin.

MUXOUT

The MUXOUT pin allows access to various digital points in the ADF7021-V. The state of MUXOUT is controlled in Register 0, Bits[DB31:DB29].

REGULATOR_READY

REGULATOR_READY is the default setting on MUXOUT after the transceiver is powered up. The power-up time of the regulator is typically 50 µs. Because the serial interface is powered from the regulator, the regulator must be at its nominal voltage before the ADF7021-V can be programmed. The regulator status can be monitored at MUXOUT. When the regulator ready signal on MUXOUT is high, programming of the ADF7021-V can begin.

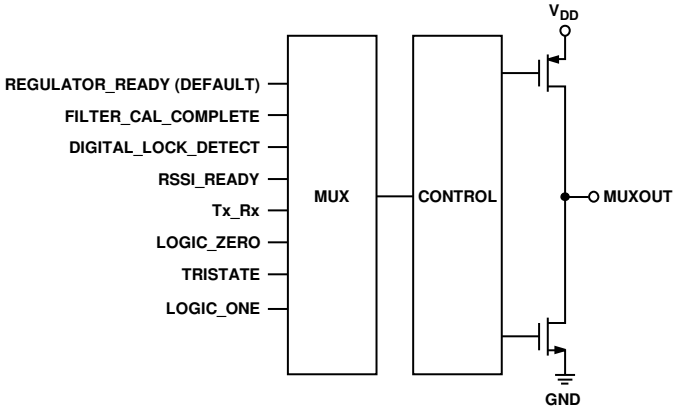

Figure 36. MUXOUT Circuit

FILTER_CAL_COMPLETE

MUXOUT can be set to FILTER_CAL_COMPLETE. This signal goes low for the duration of both a coarse IF filter calibration and a fine IF filter calibration. It can be used as an interrupt to a microcontroller to signal the end of the IF filter calibration.

DIGITAL_LOCK_DETECT

DIGITAL_LOCK_DETECT indicates when the PLL has locked. The lock detect circuit is located at the PFD. When the phase error on five consecutive cycles is less than 15 ns, lock detect is set high. Lock detect remains high until a 25 ns phase error is detected at the PFD.

RSSI_READY

MUXOUT can be set to RSSI_READY. This indicates that the internal analog RSSI has settled and that a digital RSSI readback can be performed.

Tx_Rx

Tx_Rx signifies whether the ADF7021-V is in transmit or receive mode. When in transmit mode, this signal is low. When in receive mode, this signal is high. It can be used to control an external Tx/Rx switch.

VOLTAGE CONTROLLED OSCILLATOR (VCO)

To minimize feedthrough and spurious emissions, the external VCO must be chosen to operate at a minimum of twice the required RF frequency. The VCO frequency is divided by 2 inside the synthesizer loop, providing the required frequency for the transmitter and for the local oscillator (LO) of the receiver. For improved phase noise performance, an additional divide-by-2 can be enabled by setting the RF_DIVIDE_BY_2 bit (Bit DB18) in Register 1.

As an example, for 80 MHz operation, a 160 MHz external VCO could be used with the RF_DIVIDE_BY_2 bit disabled, or a 320 MHz VCO could be used with the RF_DIVIDE_BY_2 bit enabled to support operation in the 80 MHz band. Assuming that both VCOs have similar phase noise performance, the 320 MHz design using the additional divide-by-2 results in improved transmit ACP, as well as improved ACR, blocking, and image rejection in the receiver.

The maximum VCO frequency of operation supported on the ADF7021-V is 1920 MHz, which results in a maximum RF channel frequency of 960 MHz using a 2× VCO or 480 MHz using a 4× VCO.

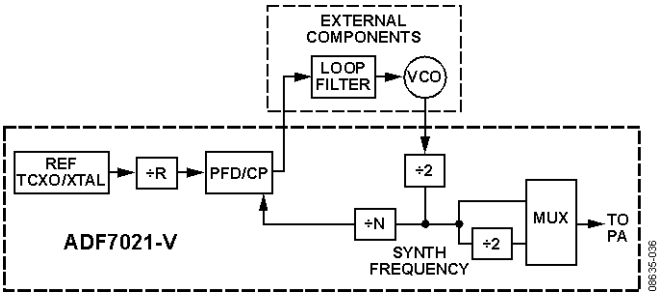

Figure 37. Voltage Controlled Oscillator (VCO)

The VCO tuning voltage can be checked for a particular RF output frequency by measuring the voltage on the CPOUT pin when the part is fully powered up in transmit or receive mode. The VCO tuning range of the external VCO must be 0.2 V to 2 V.

The input impedance of the L2 pin is programmable and can be selected to have a high impedance value or 50 Ω impedance, depending on the VCO selected. The impedance of this pin can be set using the BUFFER_IMPEDANCE bit (Bit DB17) in Register 1.

CHOOSING A VCO FOR BEST SYSTEM PERFORMANCE

The interaction between the RF VCO frequency and the reference frequency can lead to fractional spur creation. When the synthesizer is in fractional mode (that is, the RF VCO and reference frequencies are not integer related), spurs can appear on the VCO output spectrum at an offset frequency that corresponds to the difference frequency between an integer multiple of the reference and the VCO frequency.

These spurs are attenuated by the loop filter. They are more noticeable on channels close to integer multiples of the reference where the difference frequency may be inside the loop bandwidth (thus, the name integer boundary spurs). The occurrence of these spurs is rare because the integer frequencies are around multiples of the reference, which is typically >10 MHz. To avoid having very small or very large values in the fractional register, choose a suitable reference frequency.

In addition to spurious considerations, the selection of a high performance VCO with very low phase noise is essential to minimize the ACP performance of the transmitter and to maximize the ACR and blocking resilience of the receiver.