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High Performance Narrow-Band Transceiver IC

Data Sheet

ADF7021

FEATURES

- Low power, narrow-band transceiver
- Frequency bands using dual VCO
  - 80 MHz to 650 MHz
  - 862 MHz to 950 MHz
- Modulation schemes
  - 2FSK, 3FSK, 4FSK, MSK
- Spectral shaping
  - Gaussian and raised cosine filtering
- Data rates supported
  - 0.05 kbps to 32.8 kbps
- 2.3 V to 3.6 V power supply
- Programmable output power
  - −16 dBm to +13 dBm in 63 steps
- Automatic PA ramp control
- Receiver sensitivity
  - −130 dBm at 100 bps, 2FSK
  - −122 dBm at 1 kbps, 2FSK
  - −113 dBm at 25 kbps, raised cosine 2FSK
- Patent pending, on-chip image rejection calibration
- On-chip VCO and fractional-N PLL
- On-chip, 7-bit ADC and temperature sensor
- Fully automatic frequency control loop (AFC)
- Digital received signal strength indication (RSSI)
- Integrated Tx/Rx switch
- 0.1 µA leakage current in power-down mode

APPLICATIONS

- Narrow-band standards
  - ETSI EN 300 220, FCC Part 15, FCC Part 90, FCC Part 95, ARIB STD-T67
- Low cost, wireless data transfer
- Remote control/security systems
- Wireless metering
- Private mobile radio
- Wireless medical telemetry service (WMTS)
- Keyless entry
- Home automation
- Process and building control
- Pagers

FUNCTIONAL BLOCK DIAGRAM

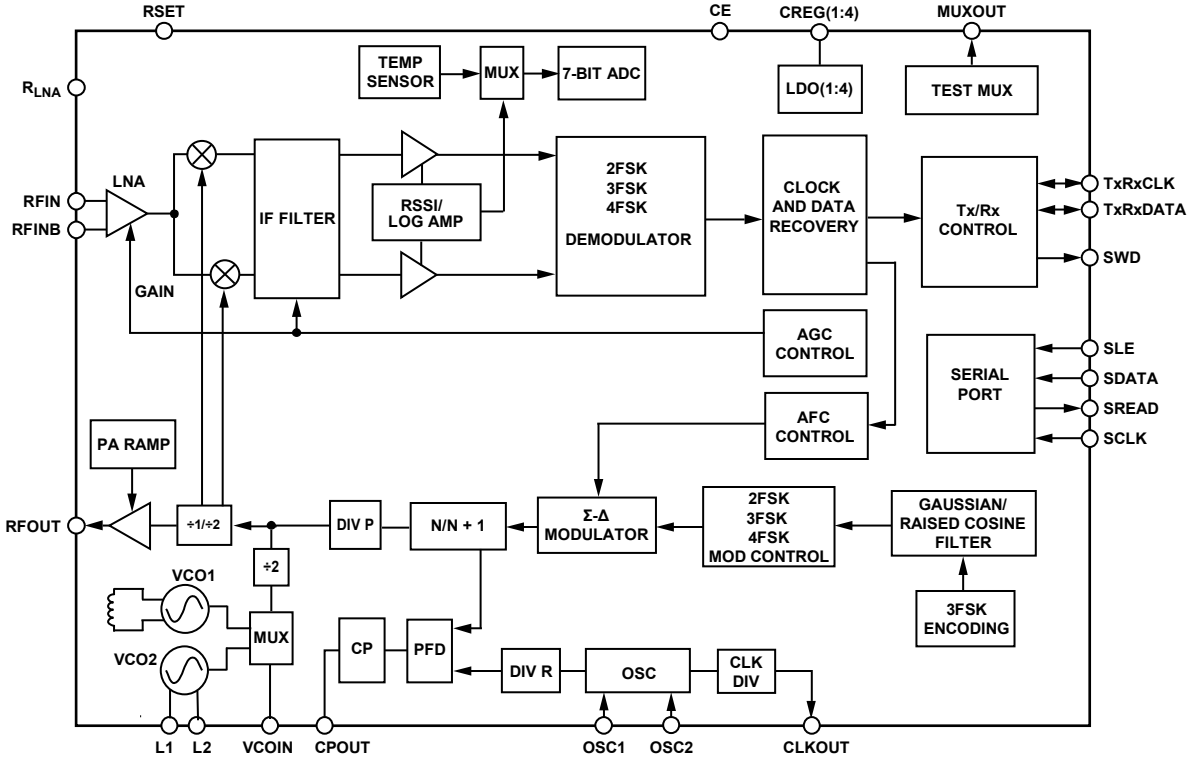

Figure 1.

Rev. D Document Feedback

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADF7021 Evaluation Boards

DOCUMENTATION

Application Notes

- AN-0987: Designing a Wireless Transceiver System to Meet the Wireless M-Bus Standard
- AN-1182: Understanding and Optimizing the AFC Loop on the ADF7021 for Minimum Preamble
- AN-1258: Image Rejection Calibration on the ADF7021, ADF7021-N, and ADF7021-V
- AN-1285: ADF7021-N Radio Performance for Wireless Meter-Bus (WM-Bus), Mode N
- AN-1389: Recommended Rework Procedure for the Lead Frame Chip Scale Package (LFCSP)
- AN-771: ADSP-BF533 EZ-KIT Lite and ADF70xx Interface
- AN-772: A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)
- AN-852: Using the Test DAC on the ADF702x to Implement Functions Such as Analog FM DEMOD, SNR Measurement, FEC Decoding, and PSK/4FSK Demodulation
- AN-859: RF Port Impedance Data, Matching, and External Component Selection for the ADF7020-1, ADF7021, and ADF7021-N
- AN-915: CDR Operation for ADF7020, ADF7020-1, ADF7021, and ADF7025

Data Sheet

- ADF7021: High Performance Narrow-Band Transceiver IC Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADF70xx Evaluation Software
- ADIismLINK Development Platform

TOOLS AND SIMULATIONS

- ADIsimSRD Design Studio

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Solutions Bulletins & Brochures

- Emerging Energy Applications Solutions Bulletin, Volume 10, Issue 4

Technical Articles

- Innovative Line Sensor Design with ADI Energy Harvesting and Low Power Signal Chain
- Low Power, Low Cost, Wireless ECG Holter Monitor
- RF Meets Power Lines: Designing Intelligent Smart Grid Systems that Promote Energy Efficiency
- Smart Metering Technology Promotes Energy Efficiency for a Greener World
- The Next Generation of Line Sensors: Power Harvested, Connected, and Lower Maintenance
- The Use of Short Range Wireless in a Multi-Metering System
- Understand Wireless Short-Range Devices for Global License-Free Systems
- Wireless Short Range Devices and Narrowband Communications
- Wireless Technologies for Smart Meters: Focus on Water Metering

DESIGN RESOURCES

- ADF7021 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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3/2007—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADF7021 is a high performance, low power, highly integrated 2FSK/3FSK/4FSK transceiver. It is designed to operate in the narrowband, license-free ISM bands, and in the licensed bands with frequency ranges of 80 MHz to 650 MHz and 862 MHz to 950 MHz. The device has both Gaussian and raised cosine transmit data filtering options to improve spectral efficiency for narrowband applications. It is suitable for circuit applications targeted at European ETSI EN 300 220, the Japanese ARIB STD-T67, the Chinese short range device regulations, and the North American FCC Part 15, Part 90, and Part 95 regulatory standards. A complete transceiver can be built using a small number of external discrete components, making the ADF7021 very suitable for price sensitive and area sensitive applications.

The range of on-chip FSK modulation and data filtering options allows users greater flexibility in their choice of modulation schemes while meeting tight spectral efficiency requirements. The ADF7021 also supports protocols that dynamically switch between 2FSK/3FSK/4FSK to maximize communication range and data throughput.

The transmit section contains dual voltage controlled oscillators (VCOs) and a low noise fractional-N PLL with an output resolution of <1 ppm. The ADF7021 has a VCO using an internal LC tank (431 MHz to 475 MHz, 862 MHz to 950 MHz) and a VCO using an external inductor as part of its tank circuit (80 MHz to 650 MHz). The dual VCO design allows dual-band operation where the user can transmit and/or receive at any frequency supported by the internal inductor VCO and can also transmit and/or receive at a particular frequency band supported by the external inductor VCO.

The frequency agile PLL allows the ADF7021 to be used in frequency hopping spread spectrum (FHSS) systems. Both VCOs operate at twice the fundamental frequency to reduce spurious emissions and frequency pulling problems.

The transmitter output power is programmable in 63 steps from −16 dBm to +13 dBm, and has an automatic power ramp control to prevent spectral splatter and help meet regulatory standards. The transceiver RF frequency and modulation are programmable using a simple 3-wire interface. The device operates with a power supply range of 2.3 V to 3.6 V and can be powered down when not in use.

A low IF architecture is used in the receiver (100 kHz), which minimizes power consumption and the external component count, yet avoids dc offset and flicker noise at low frequencies. The IF filter has programmable bandwidths of 12.5 kHz, 18.75 kHz, and 25 kHz. The ADF7021 supports a wide variety of programmable features including Rx linearity, sensitivity, and IF bandwidth, allowing the user to trade off receiver sensitivity and selectivity against current consumption, depending on the application. The receiver also features a patent-pending automatic frequency control (AFC) loop with programmable pull-in range that allows the PLL to track out the frequency error in the incoming signal.

The receiver achieves an image rejection performance of 56 dB using a patent-pending IR calibration scheme that does not require the use of an external RF source.

An on-chip ADC provides readback of the integrated temperature sensor, external analog input, battery voltage, and RSSI signal, which provides savings on an ADC in some applications. The temperature sensor is accurate to ±10°C over the full operating temperature range of −40°C to +85°C. This accuracy can be improved by performing a 1-point calibration at room temperature and storing the result in memory.

SPECIFICATIONS

V_{DD} = 2.3 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C. All measurements are performed with the EVAL-ADF7021DB evaluation boards using the PN9 data sequence, unless otherwise noted.

RF AND PLL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF CHARACTERISTICS					See Table 9 for required VCO_BIAS and VCO_ADJUST settings
Frequency Ranges (Direct Output)	160		650	MHz	External inductor VCO
	862		950	MHz	Internal inductor VCO
Frequency Ranges (RF Divide-by-2 Mode)	80		325	MHz	External inductor VCO, RF divide-by-2 enabled
	431		475	MHz	Internal inductor VCO, RF divide-by-2 enabled
Phase Frequency Detector (PFD) Frequency[1]	RF/256		26/30	MHz	Crystal reference/external reference
PHASE-LOCKED LOOP (PLL)					
VCO Gain[2]					
868 MHz, Internal Inductor VCO		58		MHz/V	VCO_ADJUST = 0, VCO_BIAS = 8
434 MHz, Internal Inductor VCO		29		MHz/V	VCO_ADJUST = 0, VCO_BIAS = 8
426 MHz, External Inductor VCO		27		MHz/V	VCO_ADJUST = 0, VCO_BIAS = 3
160 MHz, External Inductor VCO		6		MHz/V	VCO_ADJUST = 0, VCO_BIAS = 2
Phase Noise (In-Band)					
868 MHz, Internal Inductor VCO		−97		dBc/Hz	10 kHz offset, PA = 10 dBm, V_{DD} = 3.0 V, PFD = 19.68 MHz, VCO_BIAS = 8
433 MHz, Internal Inductor VCO		−103		dBc/Hz	10 kHz offset, PA = 10 dBm, V_{DD} = 3.0 V, PFD = 19.68 MHz, VCO_BIAS = 8
426 MHz, External Inductor VCO		−95		dBc/Hz	10 kHz offset, PA = 10 dBm, V_{DD} = 3.0 V, PFD = 9.84 MHz, VCO_BIAS = 3
Phase Noise (Out-of-Band)		−124		dBc/Hz	1 MHz offset, f_{RF} = 433 MHz, PA = 10 dBm, V_{DD} = 3.0 V, PFD = 19.68 MHz, VCO_BIAS = 8
Normalized In-Band Phase Noise Floor[3]		−203		dBc/Hz	
PLL Settling		40		µs	Measured for a 10 MHz frequency step to within 5 ppm accuracy, PFD = 19.68 MHz, loop bandwidth (LBW) = 100 kHz
REFERENCE INPUT					
Crystal Reference[4]	3.625		26	MHz	
External Oscillator[4, 5]	3.625		30	MHz	
Crystal Start-Up Time[6]					
XTAL Bias = 20 µA		0.930		ms	10 MHz XTAL, 33 pF load capacitors, V_{DD} = 3.0 V
XTAL Bias = 35 µA		0.438		ms	10 MHz XTAL, 33 pF load capacitors, V_{DD} = 3.0 V
Input Level for External Oscillator[7]					
OSC1		0.8		V p-p	Clipped sine wave
OSC2		CMOS levels		V	
ADC PARAMETERS					
INL		±0.4		LSB	V_{DD} = 2.3 V to 3.6 V, T_A = 25°C
DNL		±0.4		LSB	V_{DD} = 2.3 V to 3.6 V, T_A = 25°C

[1] The maximum usable PFD at a particular RF frequency is limited by the minimum N divide value.
[2] VCO gain measured at a VCO tuning voltage of 1 V. The VCO gain varies across the tuning range of the VCO. The software package ADIsimPLL™ can be used to model this variation.
[3] This value can be used to calculate the in-band phase noise for any operating frequency. Use the following equation to calculate the in-band phase noise performance as seen at the PA output: −203 + 10 log(f_{PFD}) + 20 logN.
[4] Guaranteed by design. Sample tested to ensure compliance.
[5] A TCXO, VCXO, or OCXO can be used as an external oscillator.
[6] Crystal start-up time is the time from chip enable (CE) being asserted to correct clock frequency on the CLKOUT pin.
[7] Refer to the Reference Input section for details on using an external oscillator.

TRANSMISSION SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DATA RATE					
2FSK, 3FSK	0.05		25[1]	kbps	IF_BW = 25 kHz
4FSK	0.05		32.8[2]	kbps	IF_BW = 25 kHz
MODULATION					
Frequency Deviation (f_{DEV})[3]	0.056		28.26	kHz	PFD = 3.625 MHz
	0.306		156	kHz	PFD = 20 MHz
Deviation Frequency Resolution	56			Hz	PFD = 3.625 MHz
Gaussian Filter BT		0.5			
Raised Cosine Filter Alpha		0.5/0.7			Programmable
TRANSMIT POWER					
Maximum Transmit Power[4]		+13		dBm	V_{DD} = 3.0 V, T_A = 25°C
Transmit Power Variation vs. Temperature		±1		dB	−40°C to +85°C
Transmit Power Variation vs. V_{DD}		±1		dB	2.3 V to 3.6 V at 915 MHz, T_A = 25°C
Transmit Power Flatness		±1		dB	902 MHz to 928 MHz, 3 V, T_A = 25°C
Programmable Step Size		0.3125		dB	−20 dBm to +13 dBm
ADJACENT CHANNEL POWER (ACP)					
426 MHz, External Inductor VCO					PFD = 9.84 MHz
12.5 kHz Channel Spacing		−50		dBc	Gaussian 2FSK modulation, measured in a ±4.25 kHz bandwidth at ±12.5 kHz offset, 2.4 kbps PN9 data, 1.2 kHz frequency deviation, compliant with ARIB STD-T67
25 kHz Channel Spacing		−50		dBc	Gaussian 2FSK modulation, measured in a ±8 kHz bandwidth at ±25 kHz offset, 9.6 kbps PN9 data, 2.4 kHz frequency deviation, compliant with ARIB STD-T67
868 MHz, Internal Inductor VCO					PFD = 19.68 MHz
12.5 kHz Channel Spacing		−46		dBm	Gaussian 2FSK modulation, 10 dBm output power, measured in a ±6.25 kHz bandwidth at ±12.5 kHz offset, 2.4 kbps PN9 data, 1.2 kHz frequency deviation, compliant with ETSI EN 300-220
25 kHz Channel Spacing		−43		dBm	Gaussian 2FSK modulation, 10 dBm output power, measured in a ±12.5 kHz bandwidth at ±25 kHz offset, 9.6 kbps PN9 data, 2.4 kHz frequency deviation, compliant with ETSI EN 300-220
433 MHz, Internal Inductor VCO					PFD = 19.68 MHz
12.5 kHz Channel Spacing		−50		dBm	Gaussian 2FSK modulation, 10 dBm output power, measured in a ±6.25 kHz bandwidth at ±12.5 kHz offset, 2.4 kbps PN9 data, 1.2 kHz frequency deviation, compliant with ETSI EN 300-220
25 kHz Channel Spacing		−47		dBm	Gaussian 2FSK modulation, 10 dBm output power, measured in a ±12.5 kHz bandwidth at ±25 kHz offset, 9.6 kbps PN9 data, 2.4 kHz frequency deviation, compliant with ETSI EN 300-220
OCCUPIED BANDWIDTH					99.0% of total mean power; 12.5 kHz channel spacing (2.4 kbps PN9 data, 1.2 kHz frequency deviation); 25 kHz channel spacing (9.6 kbps PN9 data, 2.4 kHz frequency deviation)
2FSK Gaussian Data Filtering					
12.5 kHz Channel Spacing		3.9		kHz	
25 kHz Channel Spacing		9.9		kHz	
2FSK Raised Cosine Data Filtering					
12.5 kHz Channel Spacing		4.4		kHz	
25 kHz Channel Spacing		10.2		kHz	
3FSK Raised Cosine Filtering					
12.5 kHz Channel Spacing		3.9		kHz	
25 kHz Channel Spacing		9.5		kHz	
4FSK Raised Cosine Filtering					19.2 kbps PN9 data, 1.2 kHz frequency deviation
25 kHz Channel Spacing		13.2		kHz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPURIOUS EMISSIONS					
Reference Spurs		−65		dBc	100 kHz loop bandwidth
HARMONICS[5]					13 dBm output power, unfiltered conductive/filtered conductive
Second Harmonic		−35/−52		dBc	
Third Harmonic		−43/−60		dBc	
All Other Harmonics		−36/−65		dBc	
OPTIMUM PA LOAD IMPEDANCE[6]					
f_{RF} = 915 MHz		39 + j61		Ω	
f_{RF} = 868 MHz		48 + j54		Ω	
f_{RF} = 450 MHz		98 + j65		Ω	
f_{RF} = 426 MHz		100 + j65		Ω	
f_{RF} = 315 MHz		129 + j63		Ω	
f_{RF} = 175 MHz		173 + j49		Ω	

[1] Using Gaussian or raised cosine filtering. Choose the frequency deviation to ensure that the transmit occupied signal bandwidth is within the receiver IF filter bandwidth.
[2] Using raised cosine filtering with an alpha = 0.7. The inner frequency deviation = 1.78 kHz, and the POST_DEMOD_BW = 24.6 kHz.
[3] For the definition of frequency deviation, refer to the Register 2—Transmit Modulation Register section.
[4] Measured as maximum unmodulated power.
[5] Conductive filtered harmonic emissions measured on the EVAL-ADF7021DB models, which includes a T-stage harmonic filter (two inductors and one capacitor).
[6] For matching details, refer to the LNA/PA Matching section.

RECEIVER SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SENSITIVITY					Bit error rate (BER) = 10^{-3}, low noise amplifier (LNA) and power amplifier (PA) matched separately
2FSK					
Sensitivity at 0.1 kbps		−130		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 0.25 kbps		−127		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 1 kbps		−122		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 9.6 kbps		−115		dBm	f_{DEV} = 4 kHz, high sensitivity mode, IF_BW = 18.75 kHz
Sensitivity at 25 kbps		−110		dBm	f_{DEV} = 10 kHz, high sensitivity mode, IF_BW = 25 kHz
Gaussian 2FSK					
Sensitivity at 0.1 kbps		−129		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 0.25 kbps		−127		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 1 kbps		−121		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 9.6 kbps		−114		dBm	f_{DEV} = 4 kHz, high sensitivity mode, IF_BW = 18.75 kHz
Sensitivity at 25 kbps		−111		dBm	f_{DEV} = 10 kHz, high sensitivity mode, IF_BW = 25 kHz
GMSK					
Sensitivity at 9.6 kbps		−113		dBm	f_{DEV} = 2.4 kHz, high sensitivity mode, IF_BW = 18.75 kHz
Raised Cosine 2FSK					
Sensitivity at 0.25 kbps		−127		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 1 kbps		−121		dBm	f_{DEV} = 1 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 9.6 kbps		−114		dBm	f_{DEV} = 4 kHz, high sensitivity mode, IF_BW = 18.75 kHz
Sensitivity at 25 kbps		−113		dBm	f_{DEV} = 10 kHz, high sensitivity mode, IF_BW = 25 kHz
3FSK					
Sensitivity at 9.6 kbps		−110		dBm	f_{DEV} = 2.4 kHz, high sensitivity mode, IF_BW = 18.75 kHz, Viterbi detection on
Raised Cosine 3FSK					
Sensitivity at 9.6 kbps		−110		dBm	f_{DEV} = 2.4 kHz, high sensitivity mode, IF_BW = 12.5 kHz, alpha = 0.5, Viterbi detection on
Sensitivity at 19.6 kbps		−106		dBm	f_{DEV} = 4.8 kHz, high sensitivity mode, IF_BW = 18.75 kHz, alpha = 0.5, Viterbi detection on
4FSK					
Sensitivity at 9.6 kbps		−112		dBm	f_{DEV} (inner) = 1.2 kHz, high sensitivity mode, IF_BW = 12.5 kHz
Sensitivity at 19.6 kbps		−107		dBm	f_{DEV} (inner) = 2.4 kHz, high sensitivity mode, IF_BW = 25 kHz
Raised Cosine 4FSK					
Sensitivity at 9.6 kbps		−109		dBm	f_{DEV} (inner) = 1.2 kHz, high sensitivity mode, IF_BW = 12.5 kHz, alpha = 0.5
Sensitivity at 19.2 kbps		−103		dBm	f_{DEV} (inner) = 1.2 kHz, high sensitivity mode, IF_BW = 18.75 kHz, alpha = 0.5
Sensitivity at 32.8 kbps		−100		dBm	f_{DEV} (inner) = 1.8 kHz, high sensitivity mode, IF_BW = 25 kHz, alpha = 0.7
INPUT IP3					Two-tone test, f_{LO} = 860 MHz, F1 = f_{LO} + 100 kHz, F2 = f_{LO} − 800 kHz
Low Gain Enhanced Linearity Mode		−3		dBm	LNA_GAIN = 3, MIXER_LINEARITY = 1
Medium Gain Mode		−13.5		dBm	LNA_GAIN = 10, MIXER_LINEARITY = 0
High Sensitivity Mode		−24		dBm	LNA_GAIN = 30, MIXER_LINEARITY = 0

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADJACENT CHANNEL REJECTION					
868 MHz					Wanted signal is 3 dB above the sensitivity point (BER = 10^{-3}); unmodulated interferer is at the center of the adjacent channel; rejection measured as the difference between interferer level and wanted signal level in dB
12.5 kHz Channel Spacing		25		dB	12.5 kHz IF_BW
25 kHz Channel Spacing		27		dB	25 kHz IF_BW
25 kHz Channel Spacing		39		dB	18 kHz IF_BW
426 MHz, External Inductor VCO					Wanted signal 3 dB above reference sensitivity point (BER = 10^{-2}); modulated interferer (1 kHz sine, ±2 kHz deviation) at the center of the adjacent channel; rejection measured as the difference between interferer level and reference sensitivity level in dB
12.5 kHz Channel Spacing		25		dB	12.5 kHz IF_BW
25 kHz Channel Spacing		30		dB	25 kHz IF_BW
25 kHz Channel Spacing		41		dB	18 kHz IF_BW, compliant with ARIB STD-T67
CO-CHANNEL REJECTION					Wanted signal (2FSK, 9.6 kbps, ±4 kHz deviation) is 10 dB above the sensitivity point (BER = 10^{-3}), modulated interferer
868 MHz		−3		dB	
IMAGE CHANNEL REJECTION					Wanted signal (2FSK, 9.6 kbps, ±4 kHz deviation) is 10 dB above the sensitivity point (BER = 10^{-3}); modulated interferer (2FSK, 9.6 kbps, ±4 kHz deviation) is placed at the image frequency of f_{RF} − 200 kHz; interferer level is increased until BER = 10^{-3}
900 MHz		23/39		dB	Uncalibrated/calibrated[1], V_{DD} = 3.0 V, T_A = 25°C
450 MHz		29/50		dB	Uncalibrated/calibrated[1], V_{DD} = 3.0 V, T_A = 25°C
450 MHz, External Inductor VCO		38/53		dB	Uncalibrated/calibrated[1], V_{DD} = 3.0 V, T_A = 25°C
BLOCKING					Wanted signal is 10 dB above the input sensitivity level; CW interferer level is increased until BER = 10^{-3}
±1 MHz		69		dB	
±2 MHz		75		dB	
±5 MHz		78		dB	
±10 MHz		78.5		dB	
SATURATION (MAXIMUM INPUT LEVEL)		12		dBm	2FSK mode, BER = 10^{-3}
RSSI					
Range at Input[2]		−120 to −47		dBm	
Linearity		±2		dB	Input power range = −100 dBm to −47 dBm
Absolute Accuracy		±3		dB	Input power range = −100 dBm to −47 dBm
Response Time		300		µs	See the RSSI/AGC section
AFC					
Pull-In Range	0.5		1.5 × IF_BW	kHz	The range is programmable, R10_DB[24:31]
Response Time		48		Bits	
Accuracy		0.5		kHz	Input power range = −100 dBm to +12 dBm
Rx SPURIOUS EMISSIONS[3]					
Internal Inductor VCO		−91/−91		dBm	<1 GHz at antenna input, unfiltered conductive/filtered conductive
		−52/−70		dBm	>1 GHz at antenna input, unfiltered conductive/filtered conductive
External Inductor VCO		−62/−72		dBm	<1 GHz at antenna input, unfiltered conductive/filtered conductive
		−64/−85		dBm	>1 GHz at antenna input, unfiltered conductive/filtered conductive

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LNA INPUT IMPEDANCE					RFIN to RFGND
f_{RF} = 915 MHz		24 – j60		Ω	
f_{RF} = 868 MHz		26 – j63		Ω	
f_{RF} = 450 MHz		63 – j129		Ω	
f_{RF} = 426 MHz		68 – j134		Ω	
f_{RF} = 315 MHz		96 – j160		Ω	
f_{RF} = 175 MHz		178 – j190		Ω	

[1] Calibration of the image rejection used an external RF source.
[2] For received signal levels < −100 dBm, it is recommended to average the RSSI readback value over a number of samples to improve the RSSI accuracy at low input powers.
[3] Filtered conductive receive spurious emissions measured on the EVAL-ADF7021DB evaluation boards, which includes a T-stage harmonic filter (two inductors and one capacitor).

DIGITAL SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TIMING INFORMATION					
Chip Enabled to Regulator Ready		10		µs	C_{REG} = 100 nF
Chip Enabled to Tx Mode					32-bit register write time = 50 µs
TCXO Reference		1		ms	
XTAL		2		ms	
Chip Enabled to Rx Mode					32-bit register write time = 50 µs, IF filter coarse calibration only
TCXO Reference		1.2		ms	
XTAL		2.2		ms	
Tx to Rx Turnaround Time		300 µs + (5 × t_{BIT})			Time to synchronized data out, includes AGC settling and CDR synchronization; see AGC Information and Timing section for more details; t_{BIT} = data bit period
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7 × V_{DD}			V	
Input Low Voltage, V_{INL}			0.2 × V_{DD}	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
Control Clock Input			50	MHz	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	DV_{DD} – 0.4			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
CLKOUT Rise/Fall			5	ns	
CLKOUT Load			10	pF	

GENERAL SPECIFICATIONS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE RANGE (T_A)	−40		+85	°C	
POWER SUPPLIES					
Voltage Supply, V_{DD}	2.3		3.6	V	All VDD pins must be tied together
TRANSMIT CURRENT CONSUMPTION[1]					V_{DD} = 3.0 V, PA is matched into 50 Ω
868 MHz					VCO_BIAS = 8
0 dBm		20.2		mA	
5 dBm		24.7		mA	
10 dBm		32.3		mA	
450 MHz, Internal Inductor VCO					VCO_BIAS = 8
0 dBm		19.9		mA	
5 dBm		23.2		mA	
10 dBm		29.2		mA	
426 MHz, External Inductor VCO					VCO_BIAS = 2
0 dBm		13.5		mA	
5 dBm		17		mA	
10 dBm		23.3		mA	
RECEIVE CURRENT CONSUMPTION					V_{DD} = 3.0 V
868 MHz					VCO_BIAS = 8
Low Current Mode		22.7		mA	
High Sensitivity Mode		24.6		mA	
433MHz, Internal Inductor VCO					VCO_BIAS = 8
Low Current Mode		24.5		mA	
High Sensitivity Mode		26.4		mA	
426 MHz, External Inductor VCO					VCO_BIAS = 2
Low Current Mode		17.5		mA	
High Sensitivity Mode		19.5		mA	
POWER-DOWN CURRENT CONSUMPTION					
Low Power Sleep Mode		0.1	1	µA	CE low

[1] The transmit current consumption tests used the same combined PA and LNA matching network as that used on the EVAL-ADF7021DB evaluation boards. Improved PA efficiency is achieved by using a separate PA matching network.

TIMING CHARACTERISTICS

V_{DD} = 3 V ± 10%, DGND = AGND = 0 V, T_A = 25°C, unless otherwise noted. Guaranteed by design but not production tested.

Table 6.

Parameter	Limit at T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
t_1	>10	ns	SDATA to SCLK setup time
t_2	>10	ns	SDATA to SCLK hold time
t_3	>25	ns	SCLK high duration
t_4	>25	ns	SCLK low duration
t_5	>10	ns	SCLK to SLE setup time
t_6	>20	ns	SLE pulse width
t_8	<25	ns	SCLK to SREAD data valid, readback
t_9	<25	ns	SREAD hold time after SCLK, readback
t_{10}	>10	ns	SCLK to SLE disable time, readback
t_{11}	$5 < t_{11} < (¼ \times t_{BIT})$	ns	TxRxCLK negative edge to SLE
t_{12}	>5	ns	TxRxDATA to TxRxCLK setup time (Tx mode)
t_{13}	>5	ns	TxRxCLK to TxRxDATA hold time (Tx mode)
t_{14}	$>¼ \times t_{BIT}$	µs	TxRxCLK negative edge to SLE
t_{15}	$>¼ \times t_{BIT}$	µs	SLE positive edge to positive edge of TxRxCLK

Timing Diagrams

Serial Interface

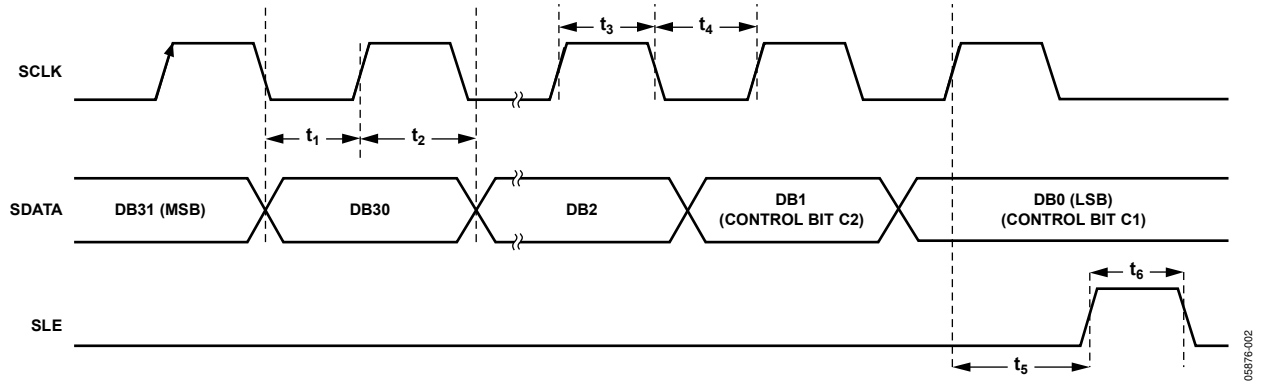

Figure 2. Serial Interface Timing Diagram

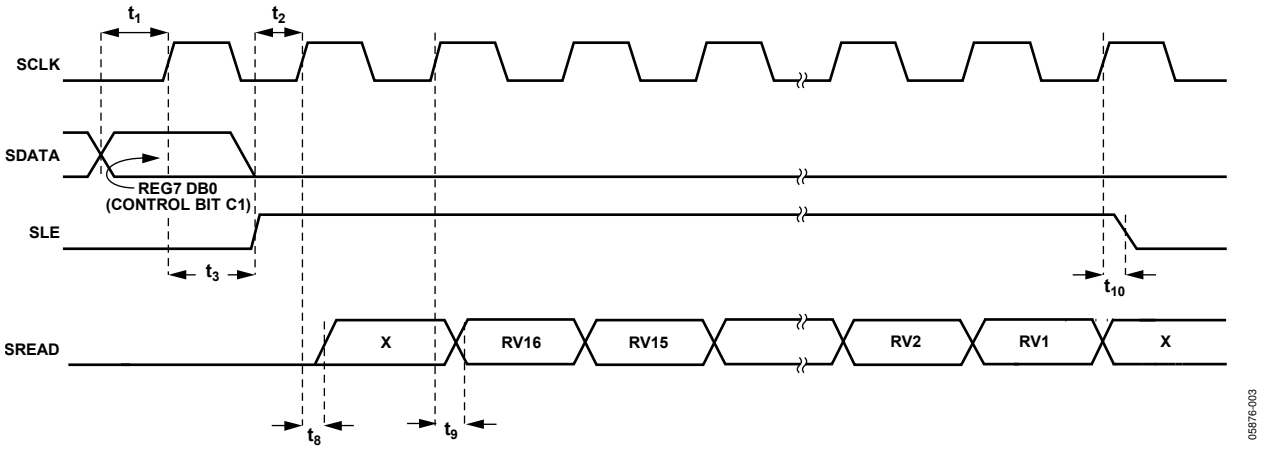

Figure 3. Serial Interface Readback Timing Diagram

2FSK/3FSK Timing

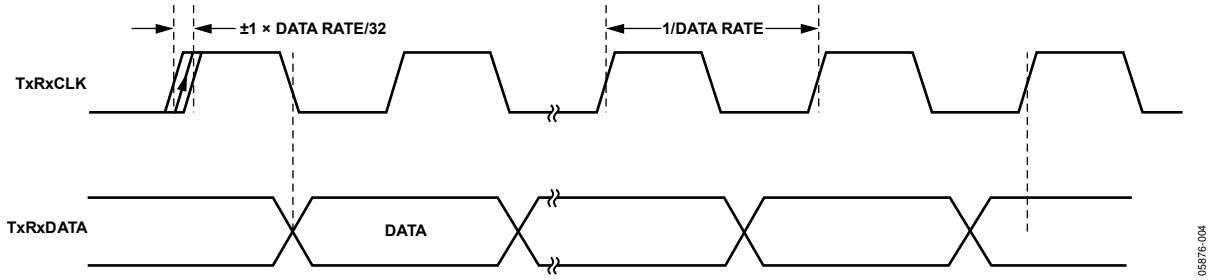

Figure 4. TxRxDATA/TxRxCLK Timing Diagram in Receive Mode

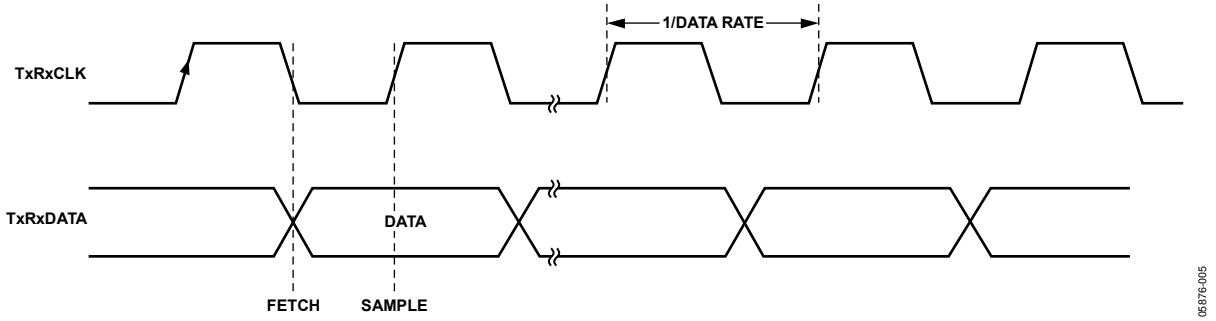

Figure 5. TxRxDATA/TxRxCLK Timing Diagram in Transmit Mode

4FSK Timing

In 4FSK receive mode, MSB/LSB synchronization is guaranteed by SWD in the receive bit stream.

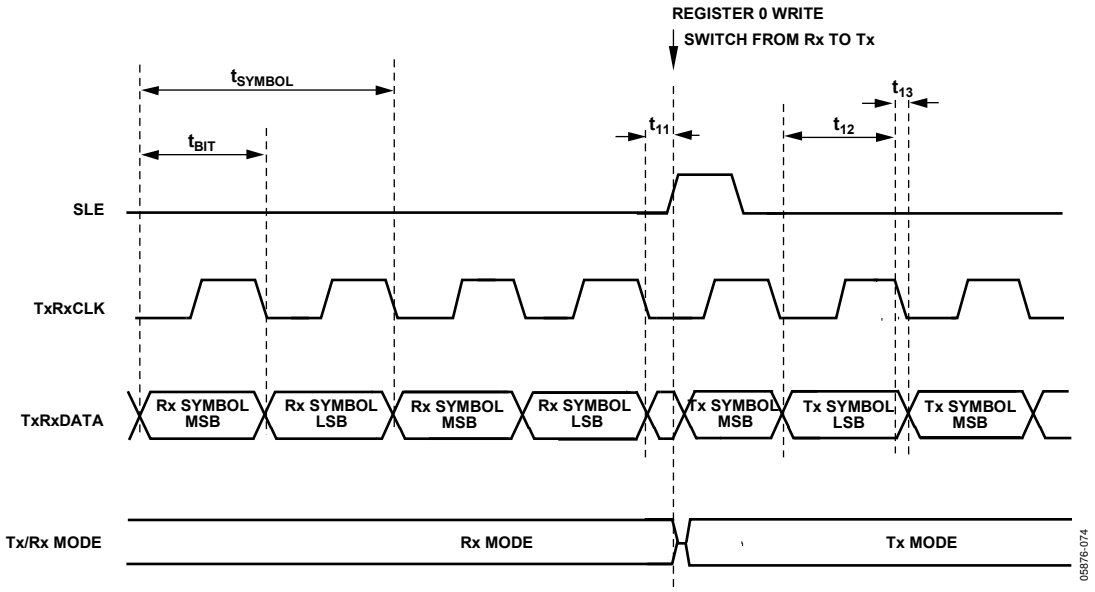

Figure 6. Receive-to-Transmit Timing Diagram in 4FSK Mode

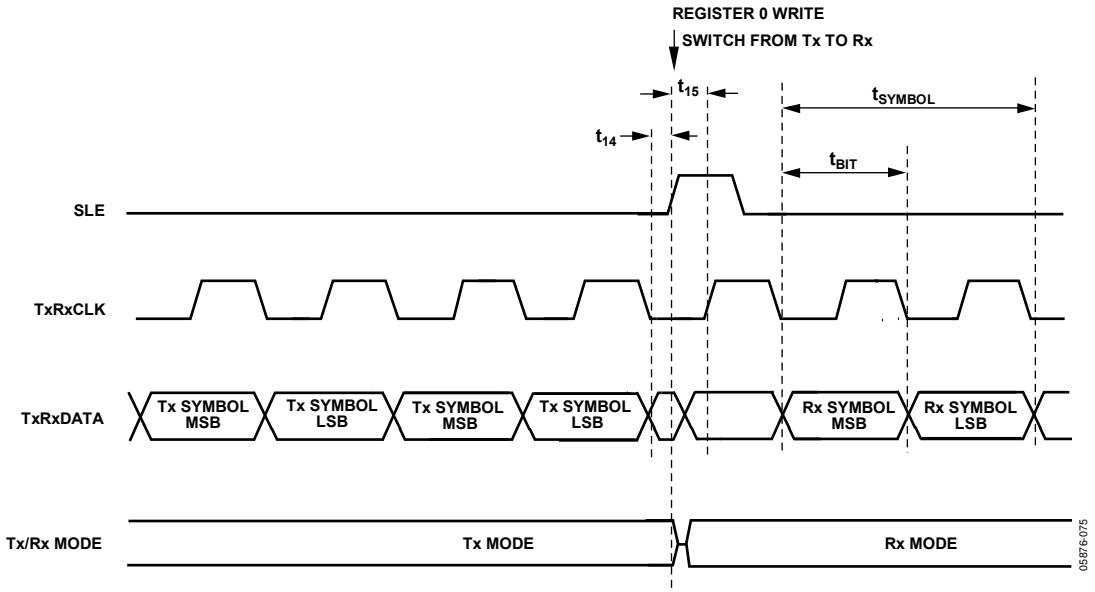

Figure 7. Transmit-to-Receive Timing Diagram in 4FSK Mode

UART/SPI Mode

UART mode is enabled by setting R0_DB28 to 1. SPI mode is enabled by setting R0_DB28 to 1 and setting R15_DB[17:19] to 0x7. The transmit/receive data clock is available on the CLKOUT pin.

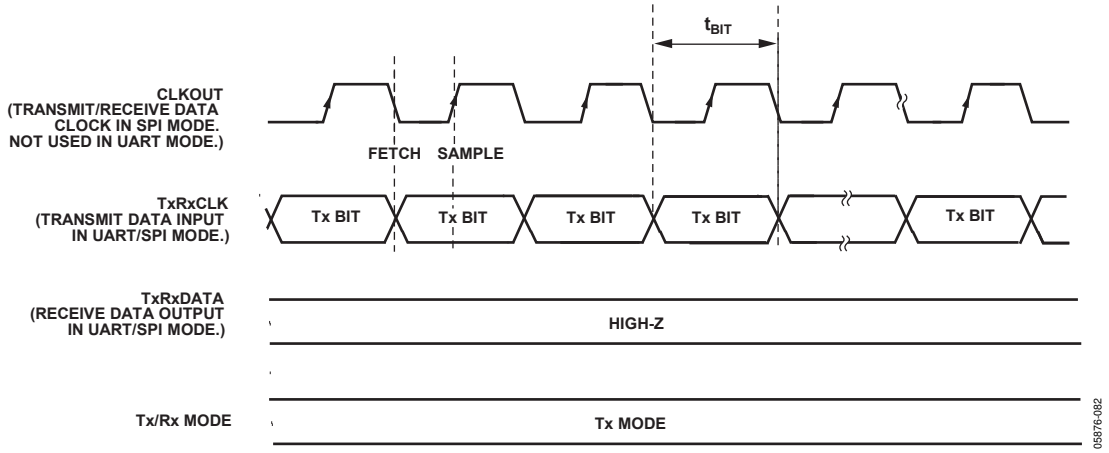

Figure 8. Transmit Timing Diagram in UART/SPI Mode

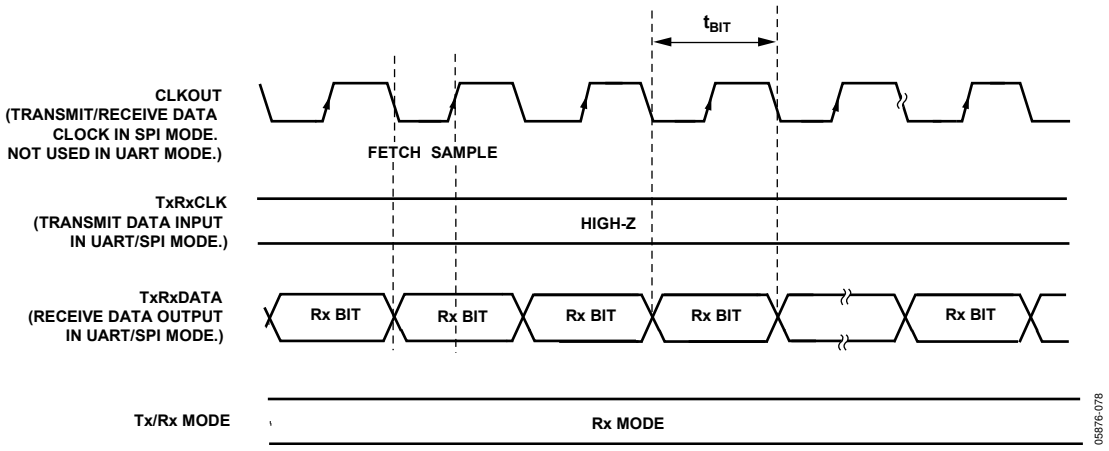

Figure 9. Receive Timing Diagram in UART/SPI Mode

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to GND[1]	−0.3 V to +5 V
Analog I/O Voltage to GND	−0.3 V to AV_{DD} + 0.3 V
Digital I/O Voltage to GND	−0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
MLF θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

[1] GND = CPGND = RFGND = DGND = AGND = 0 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV and it is ESD sensitive. Take proper precautions for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

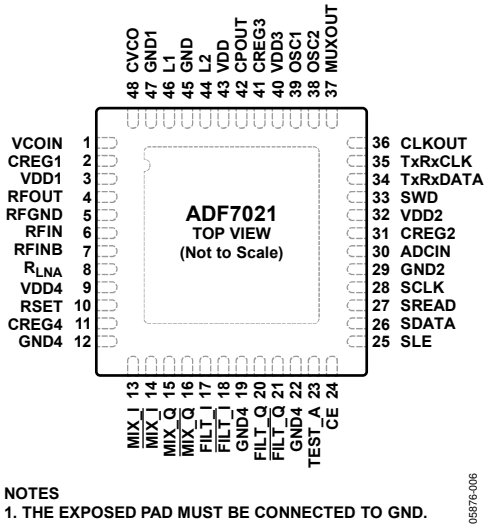

Figure 10. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCOIN	Regulator Voltage for PA Block and VCO Cores. The tuning voltage on this pin determines the output frequency of the voltage controlled oscillator (VCO). The higher the tuning voltage, the higher the output frequency.
2	CREG1	Regulator Voltage for PA Block. Place a series 3.9 Ω resistor and a 100 nF capacitor between this pin and ground for regulator stability and noise rejection.
3	VDD1	Voltage Supply for PA Block and VCO Cores. Place decoupling capacitors of 0.1 µF and 100 pF as close as possible to this pin. Tie all VDD pins together.
4	RFOUT	The modulated signal is available at this pin. Output power levels are from −16 dBm to +13 dBm. Impedance match the output to the desired load using suitable components (see the Transmitter section).
5	RFGND	Ground for Output Stage of Transmitter. Tie all GND pins together.
6	RFIN	LNA Input for Receiver Section. Input matching is required between the antenna and the differential LNA input to ensure maximum power transfer (see the LNA/PA Matching section).
7	RFINB	Complementary LNA Input (see the LNA/PA Matching section).
8	R_{LNA}	External Bias Resistor for LNA. Optimum resistor is 1.1 kΩ with 5% tolerance.
9	VDD4	Voltage Supply for LNA/MIXER Block. Decouple this pin to ground with a 10 nF capacitor.
10	RSET	External Resistor. Sets charge pump current and some internal bias currents. Use a 3.6 kΩ resistor with 5% tolerance.
11	CREG4	Regulator Voltage for LNA/MIXER Block. Place a 100 nF capacitor between this pin and GND for regulator stability and noise rejection.
12, 19, 22	GND4	Ground for LNA/MIXER Block.
13 to 18	MIX_I, $\overline{\text{MIX\_I}}$, MIX_Q, $\overline{\text{MIX\_Q}}$, FILT_I, $\overline{\text{FILT\_I}}$	Signal Chain Test Pins. These pins are high impedance under normal conditions; leave the pins unconnected.
20, 21, 23	FILT_Q, $\overline{\text{FILT\_Q}}$, TEST_A	Signal Chain Test Pins. These pins are high impedance under normal conditions; leave the pins unconnected.
24	CE	Chip Enable. Bringing CE low puts the ADF7021 into complete power-down. Register values are lost when CE is low, and the device must be reprogrammed once CE is brought high.
25	SLE	Load Enable, CMOS Input. When SLE goes high, the data stored in the shift registers is loaded into one of the four latches. A latch is selected using the control bits.
26	SDATA	Serial Data Input. The serial data is loaded MSB first with the 4 LSBs as the control bits. This pin is a high impedance CMOS input.
27	SREAD	Serial Data Output. This pin is used to feed readback data from the ADF7021 to the microcontroller. The SCLK input is used to clock each readback bit (for example, AFC or ADC) from the SREAD pin.
28	SCLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 32-bit shift register on the CLK rising edge. This pin is a digital CMOS input.

Pin No.	Mnemonic	Description
29	GND2	Ground for Digital Section.
30	ADCIN	Analog-to-Digital Converter Input. The internal 7-bit ADC can be accessed through this pin. Full scale is 0 V to 1.9 V. Readback is made using the SREAD pin.
31	CREG2	Regulator Voltage for Digital Block. Place a 100 nF capacitor between this pin and ground for regulator stability and noise rejection.
32	VDD2	Voltage Supply for Digital Block. Place a decoupling capacitor of 10 nF as close as possible to this pin.
33	SWD	Sync Word Detect. The ADF7021 asserts this pin when it has found a match for the sync word sequence (see the Register 11—Sync Word Detect Register section). This provides an interrupt for an external microcontroller indicating valid data is being received.
34	TxRxDATA	Transmit Data Input/Received Data Output. This is a digital pin and normal CMOS levels apply. In UART/SPI mode, this pin provides an output for the received data in receive mode. In transmit UART/SPI mode, this pin is high impedance (see the Interfacing to Microcontroller/DSP section).
35	TxRxCLK	Outputs the data clock in both receive and transmit modes. This is a digital pin and normal CMOS levels apply. The positive clock edge is matched to the center of the received data. In transmit mode, this pin outputs an accurate clock to latch the data from the microcontroller into the transmit section at the exact required data rate. In UART/SPI mode, this pin is used to input the transmit data in transmit mode. In receive UART/SPI mode, this pin is high impedance (see the Interfacing to Microcontroller/DSP section).
36	CLKOUT	A divided-down version of the crystal reference with output driver. The digital clock output can be used to drive several other CMOS inputs such as a microcontroller clock. The output has a 50:50 mark-space ratio and is inverted with respect to the reference. Place a series 1 kΩ resistor as close as possible to the pin in applications where the CLKOUT feature is being used.
37	MUXOUT	Provides the DIGITAL_LOCK_DETECT Signal. This signal is used to determine if the PLL is locked to the correct frequency. It also provides other signals such as REGULATOR_READY, which is an indicator of the status of the serial interface regulator (see the MUXOUT section for more information).
38	OSC2	Connect the reference crystal between this pin and OSC1. A TCXO reference can be used by driving this pin with CMOS levels and disabling the internal crystal oscillator.
39	OSC1	Connect the reference crystal between this pin and OSC2. A TCXO reference can be used by driving this pin with ac-coupled 0.8 V p-p levels and by enabling the internal crystal oscillator.
40	VDD3	Voltage Supply for the Charge Pump and PLL Dividers. Decouple this pin to ground with a 10 nF capacitor.
41	CREG3	Regulator Voltage for Charge Pump and PLL Dividers. Place a 100 nF capacitor between this pin and ground for regulator stability and noise rejection.
42	CPOUT	Charge Pump Output. This output generates current pulses that are integrated in the loop filter. The integrated current changes the control voltage on the input to the VCO.
43	VDD	Voltage Supply for XTAL and Bandgap Core. Decouple this pin to ground with a 10 nF capacitor.
44, 46	L2, L1	External VCO Inductor Pins. If using an external VCO inductor, connect a chip inductor across these pins to set the VCO operating frequency. If using t internal VCO inductor, these pins can be left floating. See the Voltage Controlled Oscillator (VCO) section he for more information.
45, 47	GND, GND1	Grounds for VCO Block.
48	CVCO	Place a 22 nF capacitor between this pin and CREG1 to reduce VCO noise.
49	EPAD	Exposed Pad. The exposed pad must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

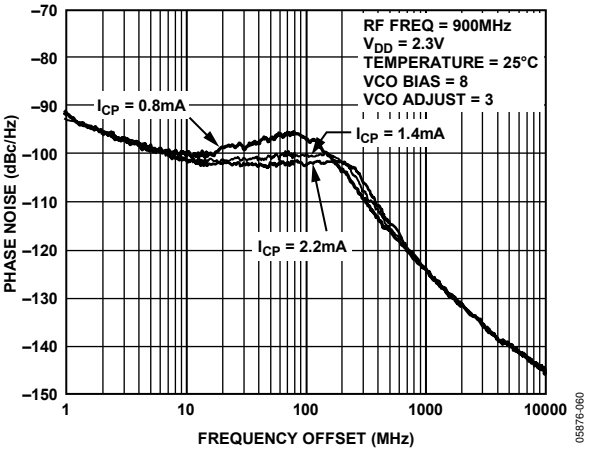

Figure 11. Phase Noise Response at 900 MHz, V_{DD} = 2.3 V

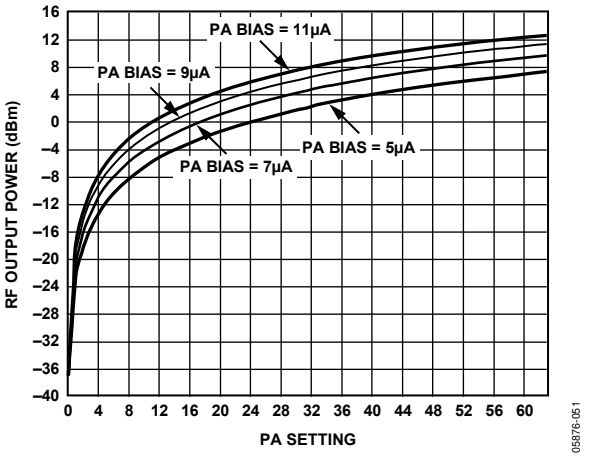

Figure 12. RF Output Power vs. PA Setting

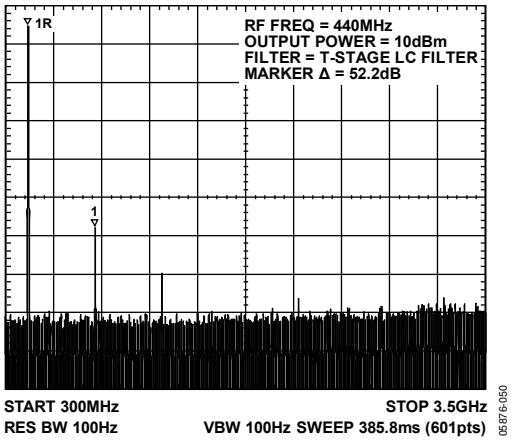

Figure 13. PA Output Harmonic Response with T-Stage LC Filter

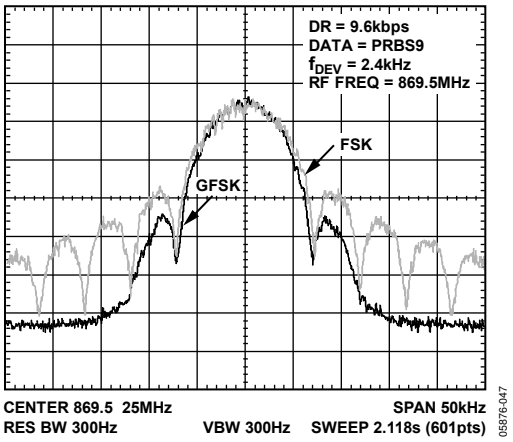

Figure 14. Output Spectrum in 2FSK and GFSK Modes

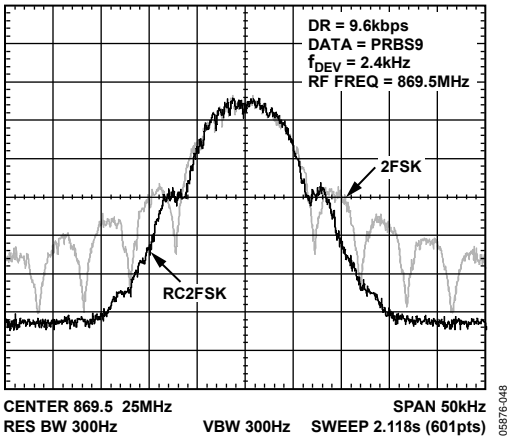

Figure 15. Output Spectrum in 2FSK and Raised Cosine 2FSK Modes

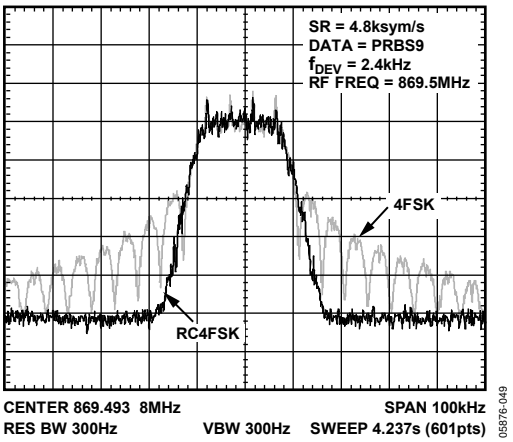

Figure 16. Output Spectrum in 4FSK and Raised Cosine 4FSK Modes

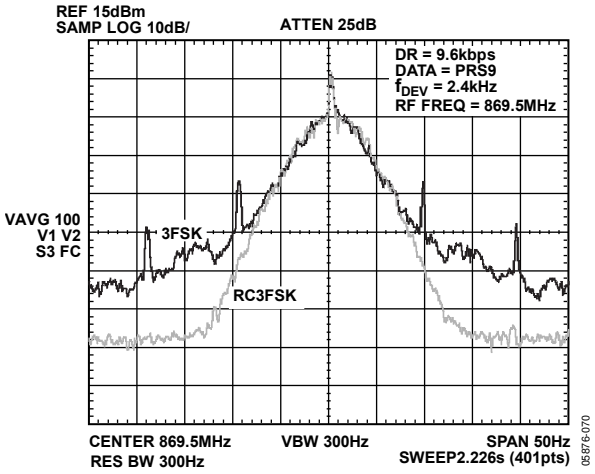

Figure 17. Output Spectrum in 3FSK and Raised Cosine 3FSK Modes

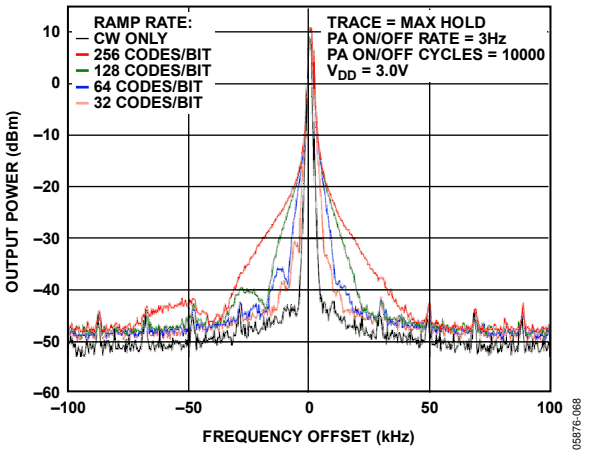

Figure 18. Output Spectrum in Maximum Hold for Various PA Ramp Rate Options

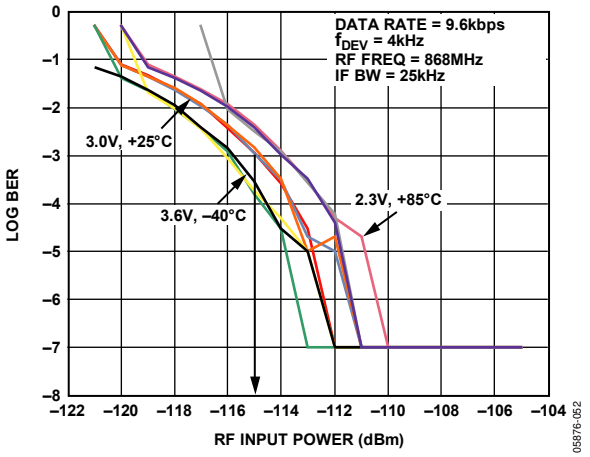

Figure 19. 2FSK Sensitivity vs. V_{DD} and Temperature, f_{RF} = 868 MHz

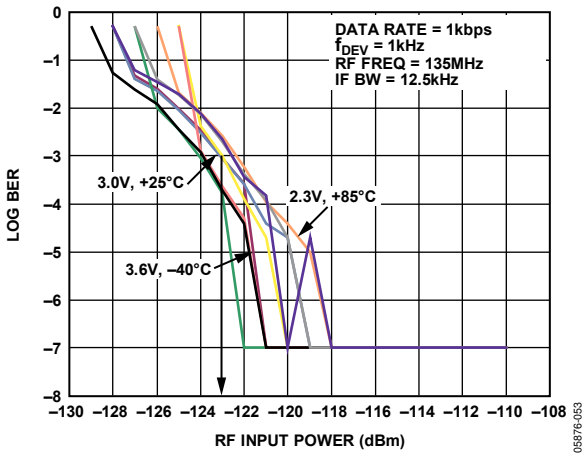

Figure 20. 2FSK Sensitivity vs. V_{DD} and Temperature, f_{RF} = 135 MHz

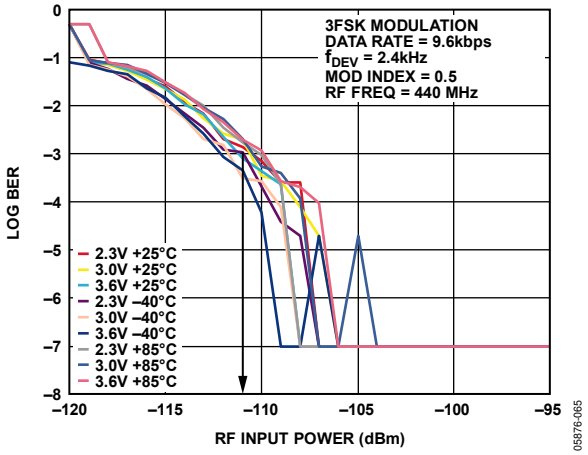

Figure 21. 3FSK Sensitivity vs. V_{DD} and Temperature, f_{RF} = 440 MHz

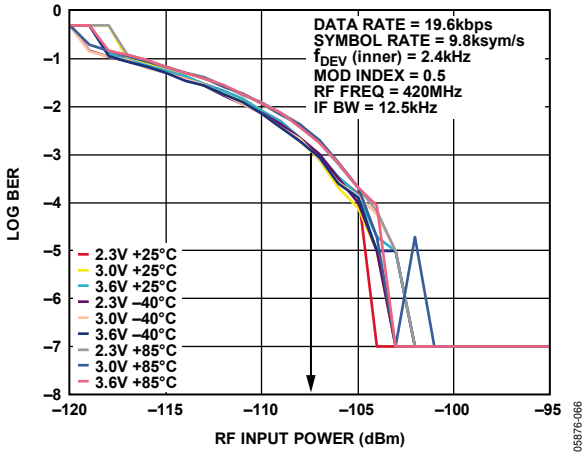

Figure 22. 4FSK Sensitivity vs. V_{DD} and Temperature, f_{RF} = 420 MHz

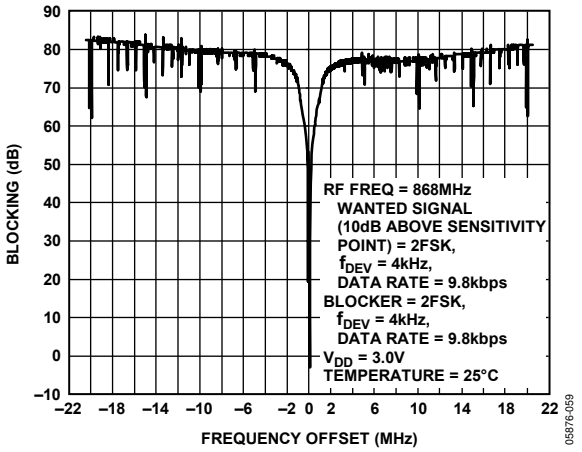

Figure 23. Wideband Interference Rejection

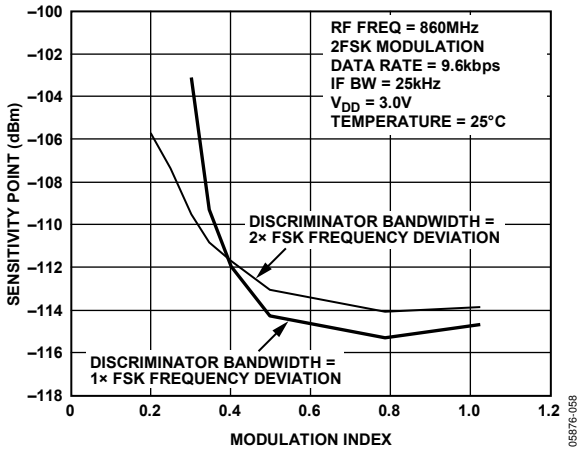

Figure 26. 2FSK Sensitivity vs. Modulation Index vs. Correlator Discriminator Bandwidth

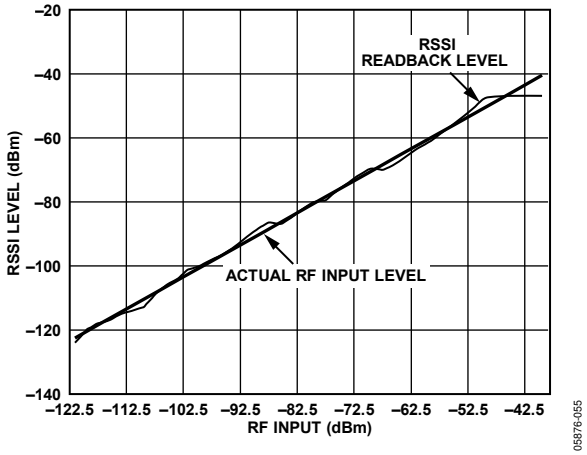

Figure 24. Digital RSSI Readback Linearity

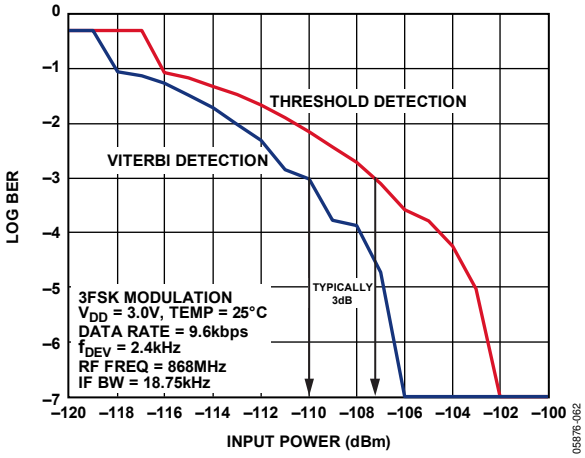

Figure 27. 3FSK Receiver Sensitivity Using Viterbi Detection and Threshold Detection

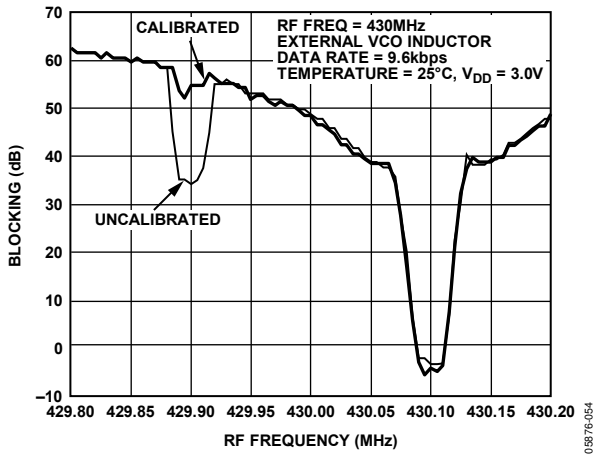

Figure 25. Image Rejection, Uncalibrated vs. Calibrated

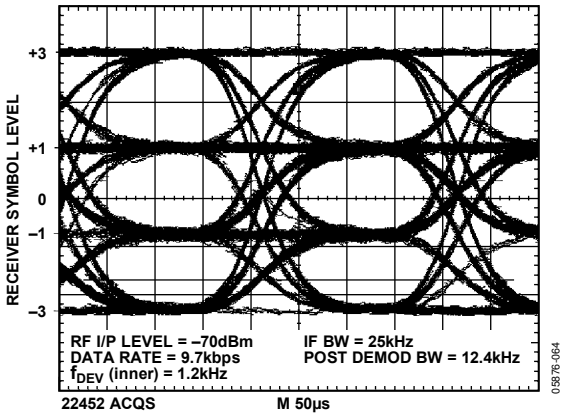

Figure 28. 4FSK Receiver Eye Diagram Measure Using the Test DAC Output

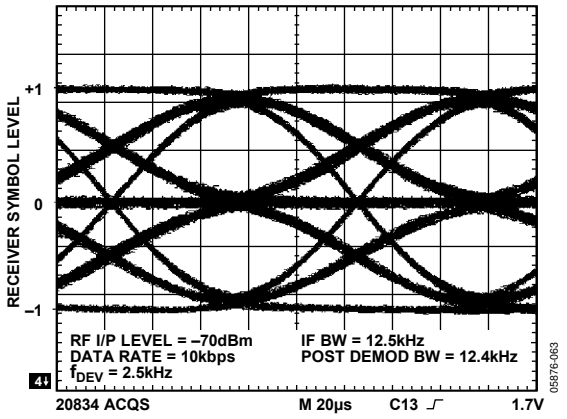

Figure 29. 3FSK Receiver Eye Diagram Measured Using the Test DAC Output

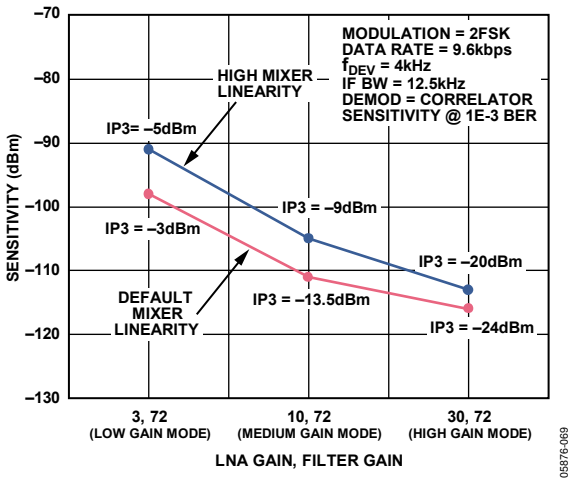

Figure 30. Receive Sensitivity vs. LNA/IF Filter Gain and Mixer Linearity Settings (The Input IP3 at Each Setting is Also Shown)

FREQUENCY SYNTHESIZER

REFERENCE INPUT

The on-board crystal oscillator circuitry (see Figure 31) can use a quartz crystal as the PLL reference. Using a quartz crystal with a frequency tolerance of ≤10 ppm for narrow-band applications is recommended. It is possible to use a quartz crystal with >10 ppm tolerance, but to comply with the absolute frequency error specifications of narrow-band regulations (for example, ARIB STD-T67 and ETSI EN 300-220), compensation for the frequency error of the crystal is necessary.

The oscillator circuit is enabled by setting R1_DB12 high. It is enabled by default on power-up and is disabled by bringing CE low. Errors in the crystal can be corrected by using the automatic frequency control feature or by adjusting the fractional-N value (see the N Counter section).

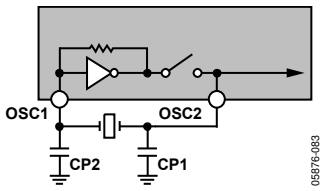

Figure 31. Oscillator Circuit on the ADF7021

Two parallel resonant capacitors are required for oscillation at the correct frequency. Their values are dependent upon the crystal specification. When choosing the values of the capacitors, make sure that the series value of capacitance added to the PCB track capacitance adds up to the specified load capacitance of the crystal, usually 12 pF to 20 pF. Track capacitance values vary from 2 pF to 5 pF, depending on board layout. When possible, choose capacitors that have a very low temperature coefficient to ensure stable frequency operation over all conditions.

Using a TCXO Reference

A single-ended reference (TCXO, VCXO, or OCXO) can also be used with the ADF7021. This is recommended for applications having absolute frequency accuracy requirements of <10 ppm, such as ARIB STD-T67 or ETSI EN 300-220. There are two options for interfacing the ADF7021 to an external reference oscillator.

- An oscillator with CMOS output levels can be applied to OSC2. Disable the internal oscillator circuit by setting R1_DB12 low.
- An oscillator with 0.8 V p-p levels can be ac-coupled through a 22 pF capacitor into OSC1. Enable the internal oscillator circuit by setting R1_DB12 high.

Programmable Crystal Bias Current

Bias current in the oscillator circuit can be configured between 20 µA and 35 µA by writing to the XTAL_BIAS bits (R1_DB[13:14]). Increasing the bias current allows the crystal oscillator to power up faster.

CLKOUT Divider and Buffer

The CLKOUT circuit takes the reference clock signal from the oscillator section, shown in Figure 32, and supplies a divided-down, 50:50 mark-space signal to the CLKOUT pin. The CLKOUT signal is inverted with respect to the reference clock. An even divide from 2 to 30 is available. This divide number is set in R1_DB[7:10]. On power-up, the CLKOUT defaults to divide-by-8.

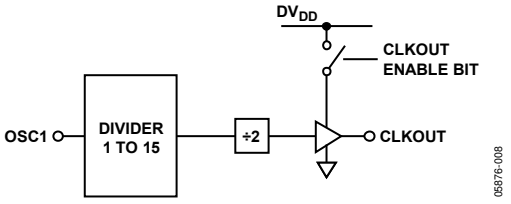

Figure 32. CLKOUT Stage

To disable CLKOUT, set the divide number to 0. The output buffer can drive up to a 20 pF load with a 10% rise time at 4.8 MHz. Faster edges can result in some spurious feedthrough to the output. A series resistor (1 kΩ) can be used to slow the clock edges to reduce these spurs at the CLKOUT frequency.

R Counter

The 3-bit R counter divides the reference input frequency by an integer of 1 to 7. The divided-down signal is presented as the reference clock to the phase frequency detector (PFD). The divide ratio is set in R1_DB[4:6]. Maximizing the PFD frequency reduces the N value. This reduces the noise multiplied at a rate of 20 log(N) to the output and reduces occurrences of spurious components.

Register 1 defaults to R = 1 on power-up.

$$PFD\ [\text{Hz}] = XTAL/R$$

Loop Filter

The loop filter integrates the current pulses from the charge pump to form a voltage that tunes the output of the VCO to the desired frequency. It also attenuates spurious levels generated by the PLL. A typical loop filter design is shown in Figure 33.

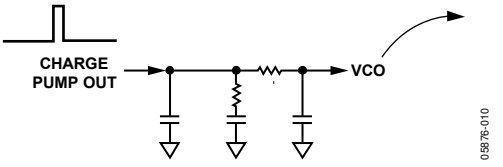

Figure 33. Typical Loop Filter Configuration

Design the loop so that the loop bandwidth (LBW) is approximately 100 kHz. This provides a good compromise between in-band phase noise and out-of-band spurious rejection. Widening the LBW excessively reduces the time spent jumping between frequencies, but it can cause insufficient spurious attenuation. Narrow-loop bandwidths can result in the loop taking long periods to attain lock and can also result in a higher level of power falling into the adjacent channel. Use the loop filter design on the EVAL-ADF7021DB evaluation boards for optimum performance.

The free design tool ADIsimPLL can also be used to design loop filters for the ADF7021 (go to www.analog.com/ADIsimPLL for details).

N Counter

The feedback divider in the ADF7021 PLL consists of an 8-bit integer counter (R0_DB[19:26]) and a 15-bit Σ-Δ FRACTIONAL_N divider (R0_DB[4:18]). The integer counter is the standard pulse-swallow type that is common in PLLs. This sets the minimum integer divide value to 23. The fractional divide value provides very fine resolution at the output, where the output frequency of the PLL is calculated as

$$f_{OUT} = \frac{XTAL}{R} \times \left(INTEGER\_N + \frac{FRACTIONAL\_N}{2^{15}} \right)$$

When RF_DIVIDE_BY_2 (see the Voltage Controlled Oscillator (VCO) section) is selected, this formula becomes

$$f_{OUT} = \frac{XTAL}{R} \times 0.5 \times \left(INTEGER\_N + \frac{FRACTIONAL\_N}{2^{15}} \right)$$

The combination of the INTEGER_N (maximum = 255) and the FRACTIONAL_N (maximum = 32,768/32,768) give a maximum N divider of 255 + 1. Therefore, the minimum usable PFD is

$$PFD_{MIN}[\text{Hz}] = \frac{Maximum\ Required\ Output\ Frequency}{(255+1)}$$

For example, when operating in the European 868 MHz to 870 MHz band, PFD_{MIN} equals 3.4 MHz.

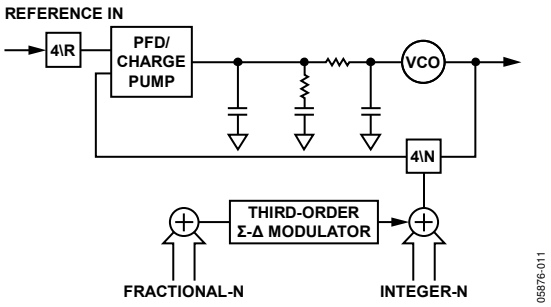

Figure 34. Fractional-N PLL

Voltage Regulators

The ADF7021 contains four regulators to supply stable voltages to the device. The nominal regulator voltage is 2.3 V. Regulator 1 requires a 3.9 Ω resistor and a 100 nF capacitor in series between CREG1 and GND, whereas the other regulators require a 100 nF capacitor connected between CREGx and GND. When CE is high, the regulators and other associated circuitry are powered on, drawing a total supply current of 2 mA. Bringing the CE pin low disables the regulators, reduces the supply current to less than 1 μA, and erases all values held in the registers. The serial interface operates from a regulator supply. Therefore, to write to the device, the user must have CE high and the regulator voltage must be stabilized. Regulator status (CREG4) can be monitored using the REGULATOR_READY signal from MUXOUT.

MUXOUT

The MUXOUT pin allows access to various digital points in the ADF7021. The state of MUXOUT is controlled by R0_DB[29:31].

REGULATOR_READY

REGULATOR_READY is the default setting on MUXOUT after the transceiver is powered up. The power-up time of the regulator is typically 50 μs. Because the serial interface is powered from the regulator, the regulator must be at its nominal voltage before the ADF7021 can be programmed. The status of the regulator can be monitored at MUXOUT. When the regulator ready signal on MUXOUT is high, programming of the ADF7021 can begin.

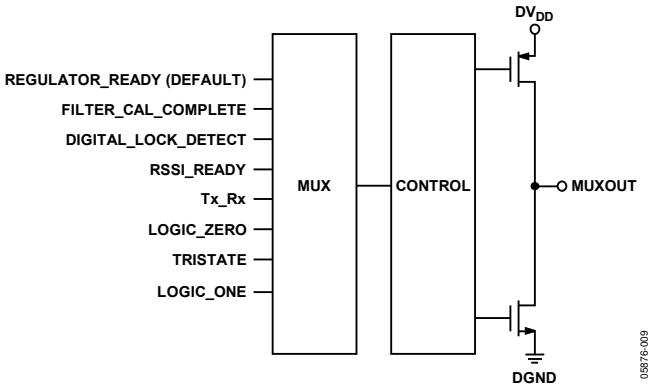

Figure 35. MUXOUT Circuit

FILTER_CAL_COMPLETE

MUXOUT can be set to FILTER_CAL_COMPLETE. This signal goes low for the duration of both a coarse IF filter calibration and a fine IF filter calibration. It can be used as an interrupt to a microcontroller to signal the end of the IF filter calibration.

DIGITAL_LOCK_DETECT

DIGITAL_LOCK_DETECT indicates when the PLL has locked. The lock detect circuit is located at the PFD. When the phase error on five consecutive cycles is less than 15 ns, lock detect is set high. Lock detect remains high until a 25 ns phase error is detected at the PFD.

RSSI_READY

MUXOUT can be set to RSSI_READY. This indicates that the internal analog RSSI has settled and a digital RSSI readback can be performed.

Tx_Rx

Tx_Rx signifies whether the ADF7021 is in transmit or receive mode. When in transmit mode, this signal is low. When in receive mode, this signal is high. It can be used to control an external Tx/Rx switch.