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High Performance, Low Power, ISM Band FSK/GFSK/MSK/GMSK Transceiver IC

Data Sheet **ADF7023-J**

FEATURES

- Ultralow power, high performance transceiver
- Frequency bands: 902 MHz to 958 MHz
- Data rates supported: 1 kbps to 300 kbps
- 2.2 V to 3.6 V power supply
- Single-ended and differential power amplifiers (PAs)
- Low IF receiver with programmable IF bandwidths
  - 100 kHz, 150 kHz, 200 kHz, 300 kHz
- Receiver sensitivity (BER)
  - −116 dBm at 1.0 kbps, 2FSK, GFSK
  - −107.5 dBm at 38.4 kbps, 2FSK, GFSK
  - −106.5 dBm at 50 kbps, 2FSK, GFSK
  - −105 dBm at 100 kbps, 2FSK, GFSK
  - −104 dBm at 150 kbps, GFSK, GMSK
  - −103 dBm at 200 kbps, GFSK, GMSK
  - −100.5 dBm at 300 kbps, GFSK, GMSK
- Very low power consumption
  - 12.8 mA in PHY_RX mode (maximum front-end gain)
  - 11.9 mA in PHY_RX mode (AGC off, ADC off)
  - 24.1 mA in PHY_TX mode (10 dBm output, single-ended PA)
  - 0.75 µA in PHY_SLEEP mode (32 kHz RC oscillator active)
  - 1.28 µA in PHY_SLEEP mode (32 kHz XTAL oscillator active)
  - 0.33 µA in PHY_SLEEP mode (Deep Sleep Mode 1)
- RF output power of −20 dBm to +13.5 dBm (single-ended PA)
- RF output power of −20 dBm to +10 dBm (differential PA)
- Patented fast settling automatic frequency control (AFC)
- Digital received signal strength indication (RSSI)
- Integrated PLL loop filter and Tx/Rx switch
- Fast automatic voltage controlled oscillator (VCO) calibration
- Automatic synthesizer bandwidth optimization
- On-chip, low power, custom 8-bit processor
  - Radio control
  - Packet management
  - Smart wake mode
- SPORT mode support
  - High speed synchronous serial interface to Tx and Rx Data for direct interfacing to processors and DSPs
- Packet management support
  - Highly flexible for a wide range of packet formats
  - Insertion/detection of preamble/sync word/CRC/address
  - Manchester and 8b/10b data encoding and decoding
  - Data whitening
- Smart wake mode
  - Current saving low power mode with autonomous receiver wake up, carrier sense, and packet reception
- Downloadable firmware modules
  - Image rejection calibration, fully automated (patent pending)
  - 128-bit AES encryption/decryption with hardware acceleration and key sizes of 128 bits, 192 bits, and 256 bits
  - Reed-Solomon error correction with hardware acceleration
- 240-byte packet buffer for Tx/Rx data
- Efficient SPI control interface with block read/write access
- Integrated battery alarm and temperature sensor
- Integrated RC and 32.768 kHz crystal oscillator
- On-chip, 8-bit ADC
- 5 mm × 5 mm, 32-lead, LFCSP package

APPLICATIONS

- Smart metering
- IEEE 802.15.4g
- Home automation
- Process and building control
- Wireless sensor networks (WSNs)
- Wireless healthcare

Rev. D
Document Feedback

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADF7023-J Evaluation Board

DOCUMENTATION

Application Notes

- AN-1276: Embedded Packet Error Rate Testing on the ADF7023 and ADF7023-J
- AN-1339: ADF7023-J AD_15d4g Firmware Download Module
- AN-1340: ADF7023-J IEEE 802.15.4g/UBUSAir/FAN Firmware Module
- AN-1394: AES Encryption and Decryption for the ADF7023 and ADF7023-J

Data Sheet

- ADF7023-J: High Performance, Low Power, ISM Band FSK/GFSK/MSK/GMSK Transceiver IC Data Sheet

Product Highlight

- ADuCM3027/ADuCM3029 Ultra Low Power Microcontrollers

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADF7023 Evaluation Board Software

TOOLS AND SIMULATIONS

- ADIsimSRD Design Studio

REFERENCE MATERIALS

Press

- Analog Devices and Renesas Wireless Communications Platform Achieves Wi-SUN Alliance Certification

Product Selection Guide

- Connectivity Solutions for the Internet of Things
- RF Source Booklet

Technical Articles

- Low Power, Low Cost, Wireless ECG Holter Monitor
- RF Meets Power Lines: Designing Intelligent Smart Grid Systems that Promote Energy Efficiency
- Smart Metering Technology Promotes Energy Efficiency for a Greener World
- Understand Wireless Short-Range Devices for Global License-Free Systems
- Wireless Short Range Devices and Narrowband Communications
- Wireless Technologies for Smart Meters: Focus on Water Metering

DESIGN RESOURCES

- ADF7023-J Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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View all ADF7023-J EngineerZone Discussions.

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FUNCTIONAL BLOCK DIAGRAM

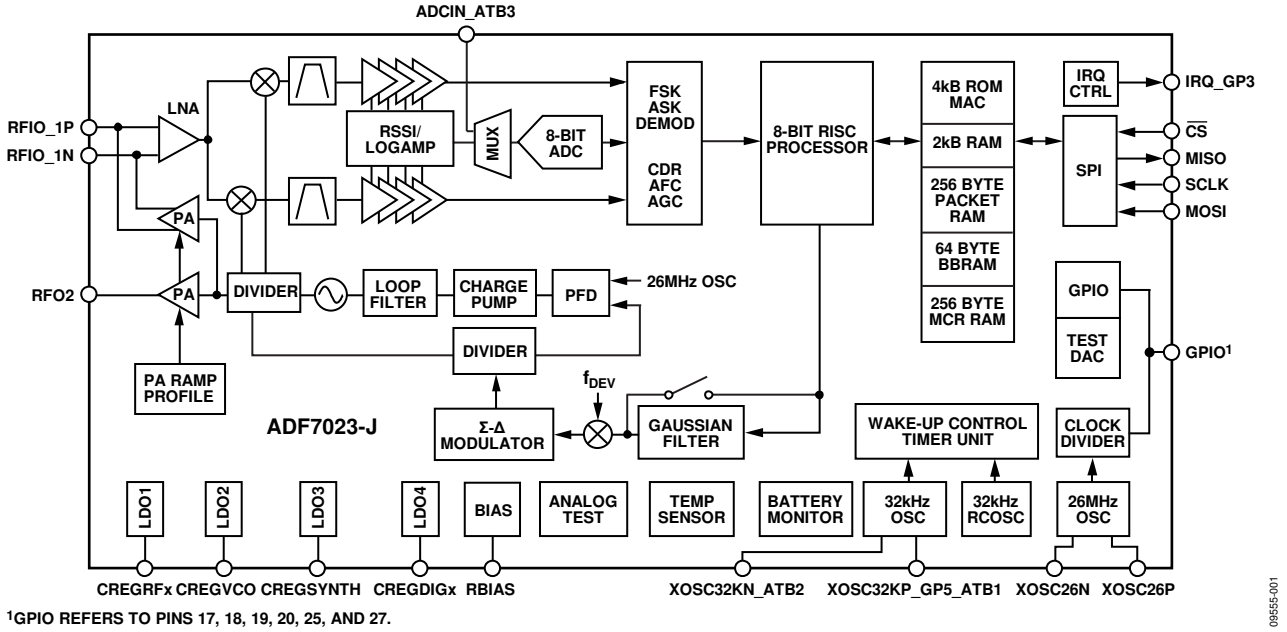

Figure 1.

GENERAL DESCRIPTION

The ADF7023-J is a very low power, high performance, highly integrated 2FSK/GFSK/MSK/GMSK transceiver designed for operation in the 902 MHz to 958 MHz frequency band, which covers the ARIB Standard T96 band at 950 MHz. Data rates from 1 kbps to 300 kbps are supported.

The transmit RF synthesizer contains a VCO and a low noise fractional-N phase locked loop (PLL) with an output channel frequency resolution of 400 Hz. The VCO operates at twice the fundamental frequency to reduce spurious emissions. The receive and transmit synthesizer bandwidths are automatically, and independently, configured to achieve optimum phase noise, modulation quality, and settling time. The transmitter output power is programmable from −20 dBm to +13.5 dBm, with automatic PA ramping to meet transient spurious specifications. The part possesses both single-ended and differential PAs, which allow for Tx antenna diversity.

The receiver is exceptionally linear, achieving an IP3 specification of −12.2 dBm and −11.5 dBm at maximum gain and minimum gain, respectively, and an IP2 specification of 18.5 dBm and 27 dBm at maximum gain and minimum gain, respectively. The receiver achieves an interference blocking specification of 66 dB at a ±2 MHz offset and 74 dB at a ±10 MHz offset. Thus, the part is extremely resilient to the presence of interferers in spectrally noisy environments. The receiver features a novel, high speed, AFC loop, allowing the PLL to find and correct any RF frequency errors in the recovered packet. A patent pending image rejection calibration scheme is available by downloading the image rejection calibration firmware module to program RAM. The algorithm does not require the use of an external RF source nor does it require any user intervention once initiated. The results of the calibration can be stored in nonvolatile memory for use on subsequent power-ups of the transceiver.

The ADF7023-J operates with a power supply range of 2.2 V to 3.6 V and has very low power consumption in both Tx and Rx modes, enabling long lifetimes in battery-operated systems while maintaining excellent RF performance. The device can enter a low power sleep mode in which the configuration settings are retained in the battery backup random access memory (BBRAM).

The ADF7023-J features an ultralow power, on-chip, communications processor. The communications processor, which is an 8-bit RISC processor, performs the radio control, packet management, and smart wake mode (SWM) functionality. The communications processor eases the processing burden of the companion processor by integrating the lower layers of a typical communication protocol stack. The communications processor also permits the download and execution of firmware modules. Available modules include image rejection (IR) calibration, advanced encryption standard (AES) encryption, and Reed-Solomon coding. These firmware modules are available online at ftp://ftp.analog.com/pub/RFL/FirmwareModules.

The communications processor provides a simple command-based radio control interface for the host processor. A single-byte command transitions the radio between states or performs a radio function.

The communications processor provides support for generic packet formats. The packet format is highly flexible and fully programmable, thereby ensuring its compatibility with proprietary packet profiles. In transmit mode, the communications processor can be configured to add preamble, sync word, and CRC to the payload data stored in packet RAM. In receive mode, the

communications processor can detect and interrupt the host processor on reception of preamble, sync word, address, and CRC and store the received payload to packet RAM. The ADF7023-J uses an efficient interrupt system comprising MAC level interrupts and PHY level interrupts that can be individually set. The payload data plus the 16-bit CRC can be encoded/decoded using Manchester or 8b/10b encoding. Alternatively, data whitening and dewhitening can be applied.

The SWM allows the ADF7023-J to wake up autonomously from sleep using the internal wake-up timer without intervention from the host processor. After wake-up, the ADF7023-J is controlled by the communications processor. This functionality allows carrier sense, packet sniffing, and packet reception while the host processor is in sleep, thereby reducing overall system current consumption. The smart wake mode can wake the host processor on an interrupt condition. These interrupt conditions can be configured to include the reception of valid preamble, sync word, CRC, or address match. Wake-up from sleep mode can also be triggered by the host processor. For systems requiring very accurate wake-up timing, a 32 kHz oscillator can be used to drive the wake-up timer. Alternatively, the internal RC oscillator can be used, which gives lower current consumption in sleep.

The ADF7023-J features an AES engine with hardware acceleration that provides 128-bit block encryption and decryption with key sizes of 128 bits, 192 bits, and 256 bits. Both electronic code book (ECB) and Cipher Block Chaining Mode 1 (CBC Mode 1) are supported. The AES engine can be used to encrypt/decrypt packet data and can be used as a stand-alone engine for encryption/decryption by the host processor. The AES engine is enabled on the ADF7023-J by downloading the AES firmware module to program RAM.

An on-chip, 8-bit ADC provides readback of an external analog input, the RSSI signal, or an integrated temperature sensor. An integrated battery voltage monitor raises an interrupt flag to the host processor whenever the battery voltage drops below a user-defined threshold.

SPECIFICATIONS

V_{DD} = VDDBAT1 = VDDBAT2 = 2.2 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V and T_A = 25°C.

RF AND SYNTHESIZER SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF CHARACTERISTICS					
Frequency Range	902		958	MHz	
PHASE-LOCKED LOOP					
Channel Frequency Resolution		396.7		Hz	
Phase Noise at Offset of					PA output power = 10 dBm, RF frequency = 950 MHz
600 kHz		−116.3		dBc/Hz	130 kHz closed-loop bandwidth[1]
800 kHz		−119.4		dBc/Hz	130 kHz closed-loop bandwidth
600 kHz		−113.8		dBc/Hz	223 kHz closed-loop bandwidth[2]
800 kHz		−117.2		dBc/Hz	223 kHz closed-loop bandwidth
1 MHz		−126		dBc/Hz	
2 MHz		−131		dBc/Hz	
10 MHz		−142		dBc/Hz	
VCO Calibration Time		142		µs	
Synthesizer Settling Time		56		µs	Frequency synthesizer settles to within ±5 ppm of the target frequency within this time following the VCO calibration, transmit, and receive, 2FSK/GFSK/MSK/GMSK
Integer Boundary Spurious[3]					N = 35 or 36
(26 MHz × N) + 0.1 MHz		−39		dBc	Using 130 kHz synthesizer bandwidth, integer boundary spur at 910 MHz (26 MHz × 35), inside synthesizer loop bandwidth
(26 MHz × N) + 1.0 MHz		−79		dBc	Using 130 kHz synthesizer bandwidth, integer boundary spur at 910 MHz (26 MHz × 35), outside synthesizer loop bandwidth
CRYSTAL OSCILLATOR					
Crystal Frequency		26		MHz	Parallel load resonant crystal
Recommended Load Capacitance	7		18	pF	
Maximum Crystal ESR		1800		Ω	26 MHz crystal with 18 pF load capacitance
Pin Capacitance		2.1		pF	Capacitance for XOSC26P and XOSC26N
Start-Up Time		310		µs	26 MHz crystal with 7 pF load capacitance
		388		µs	26 MHz crystal with 18 pF load capacitance

[1] 130 kHz closed-loop bandwidth recommended for T96/15.4 *g*, 50 kbps and 100 kbps data rates (see Table 31).
[2] 223 kHz closed-loop bandwidth recommended for T96/15.4 *g*, 200 kbps data rate (see Table 31).
[3] As the 26 MHz XTAL is fixed, integer boundary spurs occur at 910 MHz and 936 MHz (N = 35 and N = 36).

TRANSMITTER SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DATA RATE					
2FSK/GFSK/MSK/GMSK	1		300	kbps	
Data Rate Resolution		100		bps	
MODULATION ERROR RATIO (MER)[1]					RF frequency = 957.2 MHz, GFSK
10 kbps to 49.5 kbps		25.4		dB	Modulation index = 1
49.6 kbps to 129.5 kbps		25.3		dB	Modulation index = 1
129.6 kbps to 179.1 kbps		23.9		dB	Modulation index = 0.5
179.2 kbps to 239.9 kbps		23.3		dB	Modulation index = 0.5
240 kbps to 300 kbps		23		dB	Modulation index = 0.5
MODULATION ERROR RATIO 15.4 *g* DATA RATES					With T96 look-up table (LUT)[2]
50 kbps		25.4		dB	Modulation index = 1
100 kbps		28.9		dB	Modulation index = 1
200 kbps		25.9		dB	Modulation index = 1
100 kbps		24.3		dB	Modulation index = 0.5
MODULATION					
2FSK/GFSK/MSK/GMSK Frequency Deviation	0.1		409.5	kHz	
Deviation Frequency Resolution		100		Hz	
Gaussian Filter Bandwidth-Time (BT) Product		0.5			
SINGLE-ENDED PA					
Maximum Power[3]		13.5		dBm	Programmable, separate PA and LNA match[4]
Minimum Power		−20		dBm	
Transmit Power Variation vs. Temperature		±0.5		dB	From −40°C to +85°C, RF frequency = 958.0 MHz
Transmit Power Variation vs. V_{DD}		±1		dB	From 2.2 V to 3.6 V, RF frequency = 958.0 MHz
Transmit Power Flatness		±1		dB	From 902 MHz to 928 MHz and 950 MHz to 958 MHz
Programmable Step Size					
−20 dBm to +13.5 dBm		0.5		dB	Programmable in 63 steps
DIFFERENTIAL PA					
Maximum Power[3]		10		dBm	Programmable
Minimum Power		−20		dBm	
Transmit Power Variation vs. Temperature		±1		dB	From −40°C to +85°C, RF frequency = 958.0 MHz
Transmit Power Variation vs. V_{DD}		±2		dB	From 2.2 V to 3.6 V, RF frequency = 958.0 MHz
Transmit Power Flatness		±1		dB	From 902 MHz to 928 MHz and 950 MHz to 958 MHz
Programmable Step Size					
−20 dBm to +10 dBm		0.5		dB	Programmable in 63 steps

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPURIOUS EMISSIONS					Measured as per TELEC T-245 for T96 compliance, 950 MHz to 958 MHz band, single-ended PA with combined output. For spurious emissions compliance in the 1.8845 GHz to 1.9196 GHz frequency band, a seventh-order PA harmonic filter is used. This has an insertion loss of up to 1.5 dB.
30 MHz to 710 MHz		−65		dBm/100 kHz	
710 MHz to 945 MHz		−63		dBm/1 MHz	
945 MHz to 950 MHz		−66		dBm/100 kHz	
958 MHz to 960 MHz		−60.7		dBm/100 kHz	DR = 100 kbps, MI = 1, n = 2, f_C = 957.3 MHz
960 MHz to 1 GHz		−64		dBm/100 kHz	
1 GHz to 1.215 GHz		−72		dBm/1 MHz	
1.215 GHz to 1.8845 GHz		−76		dBm/1 MHz	
1.8845 GHz to 1.9196 GHz[5]		−69		dBm/1 MHz	
1.9196 GHz to 3 GHz		−66		dBm/1 MHz	
3 GHz to 5 GHz		−69		dBm/1 MHz	
OPTIMUM PA LOAD IMPEDANCE					
Single-Ended PA in Transmit Mode					
f_{RF} = 915 MHz		50.8 + j10.2		Ω	
f_{RF} = 954MHz		38.5 + j5.9		Ω	
Single-Ended PA in Receive Mode					PA Impedance in Rx mode
f_{RF} = 915 MHz		9.4 − j124		Ω	
f_{RF} = 954 MHz		8.8 − j118.5		Ω	
Differential PA in Transmit Mode					Load impedance between RFIO_1P and RFIO_1N to ensure maximum output power
f_{RF} = 915 MHz		20.5 + j36.4		Ω	
f_{RF} = 954 MHz		28.1 + j17.3		Ω	

[1] MER is a measure of signal to noise ratio at optimal eye sampling point.
[2] Optimized PLL bandwidth settings vs. data rate defined in Table 31.
[3] Measured as the maximum unmodulated power.
[4] A combined single-ended PA and LNA match can reduce the maximum achievable output power by up to 1 dB.
[5] This includes the second harmonic.

RECEIVER SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
2FSK/MSK INPUT SENSITIVITY, BIT ERROR RATE (BER)					At BER = 1E − 3, RF frequency = 915 MHz, LNA and PA matched separately[1]
1.0 kbps		−116		dBm	Frequency deviation = 4.8 kHz, IF filter bandwidth = 100 kHz
10 kbps		−111		dBm	Frequency deviation = 9.6 kHz, IF filter bandwidth = 100 kHz
38.4 kbps		−107.5		dBm	Frequency deviation = 20 kHz, IF filter bandwidth = 100 kHz
50 kbps		−106.5		dBm	Frequency deviation = 12.5 kHz, IF filter bandwidth = 100 kHz
100 kbps		−105		dBm	Frequency deviation = 25 kHz, IF filter bandwidth = 100 kHz
150 kbps		−104		dBm	Frequency deviation = 37.5 kHz, IF filter bandwidth = 150 kHz
200 kbps		−103		dBm	Frequency deviation = 50 kHz, IF filter bandwidth = 200 kHz
300 kbps		−100.5		dBm	Frequency deviation = 75 kHz, IF filter bandwidth = 300 kHz
GFSK/GMSK INPUT SENSITIVITY, BER					At BER = 1E − 3, RF frequency = 954 MHz, LNA and PA matched separately[1]
50 kbps		−107.4		dBm	Frequency deviation = 25 kHz, IF filter bandwidth = 100 kHz
100 kbps		−105		dBm	Frequency deviation = 50 kHz, IF filter bandwidth = 100 kHz
100 kbps		−106		dBm	Frequency deviation = 40 kHz, IF filter bandwidth = 100 kHz
200 kbps		−102		dBm	Frequency deviation = 100 kHz, IF filter bandwidth = 200 kHz
200 kbps		−103.3		dBm	Frequency deviation = 80 kHz, IF filter bandwidth = 200 kHz
2FSK/MSK INPUT SENSITIVITY, PACKET ERROR RATE (PER)					At PER = 1%, RF frequency = 915 MHz, LNA and PA matched separately,[1] packet length = 128 bits, packet mode
1.0 kbps		−115.5		dBm	Frequency deviation = 4.8 kHz, IF filter bandwidth = 100 kHz
9.6 kbps		−110.6		dBm	Frequency deviation = 9.6 kHz, IF filter bandwidth = 100 kHz
38.4 kbps		−106		dBm	Frequency deviation = 20 kHz, IF filter bandwidth = 100 kHz
50 kbps		−104.3		dBm	Frequency deviation = 12.5 kHz, IF filter bandwidth = 100 kHz
100 kbps		−102.6		dBm	Frequency deviation = 25 kHz, IF filter bandwidth = 100 kHz
150 kbps		−101		dBm	Frequency deviation = 37.5 kHz, IF filter bandwidth = 150 kHz
200 kbps		−99.1		dBm	Frequency deviation = 50 kHz, IF filter bandwidth = 200 kHz
300 kbps		−97.9		dBm	Frequency deviation = 75 kHz, IF filter bandwidth = 300 kHz

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
GFSK/GMSK INPUT SENSITIVITY, PER					At PER = 1%, RF frequency = 954 MHz, LNA and PA matched separately, packet length = 20 octets, packet mode
50 kbps		−104.1		dBm	Frequency deviation = 25 kHz, IF filter bandwidth = 100 kHz
100 kbps		−101.1		dBm	Frequency deviation = 50 kHz, IF filter bandwidth = 100 kHz
100 kbps		−102.2		dBm	Frequency deviation = 40 kHz, IF filter bandwidth = 100 kHz
200 kbps		−98.5		dBm	Frequency deviation = 100 kHz, IF filter bandwidth = 200 kHz
200 kbps		−99.5		dBm	Frequency deviation = 80 kHz, IF filter bandwidth = 200 kHz
LNA AND MIXER, INPUT IP3					Receiver LO frequency (f_{LO}) = 914.8 MHz, $f_{SOURCE1} = f_{LO} + 0.4$ MHz, $f_{SOURCE2} = f_{LO} + 0.7$ MHz
Minimum LNA Gain		−11.5		dBm	
Maximum LNA Gain		−12.2		dBm	
LNA AND MIXER, INPUT IP2					Receiver LO frequency (f_{LO}) = 920.8 MHz, $f_{SOURCE1} = f_{LO} + 1.1$ MHz, $f_{SOURCE2} = f_{LO} + 1.3$ MHz
Maximum LNA Gain, Maximum Mixer Gain		18.5		dBm	
Minimum LNA Gain, Minimum Mixer Gain		27		dBm	
LNA AND MIXER, 1 dB COMPRESSION POINT					RF frequency = 915 MHz
Maximum LNA Gain, Maximum Mixer Gain		−21.9		dBm	
Minimum LNA Gain, Minimum Mixer Gain		−21		dBm	
ADJACENT CHANNEL REJECTION					
CW Interferer					Desired signal at −87 dBm, CW interferer power level increased until BER = 62^{-6}, image calibrated
±200 kHz Offset		38		dB	IF BW = 100 kHz, wanted signal: f_{DEV} = 25 kHz, DR = 50 kbps
+400 kHz Offset		51		dB	
−400 kHz Offset		33/39		dB	Uncalibrated/internal calibration; using an IF of 200 kHz, −400 kHz is the image frequency
CO-CHANNEL REJECTION		−6		dB	Desired signal at −87 dBm, data rate = 50 kbps, frequency deviation = 25 kHz, RF frequency = 954 MHz
BLOCKING					
RF Frequency = 954 MHz					Desired signal 3 dB above the input sensitivity level, data rate = 50 kbps, CW interferer power level increased until BER = 10^{-3} (see the Typical Performance Characteristics section for blocking at other offsets and IF bandwidths), image calibrated
±2 MHz		65		dB	
±10 MHz		72		dB	
±60 MHz		76		dB	
IMAGE CHANNEL ATTENUATION					Measured as image attenuation at the IF filter output, carrier wave interferer at 400 kHz below the channel frequency, 100 kHz IF filter bandwidth
954 MHz		36/43.8		dB	Uncalibrated/calibrated

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
AFC					
Accuracy		1		kHz	
Maximum Pull-In Range					Achievable pull-in range dependent on discriminator bandwidth and modulation
300 kHz IF Filter Bandwidth		±150		kHz	
200 kHz IF Filter Bandwidth		±100		kHz	
150 kHz IF Filter Bandwidth		±75		kHz	
100 kHz IF Filter Bandwidth		±50		kHz	
PREAMBLE LENGTH					Minimum number of preamble bits to ensure the minimum PER across the full input power range (see Table 41)
AFC Off, AGC Lock on Sync Word Detection					Sync word length 24 bits
38.4 kbps		8		Bits	Sync word tolerance = 0
300 kbps		24		Bits	Sync word tolerance = 1
AFC On, AFC and AGC Lock on Preamble Detection					
9.6 kbps		46		Bits	
38.4 kbps		44		Bits	
50 kbps		50		Bits	
100 kbps		52		Bits	
150 kbps		54		Bits	
200 kbps		58		Bits	
300 kbps		64		Bits	
AFC On, AFC and AGC Lock on Sync Word Detection					Sync word length 24 bits
38.4 kbps		14		Bits	Sync word tolerance = 0
300 kbps		32		Bits	Sync word tolerance = 1
RSSI					
Range at Input		−97 to −26		dBm	
Linearity		±2		dB	
Absolute Accuracy		±3		dB	
SATURATION (MAXIMUM INPUT LEVEL)					
2FSK/GFSK/MSK/GMSK		12		dBm	
LNA INPUT IMPEDANCE					
Receive Mode					
f_{RF} = 915 MHz		75.9 – j32.3		Ω	
f_{RF} = 954 MHz		74.6 – j32.5		Ω	
Transmit Mode					
f_{RF} = 915 MHz		7.7 + j8.6		Ω	
f_{RF} = 954 MHz		7.7 + j8.9		Ω	
Rx SPURIOUS EMISSIONS[2]					
Maximum < 1 GHz		−66		dBm	At antenna input, unfiltered conductive
Maximum > 1 GHz		−62		dBm	At antenna input, unfiltered conductive

[1] Sensitivity for combined matching network case is typically 1 dB less than separate matching networks.
[2] Follow the matching and layout guidelines to achieve the relevant ARIB-T96/TELEC T-245 specifications.

TIMING AND DIGITAL SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Rx AND Tx TIMING PARAMETERS					See the State Transition and Command Timing section for more details
PHY_ON to PHY_RX (on CMD_PHY_RX)		300		µs	Includes VCO calibration and synthesizer settling
PHY_ON to PHY_TX (on CMD_PHY_TX)		296		µs	Includes VCO calibration and synthesizer settling, does not include PA ramp-up
LOGIC INPUTS					
Input High Voltage, V_{INH}	$0.7 \times V_{DD}$			V	
Input Low Voltage, V_{INL}			$0.2 \times V_{DD}$	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	$V_{DD} - 0.4$			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
GPIO Rise/Fall			5	ns	
GPIO Load			10	pF	
Maximum Output Current		5		mA	
ATB OUTPUTS					Used for external PA and LNA control
ADCIN_ATB3 and ATB4					
Output High Voltage, V_{OH}		1.8		V	
Output Low Voltage, V_{OL}		0.1		V	
Maximum Output Current		0.5		mA	
XOSC32KP_GP5_ATB1 and XOSC32KN_ATB2					
Output High Voltage, V_{OH}		V_{DD}		V	
Output Low Voltage, V_{OL}		0.1		V	
Maximum Output Current		5		mA	

AUXILARY BLOCK SPECIFICATIONS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
32 kHz RC OSCILLATOR					
Frequency		32.768		kHz	After calibration
Frequency Accuracy		1.5		%	After calibration at 25°C
Frequency Drift					
Temperature Coefficient		0.14		%/°C	
Voltage Coefficient		4		%/V	
Calibration Time		1.25		ms	
32 kHz XTAL OSCILLATOR					
Frequency		32.768		kHz	
Start-Up Time		630		ms	32.768 kHz crystal with 7 pF load capacitance
WAKE UP CONTROLLER (WUC)					
Hardware Timer					
Wake-Up Period	61×10^{-6}		1.31×10^{5}	sec	
Firmware Timer					
Wake-Up Period	1		2^{16}	Hardware periods	Firmware counter counts of the number of hardware wake-ups, resolution of 16 bits
ADC					Maximum input voltage at ADCIN_ATB3 is 1.8 V
Resolution		8		Bits	
DNL		±1		LSB	V_{DD} from 2.2 V to 3.6 V, T_A = 25°C
INL		±1		LSB	V_{DD} from 2.2 V to 3.6 V, T_A = 25°C
Conversion Time		1		µs	
Input Capacitance		12.4		pF	
BATTERY MONITOR					
Absolute Accuracy		±45		mV	
Alarm Voltage Setpoint	1.7		2.7	V	
Alarm Voltage Step Size		62		mV	5-bit resolution
Start-Up Time			100	µs	
Current Consumption		30		µA	When enabled
TEMPERATURE SENSOR					
Range	−40		+85	°C	
Resolution		0.3		°C	With averaging
Accuracy of Temperature Readback		+7/−4		°C	Overtemperature range −40°C to +85°C (calibrated at +25°C)
		±4		°C	Overtemperature range −36°C to +84°C (calibrated at +25°C)
		±3		°C	Overtemperature range −12°C to +79°C (calibrated at +25°C)

GENERAL SPECIFICATIONS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE RANGE, T_A	−40		+85	°C	
VOLTAGE SUPPLY					
V_{DD}	2.2		3.6	V	Applied to VDDBAT1 and VDDBAT2
TRANSMIT CURRENT CONSUMPTION					In the PHY_TX state, single-ended PA matched to 50 Ω, differential PA matched to 100 Ω, separate single-ended PA and LNA match, combined differential PA and LNA match
Single-Ended PA, 915 MHz					
−10 dBm		10.3		mA	
0 dBm		13.3		mA	
10 dBm		24.1		mA	
13.5 dBm		32.1		mA	
Differential PA, 915 MHz					
−10 dBm		9.3		mA	
0 dBm		12		mA	
5 dBm		16.7		mA	
10 dBm		28		mA	
POWER MODES					
PHY_SLEEP (Deep Sleep Mode 2)		0.18		µA	Sleep mode, wake-up configuration values (BBRAM) not retained
PHY_SLEEP (Deep Sleep Mode 1)		0.33		µA	Sleep mode, wake-up configuration values (BBRAM) retained
PHY_SLEEP (RCO Wake Mode)		0.75		µA	WUC active, RC oscillator running, wake-up configuration values retained (BBRAM)
PHY_SLEEP (XTO Wake Mode)		1.28		µA	WUC active, 32 kHz crystal running, wake-up configuration values retained (BBRAM)
PHY_OFF		1		mA	Device in PHY_OFF state, 26 MHz oscillator running, digital and synthesizer regulators active, all register values retained
PHY_ON		1		mA	Device in PHY_ON state, 26 MHz oscillator running, digital, synthesizer, VCO, and RF regulators active, baseband filter calibration performed, all register values retained
PHY_RX (ADC, AGC Off)		11.9		mA	Device in PHY_Rx state, ADC off, manual AGC gain
PHY_RX (ADC, AGC On)		12.8		mA	Device in PHY_RX state
SMART WAKE MODE					Average current consumption
		21.78		µA	Autonomous reception every 1 sec, with receive dwell time of 1.25 ms, using RC oscillator, data rate = 38.4 kbps
		11.75		µA	Autonomous reception every 1 sec, with receive dwell time of 0.5 ms, using RC oscillator, data rate = 300 kbps

TIMING SPECIFICATIONS

V_{DD} = VDDBAT1 = VDDBAT2 = 2.2 V to 3.6 V, V_{GND} = GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 7. SPI Interface Timing

Parameter	Limit	Unit	Test Conditions/Comments
t_2	85	ns min	$\overline{CS}$ low to SCLK setup time
t_3	85	ns min	SCLK high time
t_4	85	ns min	SCLK low time
t_5	170	ns min	SCLK period
t_6	10	ns max	SCLK falling edge to MISO delay
t_7	5	ns min	MOSI to SCLK rising edge setup time
t_8	5	ns min	MOSI to SCLK rising edge hold time
t_9	85	ns min	SCLK falling edge to $\overline{CS}$ hold time
t_{11}	270	ns min	$\overline{CS}$ high time
t_{12}	310	µs typ	$\overline{CS}$ low to MISO high wake-up time, 26 MHz crystal with 7 pF load capacitance, T_A = 25°C
t_{13}	20	ns max	SCLK rise time
t_{14}	20	ns max	SCLK fall time
t_{15}	25	µs max	Communications processor initialization time. Do not issue a command during this time. Alternatively, poll status word and wait for the CMD_READY bit to go high.

Timing Diagrams

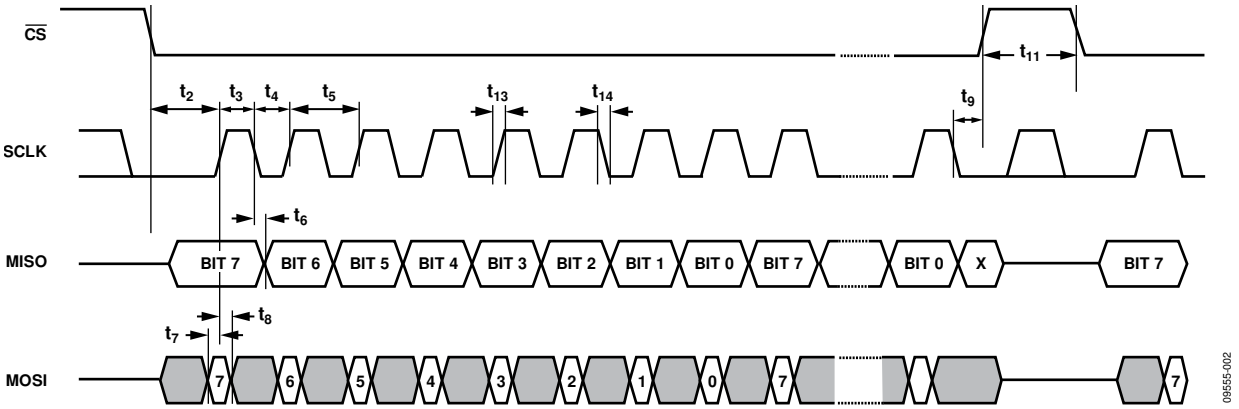

Figure 2. SPI Interface Timing

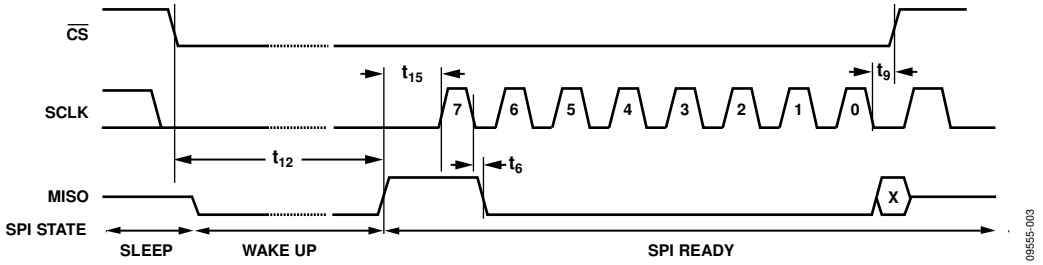

Figure 3. PHY_SLEEP to SPI Ready State Timing (SPI Ready T12 After Falling Edge of $\overline{CS}$)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Connect the exposed paddle of the LFCSP package to ground.

Table 8.

Parameter	Rating
VDDBAT1, VDDBAT2 to GND	−0.3 V to +3.96 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device is a high performance, RF integrated circuit with an ESD rating of <2 kV; it is ESD sensitive. Take proper precautions for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

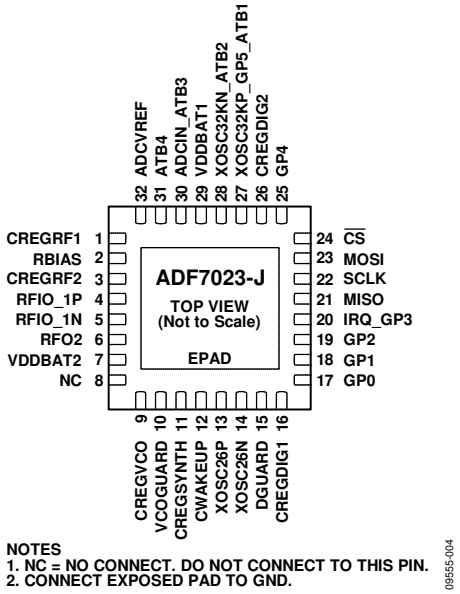

Figure 4. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CREGRF1	Regulator Voltage for RF. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
2	RBIAS	External Bias Resistor. A 36 kΩ resistor with 2% tolerance should be used.
3	CREGRF2	Regulator Voltage for RF. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
4	RFIO_1P	LNA Positive Input in Receive Mode. PA positive output in transmit mode with differential PA.
5	RFIO_1N	LNA Negative Input in Receive Mode. PA negative output in transmit mode with differential PA.
6	RFO2	Single-Ended PA Output.
7	VDDBAT2	Power Supply Pin Two. Decoupling capacitors to the ground plane should be placed as close as possible to this pin.
8	NC	No Connect.
9	CREGVCO	Regulator Voltage for the VCO. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
10	VCOGUARD	Guard/Screen for VCO. This pin should be connected to Pin 9.
11	CREGSYNTH	Regulator Voltage for the Synthesizer. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
12	CWAKEUP	External Capacitor for Wake-Up Control. A 150 nF capacitor should be placed between this pin and ground.
13	XOSC26P	The 26 MHz reference crystal should be connected between this pin and XOSC26N. If an external reference is connected to XOSC26N, this pin should be left open circuited.
14	XOSC26N	The 26 MHz reference crystal should be connected between this pin and XOSC26P. Alternatively, an external 26 MHz reference signal can be ac-coupled to this pin.
15	DGUARD	Internal Guard/Screen for the Digital Circuitry. A 220 nF capacitor should be placed between this pin and ground.
16	CREGDIG1	Regulator Voltage for Digital Section of the Chip. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection. This can be achieved by shorting it to Pin 15 and sharing the capacitor to ground.
17	GP0	Digital GPIO Pin 0.
18	GP1	Digital GPIO Pin 1.
19	GP2	Digital GPIO Pin 2.
20	IRQ_GP3	Interrupt Request, Digital GPIO Test Pin 3. An RC filter should be placed between this pin and the host processor. Recommended values are R = 1.1 kΩ and C = 1.5 nF.

Pin No.	Mnemonic	Description
21	MISO	Serial Port Master In/Slave Out.
22	SCLK	Serial Port Clock.
23	MOSI	Serial Port Master Out/Slave In.
24	$\overline{CS}$	Chip Select (Active Low). A pull-up resistor of 100 kΩ to V_{DD} is recommended to prevent the host processor from inadvertently waking the ADF7023-J from sleep.
25	GP4	Digital GPIO Test Pin 4.
26	CREGDIG2	Regulator Voltage for Digital Section of the Chip. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
27	XOSC32KP_GP5_ATB1	Digital GPIO Test Pin 5. A 32 kHz watch crystal can be connected between this pin and XOSC32KN_ATB2. Analog Test Pin 1.
28	XOSC32KN_ATB2	A 32 kHz watch crystal can be connected between this pin and XOSC32KP_GP5_ATB1. Analog Test Pin 2.
29	VDDBAT1	Digital Power Supply Pin One. Decoupling capacitors to the ground plane should be placed as close as possible to this pin.
30	ADCIN_ATB3	Analog-to-Digital Converter Input. Can be configured as an external PA enable signal. Analog Test Pin 3.
31	ATB4	Analog Test Pin 4. Can be configured as an external LNA enable signal.
32	ADCVREF	ADC Reference Output. A 220 nF capacitor should be placed between this pin and ground for adequate noise rejection.
	EPAD	The exposed package paddle must be connected to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

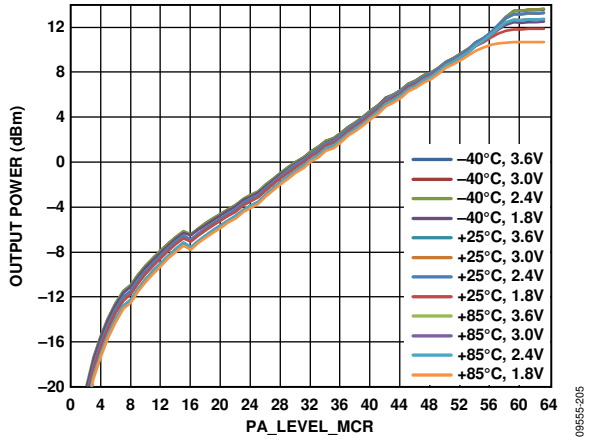

Figure 5. Single-Ended PA at 915 MHz: Output Power vs. PA_LEVEL_MCR Setting, Temperature, and V_{DD} (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

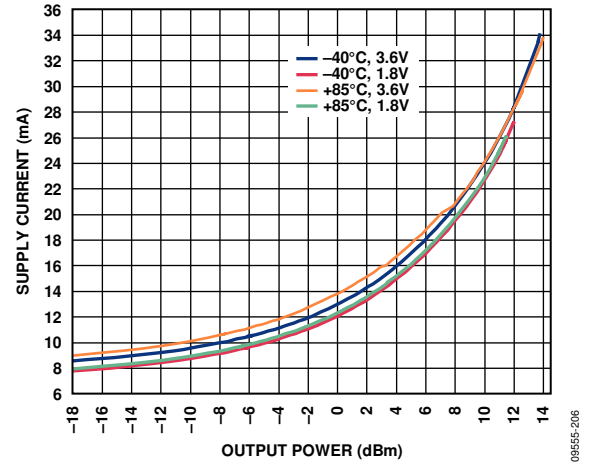

Figure 6. Single-Ended PA at 915 MHz: Supply Current vs. Output Power, Temperature, and V_{DD} (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

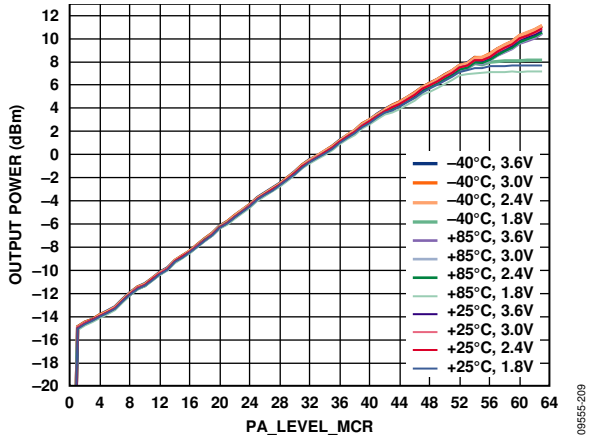

Figure 7. Differential PA at 915 MHz: Output Power vs. PA_LEVEL_MCR Setting, Temperature, and V_{DD} (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

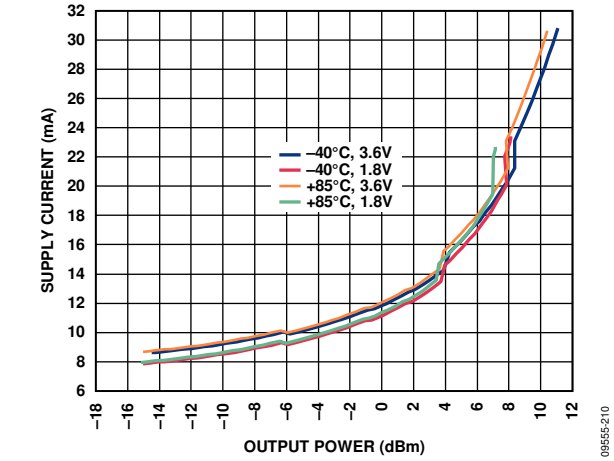

Figure 8. Differential PA at 915 MHz: Supply Current vs. Output Power, Temperature, and V_{DD} (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

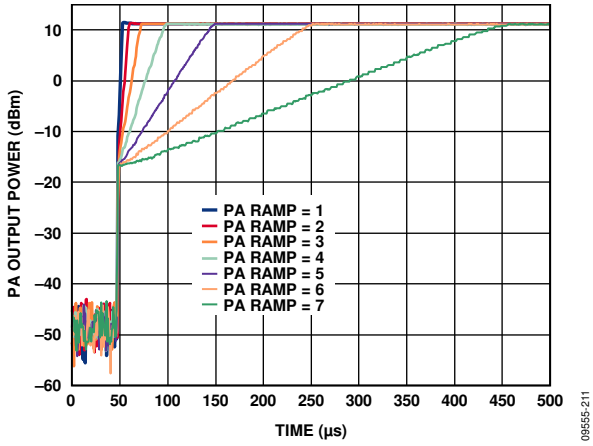

Figure 9. PA Ramp-Up at Data Rate = 38.4 kbps for Each PA_RAMP Setting, Differential PA

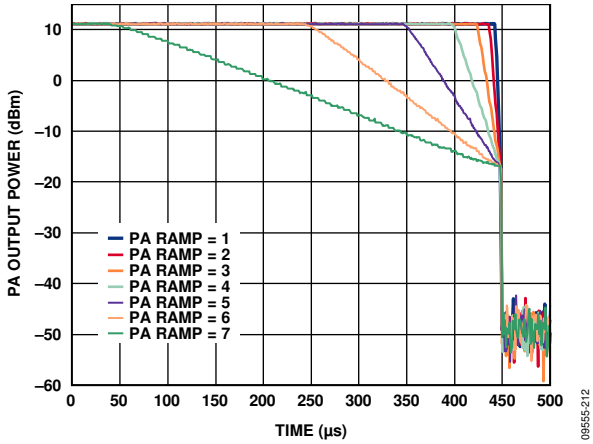

Figure 10. PA Ramp-Down at Data Rate = 38.4 kbps for Each PA_RAMP Setting, Differential PA

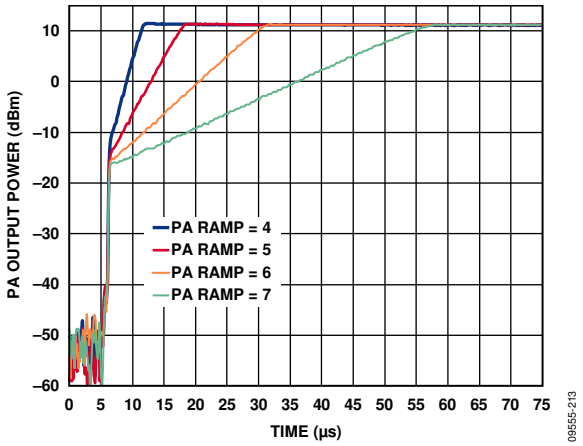

Figure 11. PA Ramp-Up at Data Rate = 300 kbps for Each PA_RAMP Setting, Differential PA

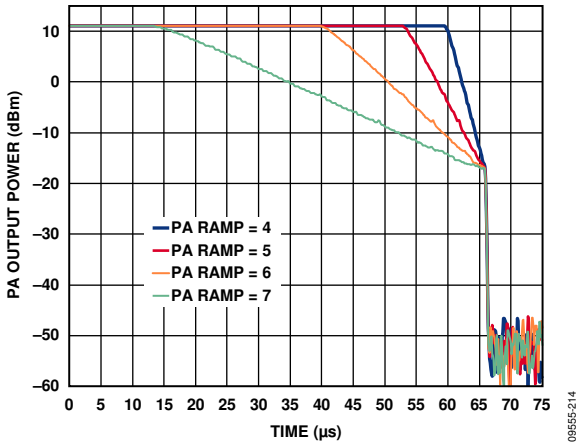

Figure 12. PA Ramp-Down at Data Rate = 300 kbps for Each PA_RAMP Setting, Differential PA

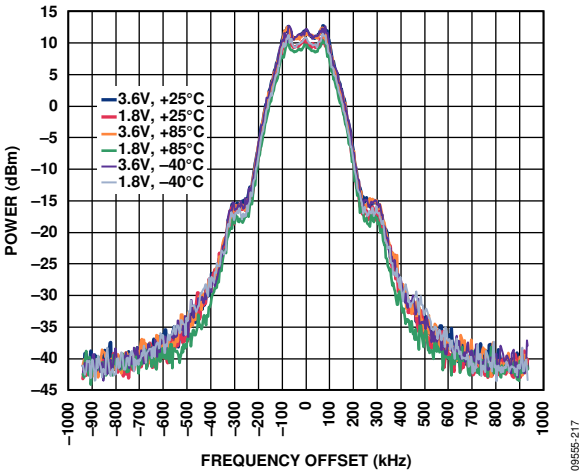

Figure 13. Transmit Spectrum at 928 MHz, GFSK, Data Rate = 300 kbps, Frequency Deviation = 75 kHz (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

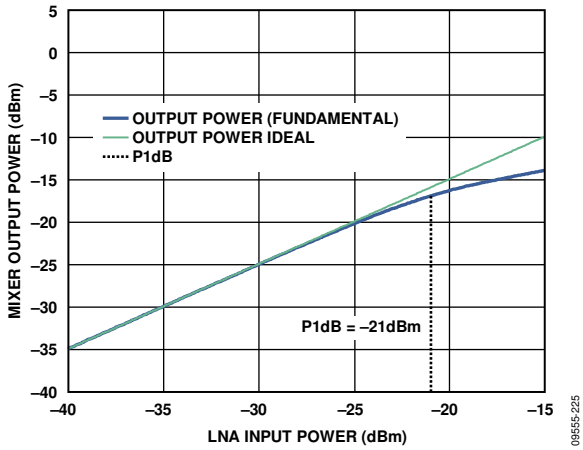

Figure 14. LNA/Mixer 1 dB Compression Point, V_{DD} = 3.0 V, Temperature = 25°C, RF Frequency = 915 MHz, LNA Gain = Low, Mixer Gain = Low

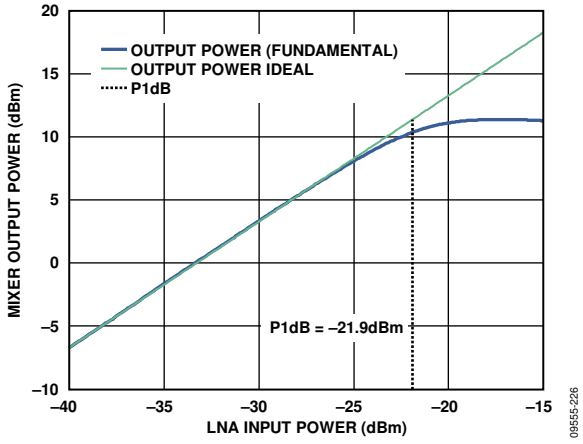

Figure 15. LNA/Mixer 1 dB Compression Point, V_{DD} = 3.0 V, Temperature = 25°C, RF Frequency = 915 MHz, LNA Gain = High, Mixer Gain = High

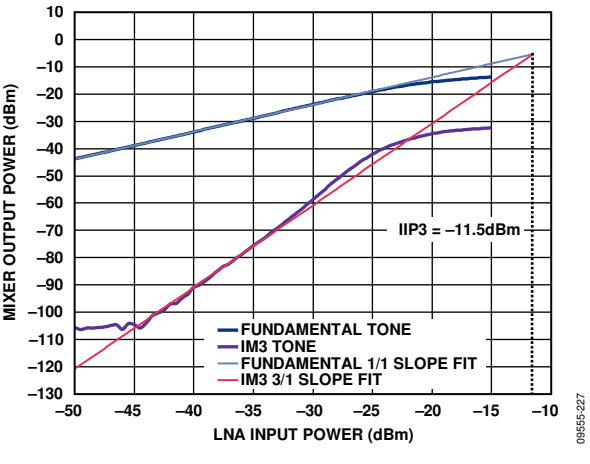

Figure 16. LNA/Mixer IIP3, V_{DD} = 3.0 V, Temperature = 25°C, RF Frequency = 915 MHz, LNA Gain = Low, Mixer Gain = Low, Source 1 Frequency = (915 + 0.4) MHz, Source 2 Frequency = (915+ 0.7) MHz

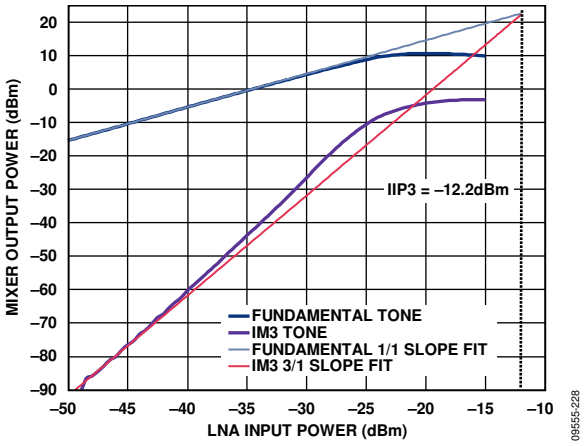

Figure 17. LNA/Mixer IIP3, V_{DD} = 3.0 V, Temperature = 25°C, RF Frequency = 915 MHz, LNA Gain = High, Mixer Gain = High, Source 1 Frequency = (915 + 0.4) MHz, Source 2 Frequency = (915+ 0.7) MHz

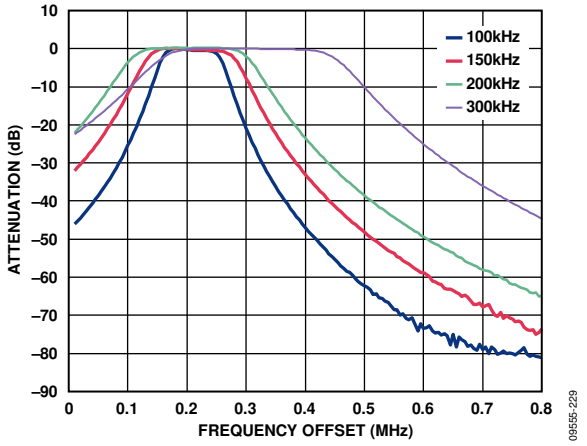

Figure 18. IF Filter Profile vs. IF Bandwidth, V_{DD} = 3.0 V, Temperature = 25°C

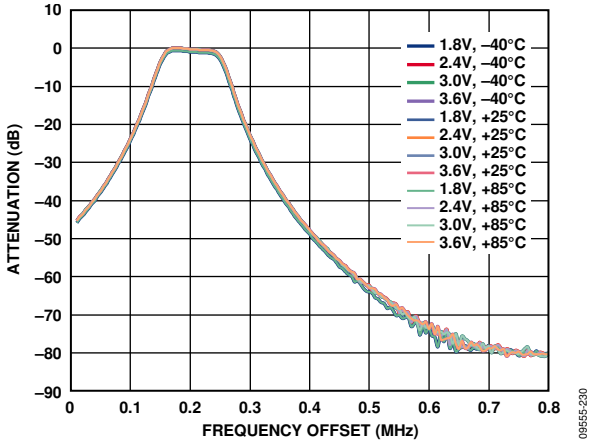

Figure 19. IF Filter Profile vs. V_{DD} and Temperature, 100 kHz IF Filter Bandwidth (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

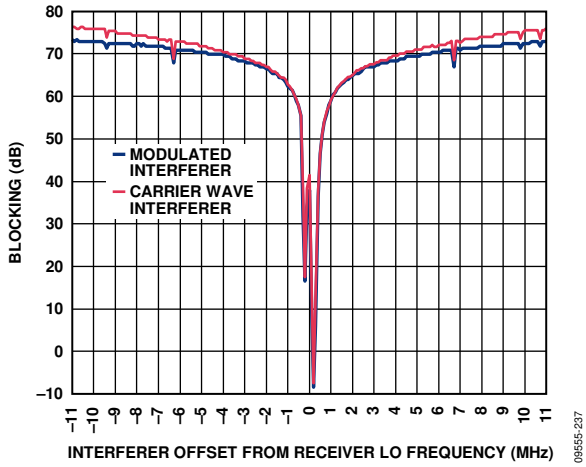

Figure 20. Receiver Wideband Blocking at 915 MHz, Data Rate = 38.4 kbps

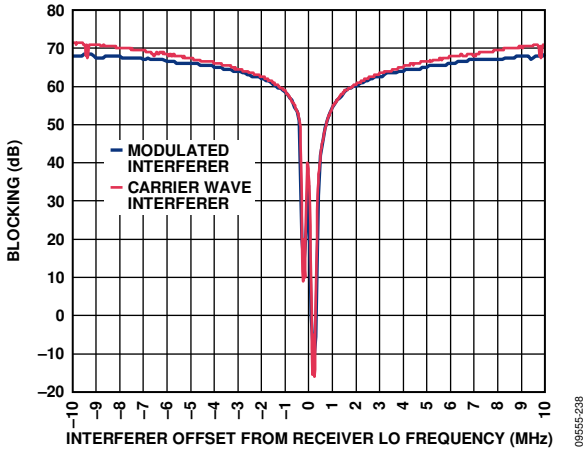

Figure 21. Receiver Wideband Blocking at 915 MHz, Data Rate = 100 kbps

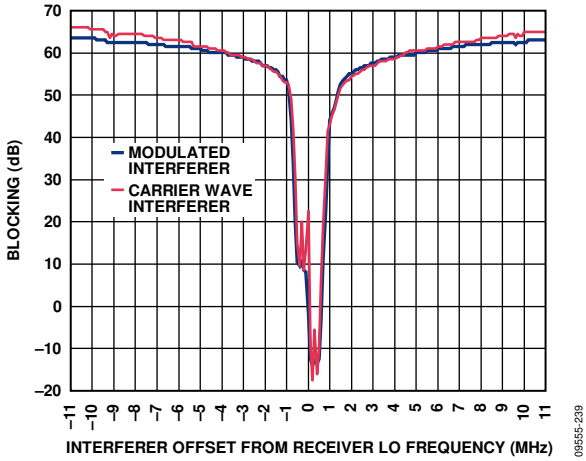

Figure 22. Receiver Wideband Blocking at 915 MHz, Data Rate = 300 kbps

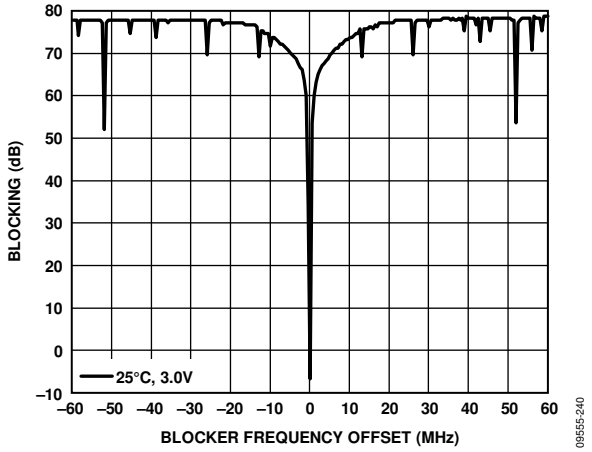

Figure 23. Receiver Wideband Blocking at 954 MHz, Data Rate = 50 kbps, Frequency Deviation = 25 kHz, Carrier Wave Interferer, $P_{WANTED} = P_{SENS} + 3$ dB

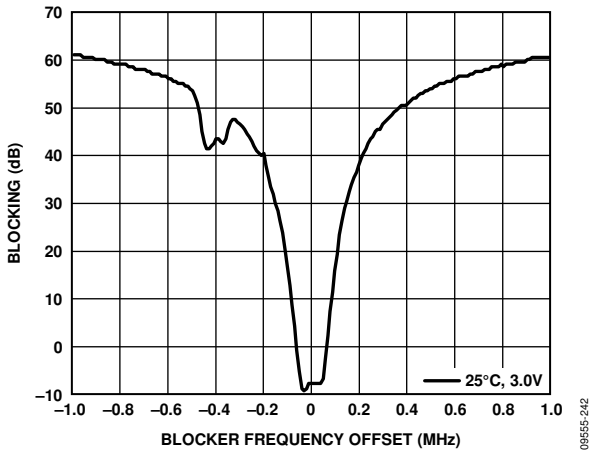

Figure 24. Receiver Close-In Blocking at 954 MHz, Data Rate = 50 kbps, IF Filter Bandwidth = 100 kHz, Image Calibrated, CW Interferer, $P_{WANTED} = P_{SENS} + 3$ dB

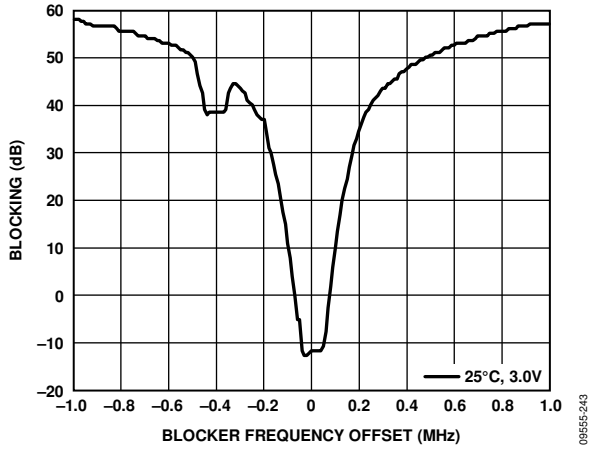

Figure 25. Receiver Close-In Blocking at 954 MHz, Data Rate = 100 kbps, IF Filter Bandwidth = 100 kHz, Image Calibrated, CW Interferer, $P_{WANTED} = P_{SENS} + 3$ dB

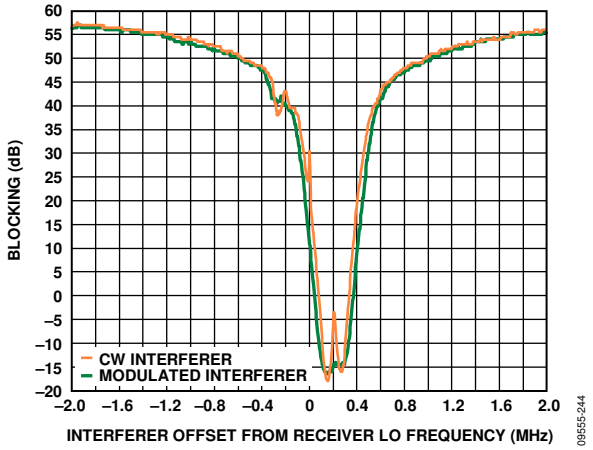

Figure 26. Receiver Close-In Blocking at 915 MHz, Data Rate = 150 kbps, IF Filter Bandwidth = 150 kHz, Image Calibrated

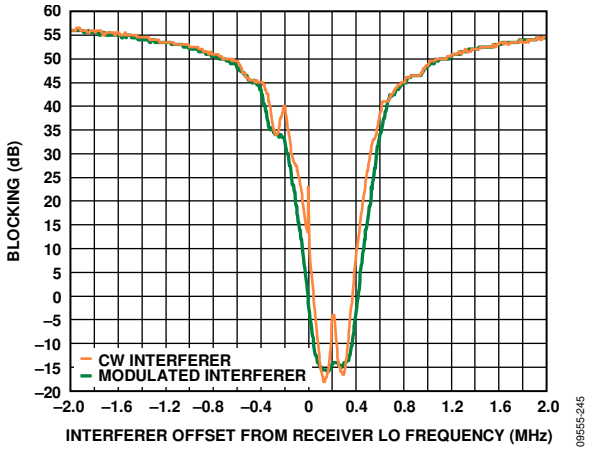

Figure 27. Receiver Close-In Blocking at 915 MHz, Data Rate = 200 kbps, IF Filter Bandwidth = 200 kHz, Image Calibrated

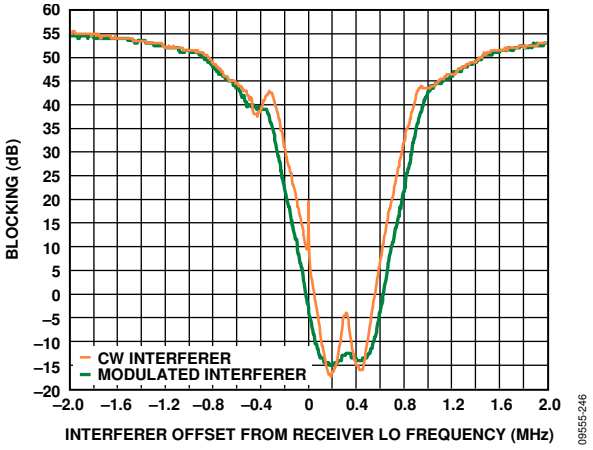

Figure 28. Receiver Close-In Blocking at 915 MHz, Data Rate = 300 kbps, IF Filter Bandwidth = 300 kHz, Image Calibrated

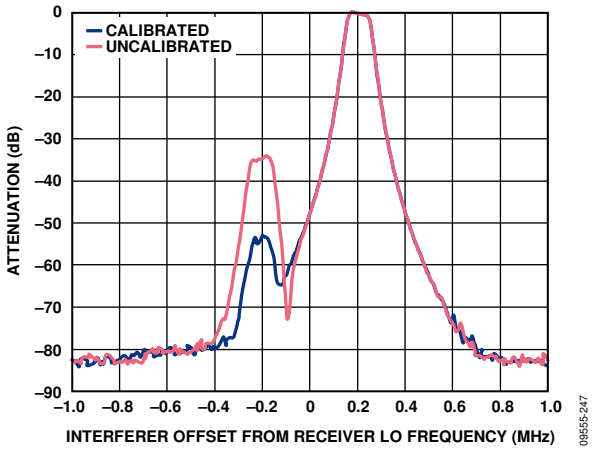

Figure 29. Image Attenuation with Calibrated and Uncalibrated Images, 915 MHz, IF Filter Bandwidth = 100 kHz, V_{DD} = 3.0 V, Temperature = 25°C

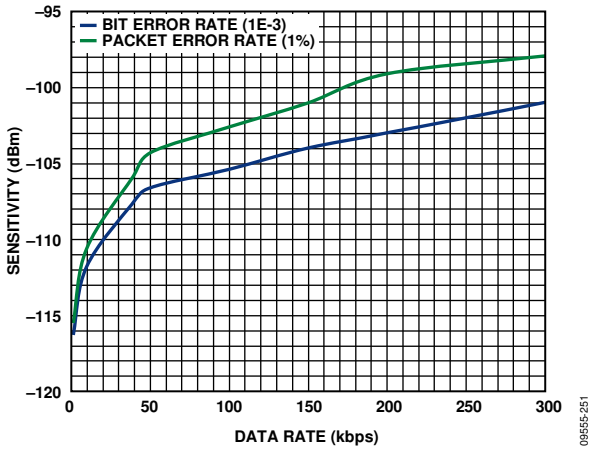

Figure 32. Bit Error Rate Sensitivity (at BER = 1E − 3) and Packet Error Rate Sensitivity (at PER = 1%) vs. Data Rate, GFSK, V_{DD} = 3.0 V, Temperature = 25°C

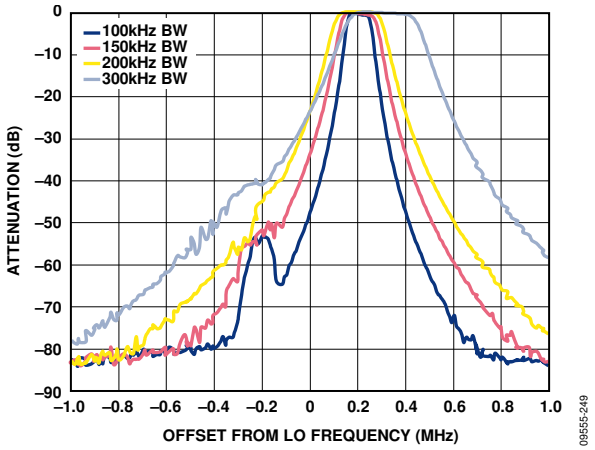

Figure 30. IF Filter Profile with Calibrated Image vs. IF Filter Bandwidth, 921 MHz, V_{DD}= 3.0 V, Temperature = 25°C

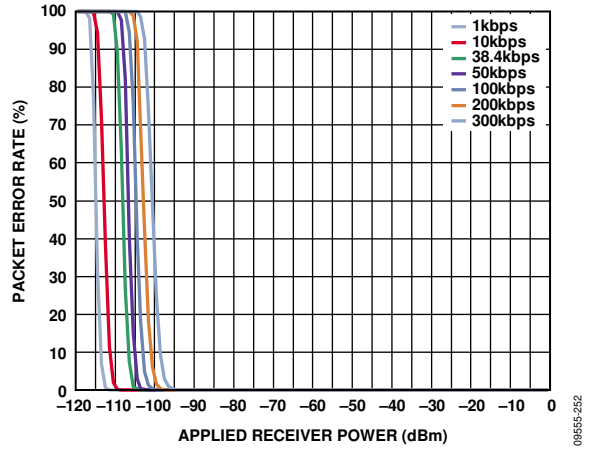

Figure 33. Packet Error Rate vs. RF Input Power and Data Rate, FSK/GFSK, 928 MHz, Preamble Length = 64 Bits, V_{DD} = 3.0 V, Temperature = 25°C

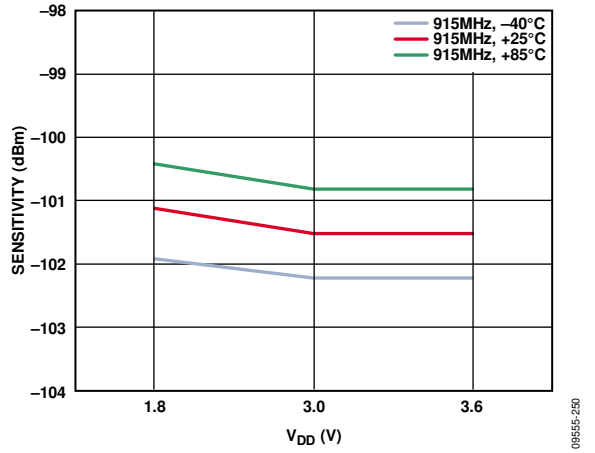

Figure 31. Receiver Sensitivity (Bit Error Rate at 1E − 3) vs. V_{DD}, Temperature, and RF Frequency, Data Rate = 300 kbps, GFSK, Frequency Deviation = 75 kHz, IF Bandwidth = 300 kHz

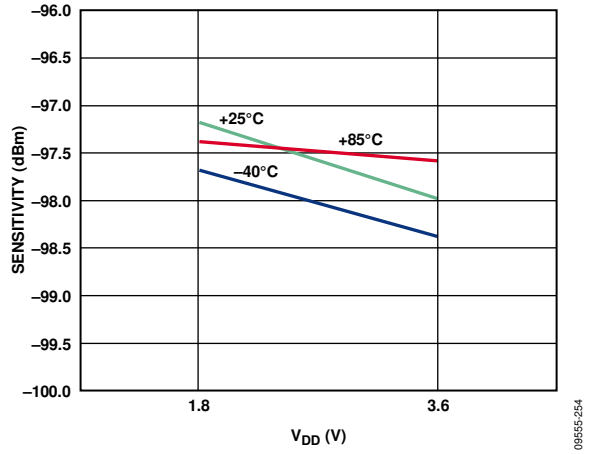

Figure 34. Receiver Sensitivity (Packet Error Rate at 1%) vs. V_{DD}, Temperature, and RF Frequency, Data Rate = 300 kbps, GFSK, Frequency Deviation = 75 kHz, IF Bandwidth = 300 kHz

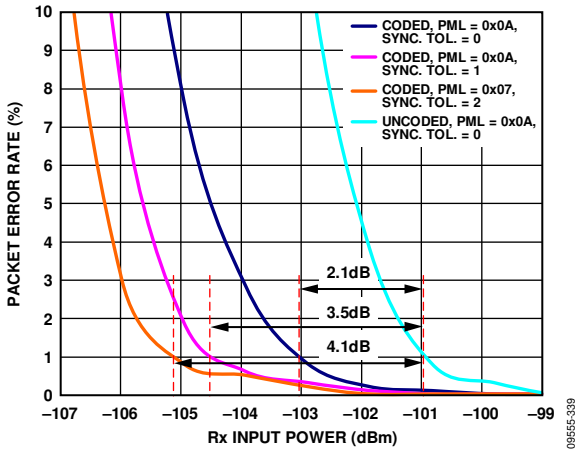

Figure 35. Receiver PER Using Reed Solomon (RS) Coding; RF Frequency = 928 MHz, GFSK, Data Rate = 100 kbps, Frequency Deviation = 50 kHz, Packet Length = 28 Bytes (Uncoded); Reed Solomon Configuration: n = 38, k = 28, t = 5, PML = Preamble Match Level Register

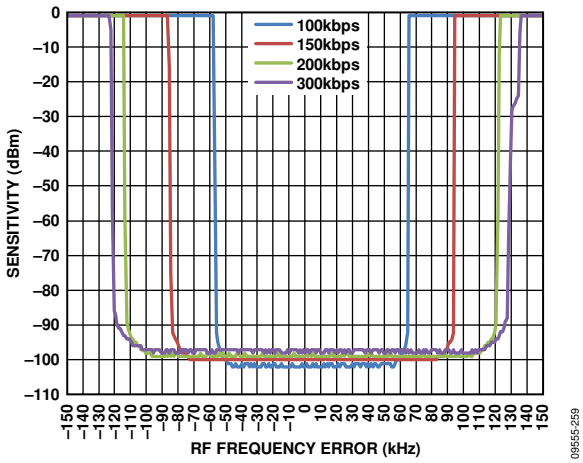

Figure 36. AFC On: Receiver Sensitivity (at PER = 1%) vs. RF Frequency Error, GFSK, 915 MHz, AFC Enabled (Ki = 7, Kp = 3), AFC Mode = Lock After Preamble, IF Bandwidth = 100 kHz (at 100 kbps), 150 kHz (at 150 kbps), 200 kHz (at 200 kbps), and 300 kHz (at 300 kbps), Preamble Length = 64 Bits

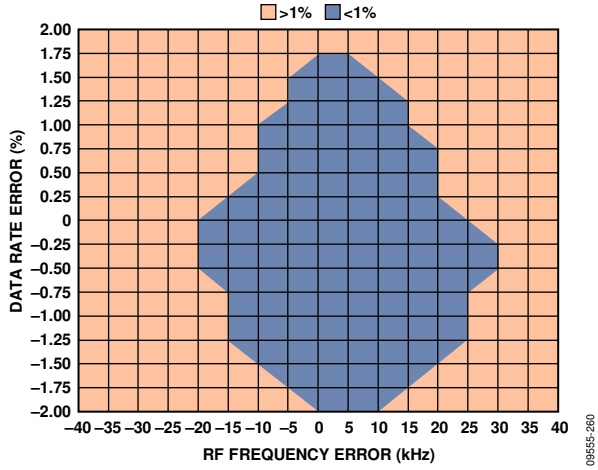

Figure 37. AFC Off: Packet Error Rate vs. RF Frequency Error and Data Rate Error, AFC Off, Data Rate = 300 kbps, Frequency Deviation = 75 kHz, GFSK, AGC_LOCK_MODE = Lock After Preamble

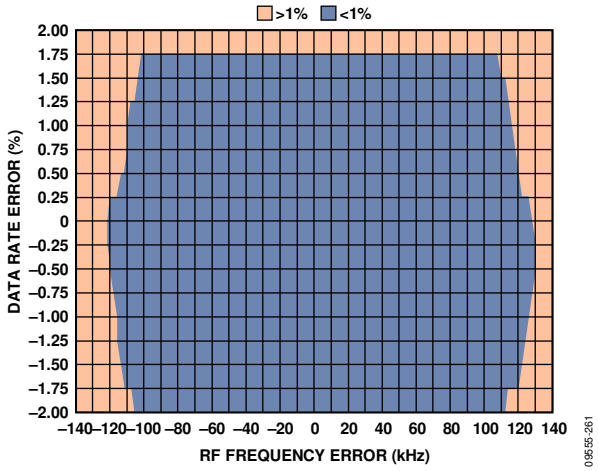

Figure 38. AFC On: Packet Error Rate vs. RF Frequency Error and Data Rate Error, AFC On, Data Rate = 300 kbps, Frequency Deviation = 75 kHz, GFSK, AGC_LOCK_MODE = Lock After Preamble

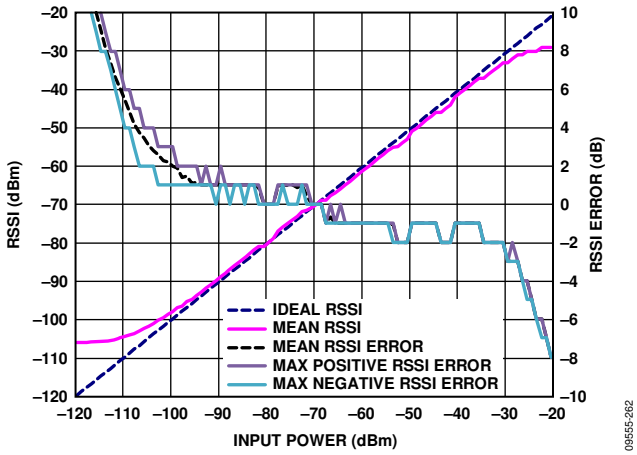

Figure 39. RSSI (via CMD_GET_RSSI) vs. RF Input Power, 950 MHz, GFSK, Data Rate = 38.4 kbps, Frequency Deviation = 20 kHz, IF Bandwidth = 100 kHz, 100 RSSI Measurements at Each Input Power Level

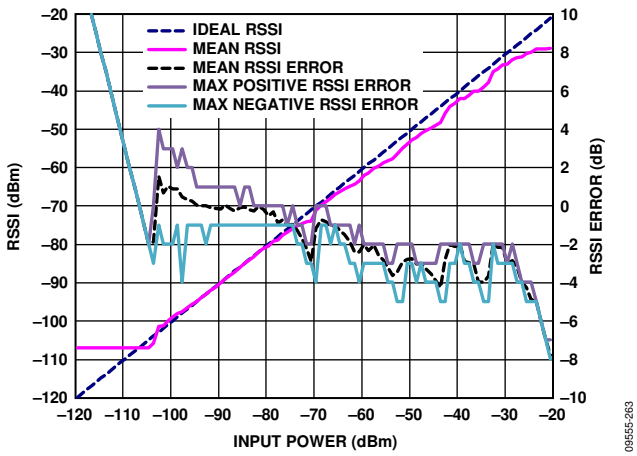

Figure 40. RSSI (via Automatic End of Packet RSSI Measurement) vs. RF Input Power, 950 MHz, GFSK, Data Rate = 300 kbps, Frequency Deviation = 75 kHz, IF Bandwidth = 300 kHz, AGC_CLOCK_DIVIDE = 15, 100 RSSI Measurements at Each Input Power Level