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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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High Performance, Low Power, ISM Band FSK/GFSK/OOK/MSK/GMSK Transceiver IC

Data Sheet

ADF7023

FEATURES

- Ultralow power, high performance transceiver
- Frequency bands
  - 862 MHz to 928 MHz
  - 431 MHz to 464 MHz
- Data rates supported
  - 1 kbps to 300 kbps
- 2.2 V to 3.6 V power supply
- Single-ended and differential PAs
- Low IF receiver with programmable IF bandwidths
  - 100 kHz, 150 kHz, 200 kHz, 300 kHz
- Receiver sensitivity (BER)
  - −116 dBm at 1.0 kbps, 2FSK, GFSK
  - −107.5 dBm at 38.4 kbps, 2FSK, GFSK
  - −102.5 dBm at 150 kbps, GFSK, GMSK
  - −100 dBm at 300 kbps, GFSK, GMSK
  - −104 dBm at 19.2 kbps, OOK
- Very low power consumption
  - 12.8 mA in PHY_RX mode (maximum front-end gain)
  - 24.1 mA in PHY_TX mode (10 dBm output, single-ended PA)
  - 0.75 µA in PHY_SLEEP mode (32 kHz RC oscillator active)
  - 1.28 µA in PHY_SLEEP mode (32 kHz XTAL oscillator active)
  - 0.33 µA in PHY_SLEEP mode (Deep Sleep Mode 1)
- RF output power of −20 dBm to +13.5 dBm (single-ended PA)
- RF output power of −20 dBm to +10 dBm (differential PA)
- Patented fast settling automatic frequency control (AFC)
- Digital received signal strength indication (RSSI)
- Integrated PLL loop filter and Tx/Rx switch
- Fast automatic VCO calibration
- Automatic synthesizer bandwidth optimization
- On-chip, low-power, custom 8-bit processor
  - Radio control
  - Packet management
  - Smart wake mode
- Packet management support
  - Highly flexible for a wide range of packet formats
  - Insertion/detection of preamble/sync word/CRC/address
  - Manchester and 8b/10b data encoding and decoding
  - Data whitening
- Smart wake mode
  - Current saving low power mode with autonomous receiver wake up, carrier sense, and packet reception
- Downloadable firmware modules
  - Image rejection calibration, fully automated (patent pending)
  - 128-bit AES encryption/decryption with hardware acceleration and key sizes of 128 bits, 192 bits, and 256 bits
  - Reed Solomon error correction with hardware acceleration
- 240-byte packet buffer for TX/RX data
- Efficient SPI control interface with block read/write access
- Integrated battery alarm and temperature sensor
- Integrated RC and 32.768 kHz crystal oscillator
- On-chip, 8-bit ADC
- 5 mm × 5 mm, 32-pin, LFCSP package

APPLICATIONS

- Smart metering
- IEEE 802.15.4g
- Wireless MBUS
- Home automation
- Process and building control
- Wireless sensor networks (WSNs)
- Wireless healthcare

Rev. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADF7023 Evaluation Boards
- Wireless Sensor Network (WSN) Development Kits for Your IoT Solutions

DOCUMENTATION

Application Notes

- AN-1275: Rolling Data Buffer on the ADF7023
- AN-1276: Embedded Packet Error Rate Testing on the ADF7023 and ADF7023-J
- AN-1278: Autonomous IR Calibration on the ADF7023
- AN-1292: Reed-Solomon Forward Error Correction and the ADF7023
- AN-1309: A Range Extension Reference Design Using the ADF7023 and RFFM6901 915 MHz ISM Band Transmit Receive Module with Diversity Switch
- AN-1394: AES Encryption and Decryption for the ADF7023 and ADF7023-J

Data Sheet

- ADF7023: High Performance, Low Power, ISM Band FSK/GFSK/OOK/MSK/GMSK Transceiver IC Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADF7023 - No-OS Driver for Renesas Microcontroller Platforms
- ADF7023 Evaluation Board Software

TOOLS AND SIMULATIONS

- ADIsimSRD Design Studio

REFERENCE MATERIALS

Product Selection Guide

- Connectivity Solutions for the Internet of Things

Solutions Bulletins & Brochures

- Emerging Energy Applications Solutions Bulletin, Volume 10, Issue 4
- Industrial ICs Solutions Bulletin, Volume 10, Issue 8

Technical Articles

- Innovative Line Sensor Design with ADI Energy Harvesting and Low Power Signal Chain
- Low Power, Low Cost, Wireless ECG Holter Monitor
- RF Meets Power Lines: Designing Intelligent Smart Grid Systems that Promote Energy Efficiency
- Smart Metering Technology Promotes Energy Efficiency for a Greener World
- The Use of Short Range Wireless in a Multi-Metering System
- Understand Wireless Short-Range Devices for Global License-Free Systems
- Wireless Short Range Devices and Narrowband Communications
- Wireless Technologies for Smart Meters: Focus on Water Metering

DESIGN RESOURCES

- ADF7023 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADF7023 EngineerZone Discussions.

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8/10—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

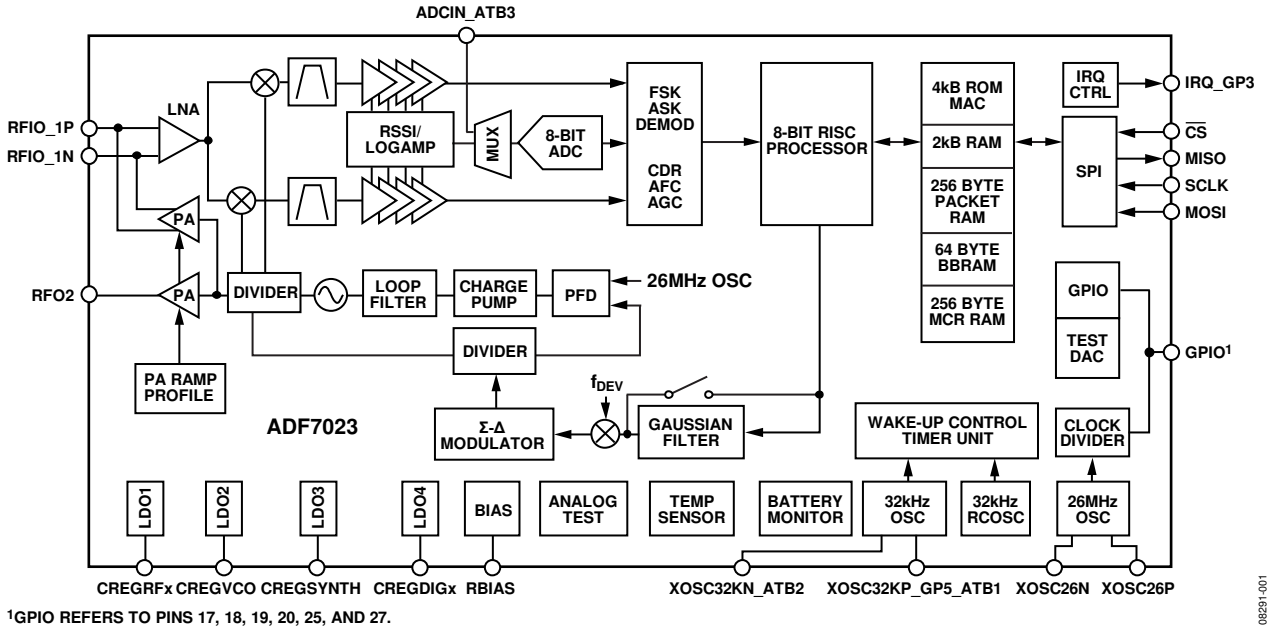


Figure 1.

GENERAL DESCRIPTION

The ADF7023 is a very low power, high performance, highly integrated 2FSK/GFSK/OOK/MSK/GMSK transceiver designed for operation in the 862 MHz to 928 MHz and 431 MHz to 464 MHz frequency bands, which cover the worldwide license-free ISM bands at 433 MHz, 868 MHz, and 915 MHz. It is suitable for circuit applications that operate under the European ETSI EN300-220, the North American FCC (Part 15), the Chinese short-range wireless regulatory standards, or other similar regional standards. Data rates from 1 kbps to 300 kbps are supported.

The transmit RF synthesizer contains a VCO and a low noise fractional-N PLL with an output channel frequency resolution of 400 Hz. The VCO operates at 2× or 4×, the fundamental frequency to reduce spurious emissions. The receive and transmit synthesizer bandwidths are automatically, and independently, configured to achieve optimum phase noise, modulation quality, and settling time. The transmitter output power is programmable from −20 dBm to +13.5 dBm, with automatic PA ramping to meet transient spurious specifications. The part possesses both single-ended and differential PAs, which allows for Tx antenna diversity.

The receiver is exceptionally linear, achieving an IP3 specification of −12.2 dBm and −11.5 dBm at maximum gain and minimum gain, respectively, and an IP2 specification of 18.5 dBm and 27 dBm at maximum gain and minimum gain, respectively. The receiver achieves an interference blocking specification of 66 dB at ±2 MHz offset and 74 dB at ±10 MHz offset. Thus, the part is extremely resilient to the presence of interferers in spectrally noisy environments. The receiver features a novel, high speed, automatic frequency control (AFC) loop, allowing the PLL to find and correct any RF frequency errors in the recovered packet.

A patent pending, image rejection calibration scheme is available through a program download. The algorithm does not require the use of an external RF source nor does it require any user intervention once initiated. The results of the calibration can be stored in nonvolatile memory for use on subsequent power-ups of the transceiver.

The ADF7023 operates with a power supply range of 2.2 V to 3.6 V and has very low power consumption in both Tx and Rx modes, enabling long lifetimes in battery-operated systems while maintaining excellent RF performance. The device can enter a low power sleep mode in which the configuration settings are retained in BBRAM.

The ADF7023 features an ultralow power, on-chip, communications processor. The communications processor, which is an 8-bit RISC processor, performs the radio control, packet management, and smart wake mode (SWM) functionality. The communications processor eases the processing burden of the companion processor by integrating the lower layers of a typical communication protocol stack. The communications processor also permits the download and execution of a set of firmware modules that include image rejection (IR) calibration, AES encryption, and Reed Solomon coding.

The communications processor provides a simple command-based radio control interface for the host processor. A single-byte command transitions the radio between states or performs a radio function.

The communications processor provides support for generic packet formats. The packet format is highly flexible and fully programmable, thereby ensuring its compatibility with proprietary packet profiles. In transmit mode, the communications processor can be configured to add preamble, sync word, and CRC to the payload data stored in packet RAM. In receive mode, the communications processor can detect and interrupt the host processor on reception of preamble, sync word, address, and CRC and store the received payload to packet RAM. The ADF7023 uses an efficient interrupt system comprising MAC level interrupts and PHY level interrupts that can be individually set. The payload data plus the 16-bit CRC can be encoded/decoded using Manchester or 8b/10b encoding. Alternatively, data whitening and dewhitening can be applied.

The smart wake mode (SWM) allows the ADF7023 to wake up autonomously from sleep using the internal wake-up timer without intervention from the host processor. After wake-up, the ADF7023 is controlled by the communications processor. This functionality allows carrier sense, packet sniffing, and packet reception while the host processor is in sleep, thereby reducing overall system current consumption. The smart wake mode can wake the host processor on an interrupt condition. These interrupt conditions can be configured to include the reception of valid preamble, sync word, CRC, or address match. Wake-up from sleep mode can also be triggered by the host processor. For systems requiring very accurate wake-up timing, a 32 kHz oscillator can be used to drive the wake-up timer. Alternatively, the internal RC oscillator can be used, which gives lower current consumption in sleep.

The ADF7023 features an advanced encryption standard (AES) engine with hardware acceleration that provides 128-bit block encryption and decryption with key sizes of 128 bits, 192 bits, and 256 bits. Both electronic code book (ECB) and Cipher Block Chaining Mode 1 (CBC Mode 1) are supported. The AES engine can be used to encrypt/decrypt packet data and can be used as a standalone engine for encryption/decryption by the host processor. The AES engine is enabled on the ADF7023 by downloading the AES software module to program RAM. The AES software module is available from Analog Devices, Inc.

An on-chip, 8-bit ADC provides readback of an external analog input, the RSSI signal, or an integrated temperature sensor. An integrated battery voltage monitor raises an interrupt flag to the host processor whenever the battery voltage drops below a user-defined threshold.

SPECIFICATIONS

V_{DD} = VDDBAT1 = VDDBAT2 = 2.2 V to 3.6 V, GND = 0 V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C.

RF AND SYNTHESIZER SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
RF CHARACTERISTICS					
Frequency Ranges	862		928	MHz	
	431		464	MHz	
PHASE-LOCKED LOOP					
Channel Frequency Resolution		396.7		Hz	
Phase Noise (In-Band)		−88		dBc/Hz	10 kHz offset, PA output power = 10 dBm, RF = 868 MHz
Phase Noise at Offset of					
1 MHz		−126		dBc/Hz	PA output power = 10 dBm, RF frequency = 868 MHz
2 MHz		−131		dBc/Hz	PA output power = 10 dBm, RF frequency = 868 MHz
10 MHz		−142		dBc/Hz	PA output power = 10 dBm, RF frequency = 868 MHz
VCO Calibration Time		142		µs	
Synthesizer Settling Time		56		µs	Frequency synthesizer settles to within ±5 ppm of the target frequency within this time following the VCO calibration, transmit, and receive, 2FSK/GFSK/MSK/GMSK
CRYSTAL OSCILLATOR					
Crystal Frequency		26		MHz	Parallel load resonant crystal
Recommended Load Capacitance	7		18	pF	
Maximum Crystal ESR		1800		Ω	26 MHz crystal with 18 pF load capacitance
Pin Capacitance		2.1		pF	Capacitance for XOSC26P and XOSC26N
Start-Up Time		310		µs	26 MHz crystal with 7 pF load capacitance
		388		µs	26 MHz crystal with 18 pF load capacitance
SPURIOUS EMISSIONS					
Integer Boundary Spurious					
910.1 MHz		−39		dBc	Using 130 kHz synthesizer bandwidth, integer boundary spur at 910 MHz (26 MHz × 35), inside synthesizer loop bandwidth
911.0 MHz		−79		dBc	Using 130 kHz synthesizer bandwidth, integer boundary spur at 910 MHz (26 MHz × 35), outside synthesizer loop bandwidth
Reference Spurious					
868 MHz/915 MHz		−80		dBc	Using 130 kHz synthesizer bandwidth and using 92 kHz synthesizer bandwidth (default for PHY_RX)
Clock-Related Spur Level		−60		dBc	Measured in a span of ±350 MHz for synthesizer bandwidth = 92 kHz, RF frequency = 868.95 MHz, PA output power = 10 dBm, V_{DD} = 3.6 V, single-ended PA used

TRANSMITTER SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions
DATA RATE					
2FSK/GFSK/MSK/GMSK	1		300	kbps	
OOK	2.4		19.2	kbps	Manchester encoding enabled (Manchester chip rate = 2 × data rate)
Data Rate Resolution		100		bps	
MODULATION ERROR RATE (MER)					RF frequency = 928 MHz, GFSK
10 kbps to 49.5 kbps		25.4		dB	Modulation index = 1
49.6 kbps to 129.5 kbps		25.3		dB	Modulation index = 1
129.6 kbps to 179.1 kbps		23.9		dB	Modulation index = 0.5
179.2 kbps to 239.9 kbps		23.3		dB	Modulation index = 0.5
240 kbps to 300 kbps		23		dB	Modulation index = 0.5
MODULATION					
2FSK/GFSK/MSK/GMSK Frequency Deviation	0.1		409.5	kHz	
Deviation Frequency Resolution		100		Hz	
Gaussian Filter BT		0.5			Nonprogrammable
OOK					
PA Off Feedthrough		−94		dBm	
VCO Frequency Pulling		30		kHz rms	Data rate = 19.2 kbps (38.4 kcps Manchester encoded), PA output = 10 dBm, PA ramp rate = 64 codes/bit
SINGLE-ENDED PA					
Maximum Power[1]		13.5		dBm	Programmable, separate PA and LNA match[2]
Minimum Power		−20		dBm	
Transmit Power Variation vs. Temperature		±0.5		dB	From −40°C to +85°C, RF frequency = 868 MHz
Transmit Power Variation vs. V_{DD}		±1		dB	From 2.2 V to 3.6 V, RF frequency = 868 MHz
Transmit Power Flatness		±1		dB	From 902 MHz to 928 MHz and 863 MHz to 870 MHz
Programmable Step Size					
−20 dBm to +13.5 dBm		0.5		dB	Programmable in 63 steps
DIFFERENTIAL PA					
Maximum Power[1]		10		dBm	Programmable
Minimum Power		−20		dBm	
Transmit Power Variation vs. Temperature		±1		dB	From −40°C to +85°C, RF frequency = 868 MHz
Transmit Power Variation vs. V_{DD}		±2		dB	From 2.2 V to 3.6 V, RF frequency = 868 MHz
Transmit Power Flatness		±1		dB	From 863 MHz to 870 MHz
Programmable Step Size					
−20 dBm to +10 dBm		0.5		dB	Programmable in 63 steps
HARMONICS					868 MHz, unfiltered conductive, PA output power = 10 dBm
Single-Ended PA					
Second Harmonic		−15.1		dBc	
Third Harmonic		−29.3		dBc	
All Other Harmonics		−47.6		dBc	
Differential PA					
Second Harmonic		−23.2		dBc	
Third Harmonic		−25.2		dBc	
All Other Harmonics		−24.2		dBc	

Parameter	Min	Typ	Max	Unit	Test Conditions
OPTIMUM PA LOAD IMPEDANCE					
Single-Ended PA, in Transmit Mode					
f_{RF} = 915 MHz		50.8 + j10.2		Ω	
f_{RF} = 868 MHz		45.5 + j12.1		Ω	
f_{RF} = 433 MHz		46.8 + j19.9		Ω	
Single-Ended PA, in Receive Mode					
f_{RF} = 915 MHz		9.4 – j124		Ω	
f_{RF} = 868 MHz		9.5 – j130.6		Ω	
f_{RF} = 433 MHz		11.9 – j260.1		Ω	
Differential PA, in Transmit Mode					Load impedance between RFIO_1P and RFIO_1N to ensure maximum output power
f_{RF} = 915 MHz		20.5 + j36.4		Ω	
f_{RF} = 868 MHz		24.7 + j36.5		Ω	
f_{RF} = 433 MHz		55.6 + j81.5		Ω	

[1] Measured as the maximum unmodulated power.
[2] A combined single-ended PA and LNA match can reduce the maximum achievable output power by up to 1 dB.

RECEIVER SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions
2FSK/GFSK/MSK/GMSK INPUT SENSITIVITY, BIT ERROR RATE (BER)					At BER = 1E − 3, RF frequency = 433 MHz, 868 MHz, 915 MHz, LNA and PA matched separately[1]
1.0 kbps		−116		dBm	Frequency deviation = 4.8 kHz, IF filter bandwidth = 100 kHz
10 kbps		−111		dBm	Frequency deviation = 9.6 kHz, IF filter bandwidth = 100 kHz
38.4 kbps		−107.5		dBm	Frequency deviation = 20 kHz, IF filter bandwidth = 100 kHz
50 kbps		−106.5		dBm	Frequency deviation = 12.5 kHz, IF filter bandwidth = 100 kHz
100 kbps		−105		dBm	Frequency deviation = 25 kHz, IF filter bandwidth = 100 kHz
150 kbps		−104		dBm	Frequency deviation = 37.5 kHz, IF filter bandwidth = 150 kHz
200 kbps		−103		dBm	Frequency deviation = 50 kHz, IF filter bandwidth = 200 kHz
300 kbps		−100.5		dBm	Frequency deviation = 75 kHz, IF filter bandwidth = 300 kHz
2FSK/GFSK/MSK/GMSK INPUT SENSITIVITY, PACKET ERROR RATE (PER)					At PER = 1%, RF frequency = 433 MHz, 868 MHz, 915 MHz, LNA and PA matched separately[1], packet length = 128 bits, packet mode
1.0 kbps		−115.5		dBm	Frequency deviation = 4.8 kHz, IF filter bandwidth = 100 kHz
9.6 kbps		−110.6		dBm	Frequency deviation = 9.6 kHz, IF filter bandwidth = 100 kHz
38.4 kbps		−106		dBm	Frequency deviation = 20 kHz, IF filter bandwidth = 100 kHz
50 kbps		−104.3		dBm	Frequency deviation = 12.5 kHz, IF filter bandwidth = 100 kHz
100 kbps		−102.6		dBm	Frequency deviation = 25 kHz, IF filter bandwidth = 100 kHz
150 kbps		−101		dBm	Frequency deviation = 37.5 kHz, IF filter bandwidth = 150 kHz
200 kbps		−99.1		dBm	Frequency deviation = 50 kHz, IF filter bandwidth = 200 kHz
300 kbps		−97.9		dBm	Frequency deviation = 75 kHz, IF filter bandwidth = 300 kHz
OOK INPUT SENSITIVITY, PACKET ERROR RATE (PER)					At PER = 1%, RF frequency = 433 MHz, 868 MHz, 915 MHz, LNA and PA matched separately[1], packet length = 128 bits, packet mode, IF filter bandwidth = 100 kHz
19.2 kbps (38.4 kcps, Manchester Encoded)		−104.7		dBm	
2.4 kbps (4.8 kcps, Manchester Encoded)		−109.7		dBm	
LNA AND MIXER, INPUT IP3					Receiver LO frequency (f_{LO}) = 914.8 MHz, $f_{SOURCE1} = f_{LO}$ + 0.4 MHz, $f_{SOURCE2} = f_{LO}$ + 0.7 MHz
Minimum LNA Gain		−11.5		dBm	
Maximum LNA Gain		−12.2		dBm	
LNA AND MIXER, INPUT IP2					Receiver LO frequency (f_{LO}) = 920.8 MHz, $f_{SOURCE1} = f_{LO}$ + 1.1 MHz, $f_{SOURCE2} = f_{LO}$ + 1.3 MHz
Max LNA Gain, Max Mixer Gain		18.5		dBm	
Min LNA Gain, Min Mixer Gain		27		dBm	

Parameter	Min	Typ	Max	Unit	Test Conditions
LNA AND MIXER, 1 dB COMPRESSION POINT					RF frequency = 915 MHz
Max LNA Gain, Max Mixer Gain		−21.9		dBm	
Min LNA Gain, Min Mixer Gain		−21		dBm	
ADJACENT CHANNEL REJECTION					
CW Interferer					Wanted signal 3 dB above the input sensitivity level (BER = 10^{-3}), CW interferer power level increased until BER = 10^{-3}, image calibrated
200 kHz Channel Spacing		38		dB	IF BW = 100 kHz, wanted signal: F_{DEV} = 12.5 kHz, DR = 50 kbps
300 kHz Channel Spacing		39		dB	IF BW = 100 kHz, wanted signal: F_{DEV} = 25 kHz, DR = 100 kbps
		38		dB	IF BW = 150 kHz, wanted signal: F_{DEV} = 37.5 kHz, DR = 150 kbps
400 kHz Channel Spacing		40		dB	IF BW = 200 kHz, wanted signal: F_{DEV} = 50 kHz, DR = 200 kbps
600 kHz Channel Spacing		41		dB	IF BW = 300 kHz, wanted signal: F_{DEV} = 75 kHz, DR = 300 kbps
Modulated Interferer					Wanted signal 3 dB above the input sensitivity level (BER = 10^{-3}), modulated interferer with the same modulation as the wanted signal; interferer power level increased until BER = 10^{-3}, image calibrated
200 kHz Channel Spacing		38		dB	IF BW = 100 kHz, wanted signal: F_{DEV} = 12.5 kHz, DR = 50 kbps
300 kHz Channel Spacing		36		dB	IF BW = 100 kHz, wanted signal: F_{DEV} = 25 kHz, DR = 100 kbps
300 kHz Channel Spacing		36		dB	IF BW = 150 kHz, wanted signal: F_{DEV} = 37.5 kHz, DR = 150 kbps
400 kHz Channel Spacing		34		dB	IF BW = 200 kHz, wanted signal: F_{DEV} = 50 kHz, DR = 200 kbps
600 kHz Channel Spacing		35		dB	IF BW = 300 kHz, wanted signal: F_{DEV} = 75 kHz, DR = 300 kbps
CO-CHANNEL REJECTION		−4		dB	Desired signal 10 dB above the input sensitivity level (BER = 10^{-3}), data rate = 38.4 kbps, frequency deviation = 20 kHz, RF frequency = 868 MHz
BLOCKING					Desired signal 3 dB above the input sensitivity level (BER = 10^{-3}) of −107.5 dBm (data rate = 38.4 kbps), modulated interferer power level increased until BER = 10^{-3} (see the Typical Performance Characteristics section for blocking at other offsets and IF bandwidths)
RF Frequency = 433 MHz					
±2 MHz		68		dB	
±10 MHz		76		dB	
RF Frequency = 868 MHz					
±2 MHz		66		dB	
±10 MHz		74		dB	
RF Frequency = 915 MHz					
±2 MHz		66		dB	
±10 MHz		74		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions
BLOCKING, ETSI EN 300 220					Measurement procedure as per ETSI EN 300 220-1 V2.3.1; desired signal 3 dB above the ETSI EN 300 220 reference sensitivity level of −99 dBm, IF bandwidth = 100 kHz, data rate = 38.4 kbps, unmodulated interferer; see the Typical Performance Characteristics section for blocking at other offsets and IF bandwidths, RF frequency = 868 MHz
±2 MHz		−28		dBm	
±10 MHz		−20.5		dBm	
WIDEBAND INTERFERENCE REJECTION		75		dB	RF frequency = 868 MHz, swept from 10 MHz to 100 MHz either side of the RF frequency
IMAGE CHANNEL ATTENUATION					Measured as image attenuation at the IF filter output, carrier wave interferer at 400 kHz below the channel frequency, 100 kHz IF filter bandwidth
868 MHz, 915 MHz		36/45		dB	Uncalibrated/calibrated
433 MHz		40/54		dB	Uncalibrated/calibrated
AFC					
Accuracy		1		kHz	
Maximum Pull-In Range					Achievable pull-in range dependent on discriminator bandwidth and modulation
300 kHz IF Filter Bandwidth		±150		kHz	
200 kHz IF Filter Bandwidth		±100		kHz	
150 kHz IF Filter Bandwidth		±75		kHz	
100 kHz IF Filter Bandwidth		±50		kHz	
PREAMBLE LENGTH					Minimum number of preamble bits to ensure the minimum packet error rate across the full input power range
AFC Off, AGC Lock on Sync Word Detection					
38.4 kbps		8		Bits	
300 kbps		24		Bits	
AFC On, AFC and AGC Lock on Preamble Detection					
9.6 kbps		44		Bits	
38.4 kbps		44		Bits	
50 kbps		50		Bits	
100 kbps		52		Bits	
150 kbps		54		Bits	
200 kbps		58		Bits	
300 kbps		64		Bits	
AFC On, AFC and AGC Lock on Sync Word Detection					
38.4 kbps		14		Bits	
300 kbps		32		Bits	
RSSI					
Range at Input		−97 to −26		dBm	
Linearity		±2		dB	
Absolute Accuracy		±3		dB	
SATURATION (MAXIMUM INPUT LEVEL)					
2FSK/GFSK/MSK/GMSK		12		dBm	
OOK		−13		dBm	OOK modulation depth = 20 dB
		10		dBm	OOK modulation depth = 60 dB

Parameter	Min	Typ	Max	Unit	Test Conditions
LNA INPUT IMPEDANCE					
Receive Mode					
f_{RF} = 915 MHz		75.9 – j32.3		Ω	
f_{RF} = 868 MHz		78.0 – j32.4		Ω	
f_{RF} = 433 MHz		95.5 – j23.9		Ω	
Transmit Mode					
f_{RF} = 915 MHz		7.6 + j9.2		Ω	
f_{RF} = 868 MHz		7.7 + j8.6		Ω	
f_{RF} = 433 MHz		7.9 + j4.6		Ω	
RX SPURIOUS EMISSIONS[2]					
Maximum <1 GHz		–66		dBm	At antenna input, unfiltered conductive
Maximum >1 GHz		–62		dBm	At antenna input, unfiltered conductive

[1] Sensitivity for combined matching network case is typically 1 dB less than separate matching networks.
[2] Follow the matching and layout guidelines to achieve the relevant FCC/ETSI specifications.

TIMING AND DIGITAL SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions
RX AND TX TIMING PARAMETERS					See the State Transition and Command Timing section for more details
PHY_ON to PHY_RX (on CMD_PHY_RX)		300		µs	Includes VCO calibration and synthesizer settling
PHY_ON to PHY_TX (on CMD_PHY_TX)		296		µs	Includes VCO calibration and synthesizer settling, does not include PA ramp-up
LOGIC INPUTS					
Input High Voltage, V_{INH}	$0.7 \times V_{DD}$			V	
Input Low Voltage, V_{INL}			$0.2 \times V_{DD}$	V	
Input Current, I_{INH}/I_{INL}			±1	µA	
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	$V_{DD} - 0.4$			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
GPIO Rise/Fall			5	ns	
GPIO Load			10	pF	
Maximum Output Current		5		mA	
ATB OUTPUTS					Used for external PA and LNA control
ADCIN_ATB3 and ATB4					
Output High Voltage, V_{OH}		1.8		V	
Output Low Voltage, V_{OL}		0.1		V	
Maximum Output Current		0.5		mA	
XOSC32KP_GP5_ATB1 and XOSC32KN_ATB2					
Output High Voltage, V_{OH}		V_{DD}		V	
Output Low Voltage, V_{OL}		0.1		V	
Maximum Output Current		5		mA	

AUXILARY BLOCK SPECIFICATIONS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions
32 kHz RC OSCILLATOR					
Frequency		32.768		kHz	After calibration
Frequency Accuracy		1.5		%	After calibration at 25°C
Frequency Drift					
Temperature Coefficient		0.14		%/°C	
Voltage Coefficient		4		%/V	
Calibration Time		1.25		ms	
32 kHz XTAL OSCILLATOR					
Frequency		32.768		kHz	
Start-Up Time		630		ms	32.768 kHz crystal with 7 pF load capacitance
WAKE UP CONTROLLER (WUC)					
Hardware Timer					
Wake-Up Period	61×10^{-6}		1.31×10^{5}	sec	
Firmware Timer					
Wake-Up Period	1		2^{16}	Hardware periods	Firmware counter counts of the number of hardware wake-ups, resolution of 16 bits
ADC					
Resolution		8		Bits	
DNL		±1		LSB	V_{DD} from 2.2 V to 3.6 V, T_A = 25°C
INL		±1		LSB	V_{DD} from 2.2 V to 3.6 V, T_A = 25°C
Conversion Time		1		µs	
Input Capacitance		12.4		pF	
BATTERY MONITOR					
Absolute Accuracy		±45		mV	
Alarm Voltage Set Point	1.7		2.7	V	
Alarm Voltage Step Size		62		mV	5-bit resolution
Start-Up Time			100	µs	
Current Consumption		30		µA	When enabled
TEMPERATURE SENSOR					
Range	−40		+85	°C	
Resolution		0.3		°C	With averaging
Accuracy of Temperature Readback		+7/−4		°C	Over temperature range −40°C to +85°C (calibrated at +25°C)

GENERAL SPECIFICATIONS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions
TEMPERATURE RANGE, T_A	−40		+85	°C	
VOLTAGE SUPPLY					
V_{DD}	2.2		3.6	V	Applied to VDDBAT1 and VDDBAT2
TRANSMIT CURRENT CONSUMPTION					In the PHY_TX state, single-ended PA matched to 50 Ω, differential PA matched to 100 Ω, separate single-ended PA and LNA match, combined differential PA and LNA match
Single-Ended PA, 433 MHz					
−10 dBm		8.7		mA	
0 dBm		12.2		mA	
10 dBm		23.3		mA	
13.5 dBm		32.1		mA	
Differential PA, 433 MHz					
−10 dBm		7.9		mA	
0 dBm		11		mA	
5 dBm		15		mA	
10 dBm		22.6		mA	
Single-Ended PA, 868 MHz/915 MHz					
−10 dBm		10.3		mA	
0 dBm		13.3		mA	
10 dBm		24.1		mA	
13.5 dBm		32.1		mA	
Differential PA, 868 MHz/915 MHz					
−10 dBm		9.3		mA	
0 dBm		12		mA	
5 dBm		16.7		mA	
10 dBm		28		mA	
POWER MODES					
PHY_SLEEP (Deep Sleep Mode 2)		0.18		µA	Sleep mode, wake-up configuration values (BBRAM) not retained
PHY_SLEEP (Deep Sleep Mode 1)		0.33		µA	Sleep mode, wake-up configuration values (BBRAM) retained
PHY_SLEEP (RCO Wake Mode)		0.75		µA	WUC active, RC oscillator running, wake-up configuration values retained (BBRAM)
PHY_SLEEP (XTO Wake Mode)		1.28		µA	WUC active, 32 kHz crystal running, wake-up configuration values retained (BBRAM)
PHY_OFF		1		mA	Device in PHY_OFF state, 26 MHz oscillator running, digital and synthesizer regulators active, all register values retained
PHY_ON		1		mA	Device in PHY_ON state, 26 MHz oscillator running, digital, synthesizer, VCO, and RF regulators active, baseband filter calibration performed, all register values retained
PHY_RX		12.8		mA	Device in PHY_RX state
SMART WAKE MODE					Average current consumption
		21.78		µA	Autonomous reception every 1 sec, with receive dwell time of 1.25 ms, using RC oscillator, data rate = 38.4 kbps
		11.75		µA	Autonomous reception every 1 sec, with receive dwell time of 0.5 ms, using RC oscillator, data rate = 300 kbps

TIMING SPECIFICATIONS

V_{DD} = VDDBAT1 = VDDBAT2 = 2.2 V to 3.6 V, V_{GND} = GND = 0 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

Table 7. SPI Interface Timing

Parameter	Limit	Unit	Test Conditions/Comments
t_2	85	ns min	$\overline{CS}$ low to SCLK setup time
t_3	85	ns min	SCLK high time
t_4	85	ns min	SCLK low time
t_5	170	ns min	SCLK period
t_6	10	ns max	SCLK falling edge to MISO delay
t_7	5	ns min	MOSI to SCLK rising edge setup time
t_8	5	ns min	MOSI to SCLK rising edge hold time
t_9	85	ns min	SCLK falling edge to $\overline{CS}$ hold time
t_{11}	270	ns min	$\overline{CS}$ high time
t_{12}	310	µs typ	$\overline{CS}$ low to MISO high wake-up time, 26 MHz crystal with 7 pF load capacitance, T_A = 25°C
t_{13}	20	ns max	SCLK rise time
t_{14}	20	ns max	SCLK fall time

Timing Diagrams

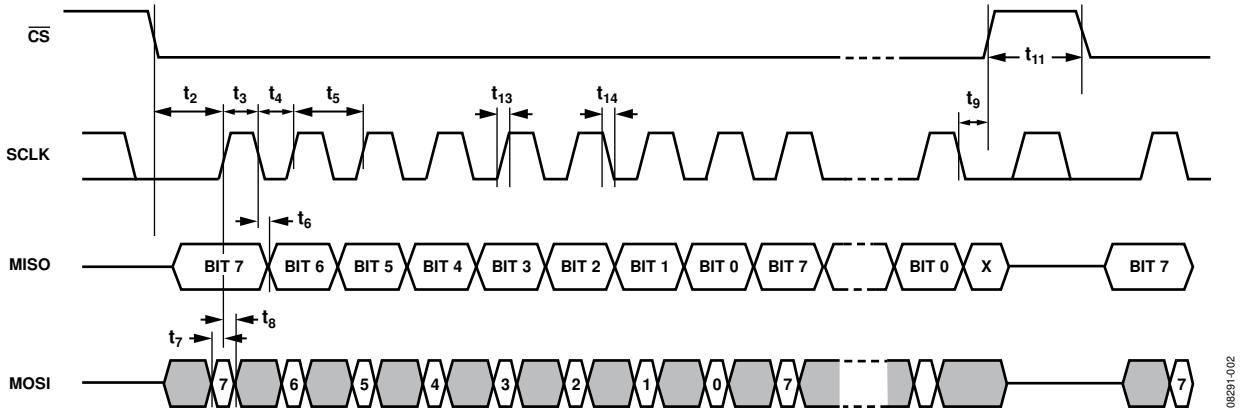


Figure 2. SPI Interface Timing

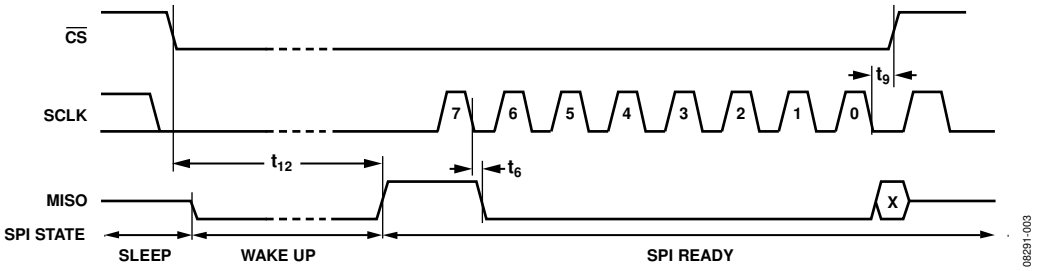


Figure 3. PHY_SLEEP to SPI Ready State Timing (SPI Ready T12 After Falling Edge of $\overline{CS}$)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
VDDBAT1, VDDBAT2 to GND	−0.3 V to +3.96 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Connect the exposed paddle of the LFCSP package to ground.

This device is a high performance, RF integrated circuit with an ESD rating of <2 kV; it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

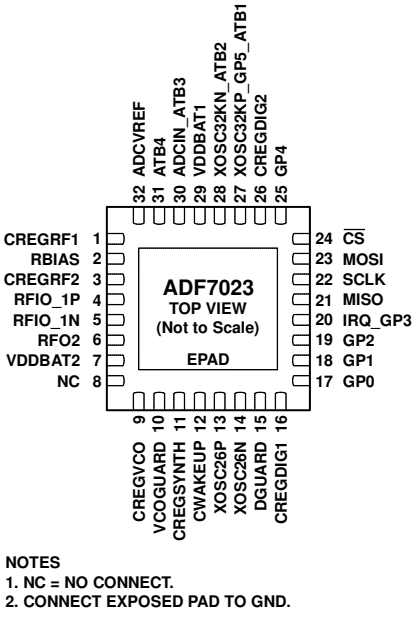


Figure 4. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	CREGRF1	Regulator Voltage for RF. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
2	RBIAS	External Bias Resistor. A 36 kΩ resistor with 2% tolerance should be used.
3	CREGRF2	Regulator Voltage for RF. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
4	RFIO_1P	LNA Positive Input in Receive Mode. PA positive output in transmit mode with differential PA.
5	RFIO_1N	LNA Negative Input in Receive Mode. PA negative output in transmit mode with differential PA.
6	RFO2	Single-Ended PA Output.
7	VDDBAT2	Power Supply Pin Two. Decoupling capacitors to the ground plane should be placed as close as possible to this pin.
8	NC	No Connect.
9	CREGVCO	Regulator Voltage for the VCO. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
10	VCOGUARD	Guard/Screen for VCO. This pin should be connected to Pin 9.
11	CREGSYNTH	Regulator Voltage for the Synthesizer. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
12	CWAKEUP	External Capacitor for Wake-Up Control. A 150 nF capacitor should be placed between this pin and ground.
13	XOSC26P	The 26 MHz reference crystal should be connected between this pin and XOSC26N. If an external reference is connected to XOSC26N, this pin should be left open circuited.
14	XOSC26N	The 26 MHz reference crystal should be connected between this pin and XOSC26P. Alternatively, an external 26 MHz reference signal can be ac-coupled to this pin.
15	DGUARD	Internal Guard/Screen for the Digital Circuitry. Connect this pin to Pin 16, CREGDIG1.
16	CREGDIG1	Regulator Voltage for Digital Section of the Chip. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
17	GP0	Digital GPIO Pin 0.
18	GP1	Digital GPIO Pin 1.
19	GP2	Digital GPIO Pin 2.
20	IRQ_GP3	Interrupt Request, Digital GPIO Test Pin 3.
21	MISO	Serial Port Master In/Slave Out.

Pin No.	Mnemonic	Function
22	SCLK	Serial Port Clock.
23	MOSI	Serial Port Master Out/Slave In.
24	$\overline{CS}$	Chip Select (Active Low). A pull-up resistor of 100 kΩ to V_{DD} is recommended to prevent the host processor from inadvertently waking the ADF7023 from sleep.
25	GP4	Digital GPIO Test Pin 4.
26	CREGDIG2	Regulator Voltage for Digital Section of the Chip. A 220 nF capacitor should be placed between this pin and ground for regulator stability and noise rejection.
27	XOSC32KP_GP5_ATB1	Digital GPIO Test Pin 5. A 32 kHz watch crystal can be connected between this pin and XOSC32KN_ATB2. Analog Test Pin 1.
28	XOSC32KN_ATB2	A 32 kHz watch crystal can be connected between this pin and XOSC32KP_GP5_ATB1. Analog Test Pin 2.
29	VDDBAT1	Digital Power Supply Pin One. Decoupling capacitors to the ground plane should be placed as close as possible to this pin.
30	ADCIN_ATB3	Analog-to-Digital Converter Input. Can be configured as an external PA enable signal. Analog Test Pin 3.
31	ATB4	Analog Test Pin 4. Can be configured as an external LNA enable signal.
32	ADCVREF	ADC Reference Output. A 220 nF capacitor should be placed between this pin and ground for adequate noise rejection.
EPAD	GND	Exposed Package Paddle. Connect to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

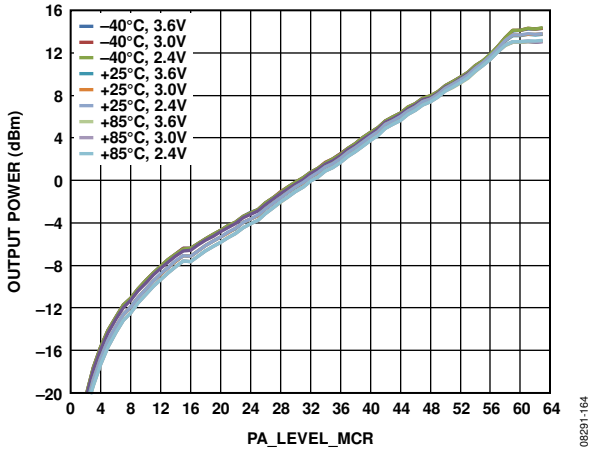


Figure 5. Single-Ended PA at 433 MHz: Output Power vs. PA_LEVEL_MCR Setting, Temperature, and V_{DD}

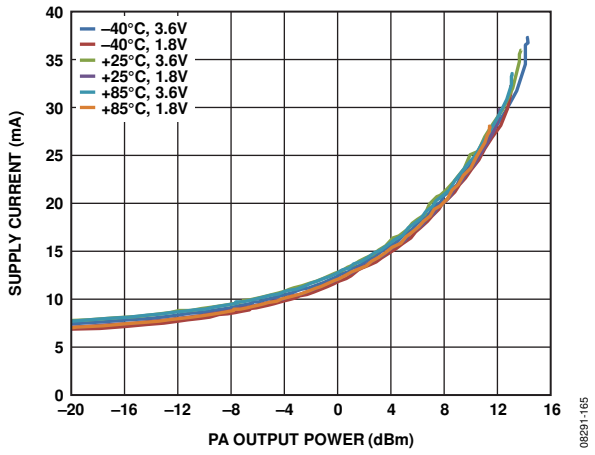


Figure 6. Single-Ended PA at 433 MHz: Supply Current vs. Output Power, Temperature, and V_{DD} (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

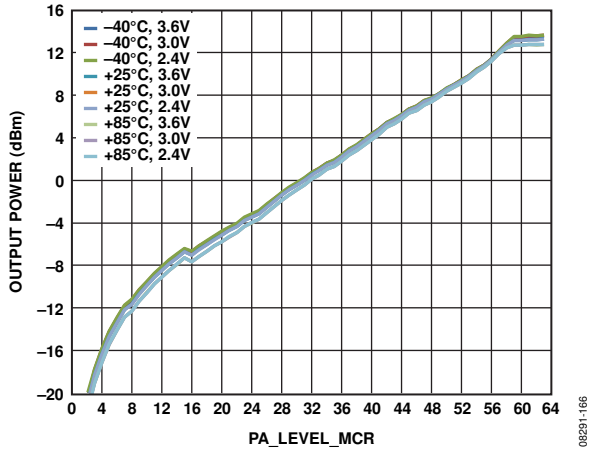


Figure 7. Single-Ended PA at 868 MHz: Output Power vs. PA_LEVEL_MCR Setting, Temperature, and V_{DD}

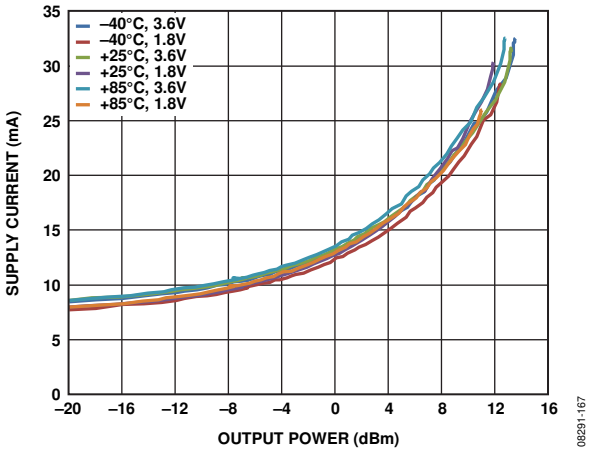


Figure 8. Single-Ended PA at 868 MHz: Supply Current vs. Output Power, Temperature, and V_{DD}

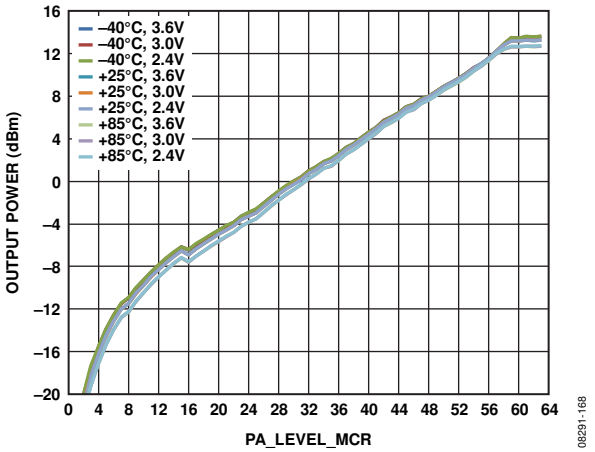


Figure 9. Single-Ended PA at 915 MHz: Output Power vs. PA_LEVEL_MCR Setting, Temperature, and V_{DD}

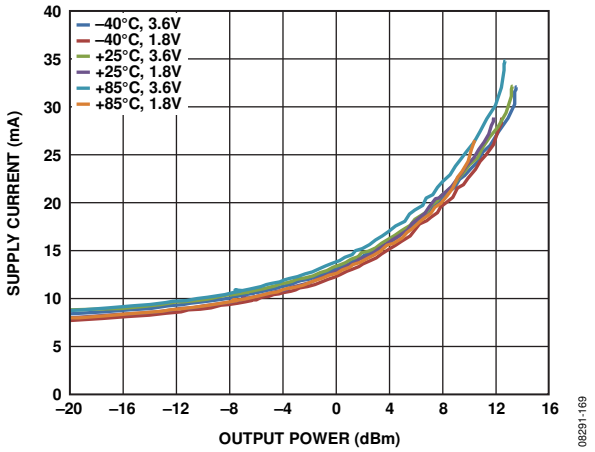


Figure 10. Single-Ended PA at 915 MHz: Supply Current vs. Output Power, Temperature, and V_{DD} (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

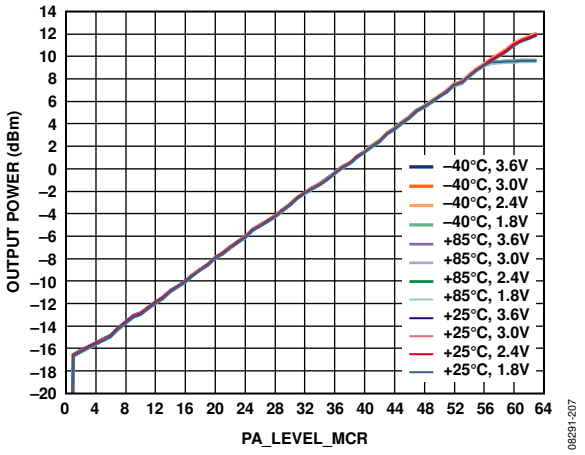


Figure 11. Differential PA at 433 MHz: Output Power vs. PA_LEVEL_MCR Setting, Temperature, and V_{DD} (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

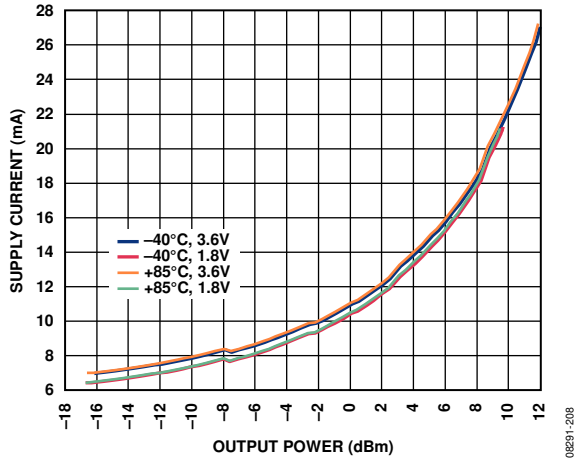


Figure 12. Differential PA at 433 MHz: Supply Current vs. Output Power, Temperature, and V_{DD} (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

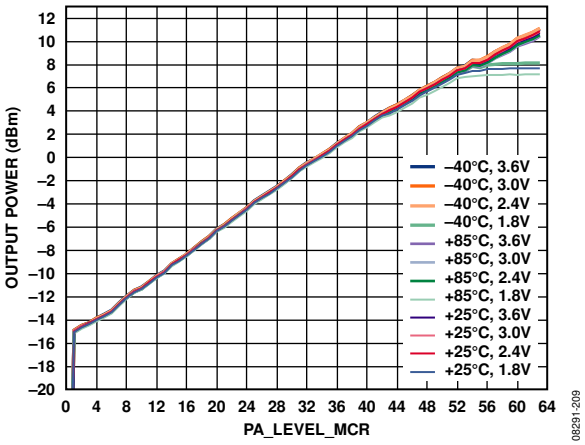


Figure 13. Differential PA at 915 MHz: Output Power vs. PA_LEVEL_MCR Setting, Temperature, and V_{DD} (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

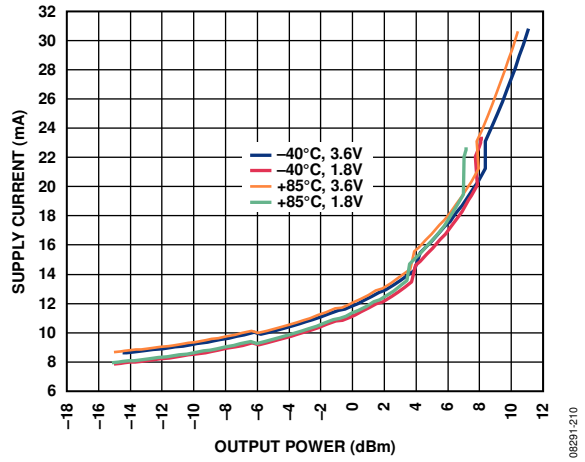


Figure 14. Differential PA at 915 MHz: Supply Current vs. Output Power, Temperature, and V_{DD} (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

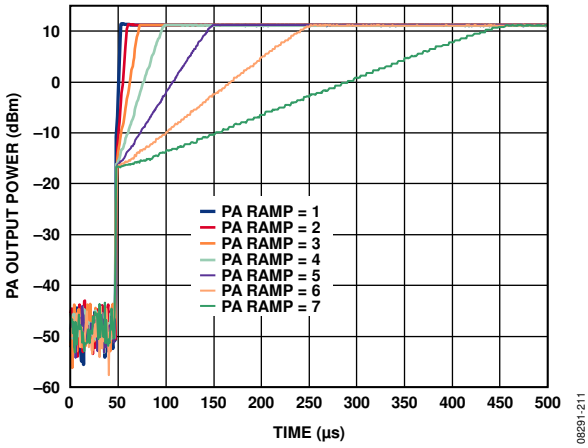


Figure 15. PA Ramp-Up at Data Rate =38.4 kbps for Each PA_RAMP Setting, Differential PA

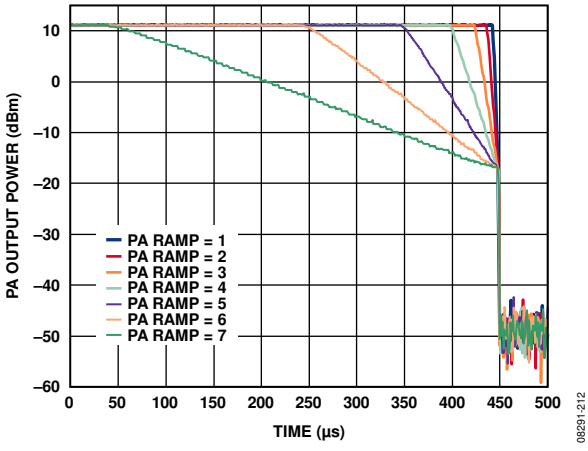
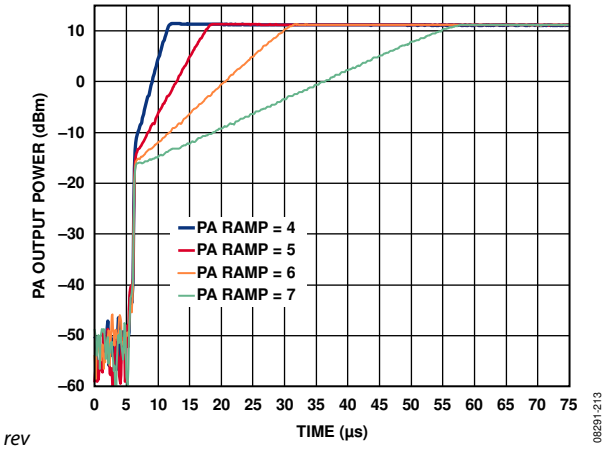


Figure 16. PA Ramp-Down at Data Rate =38.4 kbps for Each PA_RAMP Setting, Differential PA



rev

Figure 17. PA Ramp-Up at Data Rate =300 kbps for Each PA_RAMP Setting, Differential PA

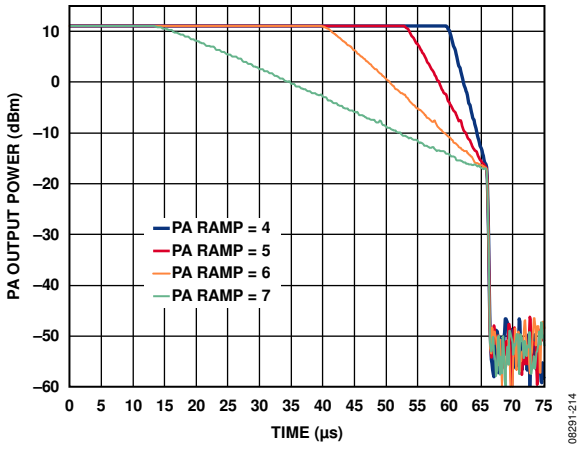


Figure 18. PA Ramp-Down at Data Rate =300 kbps for Each PA_RAMP Setting, Differential PA

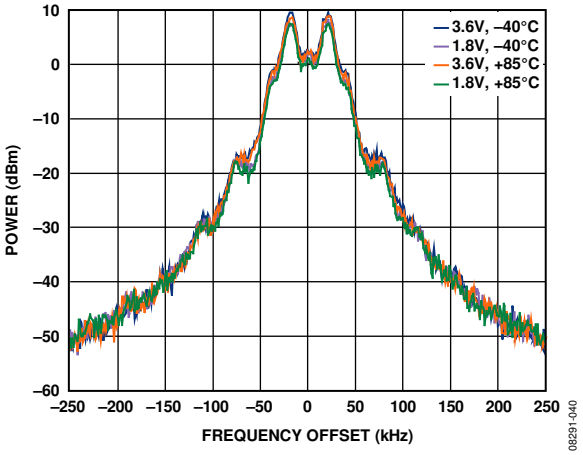


Figure 19. Transmit Spectrum at 868 MHz, FSK, Data Rate = 38.4 kbps, Frequency Deviation = 20 kHz (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

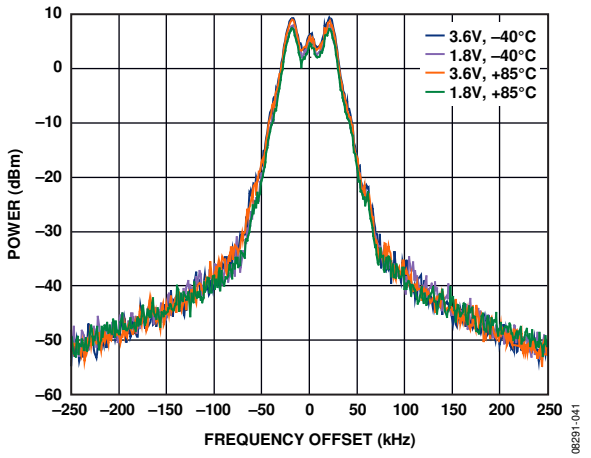


Figure 20. Transmit Spectrum at 868 MHz, GFSK, Data Rate = 38.4 kbps, Frequency Deviation = 20 kHz (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

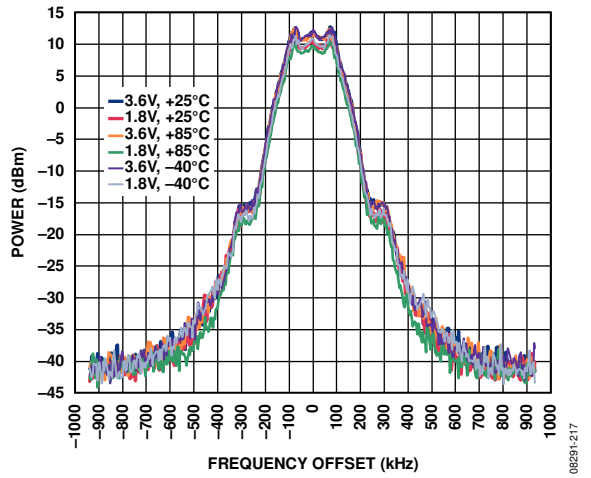


Figure 21. Transmit Spectrum at 928 MHz, GFSK, Data Rate = 300 kbps, Frequency Deviation = 75 kHz (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

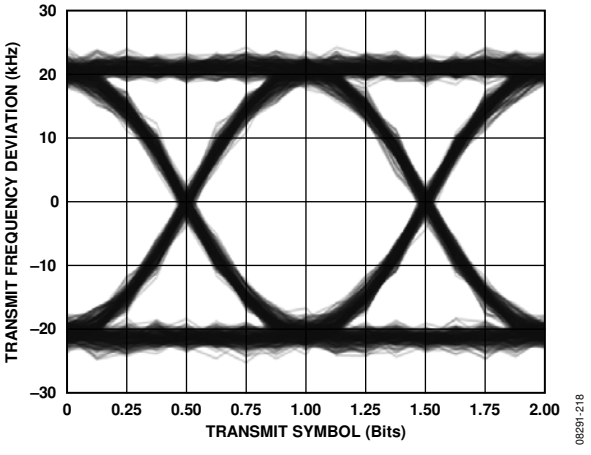


Figure 22. Transmit Eye at 868 MHz, GFSK, Data Rate = 38.4 kbps, Frequency Deviation = 21 kHz

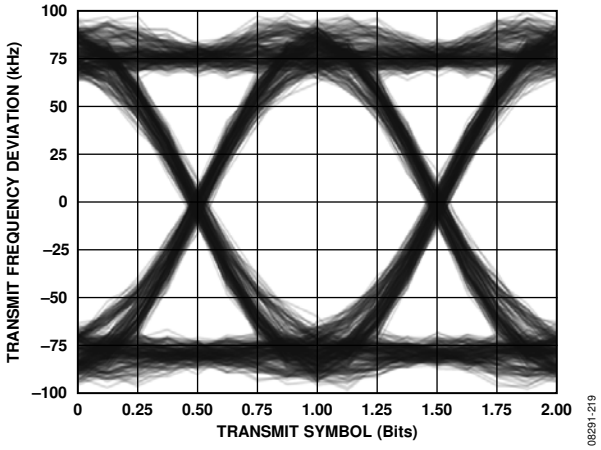


Figure 23. Transmit Eye at 868 MHz, GFSK, Data Rate = 300 kbps, Frequency Deviation = 75 kHz

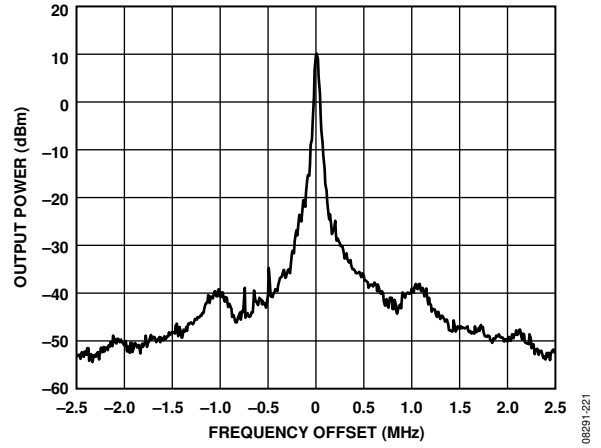


Figure 24. OOK Transmit Spectrum, Max Hold for 100 Sweeps, Single-Ended PA, 868.95 MHz, Data Rate = 16.4 kbps (32.8 kcps, Manchester Encoded), PA_RAMP = 1

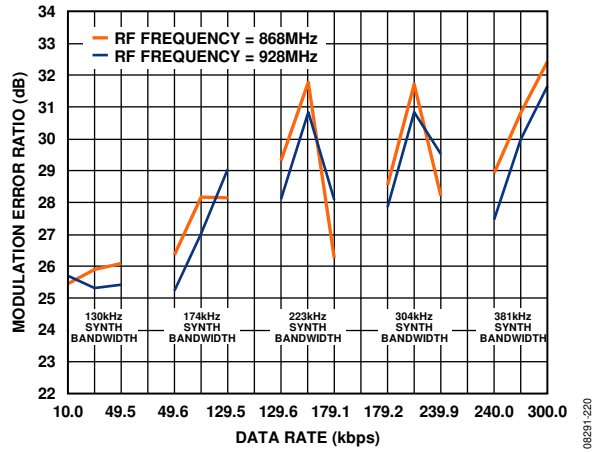


Figure 25. Modulation Error Ratio (MER) vs. Data Rate, Synthesizer Loop Bandwidth, and RF Frequency at Modulation Index = 1

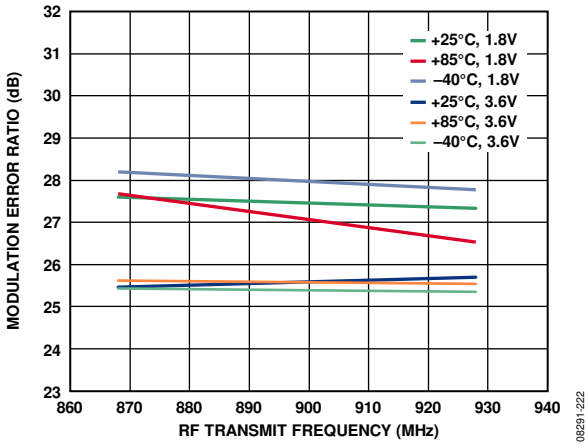


Figure 26. Modulation Error Ratio (MER) vs. RF Frequency, Temperature, and V_{DD} at Modulation Index = 1 and Data Rate = 10 kbps (Minimum Recommended V_{DD} = 2.2 V, 1.8 V Operation Shown for Robustness)

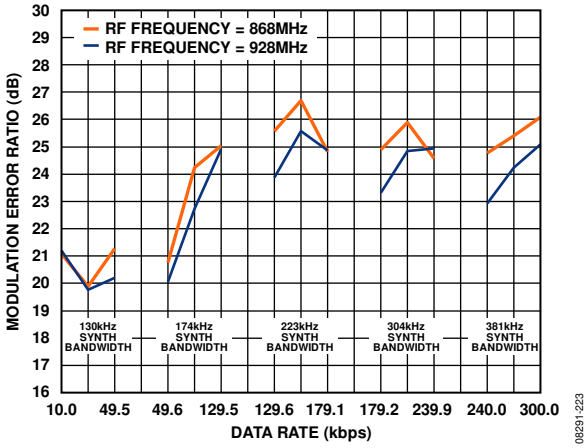


Figure 27. Modulation Error Ratio (MER) vs. Data Rate, Synthesizer Loop Bandwidth, and RF Frequency at Modulation Index = 0.5

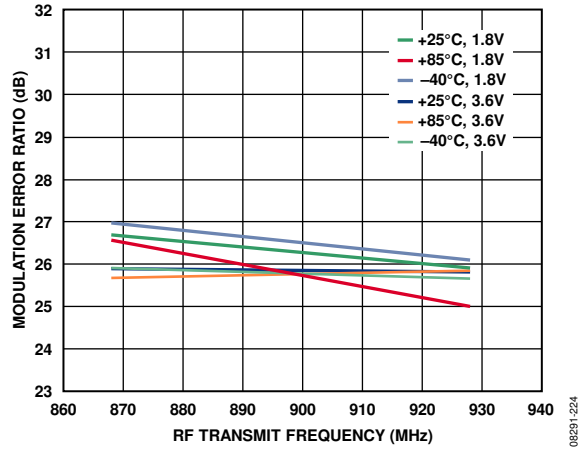


Figure 28. Modulation Error Ratio (MER) vs. RF Frequency, Temperature, and V_{DD} at Modulation Index = 0.5 and Data Rate = 10 kbps