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High Performance, Sub GHz Radio Transceiver IC

Data Sheet

ADF7030-1

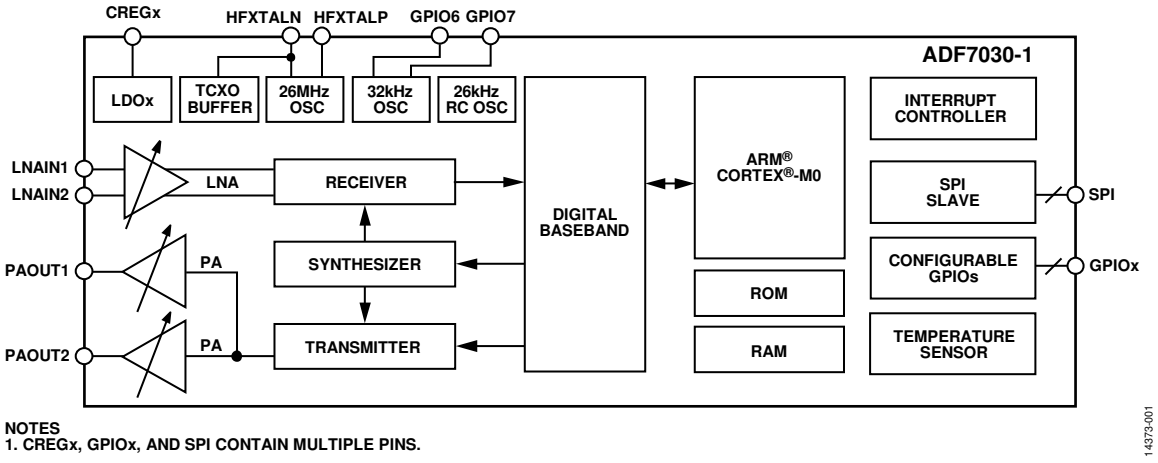
FEATURES

- Radio frequency (RF) ranges
  - 169.4 MHz to 169.6 MHz
  - 426 MHz to 470 MHz
  - 863 MHz to 960 MHz
- Data rates
  - 2FSK/2GFSK: 0.1 kbps to 300 kbps
  - 4FSK/4GFSK: 1 kbps to 360 kbps (transmit only)
- Dual power amplifiers (PAs)
- Programmable receiver channel bandwidth (BW) from
  - 2.6 kHz to 738 kHz
- Receiver (Rx) performance
  - Up to 102 dB blocking at ±20 MHz offset
  - Up to 66 dB adjacent channel rejection
  - −134.3 dBm sensitivity at 0.1 kbps
  - −121.2 dBm sensitivity at 2.4 kbps
- Transmitter (Tx) performance
  - −20 dBm to +17 dBm range with 0.1 dB step resolution
  - Very low output power variation vs. temperature and supply
- Low active current
  - 50 mA Tx current at 17 dBm
  - 21.2 mA Rx current at12.5 kbps
- Ultralow sleep current
  - 10 nA with memory retained
  - Autonomous smart wake modes
- Host microprocessor interface
  - Easy to use programming serial peripheral interface (SPI)
  - Configurable 8-bit general-purpose input/output (GPIO) bus
- On-chip ARM Cortex-M0 processor for
  - Radio control and calibration
  - Packet management
  - Clear channel assessment (CCA)
- IEEE802.15.4g support
  - Frame format
  - Data whitening
  - Dual-sync word detection
  - Forward error correction (FEC) and interleaving
- Suitable for systems targeting compliance with
  - ETSI EN 300 220-1
  - EN 54-25, EN 13757-4
  - FCC Part 15, Part 22, Part 24, Part 90, and Part 101
  - ARIB STD-T30, STD-T67, STD-T108, STD-T96
- Packages
  - 6 mm × 6 mm, 40-lead LFCSP
  - 7 mm × 7 mm, 48-lead LQFP

APPLICATIONS

- IEEE 802.15.4g (MR-FSK PHY)
- Wireless M-Bus (EN 13757-4)
- Smart metering
- Security and building automation
- Active tag asset tracking
- Industrial control
- Wireless sensor networks (WSNs)

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. CREGx, GPIOx, AND SPI CONTAIN MULTIPLE PINS.

Figure 1.

Rev. 0

Document Feedback

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- ADF7030-1 Evaluation and Development Kit

DOCUMENTATION

Data Sheet

- ADF7030-1: High Performance, Sub GHz Radio Transceiver IC Data Sheet

Product Highlight

- ADF7030-1: Ultralow Power, Sub GHz RF Transceiver

User Guides

- UG-1002: ADF7030-1 Software Reference Manual
- UG-1006: ADF7030-1 EZ-KIT User Guide
- UG-957: ADF7030-1 Hardware Reference Manual

REFERENCE MATERIALS

Press

- Transceiver Provides Reliable Radio Connections and Extended Battery Life for IoT and Other Wireless Applications

Product Selection Guide

- Connectivity Solutions for the Internet of Things

Solutions Bulletins & Brochures

- Technologies and Applications for the Internet of Things

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REVISION HISTORY

6/2016—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADF7030-1 is a fully integrated, radio transceiver achieving high performance at very low power. The ADF7030-1 is ideally suited for applications that require long range, network robustness, and long battery life. It is suitable for applications that operate in the ISM, SRD, and licensed frequency bands at 169.4 MHz to 169.6 MHz, 426 MHz to 470 MHz, and 863 MHz to 960 MHz. It provides extensive support for standards-based protocols like IEEE802.15.4g while also providing flexibility to support a wide range of proprietary protocols.

The highly configurable low intermediate frequency (IF) receiver supports a large range of receiver channel bandwidths from 2.6 kHz to 738 kHz. This range of receiver channel bandwidths allows the ADF7030-1 to support ultranarrow-band, narrow-band, and wideband channel spacing.

The ADF7030-1 features two independent PAs supporting output power ranges of −20 dBm to +13 dBm and −20 dBm to +17 dBm. The PAs support ultrafine adjustment of the power with a step resolution of 0.1 dB. The PA output power is exceptionally robust over temperature and voltage. The PAs have an automatic power ramp control to limit spectral splatter to meet regulatory standards.

The ADF7030-1 features an on-chip ARM® Cortex®-M0 processor that performs radio control, radio calibration, and packet management. Cortex-M0 eases the processing burden of the host processor because the ADF7030-1 integrates the lower layers of a typical communication protocol stack. This internal processor also permits the download and execution of Analog Devices, Inc., provided firmware modules that can extend the functionality of the ADF7030-1.

The ADF7030-1 has two packet modes: generic packet mode and IEEE802.15.4g mode. In generic packet mode, the packet format is highly flexible and fully programmable, thereby ensuring its compatibility with proprietary packet formats. In IEEE802.15.4g packet mode, the packet format conforms to the IEEE802.15.4g standard. FEC, as per the IEEE802.15.4g standard, is also supported.

The ADF7030-1 operates with a power supply range of 2.2 V to 3.6 V and has very low power consumption in both Tx and Rx modes, enabling long lifetimes in battery-operated systems. An ultralow power deep sleep mode achieves a typical current of 10 nA with the configuration memory retained.

The ADF7030-1 supports smart wake mode (SWM) where the ADF7030-1 can wake up autonomously from sleep using an internal real-time clock (RTC) without intervention from the host processor. After wake-up, the ADF7030-1 operates autonomously. This functionality allows carrier sense, packet sniffing, and packet reception while the host processor is in sleep mode, thereby reducing overall system current consumption. The ADF7030-1 autonomous operation can also be triggered by the host processor using the interrupt input of the ADF7030-1.

A complete wireless solution can be built using a small number of external discrete components and a host processor (typically a microcontroller). The host processor can configure the ADF7030-1 using a simple command-based protocol over a standard 4-wire SPI interface. A single-byte command transitions the radio between states or performs a radio function.

The ADF7030-1 is available in two package types: a 6 mm × 6 mm, 40-lead LFCSP and a 7 mm × 7 mm, 48-lead LQFP. Both package types use NiPdAu plating to mitigate against silver migration in high humidity applications. The ADF7030-1 operating temperature range is −40°C to +85°C.

For Figure 13 to Figure 19, Figure 30, Figure 42, Figure 60, Figure 61, and Figure 77 in the Typical Performance Characteristics section, PA_COARSE is a programmable value that provides a coarse adjustment of the PA output power. This value can be programmed in the range of 1 to 6 for PA1, and from 1 to 10 for PA2. PA_FINE is a programmable value that provides a fine adjustment of the PA output power. This value can be programmed in the range of 3 to 127 for both PA1 and PA2. PA_MICRO is a programmable value that provides a microadjustment (typically <0.1 dB) of the PA output power. This value can be programmed in the range of 1 to 31 for both PA1 and PA2. PAOLDO_VOUT_CON is a programmable value that configures the internal LDO voltage that provides bias for the PA. For additional information on these bit settings, see the ADF7030-1 Software Reference Manual, which is the detailed programming guide for the device.

SPECIFICATIONS

V_{DD} = VBAT1 = VBAT2 = VBAT3 = VBAT4 = VBAT5 = VBAT6 = 2.2 V to 3.6 V, exposed pad (EPAD) = 0 V (ground), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical specifications are at V_{DD} = 3 V, T_A = 25°C, unless otherwise noted. All VBATx pins must be tied together. A one-time radio calibration is required, unless otherwise noted.

TEMPERATURE AND VOLTAGE

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE RANGE, T_A	−40		+85	°C	
VOLTAGE SUPPLY					
VBATx Pin Voltage	2.2		3.6	V	Transmit power ≤ 13 dBm
	2.85		3.6	V	Transmit power ≥ 17 dBm, PA LDO voltage = 2.65 V
	PA LDO voltage + 0.2 V		3.6	V	Transmit power >13 dBm and < 17 dBm; the PA LDO voltage is configurable

GENERAL RF

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RF FREQUENCY					
Frequency Range	169.4		169.6	MHz	
	426		470	MHz	
	863		960	MHz	
Channel Frequency Resolution		1.5		Hz	
DATA RATE					
IEEE802.15.4g Packet Mode				kbps	
2FSK, 2GFSK Modulation	2.4		150	kbps	
Generic Packet Mode					
2FSK, 2GFSK Modulation	0.1		300	kbps	
4FSK, 4GFSK Modulation	1		360	kbps	Tx only, generic packet mode only
On/Off Keying (OOK) Modulation		16.384		kbps	Tx only, Manchester encoded, generic packet mode only
Resolution		1		bps	
FREQUENCY DEVIATION					
Range					
2FSK, 2GFSK Modulation	1		250	kHz	
4FSK, 4GFSK Modulation	1		250	kHz	Tx only, generic packet mode only
Resolution		100		Hz	
GAUSSIAN FILTER BANDWIDTH TIME (BT) PRODUCT		0.3, 0.35, 0.4, 0.5			Programmable

RECEIVE

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MAXIMUM DATA RATE ERROR TOLERANCE		±0.1		%	
RECEIVER CHANNEL FILTER BANDWIDTH					Programmable; see Table 27 and Table 28 for a list of all supported values
Narrow-Band Mode					
Maximum		20.0		kHz	
Minimum		2.6		kHz	
Wideband Mode					
Maximum		738		kHz	
Minimum		77		kHz	
MAXIMUM RF INPUT LEVEL		10		dBm	
RECEIVER LINEARITY					Measured at maximum receiver gain
Input Third-Order Intercept (IIP3)		−8.5		dBm	Receiver channel frequency = 169.43125 MHz, $f_{SOURCE1}$ = 171.35 MHz, $f_{SOURCE2}$ = 173.26875 MHz
Input Second-Order Intercept (IIP2)		53		dBm	Receiver channel frequency = 169.53125 MHz, $f_{SOURCE1}$ = 171.55 MHz, $f_{SOURCE2}$ = 171.63125 MHz
1 dB Compression (P1dB)		−18.7		dBm	Receiver channel frequency = 169.43125 MHz, $f_{SOURCE1}$ = 171.43125 MHz
RECEIVED SIGNAL STRENGTH INDICATOR (RSSI)					Refer to the Typical Performance Characteristics section for further detail; sensitivity defined as bit error rate (BER) = 0.1%
Resolution		0.25		dB	
Calibrated Absolute Accuracy		±2		dB	−40 dBm to sensitivity + 6 dB; one-point offset calibration
DIFFERENTIAL LOW NOISE AMPLIFIER (LNA) INPUT IMPEDANCE, 40-LEAD LFCSP PACKAGE					
LNA in Rx Mode					
f = 169 MHz		78 − j20		Ω	
f = 433 MHz		69 − j25		Ω	
f = 460 MHz		68 − j25		Ω	
f = 868 MHz		56 − j29		Ω	
f = 915 MHz		55 − j30		Ω	
LNA in Tx Mode					Combined match enabled
f = 169 MHz		7 + j2		Ω	
f = 433 MHz		7 + j4		Ω	
f = 460 MHz		7 + j4		Ω	
f = 868 MHz		8 + j8		Ω	
f = 915 MHz		8 + j8		Ω	
DIFFERENTIAL LNA INPUT IMPEDANCE, 48-LEAD LQFP PACKAGE					
LNA in Rx Mode					
f = 169 MHz		78 − j16		Ω	
f = 433 MHz		71 − j18		Ω	
f = 460 MHz		73 − j22		Ω	
f = 868 MHz		58 − j20		Ω	
f = 915 MHz		57 − j20		Ω	
LNA in Tx Mode					Combined match enabled
f = 169 MHz		7 + j3		Ω	
f = 433 MHz		8 + j9		Ω	
f = 460 MHz		8 + j9		Ω	
f = 868 MHz		9 + j18		Ω	
f = 915 MHz		9 + j19		Ω	

TRANSMIT

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER AMPLIFIER (PA)					
Power Amplifier 1 (PA1)					
Transmit Power Maximum		13		dBm	
Transmit Power Minimum		−20		dBm	
Transmit Power Step Resolution		0.1		dB	
Transmit Power Variation vs. Temperature		±0.15			From −40°C to +85°C, transmit power = 13 dBm, RF frequency = 169 MHz
Transmit Power Variation vs. V_{DD}		±0.1			From V_{DD} = 2.2 V to V_{DD} = 3.6 V, transmit power = 13 dBm, RF frequency = 169 MHz
Transmit Power Accuracy		±0.3			transmit power = 13 dBm, RF frequency = 169 MHz
Power Amplifier 2 (PA2)					
Transmit Power Maximum					The maximum output power level achievable on PA2 depends on the programmable PA CREG3 LDO voltage setting; refer to the ADF7030-1 Software Reference Manual for further details
		17		dBm	2.85 V ≤ V_{DD} ≤ 3.6 V
		13		dBm	2.2 V ≤ V_{DD} ≤ 3.6 V
Transmit Power Minimum		−20		dBm	
Transmit Power Step Resolution		0.1		dB	
Transmit Power Variation vs. Temperature		±0.1		dB	From −40°C to +85°C, transmit power = 17 dBm, RF frequency = 169 MHz
Transmit Power Variation vs. V_{DD}		±0.1		dB	From V_{DD} = 3.0 V to V_{DD} = 3.6 V, transmit power = 17 dBm, RF frequency = 169 MHz
Transmit Power Accuracy		±0.25		dB	Transmit power = 17 dBm, RF frequency = 169 MHz
PA IMPEDANCE, 40-LEAD LFCSP PACKAGE					For guidance on impedance matching, refer to the ADF7030-1 Hardware Reference Manual
Optimum PA Load While in Transmit					
PA1					
f = 169 MHz		50 + j0		Ω	
f = 433 MHz, f = 460 MHz		45 + j30		Ω	
f = 868 MHz, f = 915 MHz		50 + j20		Ω	
PA2					
f = 169 MHz		38 + j0		Ω	
f = 433 MHz, f = 460 MHz		38 + j25		Ω	
f = 868 MHz, f = 915 MHz		38 + j18.5		Ω	
PA Input Impedance While in Rx					
PA1					
f = 169 MHz		7 − j232		Ω	
f = 433 MHz		5 − j102		Ω	
f = 460 MHz		5 − j96		Ω	
f = 868 MHz		4 − j49		Ω	
f = 915 MHz		4 − j46		Ω	
PA2					
f = 169 MHz		5 − j177		Ω	
f = 433 MHz		3 − j69		Ω	
f = 460 MHz		3 − j65		Ω	
f = 868 MHz		3 − j33		Ω	
f = 915 MHz		3 − j31		Ω	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PA IMPEDANCE, 48-LEAD LQFP PACKAGE					For guidance on impedance matching, refer to the ADF7030-1 Hardware Reference Manual
Optimum PA Load While in Transmit					
PA1					
f = 169 MHz		45 + j 8		Ω	
f = 433 MHz, f = 460 MHz		40 + j20		Ω	
f = 868 MHz		40 + j20		Ω	
f = 915 MHz		40 + j20		Ω	
PA2					
f = 169 MHz		37 + j 9		Ω	
f = 433 MHz, f = 460 MHz		30 + j25		Ω	
f = 868 MHz, f = 915 MHz		30 + j15		Ω	
PA Input Impedance While in Rx					
PA1					
f = 169 MHz		6 – j236		Ω	
f = 433 MHz, f = 460 MHz		6 – j87		Ω	
f = 868 MHz		5 – j37		Ω	
f = 915 MHz		5 – j34		Ω	
PA2					
f = 169 MHz		5 – j169		Ω	
f = 433 MHz, f = 460 MHz		4 – j58		Ω	
f = 868 MHz		3 – j22		Ω	
f = 915 MHz		3 – j19		Ω	

CURRENT CONSUMPTION

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSMIT CURRENT CONSUMPTION					In the PHY_TX state transmitting a carrier
f = 169.4 MHz					
Tx Power = 0 dBm, PA1		18		mA	
Tx Power = 10 dBm, PA1		31		mA	
Tx Power = 13 dBm, PA1		39		mA	
Tx Power = 17 dBm, PA2		65		mA	
f = 433 MHz					
Tx Power = 0 dBm, PA1		19		mA	
Tx Power = 10 dBm, PA1		31		mA	
Tx Power = 13 dBm, PA1		39		mA	
f = 460 MHz					
Tx Power = 17 dBm, PA2		50		mA	
f = 868 MHz, f = 915 MHz					
Tx Power = 0 dBm, PA1		20		mA	
Tx Power = 10 dBm, PA1		34		mA	
Tx Power = 13 dBm, PA1		43		mA	
Tx Power = 17 dBm, PA2		65		mA	
RECEIVE CURRENT CONSUMPTION					In the PHY_RX state, waiting for preamble
f = 169.4 MHz					
Data Rate = 4.8 kbps		24.8		mA	Narrow-band receive path
f = 433 MHz, f = 460 MHz					
Data Rate = 4.8 kbps		24.5		mA	Narrow-band receive path
Data Rate = 50 kbps		24		mA	Wideband receive path
f = 868 MHz, f = 915 MHz					
Data Rate = 5 kbps		23.2		mA	Narrow-band receive path
Data Rate = 12.5 kbps		21.2		mA	Wideband receive path
Data Rate = 50 kbps		21.4		mA	Wideband receive path
Data Rate = 100 kbps		23.7		mA	Wideband receive path
Data Rate = 150 kbps		24		mA	Wideband receive path
Data Rate = 300 kbps		25.4		mA	Wideband receive path
RADIO STATE CURRENT CONSUMPTION					
PHY_SLEEP State					
		2		nA	Memory not retained, no wakeup oscillator enabled, RTC disabled
		10		nA	Memory retained, no wakeup oscillator enabled, RTC disabled
		1		µA	Memory retained, internal 26 kHz RC oscillator enabled, RTC enabled
		1		µA	Memory retained, external 32 kHz oscillator enabled, RTC enabled
PHY_OFF State		1.9		mA	First entry to PHY_OFF after wake from PHY_SLEEP or after reset event
PHY_OFF State		3.7		mA	Second and subsequent entries to PHY_OFF after wake from PHY_SLEEP or after reset event
PHY_ON State		3.7		mA	

BAND SPECIFIC RECEIVE AND TRANSMIT

169.4 MHz to 169.6 MHz

Unless otherwise noted, the configurations detailed in Table 6 are used to specify the performance of the ADF7030-1 in Table 7. All measurements are performed on the EV-ADF70301-169BZ evaluation board, unless otherwise noted. The EV-ADF70301-169BZ uses a separate transmit/receive match design and a 26 MHz thermally compensated crystal oscillator (TCXO) reference. N/A means not applicable.

Table 6. Configurations in the 169.4 MHz to 169.6 MHz Frequency Band

Configuration Name	RF Frequency (MHz)	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	Channel Spacing (kHz)	IF Frequency (kHz)	Receiver BW (kHz)	Packet Setup for Packet-Based Testing
169.41875 MHz/ 0.1 kbps	169.41875	0.1	2GFSK	0.5	N/A	81.25	2.6	Preamble = 0xAAAA, sync word = 0xF672, payload length = 23 bytes, cyclic redundancy check (CRC) = 2 bytes
169.43125 MHz/ 2.4 kbps	169.43125	2.4	2GFSK	2.4	12.5	81.25	8.7	Preamble = 0x5555, sync word = 0xF672, payload length = 23 bytes, CRC = 2 bytes
169.41875 MHz/ 4.8 kbps	169.41875	4.8	2GFSK	2.4	12.5	81.25	10.6	Preamble = 0x5555, sync word = 0xF672, payload length = 23 bytes, CRC = 2 bytes
169.46875 MHz/ 6.4 kbps	169.46875	6.4	4GFSK	3.2 (outer deviation)	12.5	N/A (Tx only)	N/A (Tx only)	N/A

Table 7. Specifications in the 169.4 MHz to 169.6 MHz Frequency Band

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SENSITIVITY, PACKET ERROR RATE (PER)					
Configuration 169.41875 MHz/0.1 kbps		−134.3		dBm	At PER = 5%, automatic frequency control (AFC) disabled
Configuration 169.43125 MHz/2.4 kbps		−121.2		dBm	At PER = 5%, AFC enabled, RF frequency error range = ±11.5 ppm
Configuration 169.41875 MHz/4.8 kbps		−119.4		dBm	At PER = 5%, AFC enabled, RF frequency error range = ±11.5 ppm
CHANNEL SELECTIVITY AND BLOCKING—BER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (BER = 0.1%), carrier wave (CW) interferer power level increased until BER = 0.1%; AFC disabled, image calibrated
Configuration 169.43125 MHz/2.4 kbps					
Adjacent Channel (±12.5 kHz)		66		dB	
Alternate Channel (±25 kHz)		66		dB	
±2 MHz		94		dB	
±10 MHz		92		dB	
±20 MHz		102		dB	
Configuration 169.41875 MHz/4.8 kbps					
Adjacent Channel (±12.5 kHz)		55		dB	
Alternate Channel (±25 kHz)		63		dB	
±2 MHz		92		dB	
±10 MHz		90		dB	
CHANNEL SELECTIVITY AND BLOCKING—PER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled, image calibrated
Configuration 169.43125 MHz/2.4 kbps					
Adjacent Channel (±12.5 kHz)		62		dB	
Alternate Channel (±25 kHz)		70		dB	
±2 MHz		94		dB	
±10 MHz		96		dB	
Configuration 169.41875 MHz/4.8 kbps					
Adjacent Channel (±12.5 kHz)		55		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Alternate Channel (±25 kHz)		69		dB	
±2 MHz		91		dB	
±10 MHz		95		dB	
CHANNEL SELECTIVITY AND BLOCKING—ETSI EN 300 220-1 TEST METHOD					Measured as per EN 300 220-1 V2.4.1, AFC disabled
Configuration 169.43125 MHz/2.4 kbps					Desired signal level = −106.7 dBm (3 dB above the reference sensitivity level)
±2 MHz		−15		dBm	
±10 MHz		−12		dBm	
Configuration 169.41875 MHz/4.8 kbps					Desired signal level = −105.8 dBm (3 dB above the reference sensitivity level)
±2 MHz		−16		dBm	
±10 MHz		−13		dBm	
COCHANNEL REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled
Configuration 169.43125 MHz/2.4 kbps		−10		dB	
Configuration 169.41875 MHz/4.8 kbps		−10		dB	
CALIBRATED IMAGE REJECTION				dB	Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled, image calibrated
Configuration 169.43125 MHz/2.4 kbps		55		dB	
ADJACENT CHANNEL POWER (ACP)					Spectrum analyzer settings: resolution bandwidth (RBW) = 100 Hz, video bandwidth (VBW) = 300 Hz
Configuration 169.43125 MHz/2.4 kbps					PA1, output power = 13 dBm
Adjacent Channel		−83		dBc	
Alternate Channel		−82		dBc	
Configuration 169.41875 MHz/4.8 kbps					PA2, output power = 17 dBm
Adjacent Channel		−59		dBc	
Alternate Channel		−81		dBc	
Configuration 169.46875 MHz/6.4 kbps					PA1, output power = 13 dBm
Adjacent Channel		−68		dBc	
Alternate Channel		−81		dBc	
OCCUPIED BANDWIDTH (OBW)					Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings: RBW = 100 Hz, VBW = 300 Hz
Configuration 169.43125 MHz/2.4 kbps		6.3		kHz	PA1, output power = 13 dBm
Configuration 169.41875 MHz/4.8 kbps		7.8		kHz	PA2, output power = 17 dBm
Configuration 169.46875 MHz/6.4 kbps		8.2		kHz	PA1, output power = 13 dBm
SPURIOUS EMISSIONS (EXCLUDING HARMONICS)					Measured conductively at antenna input; RF frequency = 169.43125 MHz
Receive					
<1 GHz		−58		dBm	
1 GHz to 4 GHz		−49		dBm	
Transmit					PA2, output power = 17 dBm, transmitting continuous carrier wave
<1 GHz		−75		dBc	
1 GHz to 4 GHz		−78		dBc	
HARMONIC EMISSIONS					Measured conductively at antenna input, transmitting continuous carrier wave; RF frequency = 169.43125 MHz
17 dBm Output Power					PA2
Second Harmonic		−81		dBc	
Third Harmonic		−90		dBc	
All Other Harmonics		<−90		dBc	

433 MHz

Unless otherwise noted, the configuration detailed in Table 8 is used to specify the performance of the ADF7030-1 in Table 9. All measurements are performed on the EV-ADF70301-460BZ evaluation board, unless otherwise noted. The EV-ADF70301-460BZ uses a separate transmit/receive match design and a 26 MHz TCXO reference.

Table 8. 433 MHz Configurations

Configuration Name	RF Frequency (MHz)	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	Channel Spacing (kHz)	IF Frequency (kHz)	Receiver BW (kHz)	Packet Setup for Packet Based Testing
433 MHz/50 kbps	433	50	2GFSK	25	200	154	127	Preamble = 0xAAAA, sync word = 0xF672, payload length = 16 bytes, CRC = 2 bytes

Table 9. 433 MHz Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SENSITIVITY, PER					
Configuration 433 MHz/50 kbps		−108.2		dBm	At PER = 5%, AFC enabled, RF frequency error range = ±25 ppm
CHANNEL SELECTIVITY AND BLOCKING—BER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (BER = 0.1%), CW interferer power level increased until BER = 0.1%, image calibrated, AFC disabled
Configuration 433 MHz/50 kbps					
Adjacent Channel (±200 kHz)		48		dB	
Alternate Channel (±400 kHz)		58		dB	
±2 MHz		74		dB	
±10 MHz		83		dB	
±20 MHz		91		dB	
CHANNEL SELECTIVITY AND BLOCKING—PER BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, image calibrated, AFC enabled
Configuration 433 MHz/50 kbps					
Adjacent Channel (±200 kHz)		46		dB	
Alternate Channel (±400 kHz)		55		dB	
±2 MHz		71.5		dB	
±10 MHz		77		dB	
COCHANNEL REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled
Configuration 433 MHz/50 kbps		−10		dB	
CALIBRATED IMAGE REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled, image calibrated
Configuration 433 MHz/50 kbps		54		dB	
ACP					Spectrum analyzer settings: RBW = 100 Hz, VBW = 300 Hz
Configuration 433 MHz/50 kbps		−59		dBc	
OCCUPIED BANDWIDTH (OBW)					Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings: RBW = 100 Hz, VBW = 300 Hz
Configuration 433 MHz/50 kbps		86		kHz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPURIOUS EMISSIONS (EXCLUDING HARMONICS)					Measured conductively at antenna port; RF frequency = 433 MHz
Receive					
<1 GHz		−82		dBm	
1 GHz to 4 GHz		−47		dBm	
Transmit					PA1, output power = 10 dBm, transmitting continuous carrier wave
<1 GHz		−53		dBc	
1 GHz to 4 GHz		−76		dBc	
HARMONIC EMISSIONS					Measured conductively at antenna input, transmitting continuous carrier wave; RF frequency = 433 MHz, PA1, output power = 10 dBm
Second Harmonic		−64		dBc	
All Other Harmonics		<−90		dBc	

450 MHz to 470 MHz

Unless otherwise noted, the configuration detailed in Table 10 is used to specify the performance of the ADF7030-1 in Table 11. All measurements are performed on the EV-ADF70301-460BZ evaluation board, unless otherwise noted. The EV-ADF70301-460BZ uses a separate transmit/receive match design and a 26 MHz TCXO reference.

Table 10. Configurations in the 450 MHz to 470 MHz Frequency Band

Configuration Name	RF Frequency (MHz)	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	Channel Spacing (kHz)	IF Frequency (kHz)	Receiver BW (kHz)	Packet Setup for Packet Based Testing
460 MHz/7.2 kbps	460	7.2	2GFSK	2.0	12.5	81.25	11.7	Preamble = 0xAAAA, sync word = 0xF672, payload length = 23 bytes, CRC = 2 bytes

Table 11. Specifications in the 450 MHz to 470 MHz Frequency Band

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SENSITIVITY, PER					
Configuration 460 MHz/7.2 kbps		−116		dBm	At PER = 5%, AFC enabled, RF frequency error range = ±3.9 ppm
CHANNEL SELECTIVITY AND BLOCKING—BER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (BER = 0.1%), CW interferer power level increased until BER = 0.1%, image calibrated, AFC disabled
Configuration 460 MHz/7.2 kbps					
Adjacent Channel (±12.5 kHz)		54		dB	
Alternate Channel (±25 kHz)		61		dB	
±2 MHz		84		dB	
±10 MHz		92		dB	
±20 MHz		98		dB	
CHANNEL SELECTIVITY AND BLOCKING—PER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, image calibrated, AFC enabled
Configuration 460 MHz/7.2 kbps					
Adjacent Channel (±12.5 kHz)		38		dB	
Alternate Channel (±25 kHz)		57		dB	
±2 MHz		80		dB	
±10 MHz		85		dB	
COCHANNEL REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled
Configuration 460 MHz/7.2 kbps		10		dB	
CALIBRATED IMAGE REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled, image calibrated
Configuration 460 MHz/7.2 kbps		51		dB	
ACP					Spectrum analyzer settings: RBW = 100 Hz, VBW = 300 Hz
Configuration 460 MHz/7.2 kbps		−45		dBc	
OBW					Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings: RBW = 100 Hz, VBW = 300 Hz
Configuration 460 MHz/7.2 kbps		7.7		kHz	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SPURIOUS EMISSIONS (EXCLUDING HARMONICS)					Measured conductively at antenna port; RF frequency = 460 MHz
Receive					
<960 MHz		−57		dBm	
960 MHz to 12.7 GHz		−66		dBm	
Transmit					PA2, output power = 17 dBm, transmitting continuous carrier wave
<960 MHz		−59		dBc	
960 MHz to 12.7 GHz		−76		dBc	
HARMONIC EMISSIONS					Measured conductively at antenna port, transmitting continuous carrier wave; RF frequency = 460 MHz, output power = 17 dBm, PA2
Second Harmonic		−60		dBc	
All Other Harmonics		< −90		dBc	

863 MHz to 876 MHz

Unless otherwise noted, the configurations detailed in Table 12 are used to specify the performance of the ADF7030-1 in Table 13. All measurements are performed on the EV-ADF70301-868BZ evaluation board, unless otherwise noted. The EV-ADF70301-868BZ uses a separate transmit/receive match design and a 26 MHz TCXO reference.

Table 12. Configurations in the 863 MHz to 876 MHz Frequency Band

Configuration Name	RF Frequency (MHz)	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	Channel Spacing (kHz)	IF Frequency (kHz)	Receiver BW (kHz)	Packet Setup for Packet Based Testing
868 MHz/4.8 kbps	868	4.8	2GFSK	2.4	12.5	81.25	10.6	Preamble = 0xAAAA, sync word = 0xF672, payload length = 23 bytes, CRC = 2 bytes
868 MHz/100 kbps	868	100	2FSK	50	500	241	231	Preamble = 0xAAAAAAAA, sync word = 0x543D54CD, payload length = 20 bytes, CRC = 2 bytes

Table 13. Specifications in the 863 MHz to 876 MHz Frequency Band

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SENSITIVITY, PER					
Configuration 868 MHz/4.8 kbps		−118.5		dBm	At PER = 5%, AFC enabled, RF frequency error range = ±3 ppm
Configuration 868 MHz/100 kbps		−106		dBm	At PER = 5%, AFC enabled, RF frequency error range = ±25 ppm, data rate error range = ±100 ppm, frequency deviation error range = ±25%
CHANNEL SELECTIVITY AND BLOCKING—BER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (BER = 0.1%), CW interferer power level increased until BER = 0.1%, image calibrated, AFC disabled
Configuration 868 MHz/4.8 kbps					
Adjacent Channel (±12.5 kHz)		56		dB	
Alternate Channel (±25 kHz)		56		dB	
±2 MHz		78		dB	
±10 MHz		87		dB	
±20 MHz		98		dB	
CHANNEL SELECTIVITY AND BLOCKING—PER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, image calibrated, AFC enabled
Configuration 868 MHz/4.8 kbps					
Adjacent Channel (±12.5 kHz)		47		dB	
Alternate Channel (±25 kHz)		55		dB	
±2 MHz		79		dB	
±10 MHz		90		dB	
Configuration 868 MHz/100 kbps					
Adjacent Channel (±500 kHz)		44		dB	
Alternate Channel (±1000 kHz)		59		dB	
±2 MHz		65		dB	
±10 MHz		76		dB	
COCHANNEL REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled
Configuration 868 MHz/4.8 kbps		−10		dB	
Configuration 868 MHz/100 kbps		−10		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
UNCALIBRATED IMAGE REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, AFC enabled
Configuration 868 MHz/4.8 kbps		35		dB	
Configuration 868 MHz/100 kbps		35		dB	
ACP					Spectrum analyzer settings: RBW = 100 Hz, VBW = 300 Hz
Configuration 868 MHz/4.8 kbps		−65		dBc	
Configuration 868 MHz/100 kbps		−41		dBc	
OBW					Occupied bandwidth is the bandwidth containing 99% of the total integrated power; spectrum analyzer settings: RBW = 100 Hz, VBW = 300 Hz
Configuration 868 MHz/4.8 kbps		7.8		kHz	
Configuration 868 MHz/100 kbps		226		kHz	
SPURIOUS EMISSIONS (EXCLUDING HARMONICS)					Measured conductively at antenna input; RF Frequency = 868 MHz
Receive					
<1 GHz		−58		dBm	
1 GHz to 4 GHz		−46		dBm	
Transmit					PA2, 17dBm output power, transmitting continuous carrier wave
<1 GHz		−74		dBc	
1 GHz to 4 GHz		−77		dBc	
HARMONIC EMISSIONS					Measured conductively at antenna input, transmitting continuous carrier wave; RF frequency = 868 MHz
13 dBm Output Power					PA1
Second Harmonic		−50		dBc	
Third Harmonic		−78		dBc	
Seventh Harmonic		−88		dBc	
All Other Harmonics		<−90		dBc	
17 dBm Output Power					PA2
Second Harmonic		−55		dBc	
Third Harmonic		−73		dBc	
All Other Harmonics		<−90		dBc	

902 MHz to 928 MHz

Unless otherwise noted, the configurations detailed in Table 14 are used to specify the performance of the ADF7030-1 in Table 15. All measurements are performed on the EV-ADF70301-868BZ evaluation board, unless otherwise noted. The EV-ADF70301-868BZ uses a separate transmit/receive match design and a 26 MHz TCXO reference.

Table 14. Configurations in the 902 MHz to 928 MHz Frequency Band

Configuration Name	RF Frequency (MHz)	Data Rate (kbps)	Modulation	Frequency Deviation (kHz)	Channel Spacing (kHz)	IF Frequency (kHz)	Receiver BW (kHz)	Packet Setup for Packet Based Testing
915 MHz/ 50 kbps	915	50	2GFSK	25	200	154	127	Preamble = 0xAAAAAAAA, sync word = 0x904E, payload length = 100 bytes, CRC = 2 bytes
915 MHz/ 150 kbps	915	150	2GFSK	37.5	400	336	250	Preamble = 0xAAAAAAAAAAAAAAAAAAAAAAAA , sync word = 0xFF7D7F5D, payload length = 100 bytes, CRC = 2 bytes
915 MHz/ 300 kbps	915	300	2GFSK	120	600	540	530	Preamble = 0xAAAAAAAA, sync word = 0xF672, payload length = 23 bytes, CRC = 2 bytes

Table 15. 902 MHz to 928 MHz Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
2GFSK SENSITIVITY, PER					
Configuration 915 MHz/50 kbps		−108.2		dBm	At PER = 5%, FEC disabled, AFC enabled, RF frequency error range = ±40 ppm
Configuration 915 MHz/150 kbps		−100.5		dBm	At PER = 5%, FEC disabled, AFC enabled, RF frequency error range = ±40 ppm
Configuration 915 MHz/300 kbps		−102		dBm	At PER = 5%, AFC disabled, RF frequency error range = ±11.5 ppm
CHANNEL SELECTIVITY AND BLOCKING—BER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (BER = 0.1%), CW interferer power level increased until BER = 0.1%, AFC disabled
Configuration 915 MHz/150 kbps					
Adjacent Channel (±400 kHz)		46		dB	
Alternate Channel (±800 kHz)		56		dB	
±2 MHz		66		dB	
±10 MHz		77		dB	
±20 MHz		83		dB	
CHANNEL SELECTIVITY AND BLOCKING—PER-BASED TEST METHOD					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%, image calibrated
Configuration 915 MHz/50 kbps					FEC disabled, AFC enabled
Adjacent Channel (±200 kHz)		44.5		dB	
Alternate Channel (±400 kHz)		52		dB	
±2 MHz		67		dB	
±10 MHz		77		dB	
Configuration 915 MHz/150 kbps					FEC disabled, AFC enabled
Adjacent Channel (±400 kHz)		43.5		dB	
Alternate Channel (±800 kHz)		44		dB	
±2 MHz		60.5		dB	
±10 MHz		70		dB	
Configuration 915 MHz/300 kbps					AFC disabled
Adjacent Channel (±600 kHz)		28		dB	
Alternate Channel (±1200 kHz)		33		dB	
±2 MHz		62		dB	
±10 MHz		72		dB	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
COCHANNEL REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%
Configuration 915 MHz/50 kbps		−10		dB	
Configuration 915 MHz/150 kbps		−10		dB	
Configuration 915 MHz/300 kbps		−10		dB	
UNCALIBRATED IMAGE REJECTION					Desired signal 3 dB above the input sensitivity level (PER = 5%), CW interferer power level increased until PER = 5%
Configuration 915 MHz/50 kbps		35		dB	
Configuration 915 MHz/150 kbps		35		dB	
Configuration 915 MHz/300 kbps		35		dB	
ACP					
Configuration 915 MHz/50 kbps					Spectrum analyzer settings: RBW = 300 Hz, VBW = 1 kHz
Adjacent Channel (±200 kHz)		−55		dBc	
Alternate Channel (±400 kHz)		−62		dBc	
Configuration 915 MHz/150 kbps					Spectrum analyzer settings: RBW = 300 Hz, VBW = 1 kHz
Adjacent Channel (±400 kHz)		−53		dBc	
Alternate Channel (±800 kHz)		−66		dBc	
Configuration 915 MHz/300 kbps					Spectrum analyzer settings: RBW = 300 Hz, VBW = 1 kHz
Adjacent Channel (±600 kHz)		−30.5		dBc	
Alternate Channel (±1200 kHz)		−66		dBc	
OCCUPIED BANDWIDTH					Occupied bandwidth is the bandwidth containing 99% of the total integrated power
Configuration 915 MHz/50 kbps		85		kHz	Spectrum analyzer settings: RBW = 300 Hz, VBW = 1 kHz
Configuration 915 MHz/150 kbps		167		kHz	Spectrum analyzer settings: RBW = 300 Hz, VBW = 1 kHz
Configuration 915 MHz/300 kbps		475		kHz	Spectrum analyzer settings: RBW = 300 Hz, VBW = 1 kHz
SPURIOUS EMISSIONS (EXCLUDING HARMONICS)					Measured conductively at antenna input; RF frequency = 915 MHz
Receive					
<960 MHz		−82		dBm	
960 MHz to 12.7 GHz		−47		dBm	
Transmit					PA2, output power = 17 dBm, transmitting continuous carrier wave
<960 MHz		−71		dBc	
960 MHz to 12.7 GHz		−73		dBc	
HARMONIC EMISSIONS					Measured conductively at antenna input, transmitting continuous carrier wave; RF frequency = 915 MHz
13 dBm Output Power					PA1
Second Harmonic		−53		dBc	
Third Harmonic		−83		dBc	
Seventh Harmonic		−88		dBc	
All Other Harmonics		<−90		dBc	
17 dBm Output Power					PA2
Second Harmonic		−54		dBc	
Third Harmonic		−66		dBc	
All Other Harmonics		<−90		dBc	

EXTERNAL 26 MHz OSCILLATOR

The ADF7030-1 requires a 26 MHz reference clock. This reference can be a 26 MHz crystal oscillator operating in parallel mode and connected between the HFXTALP and HFXTALN pins. Alternatively, a 26 MHz TCXO can be dc-coupled to the HFXTALN input. A TCXO is typically used in narrow-band applications where the transmit and receive RF frequency must meet accuracies not supported by a crystal oscillator.

Table 16.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC-COUPLED TCXO					HFXTALN pin, clipped sine wave
TCXO Frequency		26		MHz	
Peak-to-Peak Voltage Level	0.8		1.8	V	
Voltage Level with Respect to Ground	−0.1		+1.9	V	
Duty Cycle	40		60	%	
CRYSTAL OSCILLATOR					Parallel resonant crystal
Crystal Frequency		26		MHz	
Maximum Crystal ESR			50	Ω	
Crystal Oscillator Load Capacitance		12		pF	
HFXTALN, HFXTALP Pin Capacitance in Parallel with Crystal Oscillator		5		pF	

LOW FREQUENCY OSCILLATOR

Table 17.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
26 kHz INTERNAL RC OSCIALLATOR					
Frequency		26		kHz	After calibration
Frequency Accuracy		0.2		%	After calibration at 25°C
Frequency Drift					
Temperature Coefficient		0.3		%/°C	
Voltage Coefficient		0.5		%/V	
Calibration Time		30		ms	
32 kHz EXTERNAL OSCILLATOR					
Frequency		32.768		kHz	
Start-Up Time		1.45		sec	

TEMPERATURE SENSOR

Table 18.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR					
Range	−40		+85	°C	
Accuracy		±5		°C	T_A = −40°C to +85°C; calibrated at 25°C

DIGITAL INPUT/OUTPUT

Table 19.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS						
Input Voltage						
High	V_{INH}	$0.7 \times V_{DD}$			V	
Low	V_{INL}			$0.2 \times V_{DD}$	V	
Input Capacitance	C_{IN}		3.6		pF	
LOGIC OUTPUTS						
Output Voltage						
High	V_{OH}	$V_{DD} - 0.4$			V	I_{OH} = 500 µA
Low	V_{OL}			0.4	V	I_{OL} = 500 µA
Maximum GPIO Drive Strength for V_{OH}			2		mA	
Maximum GPIO Drive Strength for V_{OL}			2		mA	

DIGITAL TIMING

Table 20. SPI Interface Timing

Parameter	Description	Min	Typ	Max	Unit
t_1	Falling edge to MISO setup time			15	ns
t_2	$\overline{CS}$ low to SCLK setup time	40			ns
t_3	SCLK high time	40			ns
t_4	SCLK low time	40			ns
t_5	SCLK period	80			ns
t_6	SCLK falling edge to MISO delay			10	ns
t_7	MOSI to SCLK rising edge setup time	5			ns
t_8	MOSI to SCLK rising edge hold time	5			ns
t_9	SCLK falling edge to $\overline{CS}$ hold time	40			ns
t_{10}	$\overline{CS}$ high time	80			ns
t_{11}	$\overline{CS}$ low to MISO high wake-up time		92		µs
t_{12}	MISO high to SCLK setup time	SCLK low time[1]			µs
t_{13}	$\overline{RST}$ low time	2			µs

[1] The minimum for t_{12} changes with the SCLK frequency.

Timing Diagrams

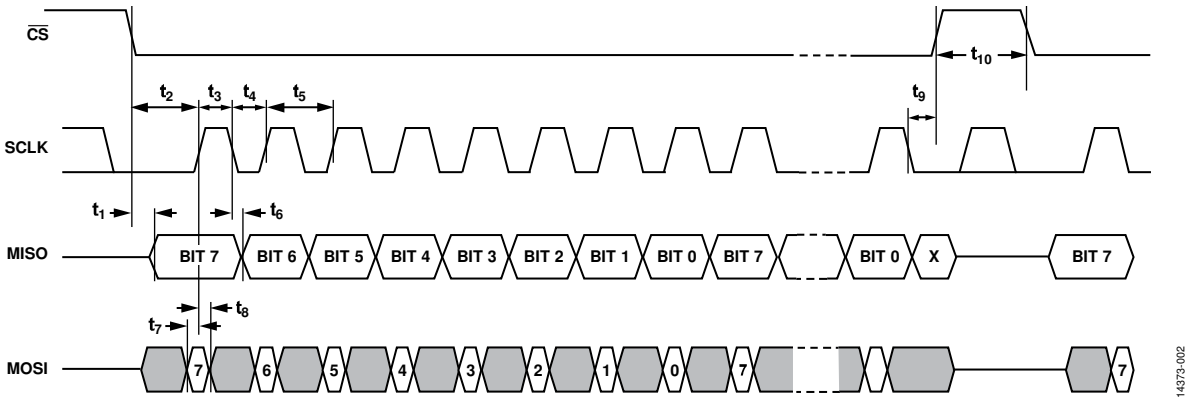

Figure 2. SPI Interface Timing

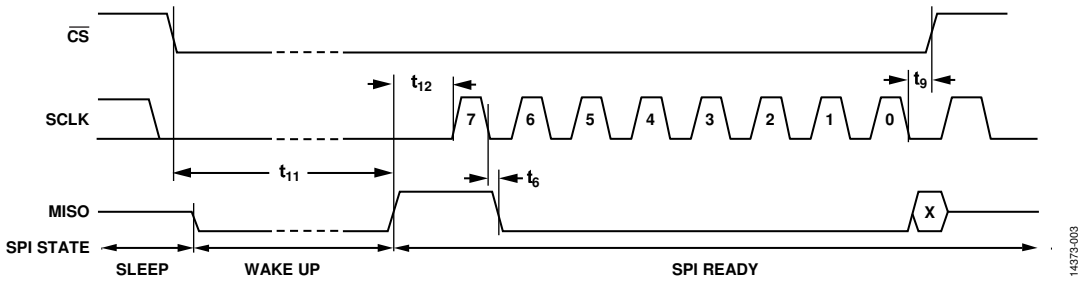

Figure 3. PHY_SLEEP to SPI Ready State Timing

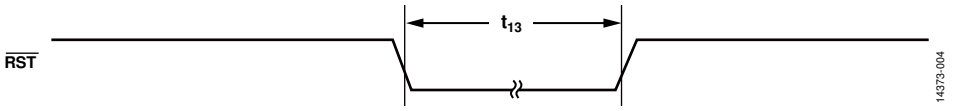

Figure 4. Reset Pin ($\overline{RST}$) Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All VBATx pins must be tied together. The LNAIN1 and LNAIN2 inputs must be ac-coupled.

Table 21.

Parameter	Rating
Supply Pins	
VBAT1, VBAT2, VBAT3, VBAT4, VBAT5, VBAT6 to Ground	−0.3 V to +3.9 V
LNAIN1, LNAIN2	−0.3 V to +1.98 V
PAOUT1, PAOUT2	−0.3 V to +3.9 V
HFXTALP, HFXTALN	−0.3 V to +1.98 V
CLF	−0.3 V to +1.98 V
CREG1, CREG2, CREG4, CREG5, CREG6, CREG7	−0.3 V to +1.98 V
CREG3	−0.3 V to +3.9 V
Digital Inputs/Outputs, GPIOx	−0.3 V to +3.9 V
MOSI, MISO, SCLK, $\overline{CS}$, $\overline{RST}$	−0.3 V to +3.9 V
Industrial Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
θ_{JA} Thermal Impedance	26°C/W
ESD Rating, Human Body Model (HBM)	
40-Lead LFCSP Package	
LNAIN1, LNAIN2, PAOUT1, PAOUT2	±250 V
All Other Pins	±2 kV
48-Lead LQFP Package	
LNAIN1, LNAIN2, PAOUT1, PAOUT2	±250 V
All Other Pins	±2 kV
ESD Rating, Field Induced Charged Device Model (FICDM)	
40-Lead LFCSP Package	
LNAIN1, LNAIN2, PAOUT1, PAOUT2	±1250 V
All Other Pins	±1250 V
48-Lead LQFP Package	
LNAIN1, LNAIN2, PAOUT1, PAOUT2	±1250 V
All Other Pins	±1250 V
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Connect the exposed pad of the 40-lead LFCSP device to ground.

This device is a high performance, RF integrated circuit with an ESD rating as indicated in Table 21; it is ESD sensitive. Take proper precautions for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

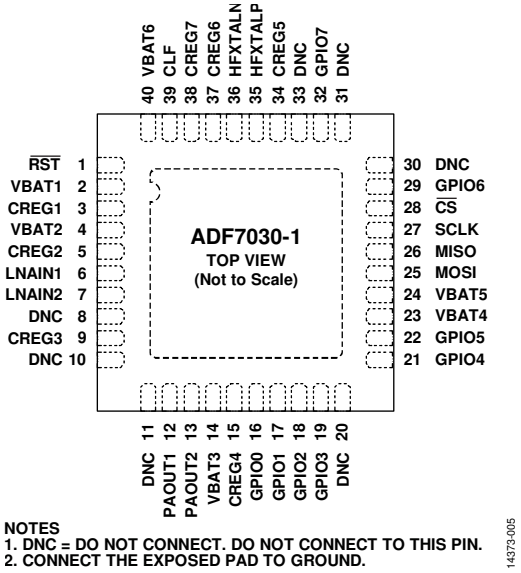

Figure 5. 40-Lead LFCSP Pin Configuration

Table 22. 40-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RST}}$	External Reset, Active Low.
2	VBAT1	Power Supply Pin 1 to the Internal Regulators.
3	CREG1	Regulator Output 1. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection. Also, place a 1.2 nF capacitor between this pin and the CLF pin.
4	VBAT2	Power Supply Pin 2 to the Internal Regulators.
5	CREG2	Regulator Output 2. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
6	LNAIN1	LNA Input 1.
7	LNAIN2	LNA Input 2.
8	DNC	Do Not Connect. Do not connect to this pin.
9	CREG3	Regulator Output 3. Connect this pin to the PA choke inductor to provide bias to the PA. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
10	DNC	Do Not Connect. Do not connect to this pin.
11	DNC	Do Not Connect. Do not connect to this pin.
12	PAOUT1	Single-Ended PA1 Output.
13	PAOUT2	Single-Ended PA2 Output.
14	VBAT3	Power Supply Pin 3 to the Internal Regulators.
15	CREG4	Regulator Output 4. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
16	GPIO0	Digital GPIO Pin 0.
17	GPIO1	Digital GPIO Pin 1.
18	GPIO2	Digital GPIO Pin 2.
19	GPIO3	Digital GPIO Pin 3.
20	DNC	Do Not Connect. Do not connect to this pin.
21	GPIO4	Digital GPIO Pin 4.
22	GPIO5	Digital GPIO Pin 5.
23	VBAT4	Power Supply Pin 4 to the Internal Regulators.
24	VBAT5	Power Supply Pin 5 to the Internal Regulators.
25	MOSI	Serial Port Master Output/Slave Input.
26	MISO	Serial Port Master Input/Slave Output.
27	SCLK	Serial Port Clock.
28	$\overline{\text{CS}}$	Chip Select (Active Low). A pull-up resistor of 100 kΩ to V_{DD} is recommended to prevent the host processor from inadvertently waking the ADF7030-1 from sleep.

Pin No.	Mnemonic	Description
29	GPIO6	Digital GPIO Pin 6.
30	DNC	Do Not Connect. Do not connect to this pin.
31	DNC	Do Not Connect. Do not connect to this pin.
32	GPIO7	Digital GPIO Pin 7.
33	DNC	Do Not Connect. Do not connect to this pin.
34	CREG5	Regulator Output 5. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
35	HFXTALP	Positive Reference Input. If a 26 MHz TCXO is used as the external reference, do not connect this pin. If a 26 MHz XTAL is used as the reference, connect this pin to the XTAL.
36	HFXTALN	Negative Reference Input. If a 26 MHz TCXO is used as the external reference, connect this pin to the TCXO output. If a 26 MHz XTAL is used as the reference, connect this pin to the XTAL.
37	CREG6	Regulator Output 6. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
38	CREG7	Regulator Output 7. Place a 220 nF capacitor between this pin and ground for regulator stability and noise rejection.
39	CLF	External Loop Filter Capacitor. Place a 1.2 nF capacitor between this pin and the CREG1 pin.
40	VBAT6	Power Supply Pin 6 to the Internal Regulators.
	EPAD	Exposed Pad. Connect the exposed pad to ground.