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Low Power IEEE 802.15.4 Zero-IF 2.4 GHz Transceiver IC

ADF7241

FEATURES

- Frequency range (global ISM band)
  - 2400 MHz to 2483.5 MHz
- IEEE 802.15.4-2006-compatible (250 kbps)
- Low power consumption
  - 19 mA (typical) in receive mode
  - 21.5 mA (typical) in transmit mode (P_O = 3 dBm)
  - 1.7 µA, 32 kHz crystal oscillator wake-up mode
- High sensitivity
  - −95 dBm at 250 kbps
- Programmable output power
  - −20 dBm to +4.8 dBm in 2 dB steps
- Integrated voltage regulators
  - 1.8 V to 3.6 V input voltage range
- Excellent receiver selectivity and blocking resilience
  - Zero-IF architecture
  - Complies with EN300 440 Class 2, EN300 328, FCC CFR47 Part 15, ARIB STD-T66
- Digital RSSI measurement
- Fast automatic VCO calibration
- Automatic RF synthesizer bandwidth optimization
- On-chip low power processor performs
  - Radio control
  - Packet management
- Packet management support
  - Insertion/detection of preamble address/SFD/FCS
  - IEEEE 802.15.4-2006 frame filtering
  - IEEEE 802.15.4-2006 CSMA/CA unslotted modes
- Flexible 256-byte transmit/receive data buffer
- SPORT mode
- Flexible multiple RF port interface
  - External PA/LNA support hardware
  - Switched antenna diversity support
- Wake-up timer
- Very few external components
  - Integrated PLL loop filter, receive/transmit switch, battery monitor, temperature sensor, 32 kHz RC and crystal oscillators
- Flexible SPI control interface with block read/write access
- Small form factor 5 mm × 5 mm 32-lead LFCSP package

APPLICATIONS

- Wireless sensor networks
- Automatic meter reading/smart metering
- Industrial wireless control
- Healthcare
- Wireless audio/video
- Consumer electronics
- ZigBee

FUNCTIONAL BLOCK DIAGRAM

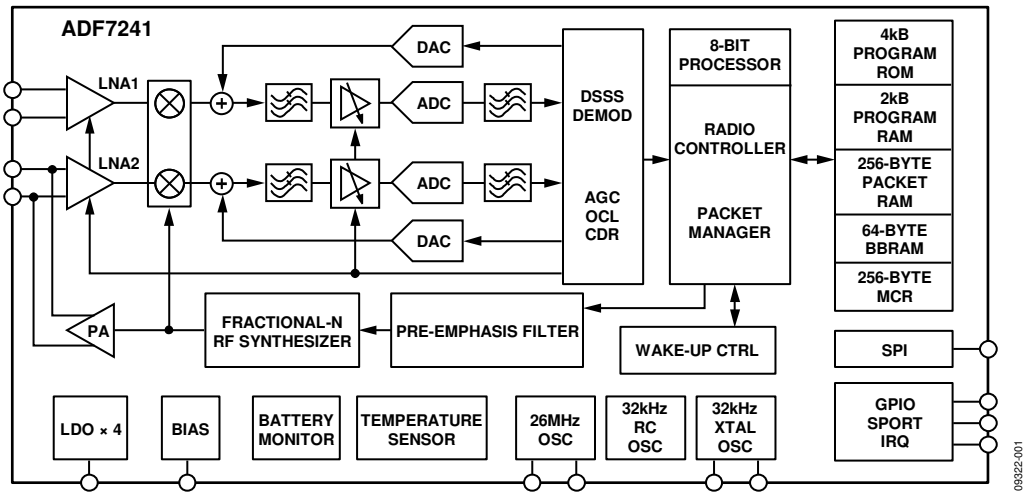

Figure 1.

Rev. 0

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Tel: 781.329.4700 www.analog.com
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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADF7241 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1082: Automatic IEEE 802.15.4 Operating Modes
- AN-1151: Using a Johanson 2450BM14E0007 Impedance-Matched, Integrated Filter Balun with the ADF7241 and ADF7242
- AN-1268: Reference Design Using the ADF7241/ADF7242 and Skyworks SE2431L

Data Sheet

- ADF7241: Low Power IEEE 802.15.4 Zero-IF 2.4 GHz Transceiver IC

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADF7241 Evaluation Software

TOOLS AND SIMULATIONS

- ADIsimSRD Design Studio

REFERENCE MATERIALS

Press

- Elster Selects ADI's Smart Metering Solution for Gas and Electricity Meters

Technical Articles

- Low Power, Low Cost, Wireless ECG Holter Monitor
- RF Meets Power Lines: Designing Intelligent Smart Grid Systems that Promote Energy Efficiency
- Smart Metering Technology Promotes Energy Efficiency for a Greener World
- The Use of Short Range Wireless in a Multi-Metering System
- Understand Wireless Short-Range Devices for Global License-Free Systems
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- ADF7241 Material Declaration
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REVISION HISTORY

1/11—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADF7241 is a highly integrated, low power, and high performance transceiver for operation in the global 2.4 GHz ISM band. It is designed with emphasis on flexibility, robustness, ease of use, and low current consumption. The IC supports the IEEE 802.15.4-2006 2.4 GHz PHY requirements in both packet and data streaming modes. With a minimum number of external components, it achieves compliance with the FCC CFR47 Part 15, ETSI EN 300 440 (Equipment Class 2), ETSI EN 300 328 (FHSS, DR > 250 kbps), and ARIB STD T-66 standards.

The ADF7241 complies with the IEEE 802.15.4-2006 2.4 GHz PHY requirements with a fixed data rate of 250 kbps and DSSS-OQPSK modulation. The transmitter path of the ADF7241 is based on a direct closed-loop VCO modulation scheme using a low noise fractional-N RF frequency synthesizer. The automatically calibrated VCO operates at twice the fundamental frequency to reduce spurious emissions and avoid PA pulling effects. The bandwidth of the RF frequency synthesizer is automatically optimized for transmit and receive operations to achieve best phase noise, modulation quality, and synthesizer settling time performance. The transmitter output power is programmable from −20 dBm to +4 dBm with automatic PA ramping to meet transient spurious specifications. An integrated biasing and control circuit is available in the IC to significantly simplify the interface to external PAs.

The receive path is based on a zero-IF architecture enabling very high blocking resilience and selectivity performance, which are critical performance metrics in interference dominated environments such as the 2.4 GHz band. In addition, the architecture does not suffer from any degradation of blocker rejection in the image channel, which is typically found in low IF receivers. The IC can operate with a supply voltage between 1.8 V and 3.6 V with very low power consumption in receive and transmit modes while maintaining its excellent RF performance, making it especially suitable for battery-powered systems.

The ADF7241 features a flexible dual-port RF interface that can be used with an external LNA and/or PA in addition to supporting switched antenna diversity.

The ADF7241 incorporates a very low power custom 8-bit processor that supports a number of transceiver management functions. These functions are handled by the two main modules of the processor: the radio controller and the packet manager.

The radio controller manages the state of the IC in various operating modes and configurations. The host MCU can use single byte commands to interface to the radio controller. In transmit mode, the packet manager can be configured to add preamble and SFD to the payload data stored in the on-chip packet RAM. In receive mode, the packet manager can detect and generate an interrupt to the MCU upon receiving a valid SFD, and store the received data payload in the packet RAM. A total of 256 bytes of transmit and receive packet RAM space is provided to decouple the over-the-air data rate from the host MCU processing speed. Thus, the ADF7241 packet manager eases the processing burden on the host MCU and saves the overall system power consumption.

In addition, for applications that require data streaming, a synchronous bidirectional serial port (SPORT) provides bit-level input/output data, and has been designed to directly interface to a wide range of DSPs, such as ADSP-21xx, SHARC®, TigerSHARC®, and Blackfin®. The SPORT interface can optionally be used.

The processor also permits the download and execution of a set of firmware modules, which include IEEE 802.15.4 automatic modes, such as node address filtering, as well as unslotted CSMA/CA. Execution code for these firmware modules is available from Analog Devices, Inc.

To further optimize the system power consumption, the ADF7241 features an integrated low power 32 kHz RC wake-up oscillator, which is calibrated from the 26 MHz crystal oscillator while the transceiver is active. Alternatively, an integrated 32 kHz crystal oscillator can be used as a wake-up timer for applications requiring very accurate wake-up timing. A battery backed-up RAM (BBRAM) is available on the IC where IEEE 802.15.4-2006 network node addresses can be retained when the IC is in the sleep state.

The ADF7241 also features a very flexible interrupt controller, which provides MAC-level and PHY-level interrupts to the host MCU. The IC is equipped with a SPI interface, which allows burst mode data transfer for high data throughput efficiency. The IC also integrates a temperature sensor with digital read-back and a battery monitor.

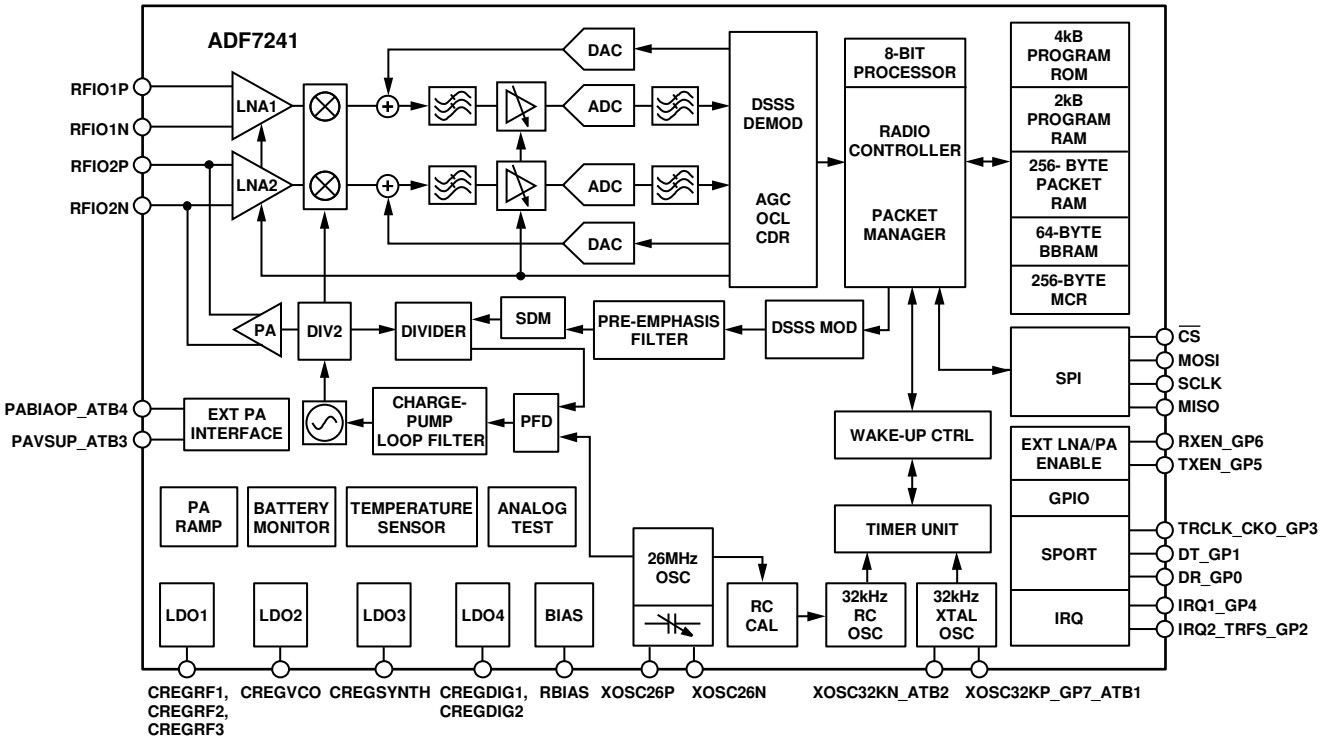

Figure 2. Detailed Functional Block Diagram

SPECIFICATIONS

VDD_BAT = 1.8 V to 3.6 V, GND = 0 V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical specifications are at VDD_BAT = 3.6 V, T_A = 25°C, $f_{CHANNEL}$ = 2450 MHz. All measurements are performed using the ADF7241 reference design, RFIO2 port, unless otherwise noted.

GENERAL SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions
GENERAL PARAMETERS					
Voltage Supply Range					
VDD_BAT Input	1.8		3.6	V	
Frequency Range	2400		2483.5	MHz	
Operating Temperature Range	−40		+85	°C	
Data Rate		250		kbps	

RF FREQUENCY SYNTHESIZER SPECIFICATIONS

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions
CHANNEL FREQUENCY RESOLUTION		10		kHz	
PHASE ERROR		3		Degrees	Receive mode; integration bandwidth from 10 kHz to 400 kHz
		1.5		Degrees	Transmit mode; integration bandwidth from 10 kHz to 1800 kHz
VCO CALIBRATION TIME		52		µs	Applies to all modes
SYNTHESIZER SETTLING TIME					Frequency synthesizer settled to <±5 ppm of the target frequency within this time following a VCO calibration
		53		µs	Receive mode
		80		µs	Transmit mode
PHASE NOISE					Receive mode
		−135		dBc/Hz	10 MHz frequency offset
		−145		dBc/Hz	≥50 MHz frequency offset
REFERENCE AND CLOCK-RELATED SPURIOUS		70		dBc	Receive mode; $f_{CHANNEL}$ = 2405 MHz, 2450 MHz, and 2480 MHz
INTEGER BOUNDARY SPURS		60		dBc	Receive mode; measured at 400 kHz offset from $f_{CHANNEL}$ = 2405 MHz, 2418 MHz, 2431 MHz, 2444 MHz, 2457 MHz, 2470 MHz
CRYSTAL OSCILLATOR					
Crystal Frequency		26		MHz	Parallel load resonant crystal
Maximum Parallel Load Capacitance		18		pF	
Minimum Parallel Load Capacitance		7		pF	
Maximum Crystal ESR		365.3		Ω	Guarantees maximum crystal frequency error of 0.2 ppm; 33 pF on XOSC26P and XOSC26N
Sleep-to-Idle Wake-Up Time		300		µs	15 pF load on XOSC26N and XOSC26P

TRANSMITTER SPECIFICATIONS

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions
TRANSMITTER SPECIFICATIONS					
Maximum Transmit Power		3		dBm	
Minimum Transmit Power		−25		dBm	
Maximum Transmit Power (High Power Mode)		4.8		dBm	Refer to Power Amplifier section for details on how to enable this mode
Minimum Transmit Power (High Power Mode)		−22		dBm	
Transmit Power Variation		2		dB	Transmit power = 3 dBm, $f_{CHANNEL}$ = 2400 MHz to 2483.5 MHz, T_A = −40°C to +85°C, VDD_BAT = 1.8 V to 3.6 V
Transmit Power Control Resolution		2		dB	Transmit power = 3 dBm
Optimum PA Matching Impedance		43.7 + 35.2j		Ω	For maximum transmit power = 3 dBm
Harmonics and Spurious Emissions					
Compliance with ETSI EN 300 440					
25 MHz to 30 MHz			−36	dBm	Unmodulated carrier, 10 kHz RBW[1]
30 MHz to 1 GHz			−36	dBm	Unmodulated carrier, 100 kHz RBW[1]
47 MHz to 74 MHz, 87.5 MHz to 118 MHz, 174 MHz to 230 MHz, 470 MHz to 862 MHz			−54	dBm	Unmodulated carrier, 100 kHz RBW[1]
Otherwise Above 1 GHz			−30	dBm	Unmodulated carrier, 1 MHz RBW[1]
Compliance with ETSI EN 300 328					
1800 MHz to 1900 MHz			−47	dBm	Unmodulated carrier
5150 MHz to 5300 MHz			−97	dBm/Hz	
Compliance with FCC CFR47, Part15					
4.5 GHz to 5.15 GHz			−41	dBm	1 MHz RBW[1]
7.25 GHz to 7.75 GHz			−41	dBm	1 MHz RBW[1]
Transmit EVM		2		%	Measured using Rohde & Schwarz FSU vector analyzer with Zigbee™ option
Transmit EVM Variation		1		%	$f_{CHANNEL}$ = 2405 MHz to 2480 MHz, T_A= −40°C to +85°C, VDD_BAT = 1.8 V to 3.6 V
Transmit PSD Mask		−56		dBm	RBW = 100 kHz; $\|f - f_{CHANNEL}\|$ > 3.5 MHz
Transmit 20 dB Bandwidth		2252		MHz	

[1] RBW = resolution bandwidth.

RECEIVER SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions
GENERAL RECEIVER SPECIFICATIONS					
RF Front-End LNA and Mixer IIP3		−13.6		dBm	At maximum gain, $f_{BLOCKER1}$ = 5 MHz, $f_{BLOCKER2}$ = 10.1 MHz, $P_{RF,IN}$ = −35 dBm
		−12.6		dBm	At maximum gain, $f_{BLOCKER1}$ = 20 MHz, $f_{BLOCKER2}$ = 40.1 MHz, $P_{RF,IN}$ = −35 dBm
		−10.5		dBm	At maximum gain, $f_{BLOCKER1}$ = 40 MHz, $f_{BLOCKER2}$ = 80.1 MHz, $P_{RF,IN}$ = −35 dBm

Parameter	Min	Typ	Max	Unit	Test Conditions
RF Front-End LNA and Mixer IIP2		24.7		dBm	At maximum gain, $f_{BLOCKER1}$ = 5 MHz, $f_{BLOCKER2}$ = 5.5 MHz, $P_{RF,IN}$ = −50 dBm
RF Front-End LNA and Mixer 1 dB Compression Point		−20.5		dBm	At maximum gain
Receiver LO Level at RFIO2 Port		−100		dBm	IEEE 802.15.4 packet mode
LNA Input Impedance at RFIO1x Port		50.2 − 52.2j		Ω	Measured in RX state
LNA Input Impedance at RFIO2x Port		74.3 − 10.7j		Ω	Measured in RX state
Receive Spurious Emissions					
Compliant with EN 300 440					
30 MHz to 1000 MHz			−57	dBm	
1 GHz to 12.75 GHz			−47	dBm	
RECEIVE PATH IEEE 802.15.4-2006 MODE					
Sensitivity ($P_{rf,in,min}$, IEEE 802.15.4)		−95		dBm	1% PER with PSDU length of 20 bytes according to the IEEE 802.15.4-2006 standard
Saturation Level		−15		dBm	1% PER with PSDU length of 20 bytes
CW Blocker Rejection					$P_{RF,IN} = P_{RF,IN,MIN}$, IEEE 802.15.4 + 3 dB
±5 MHz		55		dB	
±10 MHz		60		dB	
±20 MHz		63		dB	
±30 MHz		64		dB	
Modulated Blocker Rejection					$P_{RF,IN} = P_{RF,IN,MIN}$, IEEE 802.15.4 + 3 dB
±5 MHz		48		dB	
±10 MHz		61		dB	
±15 MHz		62.5		dB	
±20 MHz		65		dB	
±30 MHz		65		dB	
Co-Channel Rejection		−6		dB	$P_{RF,IN} = P_{RF,IN,MIN}$ + 10 dB modulated blocker
Out-of Band Blocker Rejection					$P_{RF,IN} = P_{RF,IN,MIN}$, IEEE 802.15.4 + 3 dB, measured at $f_{CHANNEL}$ = 2405 MHz
−5 MHz		−34.2		dBm	
−10 MHz		−30.7		dBm	
−20 MHz		−29.7		dBm	
−30 MHz		−25.7		dBm	
−60 MHz		−24.2		dBm	
					$P_{RF,IN} = P_{RF,IN,MIN}$, IEEE 802.15.4 + 3 dB, measured at $f_{CHANNEL}$ = 2480 MHz
+5 MHz		−33.4		dBm	
+10 MHz		−29.9		dBm	
+20 MHz		−28.2		dBm	
+30 MHz		−23.7		dBm	
+60 MHz		−29.9		dBm	
Receiver Channel Bandwidth		2252		kHz	Two-sided bandwidth; cascaded analog and digital channel filtering
Frequency Error Tolerance	−80		+80	ppm	$P_{RF,IN} = P_{RF,IN,MIN}$ + 3 dB
RSSI					Measured using IEEE 802.15.4-2006 packet mode
Dynamic range		85		dB	
Accuracy		±3		dB	
Averaging Time		128		µs	
Minimum Sensitivity		−95		dBm	

AUXILIARY SPECIFICATIONS

Table 5.

Parameter	Min	Typ	Max	Unit	Test Conditions
32 kHz RC OSCILLATOR					
Frequency		32.768		kHz	After calibration
Frequency Accuracy		1		%	After calibration at 25°C
Frequency Drift					
Temperature Coefficient		0.14		%/°C	
Voltage Coefficient		4		%/V	
Calibration Time		1		ms	
32 kHz CRYSTAL OSCILLATOR					
Frequency		32.768		kHz	
Maximum ESR		319.8		kΩ	10 pF on XOSC32KP and XOSC32KN
Start-Up Time		2000		ms	12.5 pF load capacitors on XOSC32KP and XOSC32KN
WAKE-UP TIMER					
Prescaler Tick Period	0.0305		20,000	ms	
Wake-Up Period	61×10^{-6}		1.31×10^{5}	sec	
TEMPERATURE SENSOR					
Range	−40		+85	°C	
Resolution		4.7		°C	
Accuracy		±6.4		°C	Average of 1000 ADC readbacks, after using linear fitting, with correction at known temperature
BATTERY MONITOR					
Trigger Voltage	1.7		3.6	V	
Trigger Voltage Step Size		62		mV	
Start-Up Time		5		µs	
Current Consumption		30		µA	
EXTERNAL PA INTERFACE					
R_{ON}, PAVSUP_ATB3 to VDD_BAT		5		Ω	extpa_bias_mode = 0, 1, 2, 5, 6
R_{OFF}, PAVSUP_ATB3 to GND		10		MΩ	extpa_bias_mode = 3, 4, power-down
R_{OFF}, PABIASOP_ATB4 to GND		10		MΩ	extpa_bias_mode = 0, power-down
PABIASOP_ATB4 Source Current, Maximum		80		µA	expta_bias_mode = 1, 3
PABIASOP_ATB4 Sink Current, Minimum		−80		µA	extpa_bias_mode = 2, 4
PABIASOP_ATB4 Current Control Resolution		6		Bits	extpa_bias_mode = 1, 2, 3, 4, 5
PABIASOP_ATB4 Compliance Voltage		150		mV	extpa_bias_mode = 2, 4
PABIASOP_ATB4 Compliance Voltage		3.45		V	extpa_bias_mode = 1, 3
Servo Loop Bias Current		22		mA	extpa_bias_mode = 5, 6
Servo Loop Bias Current Control Step		0.349		mA	extpa_bias_mode = 5, 6

CURRENT CONSUMPTION SPECIFICATIONS

Table 6.

Parameter	Min	Typ	Max	Unit	Test Conditions
CURRENT CONSUMPTION					
TX Mode Current Consumption					
−20 dBm		16.5		mA	IEEE 802.15.4-2006 continuous packet transmission mode
−10 dBm		17.4		mA	IEEE 802.15.4-2006 continuous packet transmission mode
0 dBm		19.6		mA	IEEE 802.15.4-2006 continuous packet transmission mode
+3 dBm		21.5		mA	IEEE 802.15.4-2006 continuous packet transmission mode
+4 dBm		25		mA	IEEE 802.15.4-2006 continuous packet transmission mode
Idle Mode		1.8		mA	XTO26M + digital active
PHY_RDY Mode		10		mA	
RX Mode Current Consumption		19		mA	IEEE 802.15.4-2006 packet mode
MEAS State		3		mA	
SLEEP_BBRAM		0.3		µA	BBRAM contents retained
SLEEP_BBRAM_RCO		1		µA	32 kHz RC oscillator running, some BBRAM contents retained, wake-up time enabled
SLEEP_BBRAM_XTO		1.7		µA	32 kHz crystal oscillator running, some BBRAM contents retained, wake-up time enabled

TIMING AND DIGITAL SPECIFICATIONS

Table 7. Logic Levels

Parameter	Min	Typ	Max	Unit	Test Conditions
LOGIC INPUTS					
Input High Voltage, V_{INH}	0.7 × VDD_BAT			V	
Input Low Voltage, V_{INL}			$0.2 \times V_{DD}$	V	
Input Current, I_{INH}/I_{INL}		±1		µA	
Input Capacitance, C_{IN}		10		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	VDD_BAT − 0.4			V	I_{OH} = 500 µA
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 500 µA
Output Rise/Fall		5		ns	
Output Load		7		pF	

Table 8. GPIOs

Parameter	Min	Typ	Max	Unit	Test Conditions
GPIO OUTPUTS					
Output Drive Level		5		mA	All GPIOs in logic high state
Output Drive Level		5		mA	All GPIOs in logic low state

Table 9. SPI Interface Timing

Parameter	Min	Typ	Max	Unit	Description
t_1			15	ns	$\overline{CS}$ falling edge to MISO setup time (TRX active)
t_2	40			ns	$\overline{CS}$ to SCLK setup time
t_3	40			ns	SCLK high time
t_4	40			ns	SCLK low time
t_5	80			ns	SCLK period
t_6			10	ns	SCLK falling edge to MISO delay
t_7	5			ns	MOSI to SCLK rising edge setup time
t_8	5			ns	MOSI to SCLK rising edge hold time

Parameter	Min	Typ	Max	Unit	Description
t_9	40			ns	SCLK to $\overline{CS}$ hold time
t_{10}	10			ns	$\overline{CS}$ high to SCLK wait time
t_{11}	270			ns	$\overline{CS}$ high time
t_{12}		300	400	µs	$\overline{CS}$ low to MISO high wake-up time, 26 MHz crystal with 10 pF load capacitance, T_A = 25°C
t_{13}			20	ns	SCLK rise time
t_{14}			20	ns	SCLK fall time
t_{15}, t_{16}	2			ms	$\overline{CS}$ high time on wake-up after RC_RESET or RC_SLEEP command (see Figure 5 and Figure 31) 26 MHz crystal with 10 pF load

Table 10. IEEE 802.15.4 State Transition Timing

Parameter	Min	Typ	Max	Unit	Test Conditions
Idle to PHY_RDY State		142		µs	
PHY_RDY to Idle State		13.5		µs	
PHY_RDY or TX to RX State (Different Channel)		192		µs	VCO calibration performed
PHY_RDY or RX to TX State (Different Channel)		192		µs	VCO calibration performed
PHY_RDY or TX to RX State (Same Channel)		140		µs	VCO calibration skipped
RX or PHY_RDY to TX State (Same Channel)		140		µs	VCO calibration skipped
RX Channel Change		192		µs	VCO calibration performed
TX Channel Change		192		µs	VCO calibration performed
TX to PHY_RDY State		23		µs	
PHY_RDY to CCA State		192		µs	
CCA to PHY_RDY State		14.5		µs	
RX to Idle State		5.5		µs	
TX to Idle State		30.5		µs	
Idle to MEAS State		19		µs	
MEAS to Idle State		6		µs	
CCA to Idle State		14.5		µs	
RX to CCA State		18		µs	
CCA to RX State		205		µs	

Table 11. Timing IEEE 802.15.4-2006 SPORT Mode

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
t_{21}	18			µs	SFD detect to TRCLK_CKO_GP3 (data bit clock) active delay
t_{22}		2		µs	TRCLK_CKO_GP3 bit period
t_{23}	0.51			µs	DR_GP0 to TRCLK_CKO_GP3 falling edge setup time
t_{24}		16		µs	TRCLK_CKO_GP3 symbol burst period
t_{35}	1.3		6.2	µs	PA nominal power to TRCLK_CKO_GP3 activity/entry into TX state
t_{36}		14		µs	RC_PHY_RDY to TRCLK_CKO_GP3 off
t_{37}		10		µs	RC_PHY_RDY to PA power shutdown

Table 12. MAC Timing

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
t_{26}		38		µs	Time from frame received to rx_pkt_rcvd interrupt generation
t_{27}			150	µs	Time allowed, from issuing a RC_TX command, to update Register delaycfg2, Bit mac_delay_ext (0x10B[7:0])
t_{28}			150	µs	Time allowed, from issuing a RC_TX command, to cancel the RC_TX command
$t_{RX\_MAC\_DELAY}$		192		µs	IEEE 802.15.4 mode as defined by the standard

TIMING DIAGRAMS

SPI Interface Timing Diagram

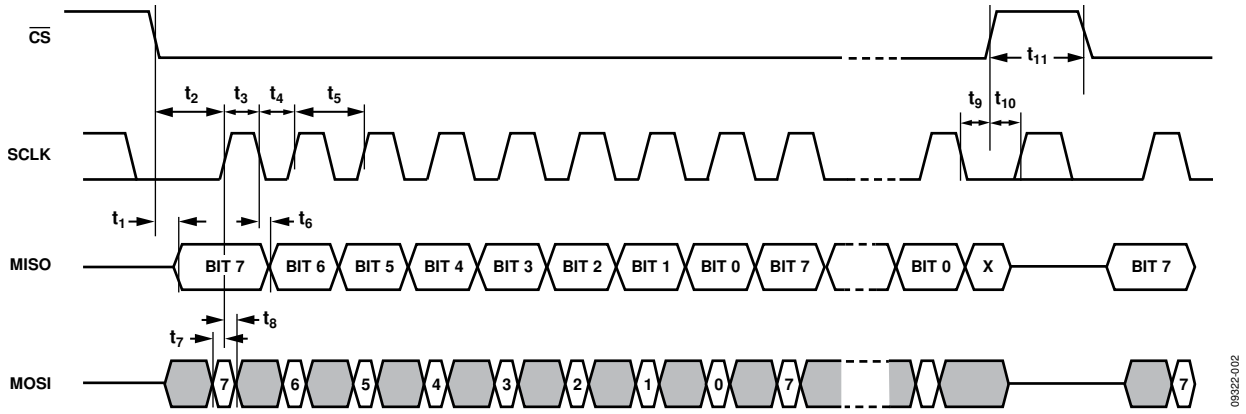

Figure 3. SPI Interface Timing

Additional description and timing diagrams are available in the Serial Peripheral interface section.

Sleep-to-Idle SPI Timing Diagrams

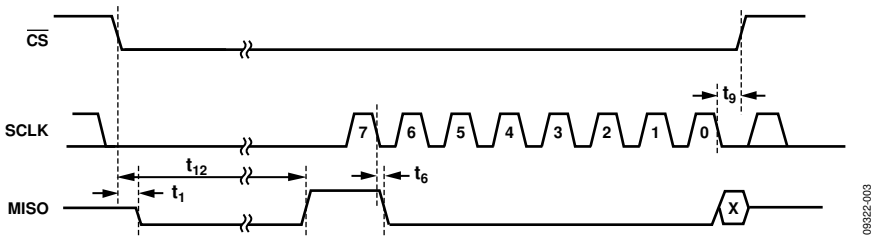

Figure 4. Sleep-to-Idle State Timing

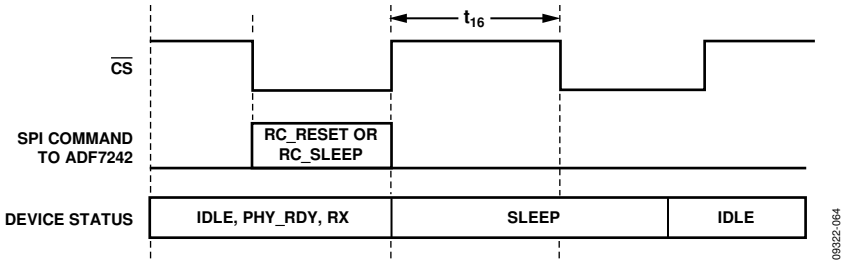

Figure 5. Wake-Up After an RC_RESET or RC_SLEEP Command

MAC Delay Timing Diagram

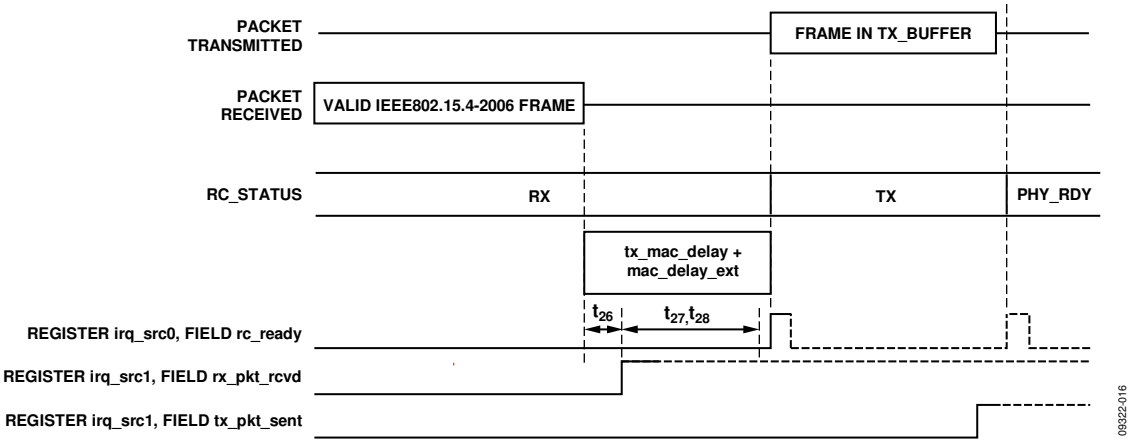

Figure 6. IEEE 802.15.4 MAC Timing

IEEE 802.15.4 RX SPORT Mode Timing Diagrams

Table 13. IEEE 802.15.4 RX SPORT Modes Configurations

Register rc_cfg, Field rc_mode (0x13E[7:0])	Register gp_cfg, Field gpio_config (0x32C[7:0])	Functionality
2	1	Bit clock and data available (see Figure 7)
0	7	Symbol clock and data available (see Figure 8)

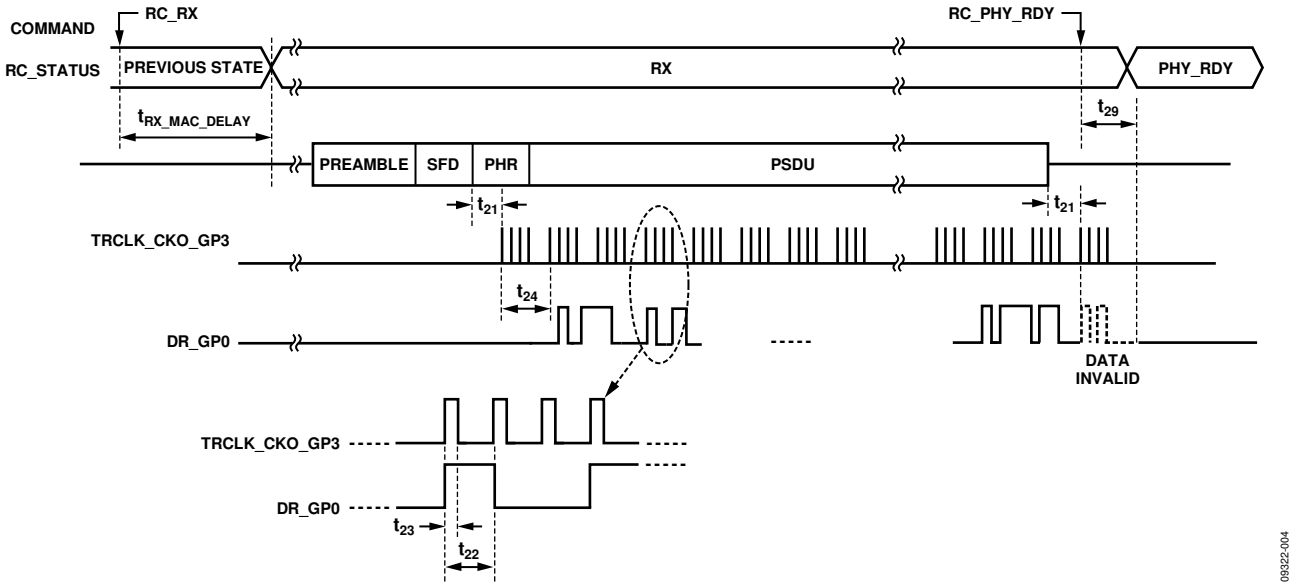

Figure 7. IEEE 802.15.4 RX SPORT Mode: Bit Clock and Data Available

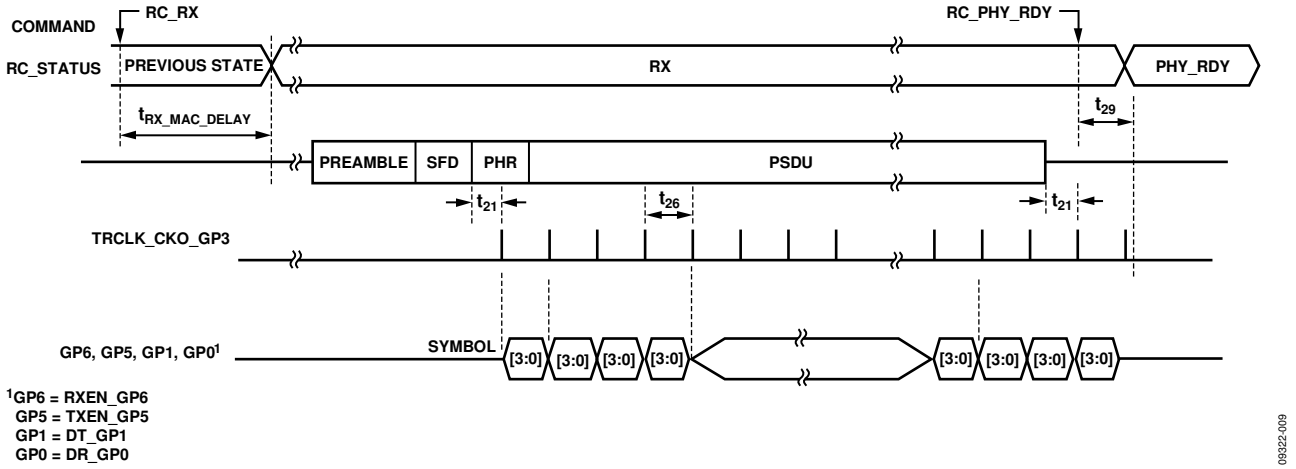

Figure 8. IEEE 802.15.4 RX SPORT Mode: Symbol Clock Output

IEEE 802.15.4 TX SPORT Mode Timing Diagram

Table 14. IEE 802.15.4 TX SPORT Mode Configurations

Register rc_cfg, Field rc_mode (0x13E[7:0])	Register gp_cfg, Field gpio_config (0x32C[7:0])	Functionality
3	1 or 4	Transmission starts after PA ramp up (see Figure 9) gpio_config = 1: data clocked in on rising edge of clock gpio_config = 4: data clocked in on falling edge of clock

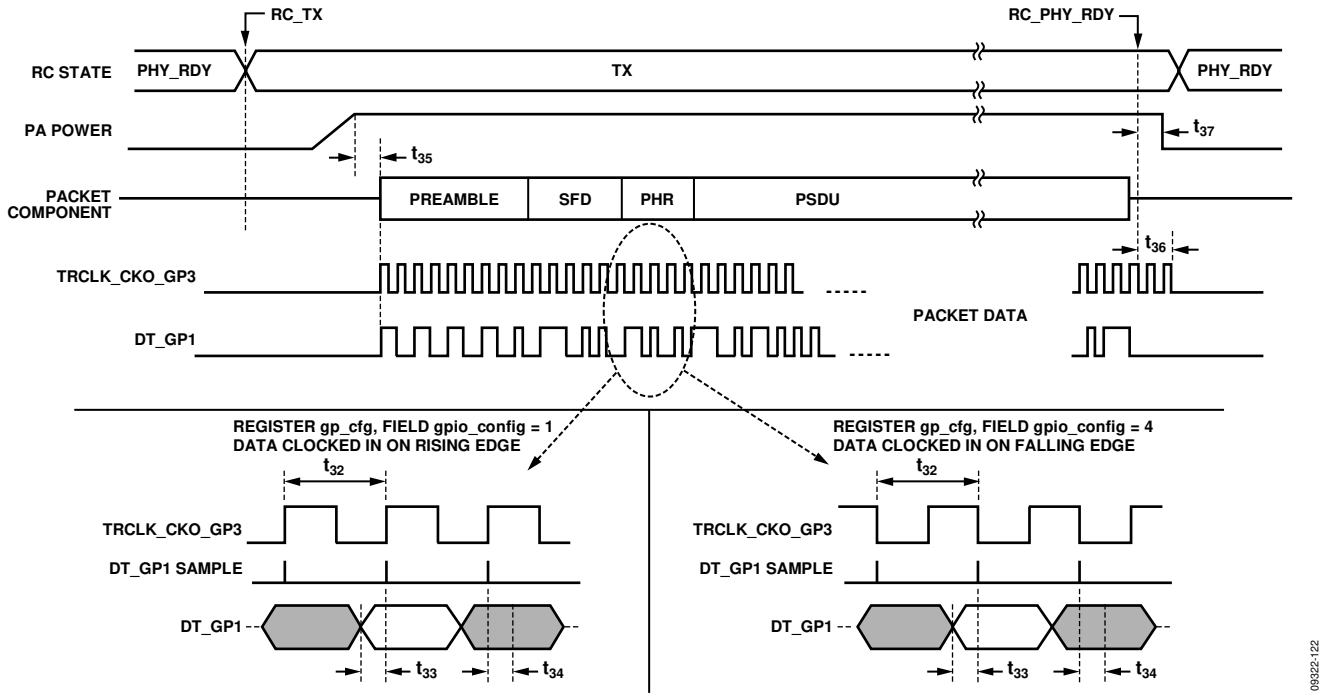

Figure 9. IEEE 802.15.4-2006 TX SPORT Mode

Refer to the SPORT Interface section for further details.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 15.

Parameter	Rating
VDD_BAT to GND	−0.3 V to +3.9 V
Operating Temperature Range	
Industrial	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C
Maximum Junction Temperature	150°C
LFCSP θ_{JA} Thermal Impedance	26°C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

The exposed paddle of the LFCSP package should be connected to ground.

This device is a high performance RF integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

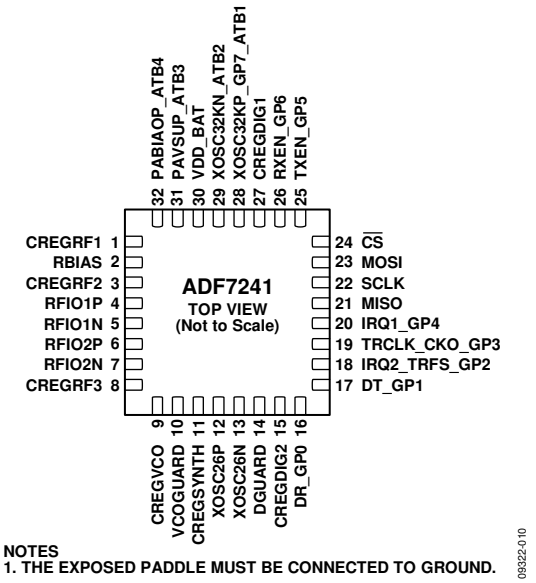

Figure 10. Pin Configuration

Table 16. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	CREGRF1	Regulated Supply Terminal for RF Section. Connect a 220 nF decoupling capacitor from this pin to GND.
2	RBIAS	Bias Resistor 27 kΩ to Ground.
3	CREGRF2	Regulated Supply for RF Section. Connect a 100 pF decoupling capacitor to ground.
4	RFIO1P	Differential RF Input Port 1 (Positive Terminal). A 10 nF coupling capacitor is required.
5	RFIO1N	Differential RF Input Port 1 (Negative Terminal). A 10 nF coupling capacitor is required.
6	RFIO2P	Differential RF Input/Output Port 2 (Positive Terminal). A 10 nF coupling capacitor required.
7	RFIO2N	Differential RF Input/Output Port 2 (Negative Terminal). A 10 nF coupling capacitor required.
8	CREGRF3	Regulated Supply for RF Section. Connect a 100 pF decoupling capacitor from this pin to GND.
9	CREGVCO	Regulated Supply for VCO Section. Connect a 220 nF decoupling capacitor from this pin to GND.
10	VCOGUARD	Guard Trench for VCO Section. Connect to Pin 9 (CREGVCO).
11	CREGSYNTH	Regulated Supply for PLL Section. Connect a 220 nF decoupling capacitor from this pin to GND.
12	XOSC26P	Terminal 1 of External Crystal and Loading Capacitor. This pin is no connect (NC) when an external oscillator is used.
13	XOSC26N	Terminal 2 of External Crystal and Loading Capacitor. Input for external oscillator.
14	DGUARD	Guard Trench for Digital Section. Connect to Pin 15 (CREGDIG2).
15	CREGDIG2	Regulated Supply for Digital Section. Connect a 220 nF decoupling capacitor to ground.
16	DR_GP0	SPORT Receive Data Output/General-Purpose IO Port.
17	DT_GP1	SPORT Transmit Data Input/General-Purpose IO Port.
18	IRQ2_TRFS_GP2	Interrupt Request Output 2/IEEE 802.15.4-2006 Symbol Clock/General-Purpose IO Port.
19	TRCLK_CKO_GP3	SPORT Clock Output/General-Purpose IO Port.
20	IRQ1_GP4	Interrupt Request Output 1/General-Purpose IO Port.
21	MISO	SPI Interface Serial Data Output.
22	SCLK	SPI Interface Data Clock Input.
23	MOSI	SPI Interface Serial Data Input.
24	$\overline{CS}$	SPI Interface Chip Select Input (and Wake-Up Signal).
25	TXEN_GP5	External PA Enable Signal/General-Purpose IO Port.
26	RXEN_GP6	External LNA Enable Signal/General-Purpose IO Port.
27	CREGDIG1	Regulated Supply for Digital Section. Connect a 1 nF decoupling capacitor from this pin to ground.
28	XOSC32KP_GP7_ATB1	Terminal 1 of 32 kHz Crystal Oscillator/General-Purpose IO Port/Analog Test Bus 1.
29	XOSC32KN_ATB2	Terminal 2 of 32 kHz Crystal Oscillator/Analog Test Bus 2.

Pin No.	Mnemonic	Description
30	VDD_BAT	Unregulated Supply Input from Battery.
31	PAVSUP_ATB3	External PA Supply Terminal/Analog Test Bus 3.
32	PABIAOP_ATB4	External PA Bias Voltage Output/Analog Test Bus 4.
33 (EPAD)	GND	Common Ground Terminal. The exposed paddle must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

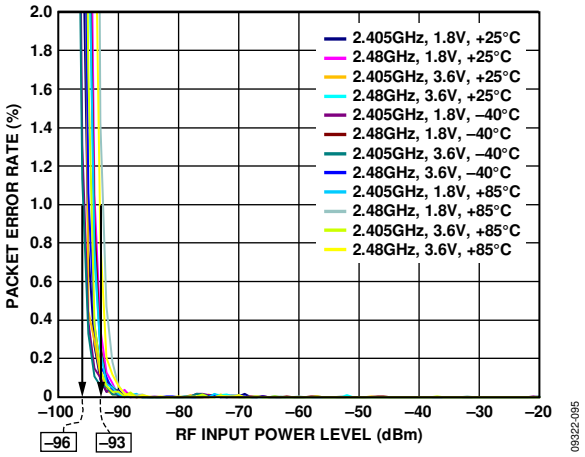

Figure 11. IEEE 802.15.4-2006 Packet Mode Sensitivity vs. Temperature and VDD_BAT, $f_{CHANNEL}$ = 2.405 GHz, 2.45 GHz, 2.48 GHz, RFIO2x

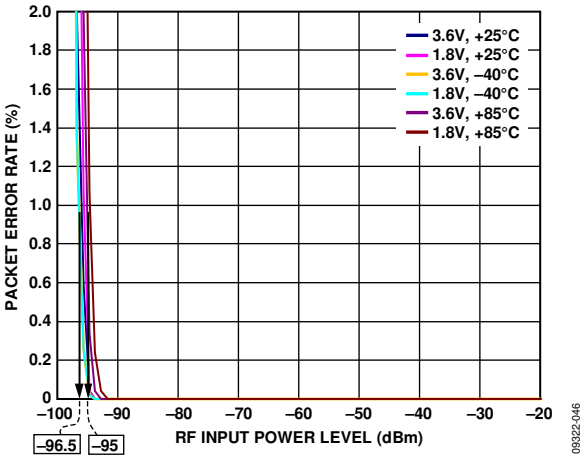

Figure 12. IEEE 802.15.4-2006 Packet Mode PER vs. RF Input Power Level vs. Temperature and VDD_BAT, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

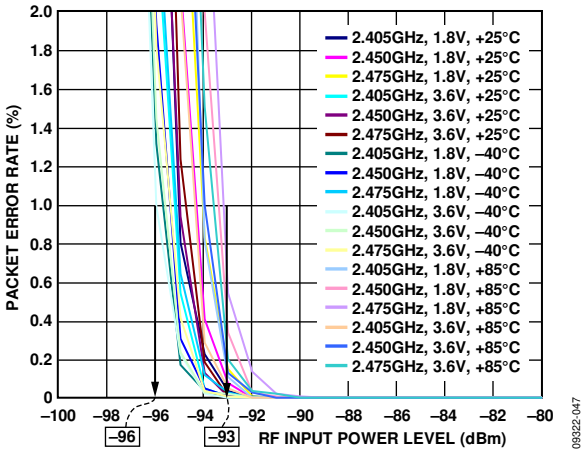

Figure 13. IEEE 802.15.4 Packet Mode Sensitivity vs. Temperature and VDD_BAT, $f_{CHANNEL}$ = 2.405 GHz, 2.45 GHz, 2.475 GHz, RFIO1x

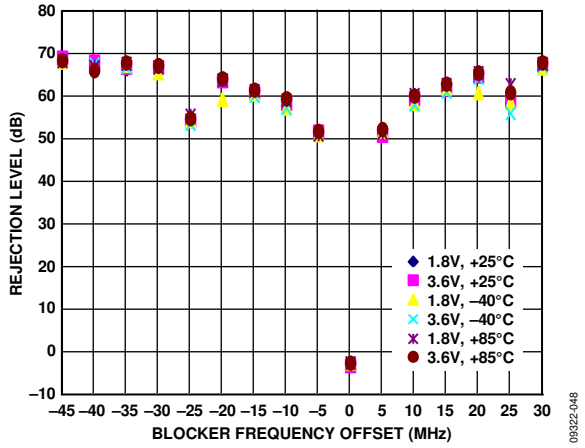

Figure 14. IEEE 802.15.4-2006 Packet Mode Blocker Rejection vs. Temperature and VDD_BAT, Modulated Blocker, P_{WANTED} = –85 dBm + 3 dB, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

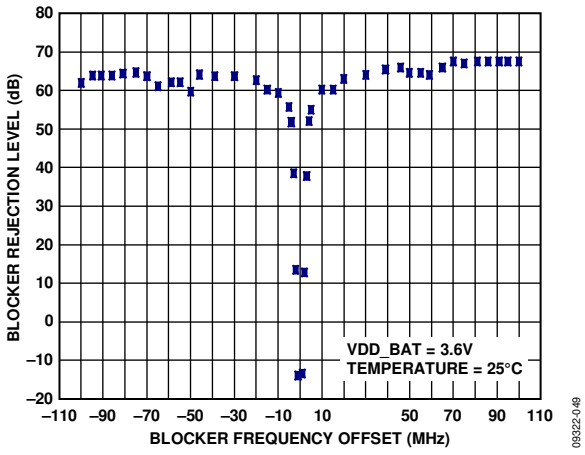

Figure 15. IEEE 802.15.4-2006 Packet Mode Wide-Band Blocker Rejection, CW Blocker, P_{WANTED} = –95 dBm + 3 dB, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

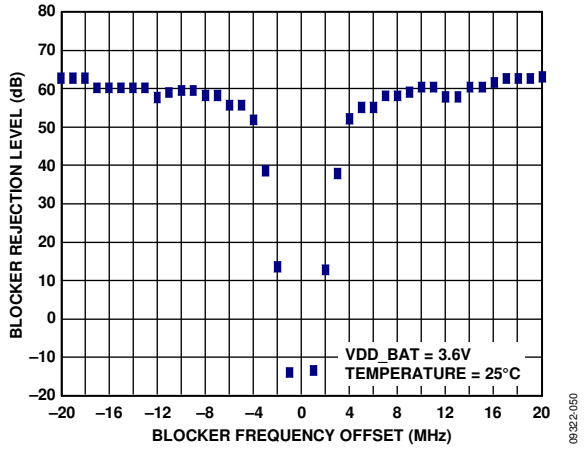

Figure 16. IEEE 802.15.4 Packet Mode Narrow-Band Blocker Rejection, CW Blocker, P_{WANTED} = –95 dBm + 3 dB, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

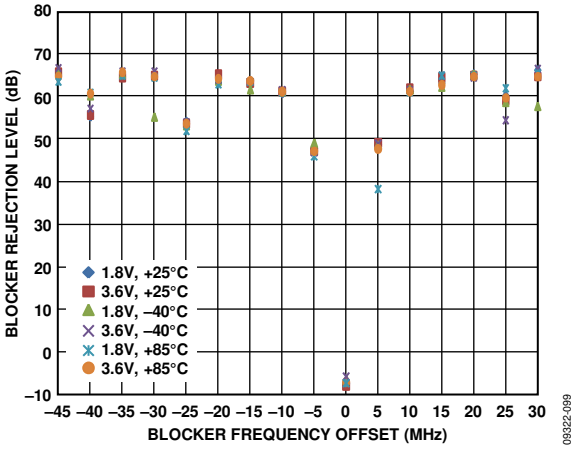

Figure 17. IEEE 802.15.4 Packet Mode Wide-Band Blocker Rejection vs. Temperature and VDD_BAT, Modulated Blocker, P_{WANTED} = −95 dBm + 3 dB, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

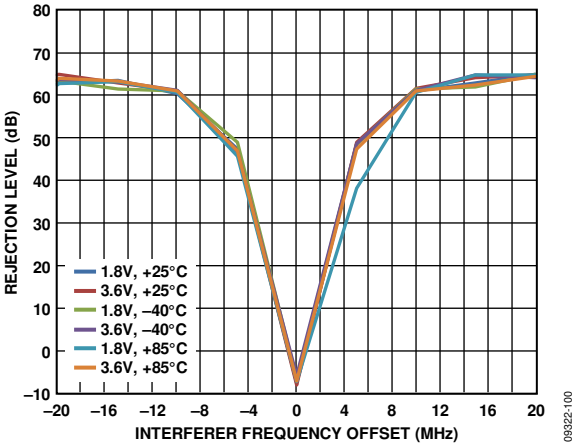

Figure 18. IEEE 802.15.4 Packet Mode Narrow-Band Blocker Rejection vs. Temperature and VDD_BAT, Modulated Blocker, P_{WANTED} = −95 dBm + 3 dB, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

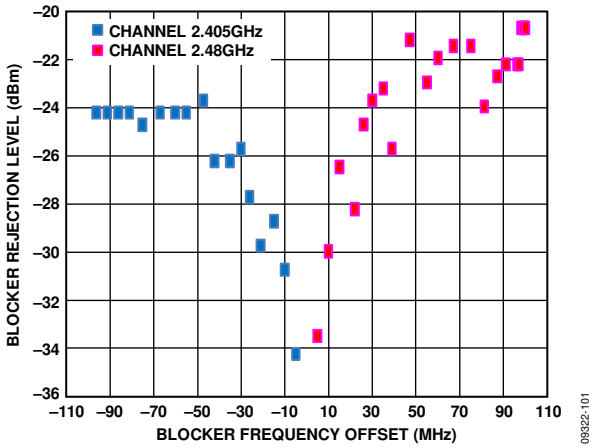

Figure 19. IEEE 802.15.4 Packet Mode Out-of-Band Blocker Rejection, CW Blocker, P_{WANTED} = −95 dBm + 3 dB, $f_{CHANNEL}$ = 2.405 GHz and 2.48 GHz, RFIO2x, VDD_BAT = 3.6 V, Temperature = 25°C

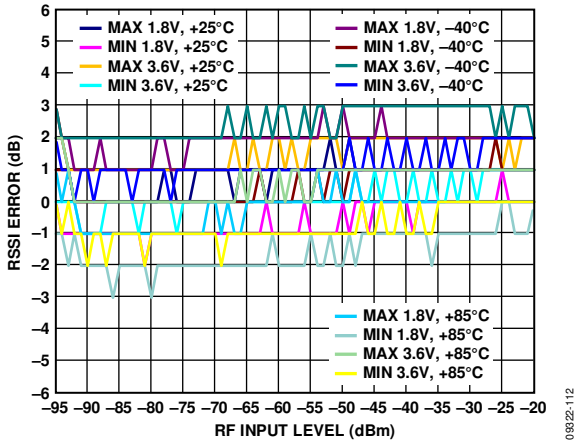

Figure 20. IEEE 802.15.4 Packet Mode RSSI Error vs. RF Input Power Level vs. Temperature and VDD_BAT, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

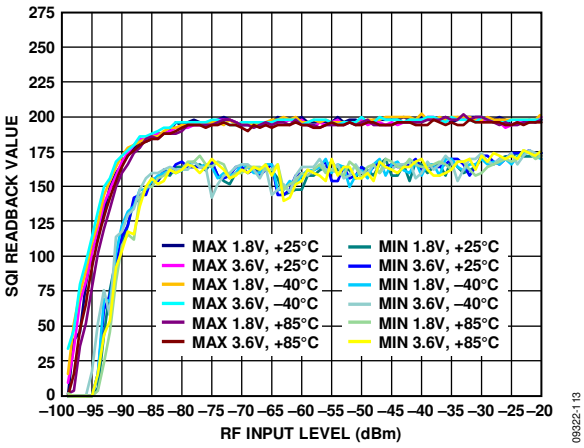

Figure 21. IEEE 802.15.4 Packet Mode SQI vs. RF Input Power Level vs. Temperature and VDD_BAT, $f_{CHANNEL}$ = 2.45 GHz, RFIO2x

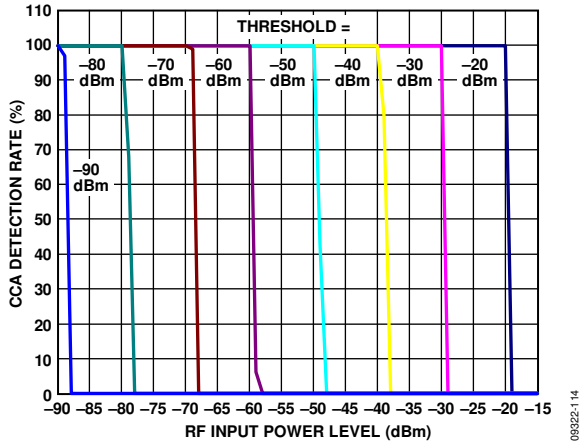

Figure 22. IEEE 802.15.4-2006 CCA Operation vs. RSSI Threshold, $f_{CHANNEL}$ = 2.45 GHz, VDD_BAT = 3.6 V, Temperature = 25°C, RFIO2x

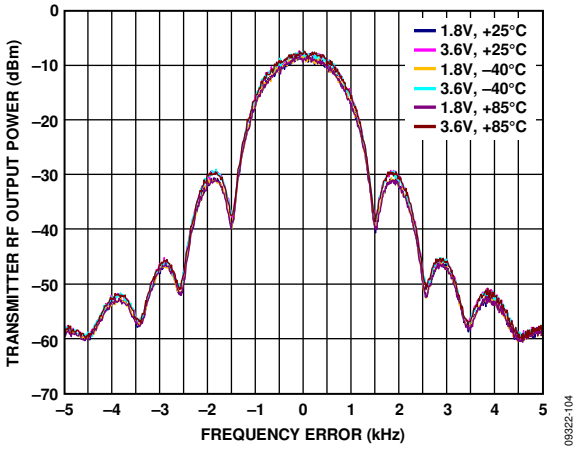

Figure 23. IEEE 802.15.4-2006 Transmitter Spectrum vs. Temperature and VDD_BAT, $f_{CHANNEL}$ = 2.45 GHz, Output Power = 3 dBm

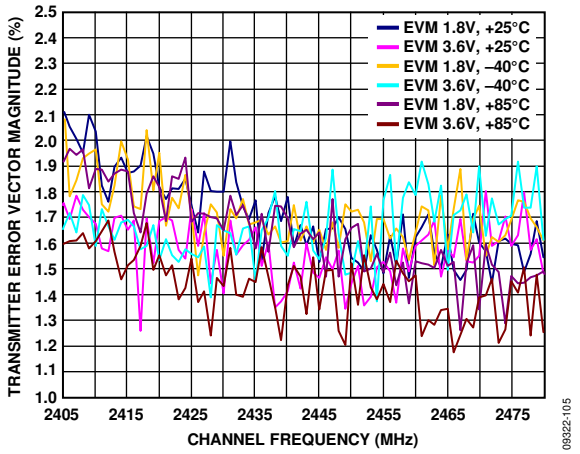

Figure 24. IEEE 802.15.4-2006 Transmitter EVM vs. Temperature and VDD_BAT at All Channels, Output Power = 3 dBm

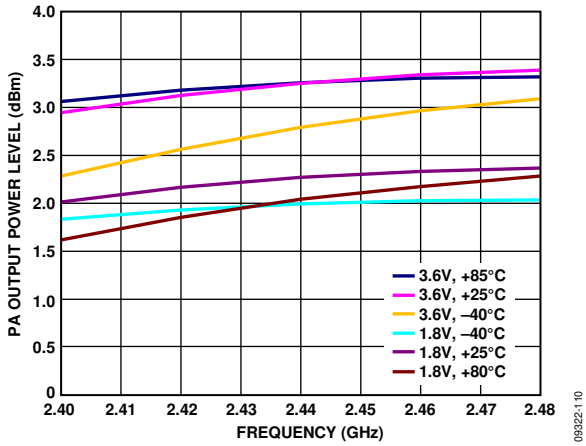

Figure 25. PA Output Power vs. RF Carrier Frequency, Temperature, and VDD_BAT (A discrete matching network and a harmonic filter are used as per the ADF7241 reference design.)

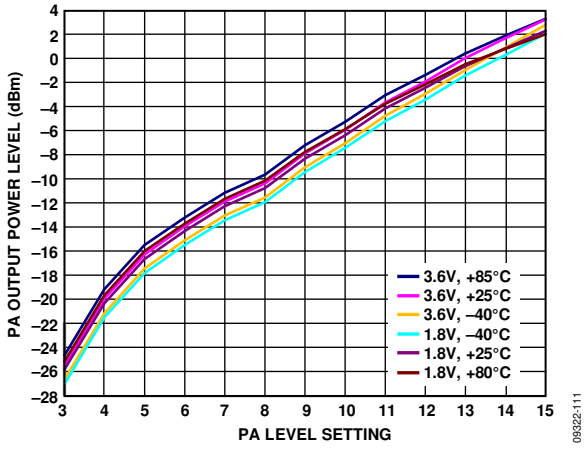

Figure 26. PA Output Power vs. Control Word, Temperature, and VDD_BAT, $f_{CHANNEL}$ = 2.44 GHz (A discrete matching network and a harmonic filter are used as per the ADF7241 reference design.)

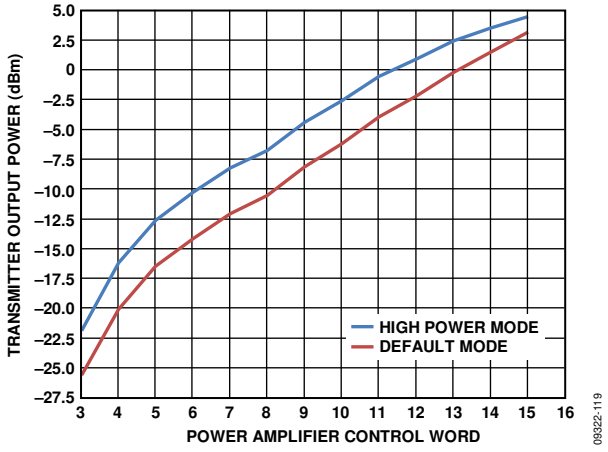

Figure 27. Transmitter Output Power vs. Control Word for Default and High Power Modes, $f_{CHANNEL}$ = 2.45 GHz, VDD_BAT = 3.6 V, Temperature = 25°C, RF Carrier Frequency, Temperature, and VDD_BAT
(A discrete matching network and a harmonic filter are used as per the ADF7241 reference design.)

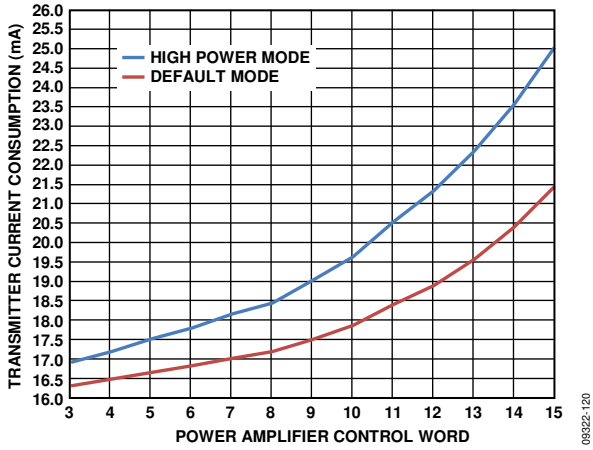

Figure 28. Transmitter Current Consumption vs. Control Word, for Default and High Power Modes, $f_{CHANNEL}$ = 2.45 GHz, VDD_BAT = 3.6 V, Temperature = 25°C

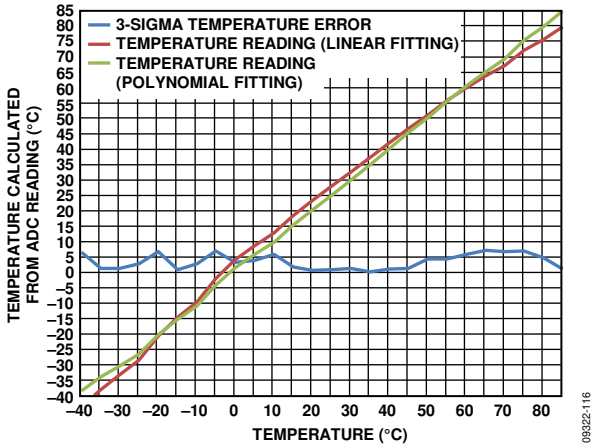

Figure 29. Temperature Sensor Performance (Average of 1000 ADC Readbacks) and 3-∑ Error vs. Temperature, VDD_BAT = 3.6 V

TERMINOLOGY

ACK
IEEE 802.15.4-2006 acknowledgment frame

ADC
Analog-to-digital converter

AGC
Automatic gain control

Battmon
Battery monitor

CCA
Clear channel assessment

BBRAM
Backup battery random access memory

CSMA/CA
Carrier-sense-multiple-access with collision avoidance

DR
Data rate

DSSS
Direct sequence spread spectrum

FCS
Frame check sequence

FHSS
Frequency hopping spread spectrum

FCF
Frame control field

LQI
Link quality indicator

MCR
Modem configuration register

MCU
Microcontroller unit

NC
Not connected

OCL
Offset correction loop

OQPSK
Offset-quadrature phase shift keying

PA
Power amplifier

PHR
PHY header

PHY
Physical layer

POR
Power-on reset

PSDU
PHY service data unit

RC
Radio controller

RCO32K
32 kHz RC oscillator

RSSI
Receive signal strength indicator

RTC
Real-time clock

SFD
Start-of-frame delimiter

SQI
Signal quality indicator

VCO
Voltage-controlled oscillator

WUC
Wake-up controller

XTO26M
26 MHz crystal oscillator

XTO32K
32 kHz crystal oscillator

RADIO CONTROLLER

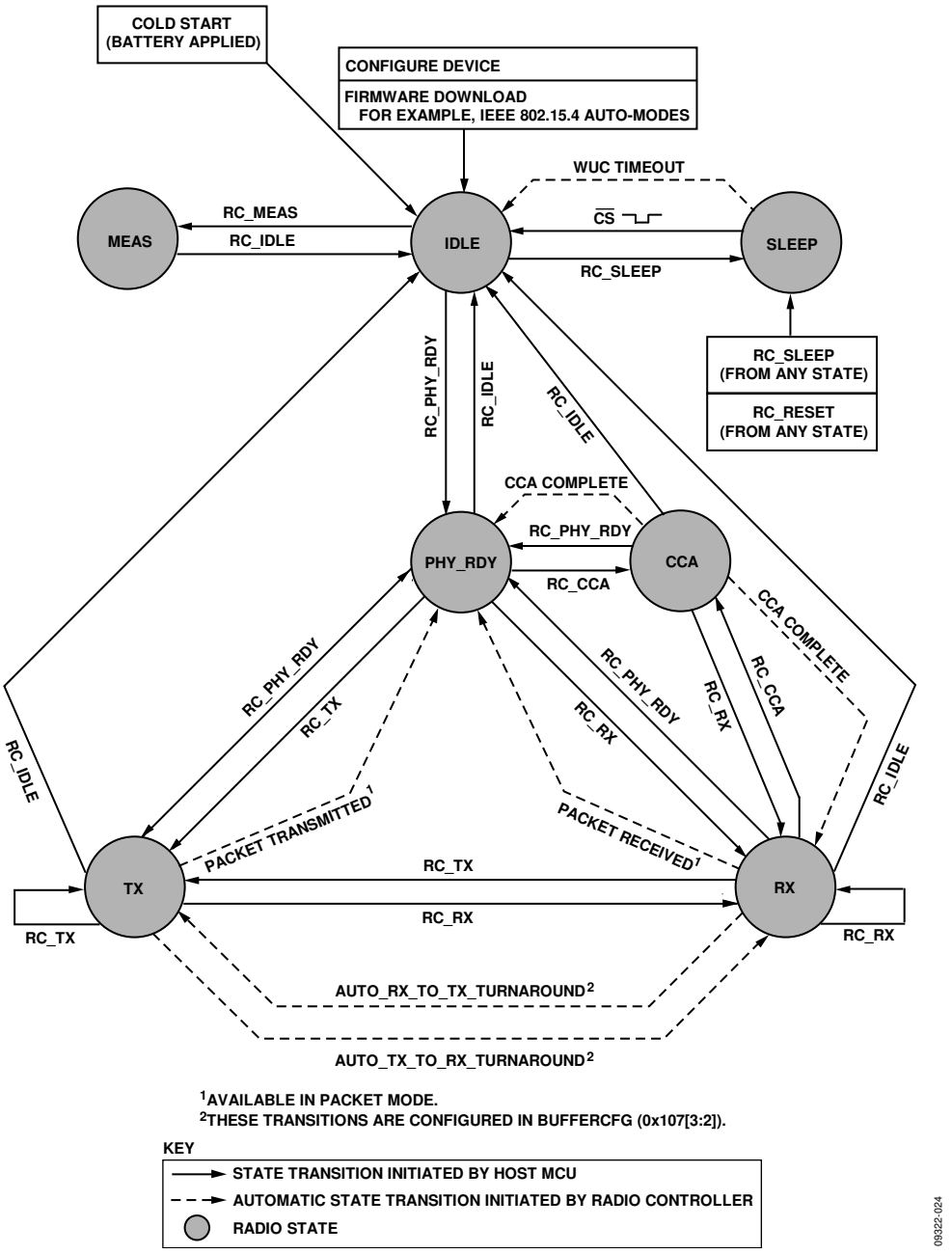

Figure 30. State Diagram

The ADF7241 incorporates a radio controller that manages the state of the IC in various operating modes and configurations. The host MCU can use single-byte commands to interface to the radio controller. The function of the radio controller includes the control of the sequence of powering up and powering down various blocks as well as system calibrations in different states of the device. Figure 30 shows the state diagram of the ADF7241 with possible transitions that are initiated by the host MCU and automatically by the radio controller.

Device Initialization

When the battery voltage is first applied to the ADF7241, a cold start-up sequence should be followed, as shown in Figure 31. The start-up sequence is as follows:

- Apply the battery voltage, VDD_BAT, to the device with the desired voltage ramp rate. After a time, t_{RAMP}, VDD_BAT reaches its final voltage value.
- After t_{RAMP}, execute the SPI command, RC_RESET. This command resets and shuts down the device.
- After the specified time, t_{15}, the host MCU can set the $\overline{CS}$ port of the SPI low.
- Wait until the MISO output of the SPI (SPI_READY flag) goes high, at which time the device is in the idle state and ready to accept commands.

A power-on reset takes place when the host MCU sets the $\overline{CS}$ port of the SPI low. All device LDOs are enabled together with the 26 MHz crystal oscillator and the digital core. After the radio controller initializes the configuration registers to their default values, the device enters the idle state.

The cold start-up sequence is needed only when the battery voltage is first applied to the device. Afterwards, a warm start-up sequence can be used where the host MCU can wake up the device from a sleep state by setting the $\overline{CS}$ port of the SPI low.

Idle State

In this state, the receive and transmit blocks are powered down. The digital section is enabled and all configuration registers, as well as the packet RAM, are accessible. The host MCU must set any configuration parameters, such as modulation scheme, channel frequency, and WUC configuration, in this state.

Bringing the $\overline{CS}$ input low in the sleep state causes a transition into the idle state. The transition from the sleep state to the idle state timing is shown in Figure 4. The idle state can also be entered by issuing an RC_IDLE command in any state other than the sleep state.

PHY_RDY State

Upon entering the PHY_RDY state from the idle state, the RF frequency synthesizer is enabled and a system calibration is carried out. The receive and transmit blocks are not enabled in this state. The system calibration is omitted when the PHY_RDY state is entered from the RX, TX, or CCA state.

The PHY_RDY state can be entered from the idle, RX, TX, or CCA state by issuing an RC_PHY_RDY command.

RX State

The RF frequency synthesizer is automatically calibrated to the programmed channel frequency upon entering the RX state from the PHY_RDY or TX state. The frequency synthesizer calibration can be omitted for single-channel communication systems if short turnaround times are required. Following a programmable MAC delay period, the ADF7241 starts searching for a preamble and a synchronization word if enabled by the user.

The RX state can be entered from the PHY_RDY, CCA, and TX states by issuing an RC_RX command. Depending on whether the device is configured to operate in packet or SPORT mode by setting Register buffercfg, Field rx_buffer_mode, the device can revert automatically to the PHY_RDY state when a packet is received, or remain in the RX state until a command to enter a different state is issued. Refer to the Receiver section for further details.

CCA State

Upon entering the CCA state, a clear channel assessment is performed. The CCA state can be entered from the PHY_RDY or RX state by issuing an RC_CCA command. By default, upon completion of the clear channel assessment, the ADF7241 automatically reverts to the state from which the RC_CCA command originated.

TX State

Upon entering the TX state, the RF frequency synthesizer is automatically calibrated to the programmed channel frequency. The frequency synthesizer calibration can be omitted for communication systems operating on a single channel if short turnaround times are required. Following a programmable delay period, the PA is ramped up and transmission is initiated.

The TX state can be entered from the PHY_RDY or RX state by issuing the RC_TX command. Depending on whether the device is configured to operate in packet or SPORT mode by setting Register buffercfg, Field rx_buffer_mode, the device can revert automatically to the PHY_RDY state when a packet is transmitted, or remain in the TX state until a command to enter a different state is issued. Refer to the Transmitter section for further details.

MEAS State

The MEAS state is used to measure the chip temperature. The transmitter and receiver blocks are not enabled in this state. The chip temperature is measured using the ADC, which can be read from Register adc_rbk, Field adc_out, and is continuously updated with the chip temperature reading.

This state is enabled by issuing the RC_MEAS command from the idle state and can be exited using the RC_IDLE command.