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ANALOG DEVICES

Low Capacitance, Low Charge Injection, ±15 V/+12 V *i*CMOS SPST in SOT-23

ADG1201/ADG1202

FEATURES

2.4 pF off capacitance
<1 pC charge injection
Low leakage; 0.6 nA maximum @ 85°C
120 Ω on resistance
Fully specified at ±15 V, +12 V
No V_L supply required
3 V logic-compatible inputs
Rail-to-rail operation
6-lead SOT-23 package

APPLICATIONS

Automatic test equipment
Data acquisition systems
Battery-powered systems
Sample-and-hold systems
Audio signal routing
Video signal routing
Communication systems

FUNCTIONAL BLOCK DIAGRAM

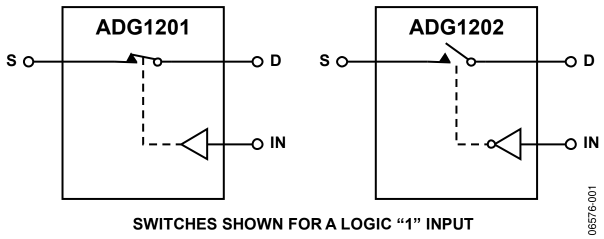

Figure 1.

GENERAL DESCRIPTION

The ADG1201/ADG1202 are monolithic complementary metal-oxide semiconductor (CMOS) devices containing an SPST switch designed in an *i*CMOS® (industrial CMOS) process. *i*CMOS is a modular manufacturing process combining high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make the parts suitable for video signal switching.

*i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

The ADG1201/ADG1202 contain a single-pole/single-throw (SPST) switch. Figure 1 shows that with a logic input of 1, the switch of the ADG1201 is closed and that of the ADG1202 is open. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

PRODUCT HIGHLIGHTS

1. Ultralow capacitance.
2. <1 pC charge injection.
3. Ultralow leakage.
4. 3 V logic-compatible digital inputs: $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V.
5. No V_L logic power supply required.
6. SOT-23 package.

Rev. 0

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REVISION HISTORY

2/08—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

	B Version[1]				
Parameter	**25°C**	**−40°C to +85°C**	**−40°C to +125°C**	**Unit**	**Test Conditions/Comments**
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	120			Ω typ	V_{DD} = +13.5 V, V_{SS} = −13.5 V
	200	240	270	Ω max	V_S = ±10 V, I_S = −1 mA; see Figure 20
On Resistance Flatness ($R_{FLAT(ON)}$)	20			Ω typ	V_S = −5 V, 0 V, and +5 V; I_S = −1 mA
	60	72	79	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.004			nA typ	V_S = ±10 V, V_D = ±10 V; see Figure 21
	±0.1	±0.6	±1	nA max	
Drain Off Leakage, I_D (Off)	±0.004			nA typ	V_S = ±10 V, V_D = ±10 V; see Figure 21
	±0.1	±0.6	±1	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04			nA typ	V_S = V_D = ±10 V; see Figure 22
	±0.15	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	2.5			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	140			ns typ	R_L = 300 Ω, C_L = 35 pF
	170	200	230	ns max	V_S = 10 V; see Figure 26
t_{OFF}	90			ns typ	R_L = 300 Ω, C_L = 35 pF
	105	130	141	ns max	V_S = 10 V; see Figure 26
Charge Injection	−0.8			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 27
Off Isolation	80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 23
Total Harmonic Distortion + Noise	0.15			% typ	R_L = 10 kΩ, 5 V rms, f = 20 Hz to 20 kHz
−3 dB Bandwidth	660			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 24
C_S (Off)	2.4			pF typ	V_S = 0 V, f = 1 MHz
	3			pF max	V_S = 0 V, f = 1 MHz
C_D (Off)	2.8			pF typ	V_S = 0 V, f = 1 MHz
	3.3			pF max	V_S = 0 V, f = 1 MHz
C_D, C_S (On)	4.7			pF typ	V_S = 0 V, f = 1 MHz
	5.6			pF max	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
I_{DD}	60			μA typ	Digital inputs = 5 V
			95	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V, 5 V or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			±5 to ±16.5	V min/max	GND = 0 V

[1] Temperature range for B version is −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	B Version[1] 25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	300			Ω typ	V_{DD} = 10.8 V, V_{SS} = 0 V
	475	567	625	Ω max	V_S = 0 V to 10 V, I_S = −1 mA; see Figure 20
On Resistance Flatness ($R_{FLAT(ON)}$)	60			Ω typ	V_S = 3 V, 6 V, and 9 V, I_S = −1 mA
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.006			nA typ	V_S = 1 V or 10 V, V_D = 10 V or 1 V; see Figure 21
	±0.1	±0.6	±1	nA max	
Drain Off Leakage, I_D (Off)	±0.006			nA typ	V_S = 1 V or 10 V, V_D = 10 V or 1 V; see Figure 21
	±0.1	±0.6	±1	nA max	
Channel On Leakage, I_D, I_S (On)	±0.04			nA typ	V_S = V_D = 1 V or 10 V; see Figure 22
	±0.15	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			µA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[2]					
t_{ON}	190			ns typ	R_L = 300 Ω, C_L = 35 pF
	250	295	340	ns max	V_S = 8 V; see Figure 26
t_{OFF}	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	155	190	210	ns max	V_S = 8 V; see Figure 26
Charge Injection	0.8			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 27
Off Isolation	80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 23
−3 dB Bandwidth	520			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 24
C_S (Off)	2.7			pF typ	V_S = 6 V, f = 1 MHz
	3.3			pF max	V_S = 6 V, f = 1 MHz
C_D (Off)	3.1			pF typ	V_S = 6 V, f = 1 MHz
	3.6			pF max	V_S = 6 V, f = 1 MHz
C_D, C_S (On)	5.3			pF typ	V_S = 6 V, f = 1 MHz
	6.3			pF max	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{DD}	60			µA typ	Digital inputs = 5 V
			95	µA max	
V_{DD}			+5/+16.5	V min/max	V_{SS} = 0 V, GND = 0 V

[1] Temperature range for B version is −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs[1]	V_{SS} – 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND – 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current per Channel, S or D	30 mA
Operating Temperature Range	−40°C to +125°C
Industrial (B Version)	
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
6 Lead SOT-23	
θ_{JA},Thermal Impedance	229.6°C/W
θ_{JC}, Thermal Impedance	91.99°C/W
Reflow Soldering Peak Temperature, Pb-free	260°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

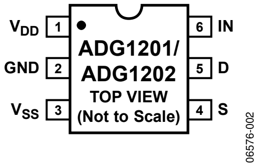


Figure 2. SOT-23 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD}	Most Positive Power Supply Potential.
2	GND	Ground (0 V) Reference.
3	V_{SS}	Most Negative Power Supply Potential.
4	S	Source Terminal. Can be an input or output.
5	D	Drain Terminal. Can be an input or output.
6	IN	Logic Control Input.

Table 5. ADG1201/ADG1202 Truth Table

ADG1201 IN	ADG1202 IN	Switch Condition
1	0	On
0	1	Off

TYPICAL PERFORMANCE CHARACTERISTICS

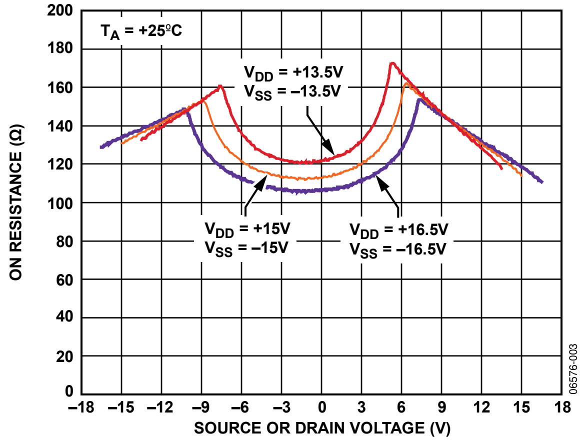


Figure 3. On Resistance as a Function of V_D (V_S) for Dual Supply

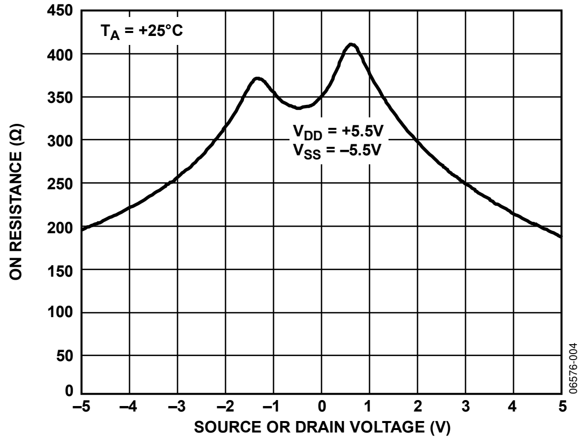


Figure 4. On Resistance as a Function of V_D (V_S) for Dual Supply

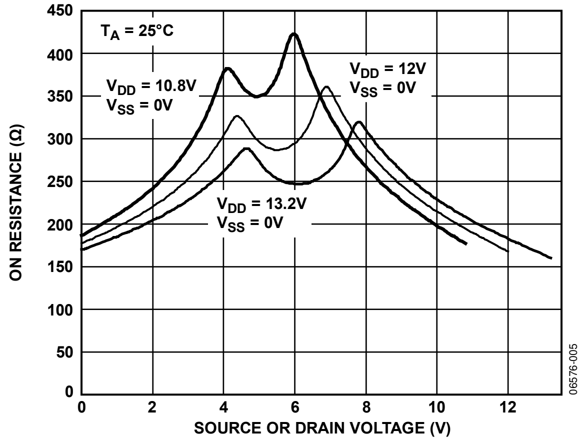


Figure 5. On Resistance as a Function of V_D (V_S) for Single Supply

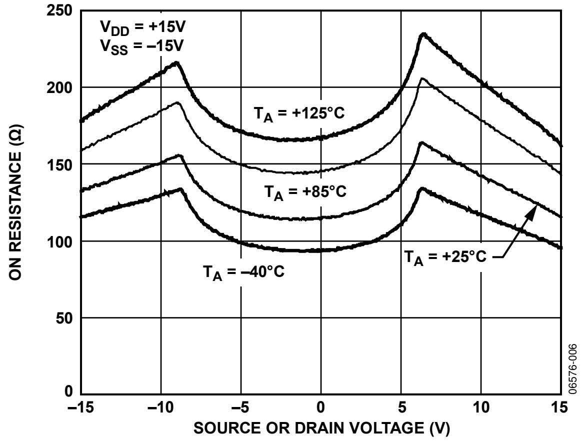


Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

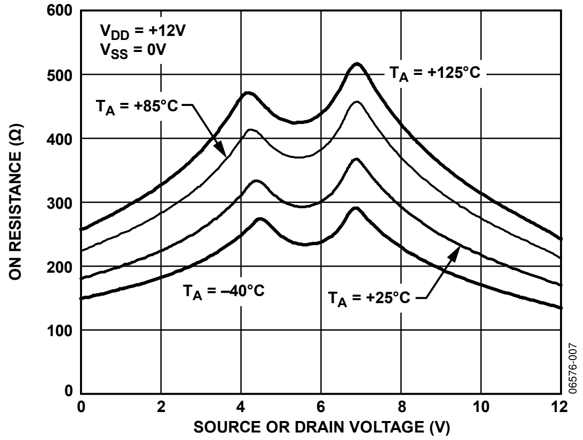


Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

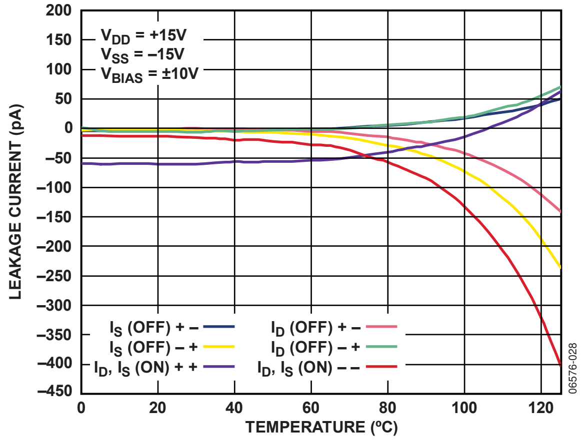


Figure 8. Leakage Currents as a Function of Temperature, Dual Supply

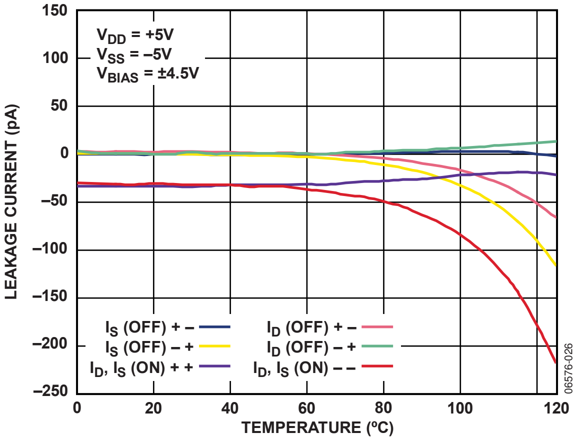


Figure 9. Leakage Currents as a Function of Temperature, Dual Supply

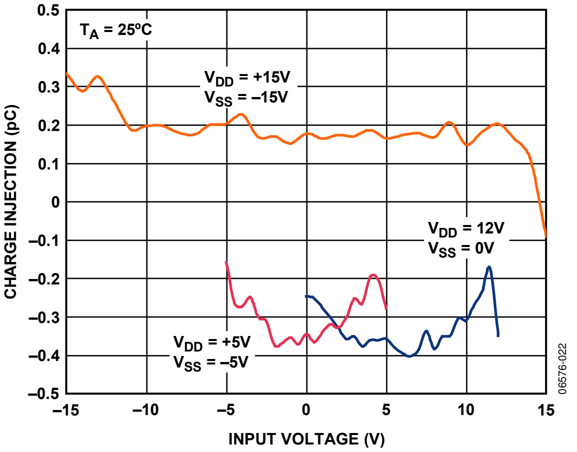


Figure 12. Charge Injection vs. Source Voltage

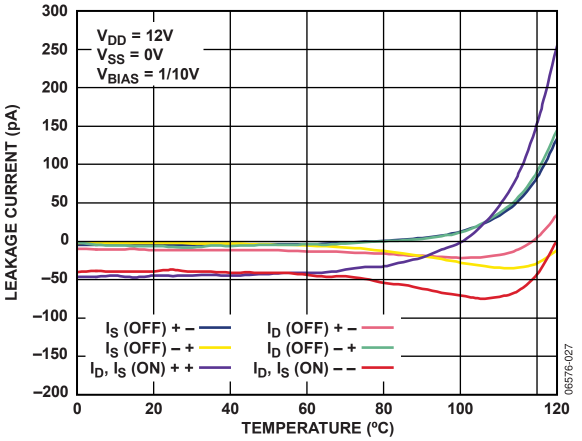


Figure 10. Leakage Currents as a Function of Temperature, Single Supply

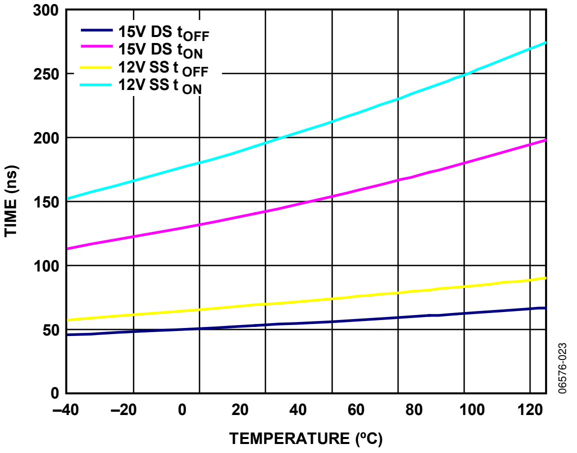


Figure 13. T_{ON}/T_{OFF} Times vs. Temperature

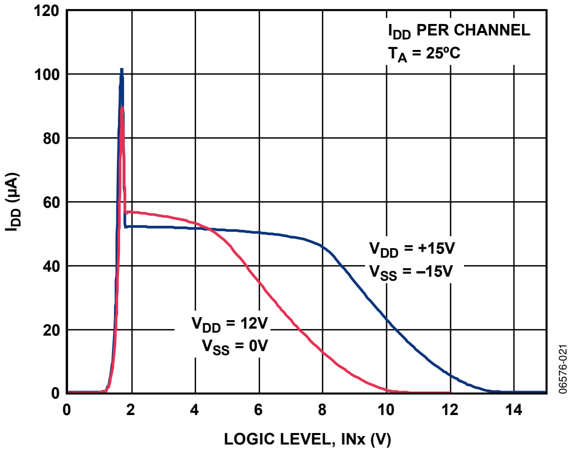


Figure 11. I_{DD} vs. Logic Level

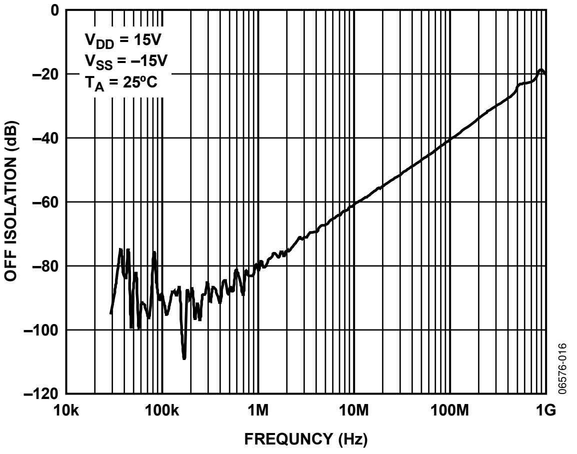


Figure 14. Off Isolation vs. Frequency

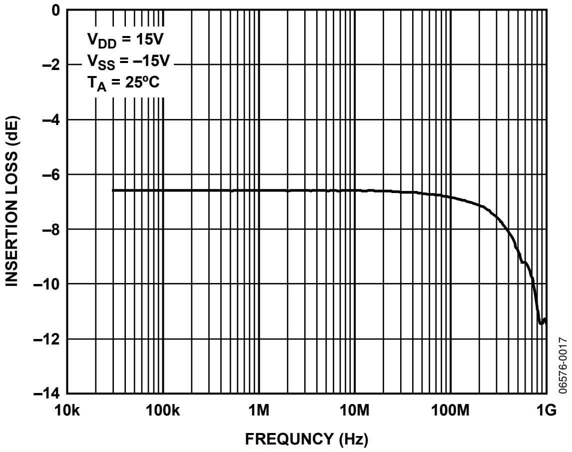


Figure 15. On Response vs. Frequency

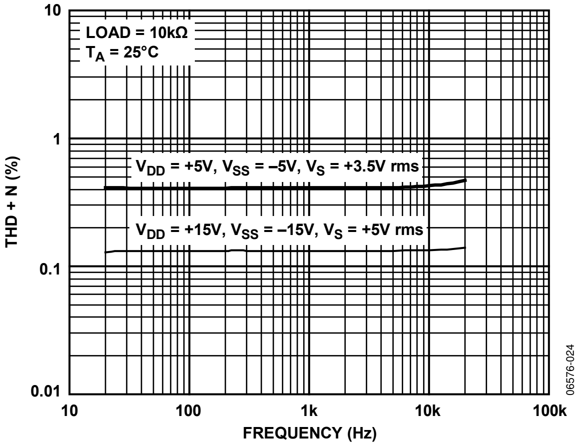


Figure 16. THD + N vs. Frequency

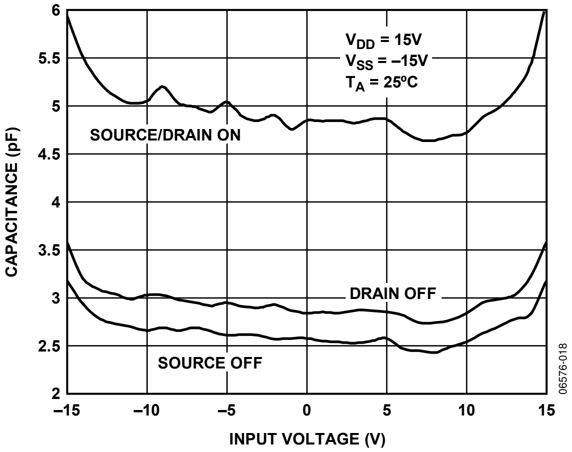


Figure 17. Capacitance vs. Input Voltage, Dual Supply

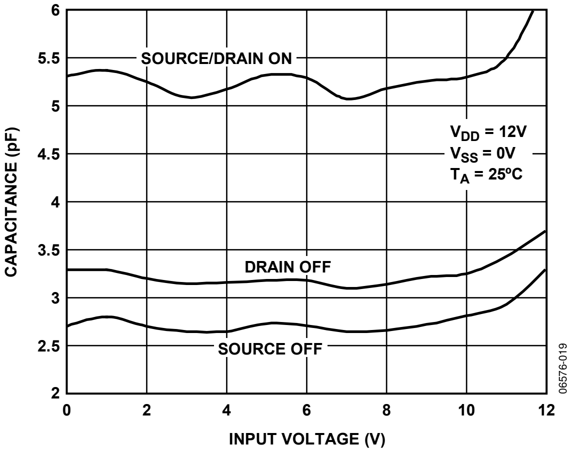


Figure 18. Capacitance vs. Input Voltage, Single Supply

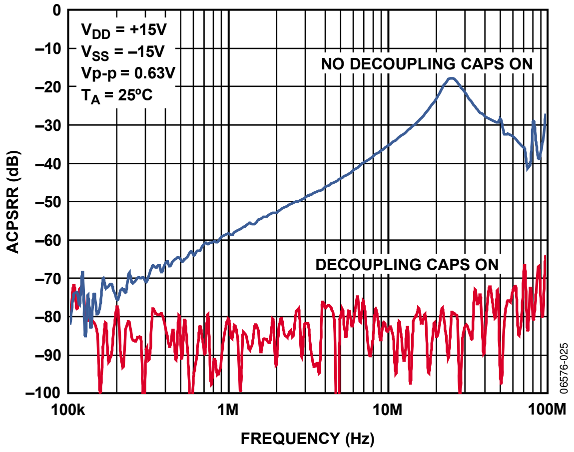


Figure 19. ACPSRR vs. Frequency

TEST CIRCUITS

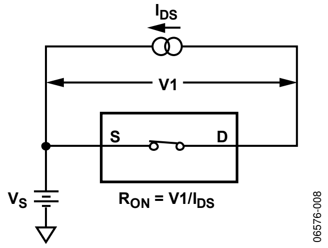


Figure 20. On Resistance

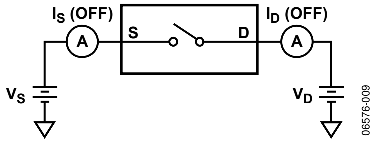


Figure 21. Off Leakage

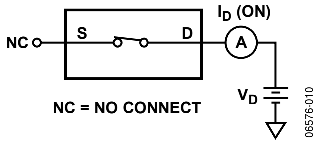


Figure 22. On Leakage

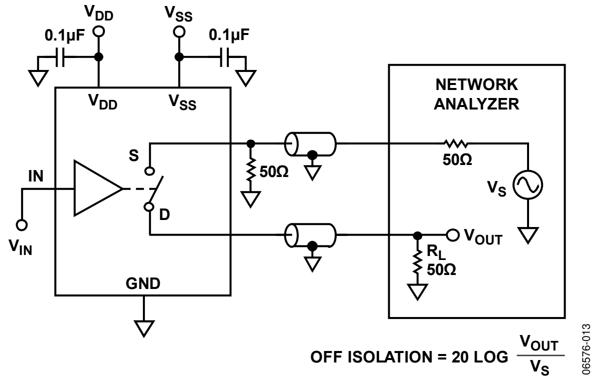


Figure 23. Off Isolation

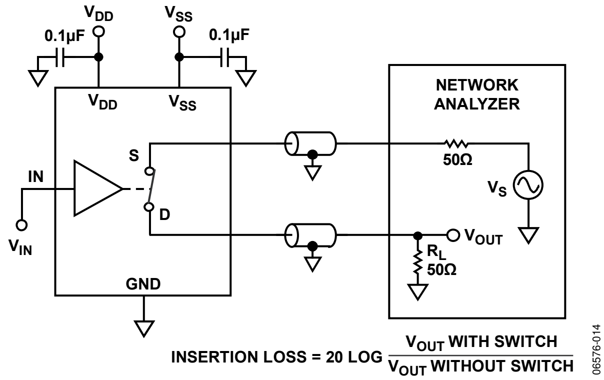


Figure 24. Bandwidth

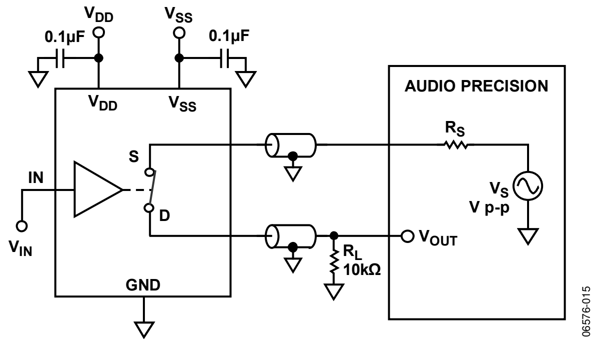


Figure 25. THD + Noise

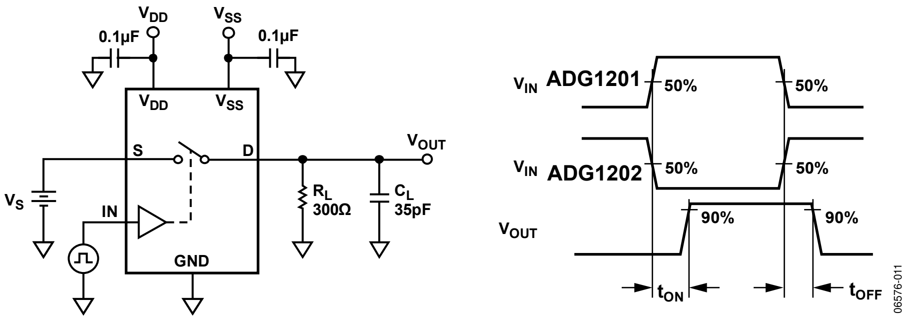


Figure 26. Switching Times

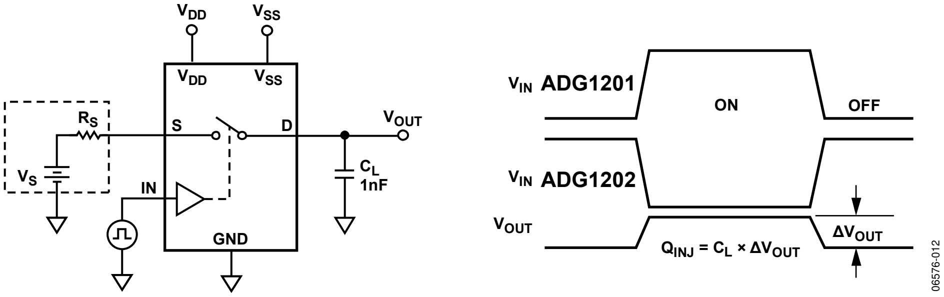


Figure 27. Charge Injection

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D (V_S)
The analog voltage on Terminal D and Terminal S.

R_{ON}
The ohmic resistance between D and S.

$R_{FLAT(ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, measured with reference to ground.

C_D (Off)
The off switch drain capacitance, measured with reference to ground.

C_D, C_S (On)
The on switch capacitance, measured with reference to ground.

C_{IN}
The digital input capacitance.

t_{ON}
The delay between applying the digital control input and the output switching on. See Figure 26.

t_{OFF}
The delay between applying the digital control input and the output switching off. See Figure 26.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

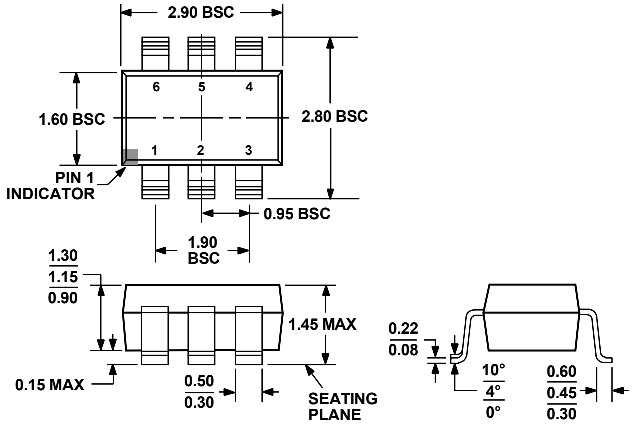
On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

ACPSRR (AC Power Supply Rejection Ratio)
Measures the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-178-AB

Figure 28. 6-Lead Small Outline Transistor Package [SOT-23]
(RJ-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADG1201BRJZ-R2[1]	−40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S25
ADG1201BRJZ-REEL7[1]	−40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S25
ADG1202BRJZ-R2[1]	−40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S26
ADG1202BRJZ-REEL7[1]	−40°C to +125°C	6-Lead Small Outline Transistor Package [SOT-23]	RJ-6	S26

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[1] Z = RoHS Compliant Part.

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