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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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User Defined Fault Protection and Detection, 0.8 pC Q_{INJ}, 8:1/Dual 4:1 Multiplexers

Data Sheet **ADG5248F/ADG5249F**

FEATURES

- User defined secondary supplies set overvoltage level
  - Overvoltage protection up to −55 V and +55 V
  - Power-off protection up to −55 V and +55 V
  - Overvoltage detection on source pins
  - Minimum secondary supply level: 4.5 V single-supply
  - Interrupt flags indicate fault status
- Low charge injection (Q_{INJ}): 0.8 pC
- Low drain/source on capacitance
  - ADG5248F: 19 pF
  - ADG5249F: 14 pF
- Latch-up immune under any circumstance
- Known state without digital inputs present
- V_{SS} to V_{DD} analog signal range
  - ±5 V to ±22 V dual-supply operation
  - 8 V to 44 V single-supply operation
  - Fully specified at ±15 V, ±20 V, +12 V, and +36 V

APPLICATIONS

- Analog input/output modules
- Process control/distributed control systems
- Data acquisition
- Instrumentation
- Avionics
- Automatic test equipment
- Communication systems
- Relay replacement

GENERAL DESCRIPTION

The ADG5248F and ADG5249F are 8:1 and dual 4:1 analog multiplexers. The ADG5248F switches one of eight inputs to a common output, and the ADG5249F switches one of four differential inputs to a common differential output. Each channel conducts equally well in both directions when on, and each channel has an input signal range that extends to the supplies. The primary supply voltages define the on-resistance profile, whereas the secondary supply voltages define the voltage level at which the overvoltage protection engages.

When no power supplies are present, the channel remains in the off condition, and the switch inputs are high impedance. Under normal operating conditions, if the analog input signal levels on any Sx pin exceed positive fault voltage (POSFV) or negative fault voltage (NEGFV) by a threshold voltage (V_T), the channel turns off and that Sx pin becomes high impedance. If the switch on, the drain pin is pulled to the secondary supply voltage that was exceeded. Input signal levels up to +55 V or −55 V relative to ground are blocked, in both the powered and unpowered conditions.

FUNCTIONAL BLOCK DIAGRAMS

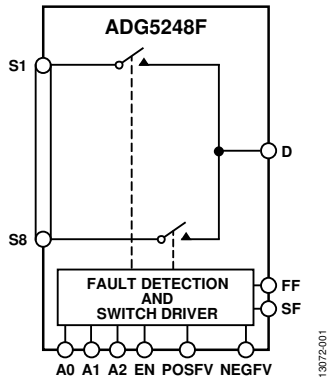

Figure 1. ADG5248F Functional Block Diagram

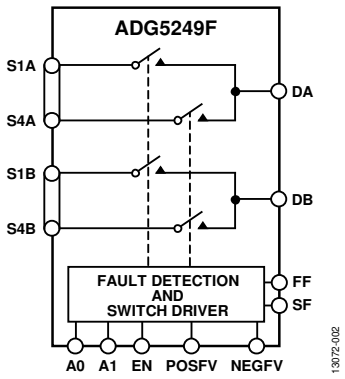

Figure 2. ADG5249F Functional Block Diagram

The low capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch switching and fast settling times are required.

Note that, throughout this data sheet, multifunction pins, such as A0/F0, are referred to either by the entire pin name or by a single function of the pin, for example, A0, when only that function is relevant.

PRODUCT HIGHLIGHTS

1. Source pins are protected against voltages greater than the secondary supply rails, up to −55 V and +55 V.
2. Source pins are protected against voltages between −55 V and +55 V in an unpowered state.
3. Overvoltage detection with digital output indicates operating state of switches.
4. Trench isolation guards against latch-up.
5. Optimized for low charge injection and on capacitance.
6. The ADG5248F/ADG5249F can be operated from a dual supply of ±5 V to ±22 V or a single power supply of 8 V to 44 V.

Rev. A Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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REVISION HISTORY

7/2016—Rev. 0 to Rev. A

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Added Figure 6 ... 16
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Updated Outline Dimensions ... 34
Changes to Ordering Guide ... 34

4/2015—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = 15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +13.5 V, V_{SS} = −13.5 V, see Figure 38
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	250			Ω typ	V_S = ±10 V, I_S = −1 mA
	270	335	395	Ω max	
	250			Ω typ	V_S = ±9 V, I_S = −1 mA
	270	335	395	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	2.5			Ω typ	V_S = ±10 V, I_S = −1 mA
	6	12	13	Ω max	
	2.5			Ω typ	V_S = ±9 V, I_S = −1 mA
	6	12	13	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	6.5			Ω typ	V_S = ±10 V, I_S = −1 mA
	8	9	9	Ω max	
	1.5			Ω typ	V_S = ±9 V, I_S = −1 mA
	3.5	4	4	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 30
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±10 V, V_D = ∓10 V, see Figure 36
	±1	±2	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±10 V, V_D = ∓10 V, see Figure 36
	±1	±5	±10	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = ±10 V, see Figure 37
	±1.5	±20	±25	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage	±66		±78	µA typ	V_{DD} = +16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±55 V, see Figure 35
Power Supplies Grounded or Floating	±25		±40	µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, Ax = 0 V or floating, V_S = ±55 V, see Figure 34
Drain Leakage Current, I_D					
With Overvoltage	±10			nA typ	V_{DD} = +16.5 V, V_{SS} = −16.5 V, GND = 0 V, V_S = ±55 V, see Figure 35
	±50	±70	±90	nA max	
Power Supplies Grounded	±500			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, Ax = 0 V, see Figure 34
	±700	±700	±700	nA max	
Power Supplies Floating	±50	±50	±50	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, Ax = 0 V, see Figure 34
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2.0	V min	
Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.7			µA typ	V_{IN} = GND or V_{DD}
	±1.1		±1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Output Voltage					
High, V_{OH}	2.0			V min	
Low, V_{OL}	0.8			V max	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	210			ns typ	R_L = 1 kΩ, C_L = 35 pF
	290	305	310	ns max	V_S = 10 V, see Figure 50
t_{ON} (EN)	200			ns typ	R_L = 1 kΩ, C_L = 35 pF
	280	295	315	ns max	V_S = 10 V, see Figure 49
t_{OFF} (EN)	105			ns typ	R_L = 1 kΩ, C_L = 35 pF
	120	160	160	ns max	V_S = 10 V, see Figure 49
Break-Before-Make Time Delay, t_D	155			ns typ	R_L = 1 kΩ, C_L = 35 pF
			90	ns min	V_S = 10 V, see Figure 48
Overvoltage Response Time, $t_{RESPONSE}$	90			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 43
	115	130	130	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	745			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 44
	945	965	970	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	90			ns typ	C_L = 12 pF, see Figure 45
Interrupt Flag Recovery Time, t_{DIGREC}	65			µs typ	C_L = 12 pF, see Figure 46
	900			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 47
Charge Injection, Q_{INJ}	−0.8			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 51
Off Isolation	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 41, worst case channel
Channel-to-Channel Crosstalk					R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 40
Adjacent Channels	−75			dB typ	
Nonadjacent Channels	−88			dB typ	
Total Harmonic Distortion Plus Noise, THD + N	0.005			% typ	R_L = 10 kΩ, V_S = 15 V p-p, f = 20 Hz to 20 kHz, see Figure 39
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF, see Figure 42
ADG5248F	190			MHz typ	
ADG5249F	320			MHz typ	
Insertion Loss	10.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 42
C_S (Off)	4			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)					V_S = 0 V, f = 1 MHz
ADG5248F	13			pF typ	
ADG5249F	8			pF typ	
C_D (On), C_S (On)					V_S = 0 V, f = 1 MHz
ADG5248F	19			pF typ	
ADG5249F	14			pF typ	
POWER REQUIREMENTS					V_{DD} = POSFV = +16.5 V; V_{SS} = NEGFV = −16.5 V; GND = 0 V; digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	1.15			mA typ	
I_{POSFV}	0.15			mA typ	
I_{DD} + I_{POSFV}	2		2	mA max	
I_{GND}	0.75			mA typ	
	1.25		1.25	mA max	
I_{SS}	0.45			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	0.8		0.85	mA max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Fault Mode					V_S = ±55 V
I_{DD}	1.4			mA typ	
I_{POSFV}	0.2			mA typ	
I_{DD} + I_{POSFV}	2.2		2.3	mA max	
I_{GND}	0.9			mA typ	
	1.6		1.7	mA max	
I_{SS}	0.45			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.1	mA max	
V_{DD}/V_{SS}			±5	V min	GND = 0 V
			±22	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = 20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = +18 V, V_{SS} = −18 V, see Figure 38
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	260			Ω typ	V_S = ±15 V, I_S = −1 mA
	280	345	405	Ω max	
	250			Ω typ	V_S = ±13.5 V, I_S = −1 mA
	270	335	395	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	2.5			Ω typ	V_S = ±15 V, I_S = −1 mA
	6	12	13	Ω max	
	2.5			Ω typ	V_S = ±13.5 V, I_S = −1 mA
	6	12	13	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	12.5			Ω typ	V_S = ±15 V, I_S = −1 mA
	14	15	15	Ω max	
	1.5			Ω typ	V_S = ±13.5 V, I_S = −1 mA
	3.5	4	4	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 30
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ∓15 V, see Figure 36
	±1	±2	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±15 V, V_D = ∓15 V, see Figure 36
	±1	±5	±10	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = ±15 V, see Figure 37
	±1.5	±20	±25	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage	±66			µA typ	V_{DD} = 22 V, V_{SS} = −22 V, GND = 0 V, V_S = ±55 V, see Figure 35
Power Supplies Grounded or Floating	±25			µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, Ax = 0 V or floating, V_S = ±55 V, see Figure 34

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Drain Leakage Current, I_D					
With Overvoltage	±10			nA typ	V_{DD} = +22 V, V_{SS} = −22 V, GND = 0 V, V_S = ±55 V, see Figure 35
	±2	±2	±2	µA max	
Power Supplies Grounded	±500			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, Ax = 0 V, see Figure 34
	±700	±700	±700	nA max	
Power Supplies Floating	±50	±50	±50	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, Ax = 0 V, see Figure 34
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2.0	V min	
Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.7			µA typ	V_{IN} = GND or V_{DD}
	±1.1		±1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	
Output Voltage					
High, V_{OH}	2.0			V min	
Low, V_{OL}	0.8			V max	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	230			ns typ	R_L = 1 kΩ, C_L = 35 pF
	335	340	340	ns max	V_S = 10 V, see Figure 50
t_{ON} (EN)	225			ns typ	R_L = 1 kΩ, C_L = 35 pF
	325	340	340	ns max	V_S = 10 V, see Figure 49
t_{OFF} (EN)	100			ns typ	R_L = 1 kΩ, C_L = 35 pF
	135	155	155	ns max	V_S = 10 V, see Figure 49
Break-Before-Make Time Delay, t_D	175			ns typ	R_L = 1 kΩ, C_L = 35 pF
			95	ns min	V_S = 10 V, see Figure 48
Overvoltage Response Time, $t_{RESPONSE}$	75			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 43
	105	105	105	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	820			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 44
	1100	1250	1400	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	75			ns typ	C_L = 12 pF, see Figure 45
Interrupt Flag Recovery Time, t_{DIGREC}	65			µs typ	C_L = 12 pF, see Figure 46
	1000			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 47
Charge Injection, Q_{INJ}	−1.2			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 51
Off Isolation	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 41, worst case channel
Channel-to-Channel Crosstalk					R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 40
Adjacent Channels	−75			dB typ	
Nonadjacent Channels	−88			dB typ	
Total Harmonic Distortion Plus Noise, THD + N	0.005			% typ	R_L = 10 kΩ, V_S = 20 V p-p, f = 20 Hz to 20 kHz, see Figure 39
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF, see Figure 42
ADG5248F	190			MHz typ	
ADG5249F	320			MHz typ	
Insertion Loss	10.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 42
C_S (Off)	4			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)					V_S = 0 V, f = 1 MHz
ADG5248F	13			pF typ	
ADG5249F	8			pF typ	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
C_D (On), C_S (On)					V_S = 0 V, f = 1 MHz
ADG5248F	19			pF typ	
ADG5249F	14			pF typ	
POWER REQUIREMENTS					V_{DD} = POSFV = +22 V; V_{SS} = NEGFV = −22 V; digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	1.15			mA typ	
I_{POSFV}	0.15			mA typ	
I_{DD} + I_{POSFV}	2		2	mA max	
I_{GND}	0.75			mA typ	
	1.25		1.25	mA max	
I_{SS}	0.45			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	0.8		0.85	mA max	
Fault Mode					V_S = ±55 V
I_{DD}	1.4			mA typ	
I_{POSFV}	0.2			mA typ	
I_{DD} + I_{POSFV}	2.2		2.3	mA max	
I_{GND}	0.9			mA typ	
	1.6		1.7	mA max	
I_{SS}	0.45			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.1	mA max	
V_{DD}/V_{SS}			±5	V min	GND = 0 V
			±22	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 10.8 V, V_{SS} = 0 V, see Figure 38
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	630			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	690	710	730	Ω max	
	270			Ω typ	V_S = 3.5 V to 8.5 V, I_S = −1 mA
	290	355	410	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	6			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	17	19	19	Ω max	
	3			Ω typ	V_S = 3.5 V to 8.5 V, I_S = −1 mA
	6.5	11	12	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	380			Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	440	460	460	Ω max	
	25			Ω typ	V_S = 3.5 V to 8.5 V, I_S = −1 mA
	27	28	28	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 30
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 36
	±1	±2	±5	nA max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 36
	±1	±5	±10	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = 1 V/10 V, see Figure 37
	±1.5	±20	±25	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage	±63			µA typ	V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, see Figure 35
Power Supplies Grounded or Floating	±25			µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, Ax = 0 V or floating, V_S = ±55 V, see Figure 34
Drain Leakage Current, I_D					
With Overvoltage	±10			nA typ	V_{DD} = 13.2 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, see Figure 35
	±50	±70	±90	nA max	
Power Supplies Grounded	±500			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, Ax = 0 V, see Figure 34
	±700	±700	±700	nA max	
Power Supplies Floating	±50	±50	±50	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, Ax = 0 V, see Figure 34
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2.0	V min	
Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.7			µA typ	V_{IN} = GND or V_{DD}
	±1.1		±1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	
Output Voltage					
High, V_{OH}	2.0			V min	
Low, V_{OL}	0.8			V max	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	165			ns typ	R_L = 1 kΩ, C_L = 35 pF
	205	215	230	ns max	V_S = 8 V, see Figure 50
t_{ON} (EN)	160			ns typ	R_L = 1 kΩ, C_L = 35 pF
	200	215	230	ns max	V_S = 8 V, see Figure 49
t_{OFF} (EN)	125			ns typ	R_L = 1 kΩ, C_L = 35 pF
	150	155	155	ns max	V_S = 8 V, see Figure 49
Break-Before-Make Time Delay, t_D	100			ns typ	R_L = 1 kΩ, C_L = 35 pF
			60	ns min	V_S = 8 V, see Figure 48
Overvoltage Response Time, $t_{RESPONSE}$	110			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 43
	145	145	145	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	500			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 44
	655	720	765	ns max	
Interrupt Flag Response Time, $t_{DIGRESP}$	95			ns typ	C_L = 12 pF, see Figure 45
Interrupt Flag Recovery Time, t_{DIGREC}	65			µs typ	C_L = 12 pF, see Figure 46
	900			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 47
Charge Injection, Q_{INJ}	0.2			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 51
Off Isolation	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 41, worst case channel
Channel-to-Channel Crosstalk					R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 40
Adjacent Channels	−75			dB typ	
Nonadjacent Channels	−88			dB typ	
Total Harmonic Distortion Plus Noise, THD + N	0.044			% typ	R_L = 10 kΩ, V_S = 6 V p-p, f = 20 Hz to 20 kHz, see Figure 39

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF, see Figure 42
ADG5248F	175			MHz typ	
ADG5249F	290			MHz typ	
Insertion Loss	10.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 42
C_S (Off)	4			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)					V_S = 6 V, f = 1 MHz
ADG5248F	14			pF typ	
ADG5249F	8			pF typ	
C_D (On), C_S (On)					V_S = 6 V, f = 1 MHz
ADG5248F	20			pF typ	
ADG5249F	14			pF typ	
POWER REQUIREMENTS					V_{DD} = 13.2 V; V_{SS} = 0 V; digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	1.15			mA typ	
I_{POSFV}	0.15			mA typ	
I_{DD} + I_{POSFV}	2		2	mA max	
I_{GND}	0.75			mA typ	
	1.4		1.4	mA max	
I_{SS}	0.3			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	0.65		0.7	mA max	
Fault Mode					V_S = ±55 V
I_{DD}	1.4			mA typ	
I_{POSFV}	0.2			mA typ	
I_{DD} + I_{POSFV}	2.2		2.3	mA max	
I_{GND}	0.9			mA typ	
	1.6		1.7	mA max	
I_{SS}	0.45			mA typ	Digital inputs = 5 V
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.1	mA max	V_S = ±55 V, V_D = 0 V
V_{DD}			8	V min	GND = 0 V
			44	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, $C_{DECOUPLING}$ = 0.1 µF, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					V_{DD} = 32.4 V, V_{SS} = 0 V, see Figure 38
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	310			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	335	415	480	Ω max	
	250			Ω typ	V_S = 4.5 V to 28 V, I_S = −1 mA
	270	335	395	Ω max	
On-Resistance Match Between Channels, ΔR_{ON}	3			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	7	16	18	Ω max	
	3			Ω typ	V_S = 4.5 V to 28 V, I_S = −1 mA
	6.5	11	12	Ω max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
On-Resistance Flatness, $R_{FLAT(ON)}$	62			Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	70	85	100	Ω max	
	1.5			Ω typ	V_S = 4.5 V to 28 V, I_S = −1 mA
	3.5	4	4	Ω max	
Threshold Voltage, V_T	0.7			V typ	See Figure 30
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V, see Figure 36
	±1	±2	±5	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V, see Figure 36
	±1	±5	±10	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.3			nA typ	V_S = V_D = 1 V/30 V, see Figure 37
	±1.5	±20	±25	nA max	
FAULT					
Source Leakage Current, I_S					
With Overvoltage	±58			µA typ	V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V, V_S = +55 V, −40 V, see Figure 35
Power Supplies Grounded or Floating	±25			µA typ	V_{DD} = 0 V or floating, V_{SS} = 0 V or floating, GND = 0 V, Ax = 0 V or floating, V_S = ±55 V, see Figure 34
Drain Leakage Current, I_D					
With Overvoltage	±10			nA typ	V_{DD} = 39.6 V, V_{SS} = 0 V, GND = 0 V, V_S = +55 V, −40 V, see Figure 35
	±50	±70	±90	nA max	
Power Supplies Grounded	±500			nA typ	V_{DD} = 0 V, V_{SS} = 0 V, GND = 0 V, V_S = ±55 V, Ax = 0 V, see Figure 34
	±700	±700	±700	nA max	
Power Supplies Floating	±50	±50	±50	µA typ	V_{DD} = floating, V_{SS} = floating, GND = 0 V, V_S = ±55 V, Ax = 0 V, see Figure 34
DIGITAL INPUTS					
Input Voltage					
High, V_{INH}			2.0	V min	
Low, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.7			µA typ	V_{IN} = V_{GND} or V_{DD}
	±1.1		±1.2	µA max	
Digital Input Capacitance, C_{IN}	5.0			pF typ	
Output Voltage					
High, V_{OH}	2.0			V min	
Low, V_{OL}	0.8			V max	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	195			ns typ	R_L = 1 kΩ, C_L = 35 pF
	255	275	285	ns max	V_S = 18 V, see Figure 50
t_{ON} (EN)	190			ns typ	R_L = 1 kΩ, C_L = 35 pF
	245	270	280	ns max	V_S = 18 V, see Figure 49
t_{OFF} (EN)	105			ns typ	R_L = 1 kΩ, C_L = 35 pF
	135	145	145	ns max	V_S = 18 V, see Figure 49
Break-Before-Make Time Delay, t_D	110			ns typ	R_L = 1 kΩ, C_L = 35 pF
			60	ns min	V_S = 18 V, see Figure 48
Overvoltage Response Time, $t_{RESPONSE}$	60			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 43
	80	85	85	ns max	
Overvoltage Recovery Time, $t_{RECOVERY}$	1400			ns typ	R_L = 1 kΩ, C_L = 5 pF, see Figure 44
	1900	2100	2200	ns max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Interrupt Flag Response Time, $t_{DIGRESP}$	85			ns typ	C_L = 12 pF, see Figure 45
Interrupt Flag Recovery Time, t_{DIGREC}	65			µs typ	C_L = 12 pF, see Figure 46
	1600			ns typ	C_L = 12 pF, R_{PULLUP} = 1 kΩ, see Figure 47
Charge Injection, Q_{INJ}	−1.2			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF, see Figure 51
Off Isolation	−75			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 41, worst case channel
Channel-to-Channel Crosstalk					R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 40
Adjacent Channels	−75			dB typ	
Nonadjacent Channels	−88			dB typ	
Total Harmonic Distortion Plus Noise, THD + N	0.007			% typ	R_L = 10 kΩ, V_S = 18 V p-p, f = 20 Hz to 20 kHz, see Figure 39
−3 dB Bandwidth					R_L = 50 Ω, C_L = 5 pF, see Figure 42
ADG5248F	200			MHz typ	
ADG5249F	320			MHz typ	
Insertion Loss	10.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 42
C_S (Off)	4			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)					V_S = 18 V, f = 1 MHz
ADG5248F	13			pF typ	
ADG5249F	7			pF typ	
C_D (On), C_S (On)					V_S = 18 V, f = 1 MHz
ADG5248F	18			pF typ	
ADG5249F	12			pF typ	
POWER REQUIREMENTS					V_{DD} = 39.6 V; V_{SS} = 0 V; digital inputs = 0 V, 5 V, or V_{DD}
Normal Mode					
I_{DD}	1.15			mA typ	
I_{POSFV}	0.15			mA typ	
I_{DD} + I_{POSFV}	2		2	mA max	
I_{GND}	0.75			mA typ	
	1.4		1.4	mA max	
I_{SS}	0.3			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	0.65		0.7	mA max	
Fault Mode					V_S = +55 V, −40 V
I_{DD}	1.4			mA typ	
I_{POSFV}	0.2			mA typ	
I_{DD} + I_{POSFV}	2.2		2.3	mA max	
I_{GND}	0.9			mA typ	
	1.6		1.7	mA max	
I_{SS}	0.45			mA typ	
I_{NEGFV}	0.2			mA typ	
I_{SS} + I_{NEGFV}	1.0		1.1	mA max	
V_{DD}			8	V min	GND = 0 V
			44	V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx,[1] D, OR Dx

Table 5.

Parameter	25°C	85°C	125°C	Unit	Test Conditions/Comments
ADG5248F					
20-Lead TSSOP, θ_{JA} = 112.6°C/W	27	16	8	mA max	$V_S = V_{SS}$ to $V_{DD} - 4.5$ V
	16	11	7	mA max	$V_S = V_{SS}$ to V_{DD}
20-Lead LFCSP, θ_{JA} = 30.4°C/W	48	25	11	mA max	$V_S = V_{SS}$ to $V_{DD} - 4.5$ V
	27	17	9	mA max	$V_S = V_{SS}$ to V_{DD}
ADG5249F					
20-Lead TSSOP, θ_{JA} = 112.6°C/W	20	13	8	mA max	$V_S = V_{SS}$ to $V_{DD} - 4.5$ V
	12	8	6	mA max	$V_S = V_{SS}$ to V_{DD}
20-Lead LFCSP, θ_{JA} = 30.4°C/W	36	20	10	mA max	$V_S = V_{SS}$ to $V_{DD} - 4.5$ V
	21	13	8	mA max	$V_S = V_{SS}$ to V_{DD}

[1] Sx is the S1 to S8 pins on the ADG5248F, and the S1A to S4A and S1B to S4B pins on the ADG5249F.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	−48 V to +0.3 V
POSFV to GND	−0.3 V to V_{DD} + 0.3 V
NEGFV to GND	V_{SS} − 0.3 V to + 0.3 V
Sx Pins	−55 V to +55 V
Sx to V_{DD} or V_{SS}	80 V
V_S to V_D	80 V
D or Dx Pins[1]	NEGFV − 0.7 V to POSFV + 0.7 V or 30 mA, whichever occurs first
Digital Inputs	GND − 0.7 V to 48 V or 30 mA, whichever occurs first
Peak Current, Sx, D, or Dx Pins	72.5 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx, D, or Dx Pins	Data[2] + 15%
Digital Outputs	GND − 0.7 V to 6 V or 30 mA, whichever occurs first
D or Dx Pins, Overvoltage State, Load Current	1 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA} (4-Layer Board)	
20-Lead TSSOP	112.6°C/W
20-Lead LFCSP	30.4°C/W
Reflow Soldering Peak Temperature, Pb-Free	As per JEDEC J-STD-020

[1] Overvoltages at the D or Dx pins are clamped by internal diodes. Limit the current to the maximum ratings given.
[2] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

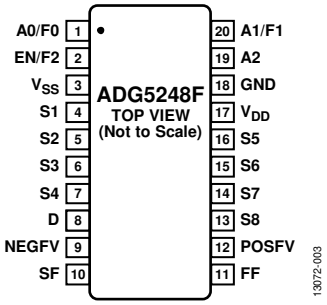

Figure 3. ADG5248F Pin Configuration (TSSOP)

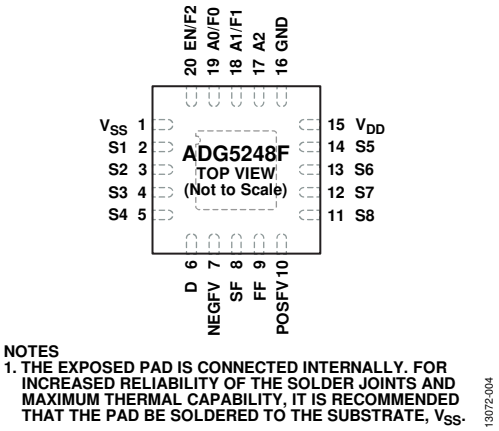

Figure 4. ADG5248F Pin Configuration (LFCSP)

Table 7. ADG5248F Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	A0/F0	Logic Control Input (A0). See Table 8. Decoder Pin (F0). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 9.
2	20	EN/F2	Active High Digital Input (EN). When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switches. Decoder Pin (F2). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 9.
3	1	V_{SS}	Most Negative Power Supply Potential.
4	2	S1	Overvoltage Protected Source Terminal 1. This pin can be an input or an output.
5	3	S2	Overvoltage Protected Source Terminal 2. This pin can be an input or an output.
6	4	S3	Overvoltage Protected Source Terminal 3. This pin can be an input or an output.
7	5	S4	Overvoltage Protected Source Terminal 4. This pin can be an input or an output.
8	6	D	Drain Terminal. This pin can be an input or an output.
9	7	NEGFV	Negative Fault Voltage. This pin is the negative supply voltage that determines the overvoltage protection level. If a secondary supply is not used, connect this pin to V_{SS}.
10	8	SF	Specific Fault Digital Output. This pin has a high output (weak internal pull-up resistor, nominally 3 V output) when the device is in normal operation, or a low output when a fault condition is detected on a specific pin, depending on the state of F0, F1, and F2 as shown in Table 9.
11	9	FF	Fault Flag Digital Output. This pin has a high output when the device is in normal operation, or a low output when a fault condition occurs on any of the Sx inputs. The FF pin has a weak internal pull-up resistor that allows multiple signals to be combined into a single interrupt for larger modules that contain multiple devices.
12	10	POSFV	Positive Fault Voltage. This pin is the positive supply voltage that determines the overvoltage protection level. If a secondary supply is not used, connect this pin to V_{DD}.
13	11	S8	Overvoltage Protected Source Terminal 8. This pin can be an input or an output.
14	12	S7	Overvoltage Protected Source Terminal 7. This pin can be an input or an output.
15	13	S6	Overvoltage Protected Source Terminal 6. This pin can be an input or an output.
16	14	S5	Overvoltage Protected Source Terminal 5. This pin can be an input or an output.
17	15	V_{DD}	Most Positive Power Supply Potential.
18	16	GND	Ground (0 V) Reference.
19	17	A2	Logic Control Input.
20	18	A1/F1	Logic Control Input (A1). See Table 8. Decoder Pin (F1). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 9.
Not Applicable	Exposed Pad	EP	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 8. ADG5248F Switch Selection Truth Table

A2	A1	A0	EN	On Switch
X[1]	X[1]	X[1]	0	None
0	0	0	1	S1
0	0	1	1	S2
0	1	0	1	S3
0	1	1	1	S4
1	0	0	1	S5
1	0	1	1	S6
1	1	0	1	S7
1	1	1	1	S8

[1] X is don't care.

Table 9. ADG5248F Fault Diagnostic Output Truth Table

	State of Specific Flag (SF) with Control Inputs (F2, F1, F0)								
Switch in Fault[1]	0, 0, 0	0, 0, 1	0, 1, 0	0, 1, 1	1, 0, 0	1, 0, 1	1, 1, 0	1, 1, 1	State of the Fault Flag (FF)
None	1	1	1	1	1	1	1	1	1
S1	0	1	1	1	1	1	1	1	0
S2	1	0	1	1	1	1	1	1	0
S3	1	1	0	1	1	1	1	1	0
S4	1	1	1	0	1	1	1	1	0
S5	1	1	1	1	0	1	1	1	0
S6	1	1	1	1	1	0	1	1	0
S7	1	1	1	1	1	1	0	1	0
S8	1	1	1	1	1	1	1	0	0

[1] More than one switch can be in fault. See the Applications Information section for more information.

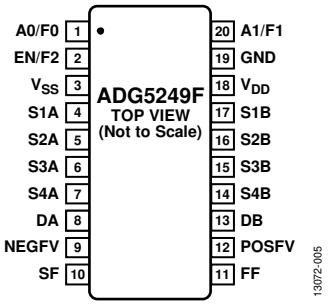

Figure 5. ADG5249F Pin Configuration (TSSOP)

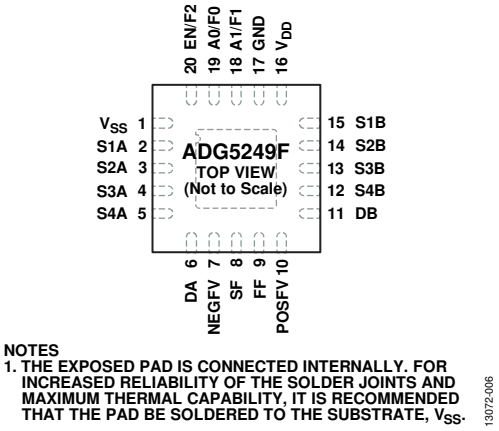

Figure 6. ADG5249F Pin Configuration (LFCSP)

Table 10. ADG5249F Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	19	A0/F0	Logic Control Input (A0). See Table 11. Decoder Pin (F0). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 12.
2	20	EN/F2	Active High Digital Input (EN). When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switches. Decoder Pin (F2). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 12.
3	1	V_{SS}	Most Negative Power Supply Potential.
4	2	S1A	Overvoltage Protected Source Terminal 1A. This pin can be an input or an output.
5	3	S2A	Overvoltage Protected Source Terminal 2A. This pin can be an input or an output.
6	4	S3A	Overvoltage Protected Source Terminal 3A. This pin can be an input or an output.
7	5	S4A	Overvoltage Protected Source Terminal 4A. This pin can be an input or an output.
8	6	DA	Drain Terminal A. This pin can be an input or an output.
9	7	NEGFV	Negative Fault Voltage. This pin is the negative supply voltage that determines the overvoltage protection level. If a secondary supply is not used, connect this pin to V_{SS}.
10	8	SF	Specific Fault Digital Output. This pin has a high output (weak internal pull-up resistor, nominally 3 V output) when the device is in normal operation, or a low output when a fault condition is detected on a specific pin, depending on the state of F0, F1, and, F2 as shown in Table 12.
11	9	FF	Fault Flag Digital Output. This pin has a high output when the device is in normal operation, or a low output when a fault condition occurs on any of the Sx inputs. The FF pin has a weak internal pull-up resistor that allows multiple signals to be combined into a single interrupt for larger modules that contain multiple devices.
12	10	POSFV	Positive Fault Voltage. This pin is the positive supply voltage that determines the overvoltage protection level. If a secondary supply is not used, connect this pin to V_{DD}.
13	11	DB	Drain Terminal B. This pin can be an input or an output.
14	12	S4B	Overvoltage Protected Source Terminal 4B. This pin can be an input or an output.
15	13	S3B	Overvoltage Protected Source Terminal 3B. This pin can be an input or an output.
16	14	S2B	Overvoltage Protected Source Terminal 2B. This pin can be an input or an output.
17	15	S1B	Overvoltage Protected Source Terminal 1B. This pin can be an input or an output.
18	16	V_{DD}	Most Positive Power Supply Potential.
19	17	GND	Ground (0 V) Reference.
20	18	A1/F1	Logic Control Input (A1). See Table 11. Decoder Pin (F1). This pin is used together with the specific fault pin (SF) to indicate which input is in a fault condition. See Table 12.
Not Applicable	Exposed Pad	EP	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 11. ADG5249F Switch Selection Truth Table

A1	A0	EN	On Switch Pair
X[1]	X[1]	0	None
0	0	1	S1x
0	1	1	S2x
1	0	1	S3x
1	1	1	S4x

[1] X is don't care.

Table 12. ADG5249F Fault Diagnostic Output Truth Table

	State of Specific Flag (SF) with Control Inputs (F2, F1, F0)								
Switch in Fault[1]	0, 0, 0	0, 0, 1	0, 1, 0	0, 1, 1	1, 0, 0	1, 0, 1	1, 1, 0	1, 1, 1	State of the Fault Flag (FF)
None	1	1	1	1	1	1	1	1	1
S1A	0	1	1	1	1	1	1	1	0
S2A	1	0	1	1	1	1	1	1	0
S3A	1	1	0	1	1	1	1	1	0
S4A	1	1	1	0	1	1	1	1	0
S1B	1	1	1	1	0	1	1	1	0
S2B	1	1	1	1	1	0	1	1	0
S3B	1	1	1	1	1	1	0	1	0
S4B	1	1	1	1	1	1	1	0	0

[1] More than one switch can be in fault. See the Applications Information section for more information.

TYPICAL PERFORMANCE CHARACTERISTICS

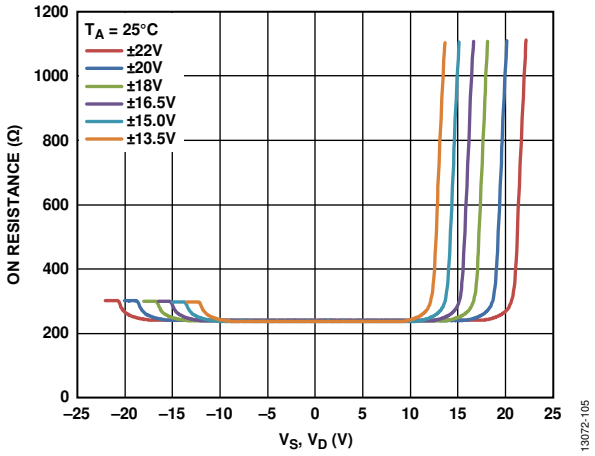

Figure 7. R_{ON} as a Function of V_S, V_D, Dual Supply

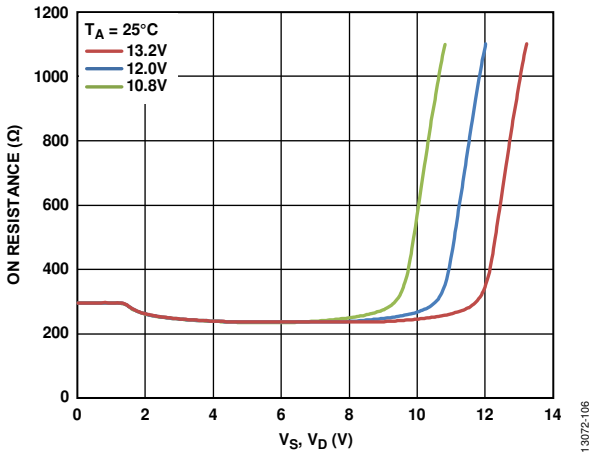

Figure 8. R_{ON} as a Function of V_S, V_D, 12 V Single Supply

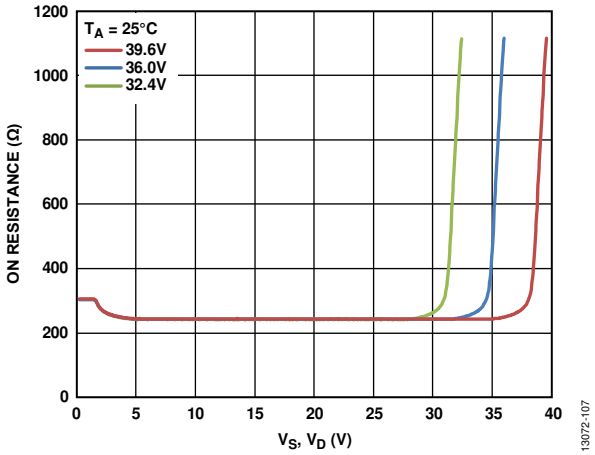

Figure 9. R_{ON} as a Function of V_S, V_D, 36 V Single Supply

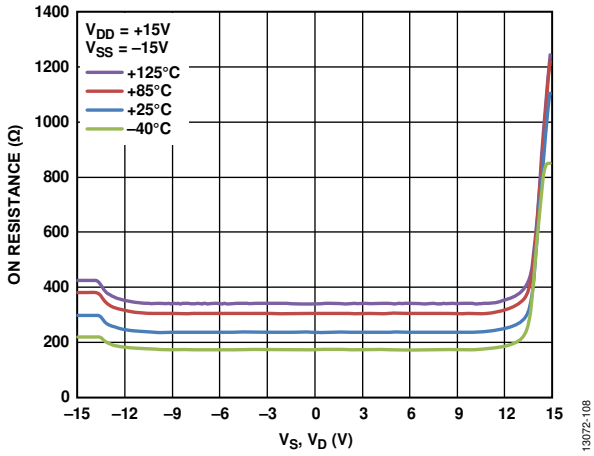

Figure 10. R_{ON} as a Function of V_S, V_D for Different Temperatures, ±15 V Dual Supply

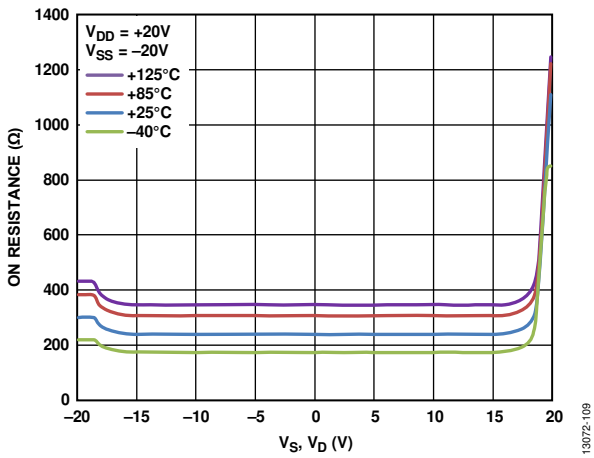

Figure 11. R_{ON} as a Function of V_S, V_D for Different Temperatures, ±20 V Dual Supply

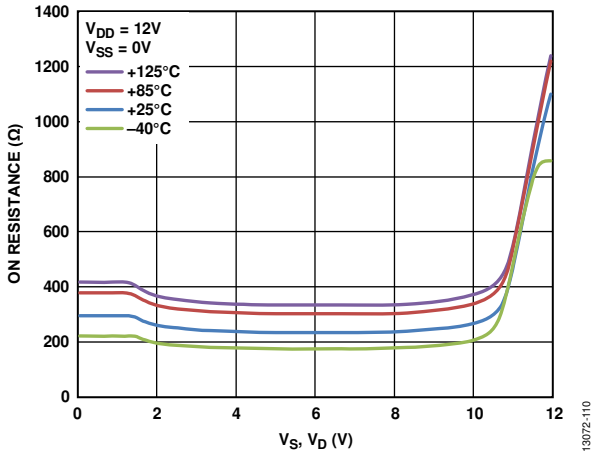

Figure 12. R_{ON} as a Function of V_S, V_D for Different Temperatures, 12 V Single Supply

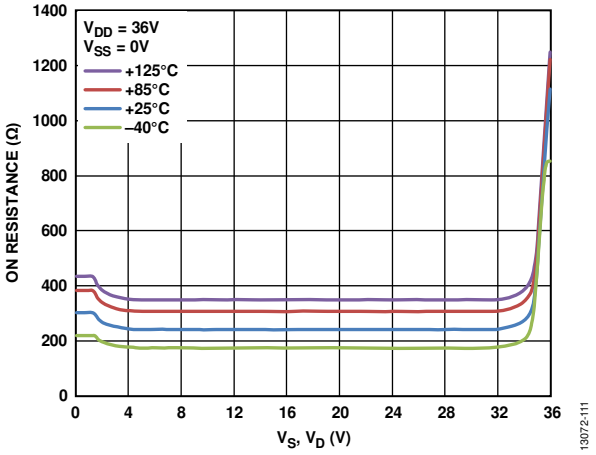

Figure 13. R_{ON} as a Function of V_S, V_D for Different Temperatures, 36 V Single Supply

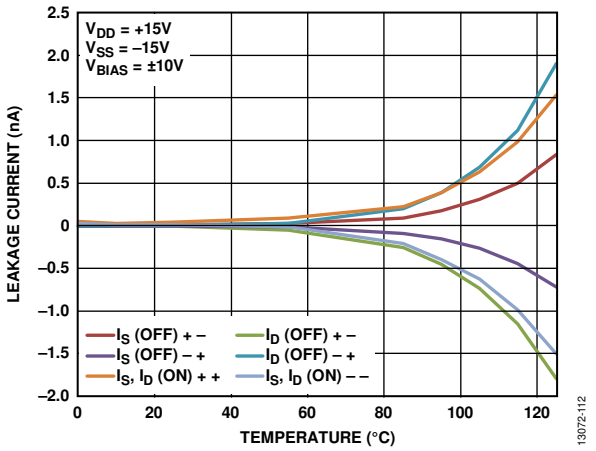

Figure 14. Leakage Current vs. Temperature, ±15 V Dual Supply

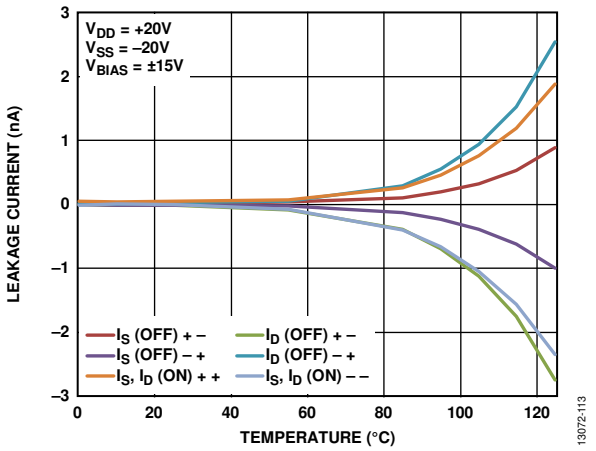

Figure 15. Leakage Current vs. Temperature, ±20 V Dual Supply

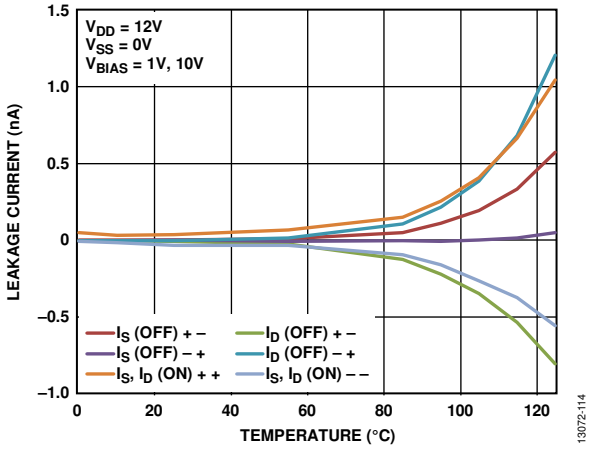

Figure 16. Leakage Current vs. Temperature, 12 V Single Supply

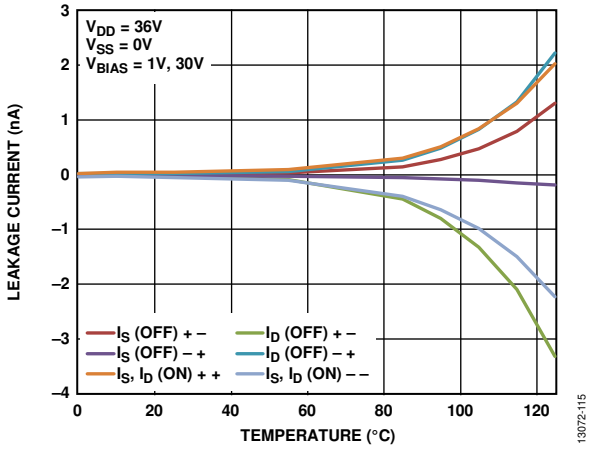

Figure 17. Leakage Current vs. Temperature, 36 V Single Supply

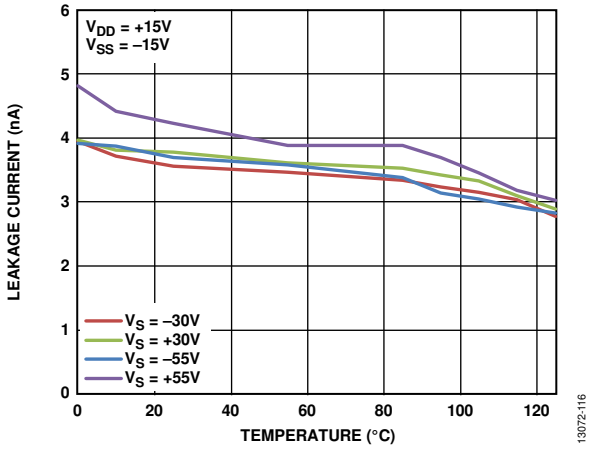

Figure 18. Overvoltage Leakage Current vs. Temperature, ±15 V Dual Supply

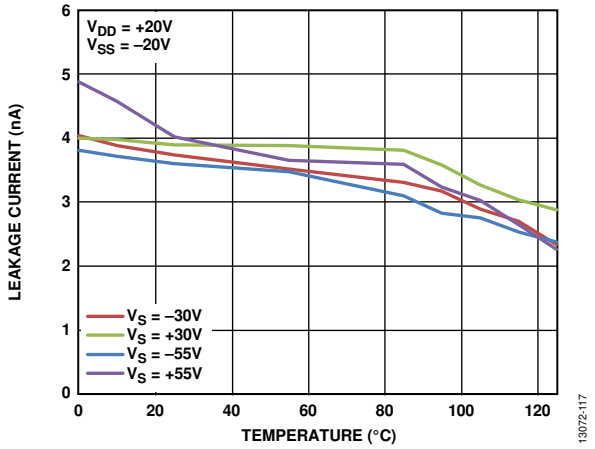

Figure 19. Overvoltage Leakage Current vs. Temperature, ±20 V Dual Supply

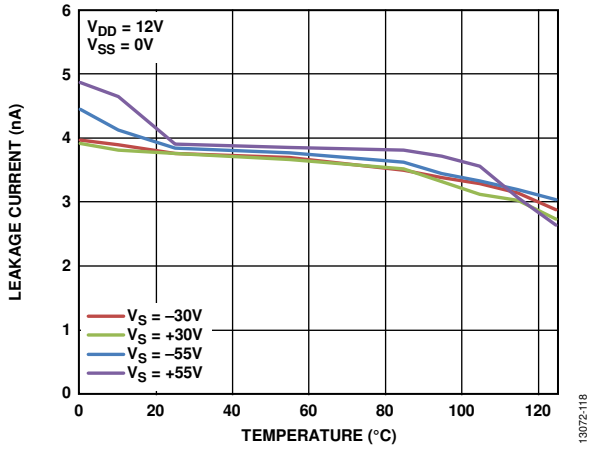

Figure 20. Overvoltage Leakage Current vs. Temperature, 12 V Single Supply

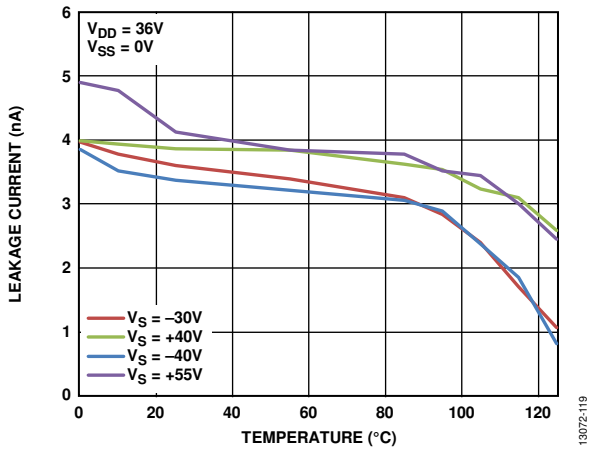

Figure 21. Overvoltage Leakage Current vs. Temperature, 36 V Single Supply

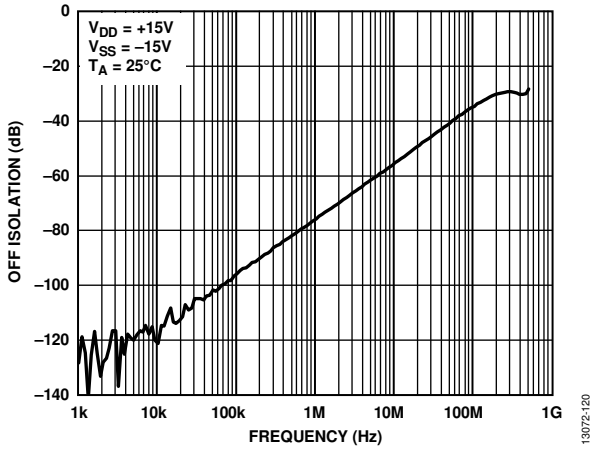

Figure 22. Off Isolation vs. Frequency, ±15 V Dual Supply

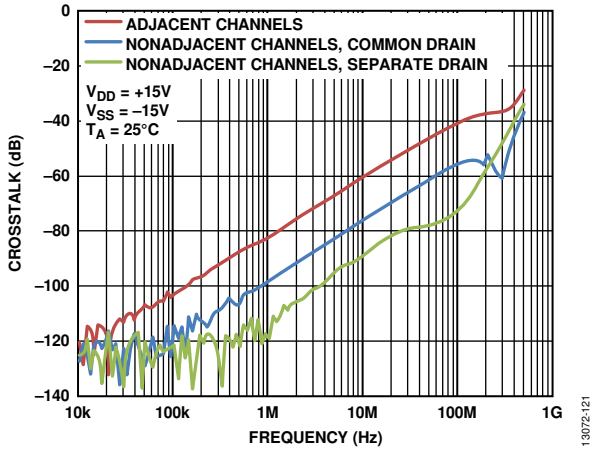

Figure 23. Crosstalk vs. Frequency, ±15 V Dual Supply

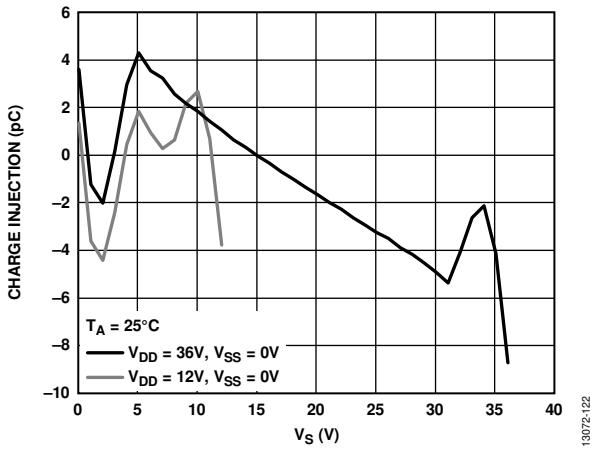

Figure 24. Charge Injection vs. Source Voltage (V_S), Single Supply

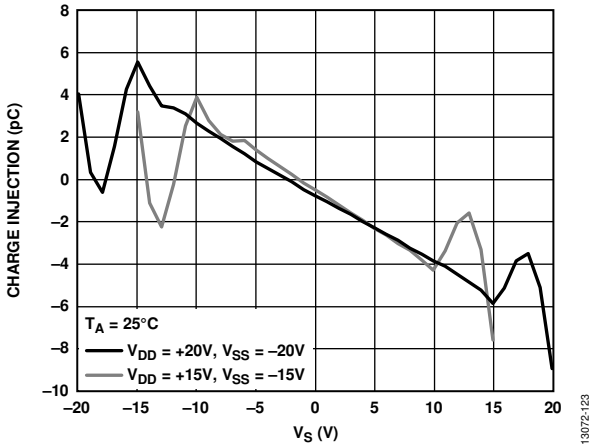

Figure 25. Charge Injection vs. Source Voltage (V_S), Dual Supply

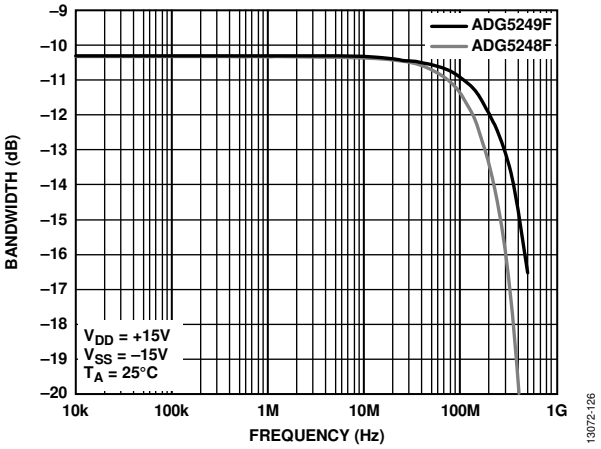

Figure 28. Bandwidth vs. Frequency

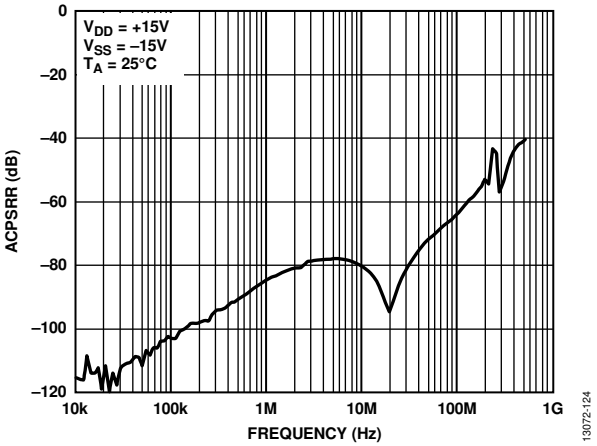

Figure 26. ACPSRR vs. Frequency, ±15 V Dual Supply

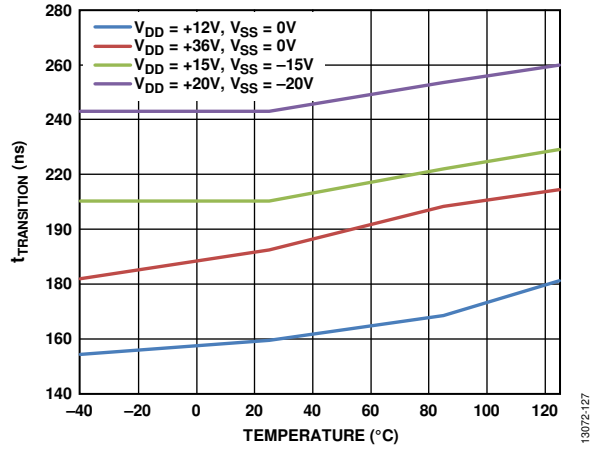

Figure 29. $t_{TRANSITION}$ vs. Temperature

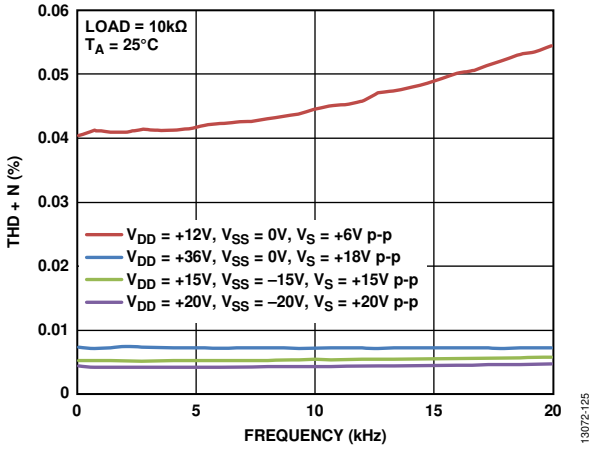

Figure 27. THD + N vs. Frequency

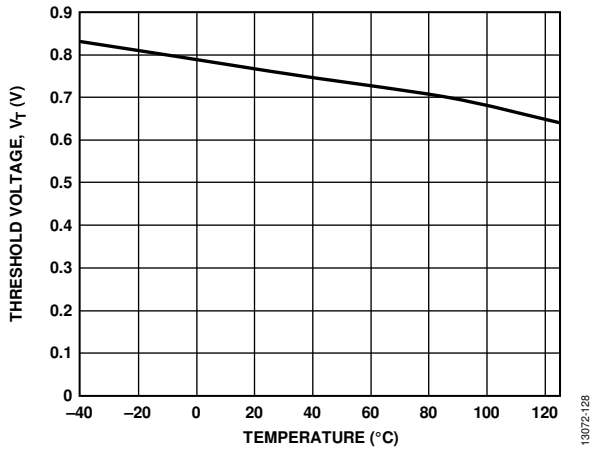

Figure 30. Threshold Voltage (V_T) vs. Temperature

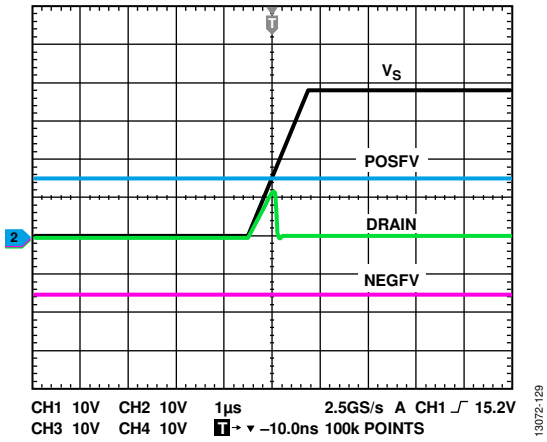

Figure 31. Drain Output Response to Positive Overvoltage

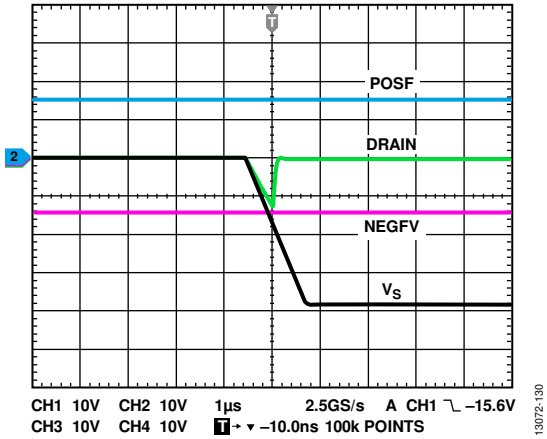

Figure 32. Drain Output Response to Negative Overvoltage

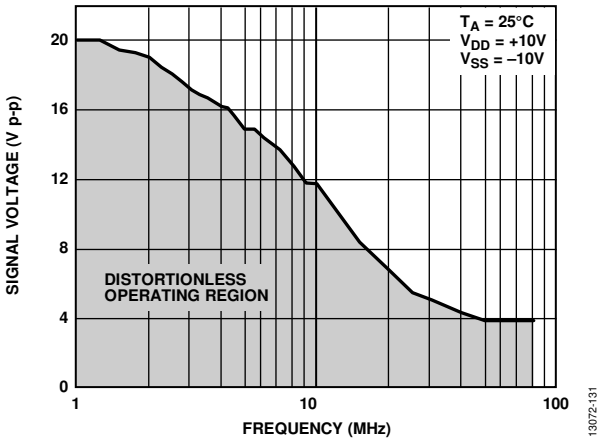

Figure 33. Large Signal Voltage Tracking vs. Frequency

TEST CIRCUITS

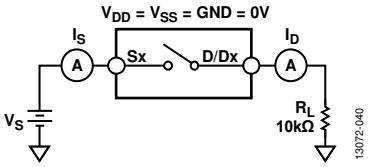

Figure 34. Switch Unpowered Leakage

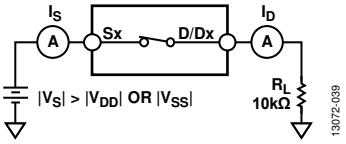

Figure 35. Switch Overvoltage Leakage

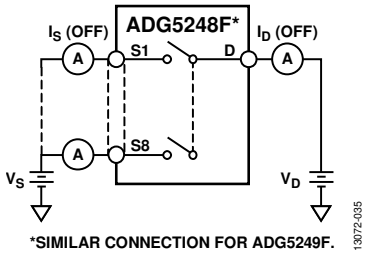

Figure 36. Off Leakage

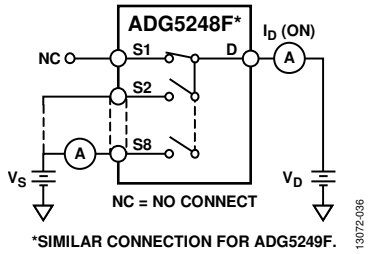

Figure 37. On Leakage

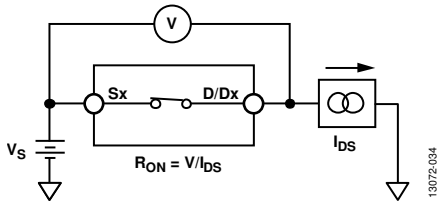

Figure 38. On Resistance

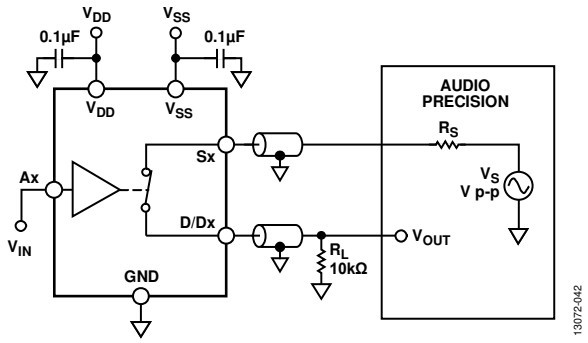

Figure 39. THD + N

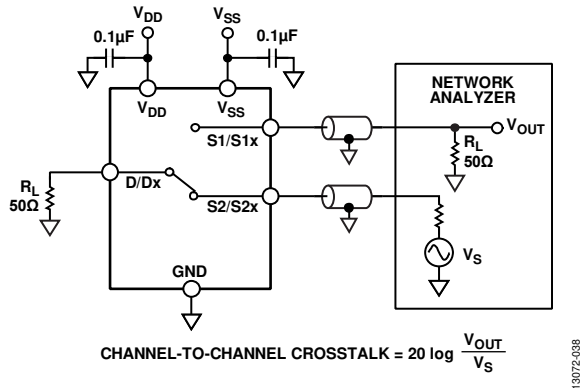

Figure 40. Channel-to-Channel Crosstalk

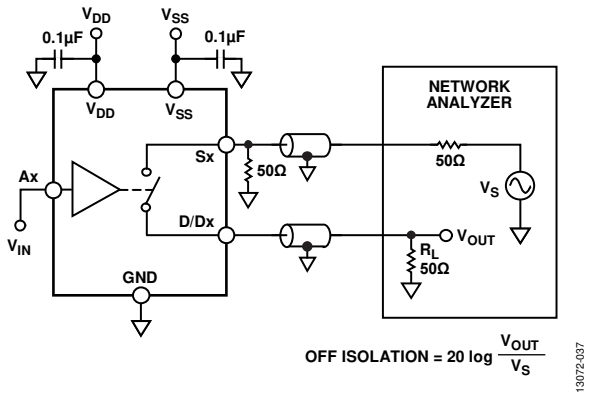

Figure 41. Off Isolation

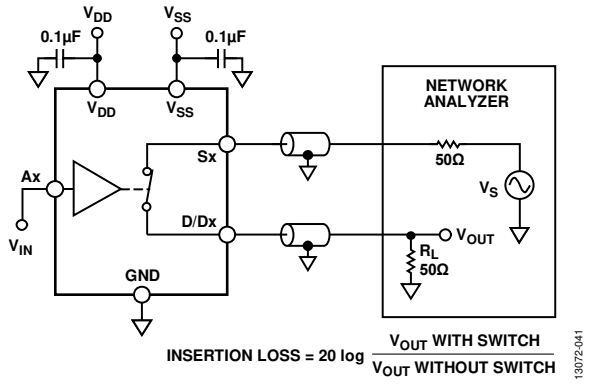

Figure 42. Bandwidth

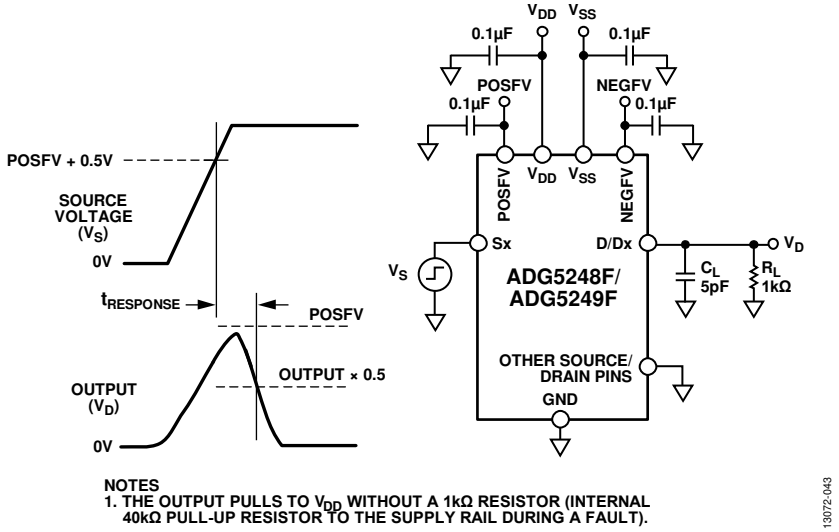

Figure 43. Overvoltage Response Time, $t_{RESPONSE}$

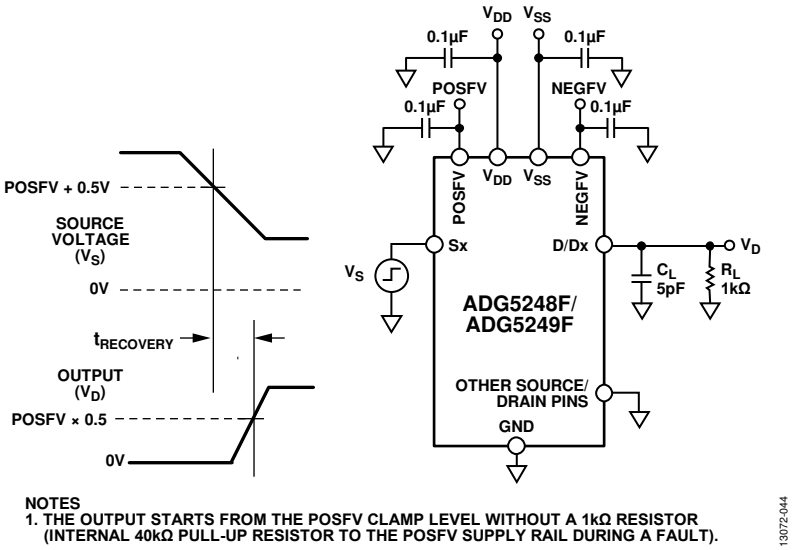

Figure 44. Overvoltage Recovery Time, $t_{RECOVERY}$

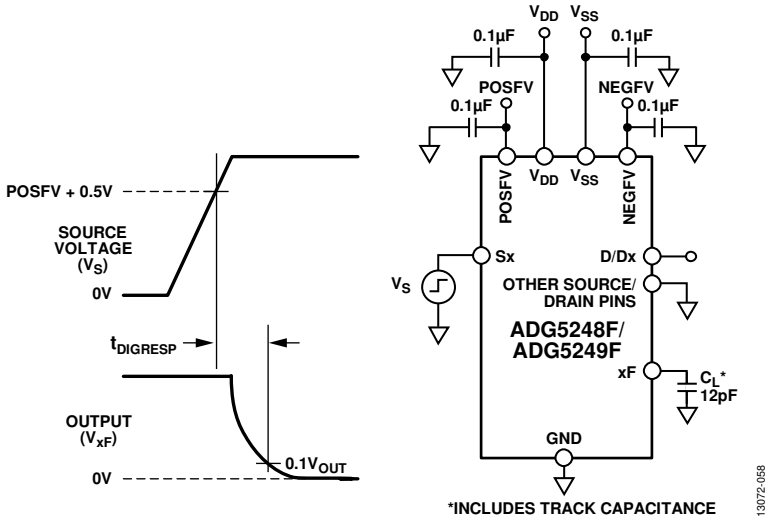

Figure 45. Interrupt Flag Response Time, $t_{DIGRESP}$

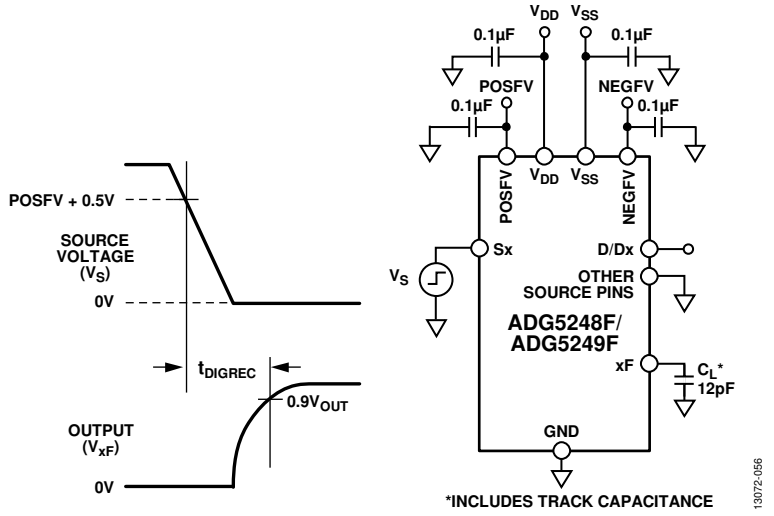

Figure 46. Interrupt Flag Recovery Time, t_{DIGREC}