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**FEATURES**

**Wireless vibration system, 902.5 MHz to 927.5 MHz**  
**Clear channel assessment and packet collision avoidance**  
**Error detection and correction in radio frequency (RF) protocol**  
**Programmable RF output power**  
**Gateway node (ADIS16000)**  
**SPI to RF function**  
**Manage up to 6 sensor nodes**  
**Sensor node (ADIS16229)**  
**Dual axis,  $\pm 18$  g MEMS accelerometer**  
**5.5 kHz sensor resonant frequency**  
**Digital FFT range settings: 1 g, 5 g, 10 g, and 20 g**  
**Sample rate up to 20 kSPS**  
**Programmable wake-up capture, update cycle times**  
**512-point, real valued FFT**  
**Rectangular, Hanning, and flat top window options**  
**Programmable decimation filter, 11 rate settings**  
**Multirecord capture for selected filter settings**  
**Manual capture mode for time domain data collection**  
**Programmable FFT averaging of up to 255 averages**  
**Record storage: 14 FFT records on two axes (x and y)**  
**Programmable alarms, 6 spectral bands, 2 levels**  
**Adjustable response delay to reduce false alarms**  
**Internal self-test with status flags**  
**Digital temperature and power supply measurements**  
**Identification registers: serial number, device ID, user ID**  
**37.8 mm  $\times$  22.8 mm  $\times$  8.8 mm MCML package (ADIS16000)**  
**37.8 mm  $\times$  22.8 mm  $\times$  13.5 mm MCML package (ADIS16229)**  
**Single-supply operation: 3.0 V to 3.6 V**  
**Operating temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$**

**APPLICATIONS**

**Vibration analysis**  
**Condition monitoring**  
**Machine health**  
**Instrumentation and diagnostics**  
**Safety shutoff sensing**

**GENERAL DESCRIPTION**

The [ADIS16000](#) and [ADIS16229](#) enable the creation of a simple wireless vibration sensing network for a wide variety of industrial equipment applications. The [ADIS16000](#) provides the gateway function, which manages the network, while the [ADIS16229](#) provides the remote sensing function.

The [ADIS16229](#) *iSensor*<sup>®</sup> is a complete wireless vibration sensor node that combines dual axis acceleration sensing with advanced time domain and frequency domain signal processing. Time domain signal processing includes a programmable decimation filter and selectable windowing function. Frequency domain processing includes a 512-point, real valued fast Fourier transform (FFT); FFT magnitude averaging; and programmable spectral alarms. The FFT record storage system offers users the ability to track changes over time and capture FFTs with multiple decimation filter settings.

The dynamic range, bandwidth, sample rate, and noise performance of the [ADIS16229](#) are well suited for a wide variety of machine health and production equipment monitoring systems. This device also provides a number of wireless configuration parameters, enabling a wide level of flexibility in managing the trade-off between battery life and communication frequency.

The [ADIS16000](#) serial peripheral interface (SPI) provides simple connectivity with most embedded processor platforms, and the SMA connector interface enables the use of many different antennas. This module supports up to six [ADIS16229](#) devices at one time, using a proprietary wireless protocol.

The [ADIS16000](#) module is available in a 37.8 mm  $\times$  22.8 mm  $\times$  8.8 mm multichip chip module laminate (MCML) structure, and the [ADIS16229](#) is available in a 37.8 mm  $\times$  22.8 mm  $\times$  13.5 mm MCML structure. Both have an SMA connector for simple antenna connection, have two mounting holes for simple installation, and support operation over a  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range. The [ADIS16000](#) also includes a standard 1 mm, 14-pin connector for connecting to an embedded processor system. The [ADIS16229](#) provides a lead structure that enables simple connection with battery leads.

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**REVISION HISTORY**

**8/13—Revision 0: Initial Version**

### FUNCTIONAL BLOCK DIAGRAMS

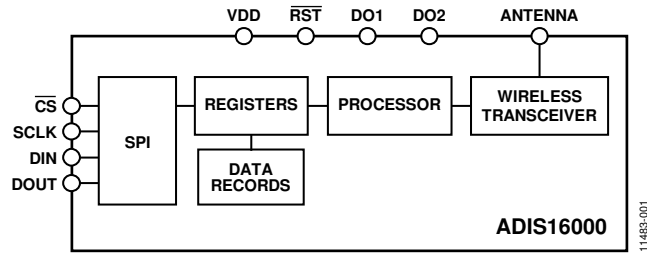


Figure 1. ADIS16000 Block Diagram

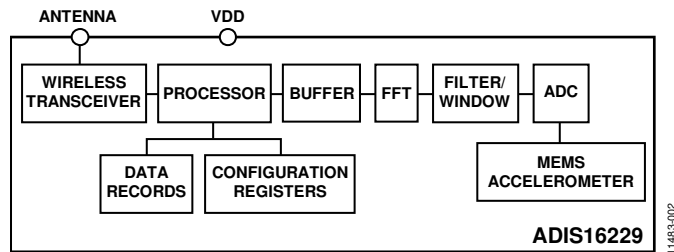


Figure 2. ADIS16229 Block Diagram

## SPECIFICATIONS

$T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = 3.3\text{ V}$ , unless otherwise noted.

Table 1.

| Parameter                                      | Test Conditions/Comments   | Min                        | Typ        | Max                        | Unit                   |
|--|--|----------------------------|------------|----------------------------|------------------------|
| <b>ACCELEROMETERS (ADIS16229)</b>              |  |                            |            |                            |                        |
| Measurement Range <sup>1</sup>                 | $T_A = 25^\circ\text{C}$   | $\pm 18$                   |            |                            | <i>g</i>               |
| Sensitivity, FFT                               | $T_A = 25^\circ\text{C}$ , 0 <i>g</i> to 20 <i>g</i> range setting |                            | 0.3052     |                            | mg/LSB                 |
| Sensitivity, Time Domain                       | $T_A = 25^\circ\text{C}$   |                            | 0.6104     |                            | mg/LSB                 |
| Sensitivity Error                              | $T_A = 25^\circ\text{C}$   |                            | $\pm 0.3$  |                            | %                      |
|  | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                |                            |            | $\pm 6$                    | %                      |
| Nonlinearity                                   | With respect to full scale   |                            | $\pm 0.2$  | $\pm 1.25$                 | %                      |
| Cross-Axis Sensitivity                         |  |                            | 4          |                            | %                      |
| Alignment Error                                | With respect to package mounting holes                             |                            | 2.3        |                            | Degrees                |
| Offset Error                                   | $T_A = 25^\circ\text{C}$   |                            | $\pm 0.01$ |                            | <i>g</i>               |
|  | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                |                            |            | $\pm 1$                    | <i>g</i>               |
| Offset Temperature Coefficient                 |  |                            | 2          |                            | mg/ $^\circ\text{C}$   |
| Output Noise                                   | $T_A = 25^\circ\text{C}$ , 20.48 kHz sample rate, time domain      |                            | 11         |                            | mg rms                 |
| Output Noise Density                           | $T_A = 25^\circ\text{C}$ , 10 Hz to 1 kHz                          |                            | 0.248      |                            | mg/ $\sqrt{\text{Hz}}$ |
| Bandwidth                                      | $\pm 5\%$ flatness, see Figure 21                                  |                            | 840        |                            | Hz                     |
| Sensor Resonant Frequency                      |  |                            | 5.5        |                            | kHz                    |
| <b>LOGIC INPUTS<sup>2</sup> (ADIS16000)</b>    |  |                            |            |                            |                        |
| Input High Voltage, $V_{\text{INH}}$           |  | $0.7 \times V_{\text{DD}}$ |            |                            | V                      |
| Input Low Voltage, $V_{\text{INL}}$            |  |                            |            | $0.2 \times V_{\text{DD}}$ | V                      |
| Input Leakage Current                          |  |                            | 0.01       |                            | $\mu\text{A}$          |
| RST, SCLK                                      |  |                            | 0.1        |                            | mA                     |
| Input Capacitance, $C_{\text{IN}}$             |  |                            | 10         |                            | pF                     |
| <b>DIGITAL OUTPUTS<sup>2</sup> (ADIS16000)</b> |  |                            |            |                            |                        |
| Output High Voltage, $V_{\text{OH}}$           | $I_{\text{SOURCE}} = 1\text{ mA}$                                  | $V_{\text{DD}} - 0.4$      |            |                            | V                      |
| Output Low Voltage, $V_{\text{OL}}$            | $I_{\text{SINK}} = 1\text{ mA}$                                    |                            |            | 0.36                       | V                      |
| <b>FLASH MEMORY</b>                            |  |                            |            |                            |                        |
| Endurance <sup>3</sup>                         |  | 20,000                     |            |                            | Cycles                 |
| Data Retention <sup>4</sup>                    | $T_J = 85^\circ\text{C}$ , see Figure 25                           | 20                         |            |                            | Years                  |
| <b>START-UP TIME<sup>5</sup></b>               |  |                            |            |                            |                        |
| Initial Startup                                | ADIS16000  |                            | 80         |                            | ms                     |
|  | ADIS16229  |                            | 150        |                            | ms                     |
| Reset Recovery <sup>6</sup>                    | ADIS16000  |                            | 80         |                            | ms                     |
|  | ADIS16229  |                            | 80         |                            | ms                     |
| Sleep Mode Recovery                            | ADIS16229  |                            | 25         |                            | ms                     |
| <b>SAMPLE RATE</b>                             |  |                            |            |                            |                        |
| Clock Accuracy                                 | Internal sample rate   |                            | 20         |                            | kSPS                   |
|  |  |                            | 3          |                            | %                      |
| <b>TRANSCEIVER</b>                             |  |                            |            |                            |                        |
| Receiver Sensitivity                           | $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$                |                            | -92        |                            | dBm                    |
| Transmission Power                             |  | -18                        |            | -10.5                      | dBm                    |

| Parameter                                       | Test Conditions/Comments                         | Min | Typ  | Max | Unit |
|---|--|-----|------|-----|------|
| POWER SUPPLY                                    | Operating voltage range, VDD                     | 3.0 | 3.3  | 3.6 | V    |
| Power Supply Current, <a href="#">ADIS16000</a> | Transmission mode, 10 dBm, 25°C                  |     | 37   |     | mA   |
|   | Transmission mode, -1 dBm, 25°C                  |     | 18   |     | mA   |
|   | Receive mode, 25°C                               |     | 20   |     | mA   |
| Power Supply Current, <a href="#">ADIS16229</a> | Transmission mode, 10 dBm, 25°C                  |     | 39   | 41  | mA   |
|   | Transmission mode, 10 dBm, -40°C to +85°C        |     | 37.5 |     | mA   |
|   | Transmission mode, -1 dBm, 25°C                  |     | 19   | 26  | mA   |
|   | Transmission mode, -1 dBm, -40°C to +85°C        | 4   | 19.5 |     | mA   |
|   | Receive mode, 25°C                               |     | 20.5 | 26  | mA   |
|   | Receive mode, -40°C to +85°C                     |     | 21.5 |     | mA   |
|   | Data capture mode, no transceiver activity, 25°C |     | 7.2  |     | mA   |
|   | Sleep mode, T <sub>A</sub> = 25°C                |     | 2.5  |     | µA   |

<sup>1</sup> The maximum range depends on the frequency of vibration.

<sup>2</sup> The digital input/output signals are 5 V tolerant.

<sup>3</sup> Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at -40°C, +25°C, +85°C, and +125°C.

<sup>4</sup> Retention lifetime equivalent at junction temperature (T<sub>J</sub>) = 85°C as per JEDEC Standard 22, Method A117. Retention lifetime depends on junction temperature.

<sup>5</sup> The start-up times presented reflect the time it takes for data collection to begin.

<sup>6</sup> Applies to the reset line ( $\overline{RST} = 0$ ) and the software reset command (GLOB\_CMD\_G[7] = 1). The  $\overline{RST}$  pin must be held low for at least 10 µs.

**TIMING SPECIFICATIONS**

T<sub>A</sub> = 25°C, V<sub>DD</sub> = 3.3 V, unless otherwise noted. See Figure 3 and Figure 4.

Table 2.

| Parameter          | Description   | Min  | Typ  | Max  | Unit |
|--------------------|---|------|------|------|------|
| f <sub>SCLK</sub>  | SCLK frequency  |      |      | 2.5  | MHz  |
| t <sub>STALL</sub> | Stall time  | 30   |      |      | μs   |
| t <sub>CS</sub>    | CS to SCLK edge                                       | 12.9 |      |      | ns   |
| t <sub>SL</sub>    | SCLK low pulse width, not shown in figures            |      | 500  |      | ns   |
| t <sub>SH</sub>    | SCLK high pulse width, not shown in figures           |      | 500  |      | ns   |
| t <sub>DAV</sub>   | Data output valid after SCLK edge                     |      |      | 47.4 | ns   |
| t <sub>DSU</sub>   | Data input setup time before SCLK edge                | 25.8 |      |      | ns   |
| t <sub>DHD</sub>   | Data input hold time after SCLK edge                  | 12.9 |      |      | ns   |
| t <sub>DF</sub>    | Data output fall time, not shown in figures           |      | 10.6 | 32.0 | ns   |
| t <sub>DR</sub>    | Data output rise time, not shown in figures           |      | 10.6 | 32.0 | ns   |
| t <sub>SR</sub>    | SCLK rise time  |      | 10.6 | 32.0 | ns   |
| t <sub>SF</sub>    | SCLK fall time  |      | 10.6 | 32.0 | ns   |
| t <sub>DOCS</sub>  | Data output valid after CS edge, not shown in figures |      |      | 59.8 | ns   |
| t <sub>SFS</sub>   | CS high after SCLK edge                               | 12.9 |      |      | ns   |

**Timing Diagrams**

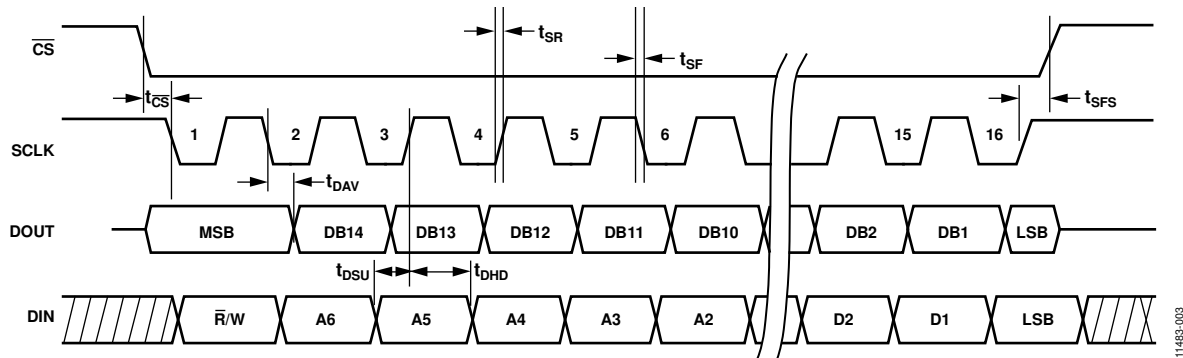


Figure 3. SPI Timing and Sequence

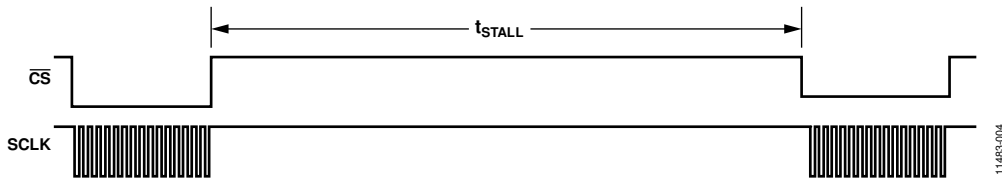


Figure 4. DIN Bit Sequence

## ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter                     | Rating            |
|-------------------------------|-------------------|
| Acceleration                  |                   |
| Any Axis, Unpowered           | 2000 <i>g</i>     |
| Any Axis, Powered             | 2000 <i>g</i>     |
| VDD to GND                    | −0.3 V to +3.96 V |
| Digital Input Voltage to GND  | −0.3 V to +3.96 V |
| Digital Output Voltage to GND | −0.3 V to +3.96 V |
| Temperature                   |                   |
| Operating Temperature Range   | −40°C to +85°C    |
| Storage Temperature Range     | −65°C to +150°C   |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Package Characteristics

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | Device Weight |
|--------------|---------------|---------------|---------------|
| 14-Pin MCML  | 31°C/W        | 11°C/W        | 6.5 grams     |

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

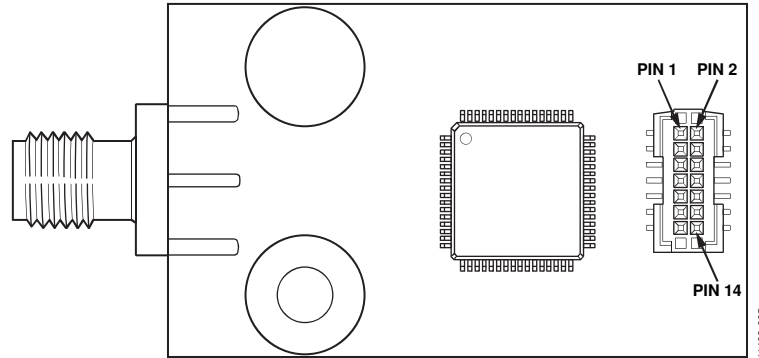
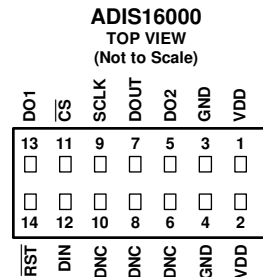


Figure 5. ADIS16000 Pin Locations



NOTES

1. THIS REPRESENTATION DISPLAYS THE TOP VIEW WHEN THE CONNECTOR IS VISIBLE AND FACING UP.
2. MATING CONNECTOR: ML-14-4 OR EQUIVALENT.
3. DNC = DO NOT CONNECT.

Figure 6. ADIS16000 Pin Configuration

Table 5. ADIS16000 Pin Function Descriptions

| Pin No.  | Mnemonic         | Type <sup>1</sup> | Description  |
|----------|------------------|-------------------|--|
| 1, 2     | VDD              | S                 | Power Supply, 3.3 V.   |
| 3, 4     | GND              | S                 | Ground.  |
| 5        | DO2              | O                 | Digital Output Line 2.   |
| 6, 8, 10 | DNC              | N/A               | Do not connect to these pins.  |
| 7        | DOUT             | O                 | SPI, Data Output. When $\overline{CS}$ is low, DOUT is an output, and when $\overline{CS}$ is high, DOUT goes into a three-state, high impedance mode. |
| 9        | SCLK             | I                 | SPI, Serial Clock.   |
| 11       | $\overline{CS}$  | I                 | SPI, Chip Select.  |
| 12       | DIN              | I                 | SPI, Data Input.   |
| 13       | DO1              | O                 | Digital Output Line 1.   |
| 14       | $\overline{RST}$ | I                 | Reset, Active Low.   |

<sup>1</sup> S = supply, O = output, I = input, and N/A = not applicable.

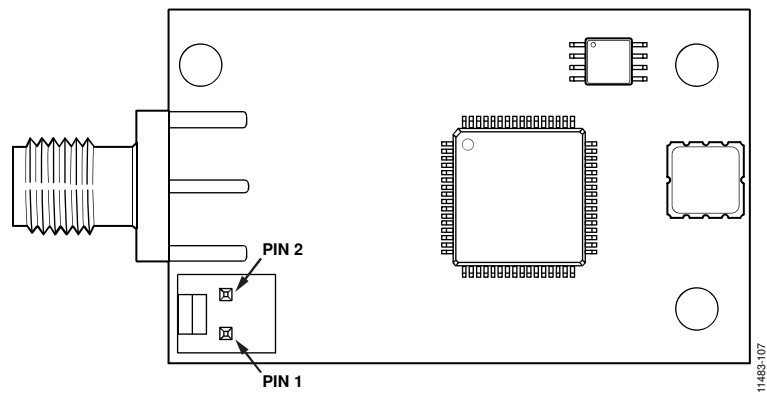


Figure 7. ADIS16229 Pin Locations

Table 6. ADIS16229 Pin Function Descriptions

| Pin No. | Mnemonic | Type <sup>1</sup> | Description         |
|---------|----------|-------------------|---------------------|
| 1       | VDD      | S                 | Power Supply, 3.3 V |
| 2       | GND      | S                 | Ground              |

<sup>1</sup> S = supply.

## THEORY OF OPERATION

The [ADIS16000](#) is the gateway node, and the [ADIS16229](#) serves as the remote sensor node in a wireless vibration monitoring system. Using a proprietary wireless protocol, one [ADIS16000](#) can support up to six [ADIS16229](#) nodes at one time in a local star network configuration (see Figure 9). As the gateway node, the SPI interface of the [ADIS16000](#) provides access to an addressable register map that manages configuration parameters (gateway and sensor node), remote alarm flags, and remote vibration data. The SPI interface of the [ADIS16000](#) enables simple connection to most embedded processors, and its standard SMA connector supports direct connection to a wide variety of antennas. The [ADIS16229](#) requires only an antenna and battery to start up and connect with the [ADIS16000](#) to begin operation.

### SENSING ELEMENT

Digital vibration sensing in the [ADIS16229](#) starts with a MEMS accelerometer core on two different axes. Accelerometers translate linear changes in velocity into a representative electrical signal, using a micromechanical system like the one shown in Figure 8. The mechanical part of this system includes two different frames, one fixed and one moving, that have a series of plates to form a variable, differential capacitive network. When experiencing the force associated with gravity or acceleration, the moving frame changes its physical position with respect to the fixed frame, which results in a change in capacitance. Tiny springs tether the moving frame to the fixed frame and govern the relationship between acceleration and physical displacement. A modulation signal on the moving plate feeds through each capacitive path into the fixed frame plates and into a demodulation circuit, which produces the electrical signal that is proportional to the acceleration acting on the device.

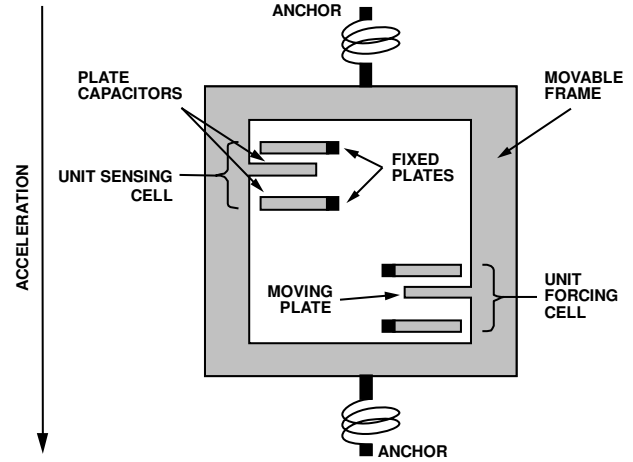


Figure 8. MEMS Sensor Diagram

### SIGNAL PROCESSING

Figure 10 offers a simplified block diagram for the [ADIS16229](#). The signal processing stage includes time-domain data capture, digital decimation/filtering, windowing, FFT analysis, FFT averaging, and record storage. See Figure 18 for more details on the signal processing operation.

### SENSOR COMMUNICATION

The [ADIS16000](#) provides access to the [ADIS16229](#) through dedicated pages in the register structure. When the [ADIS16000](#) communicates with a remote [ADIS16229](#), it copies all configuration information in these registers to their respective locations in the [ADIS16229](#) and acquires all of the data in the output registers and data records of the [ADIS16229](#).

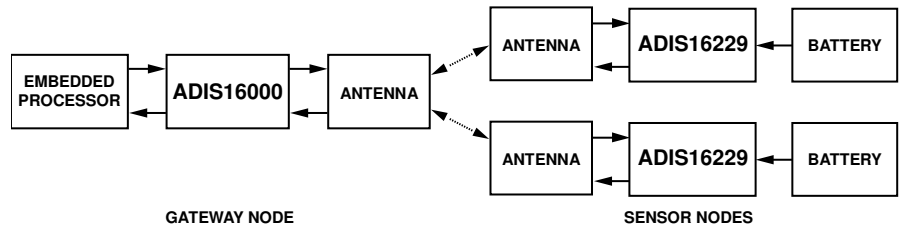


Figure 9. Star Wireless Network Example

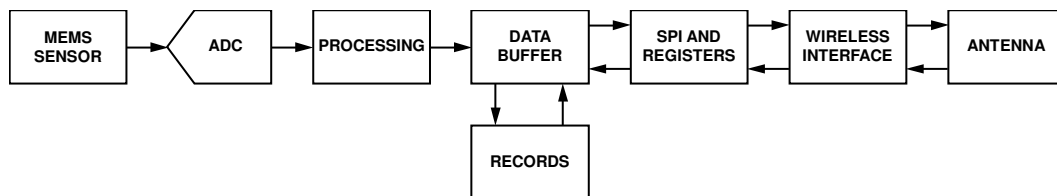


Figure 10. [ADIS16229](#) Simplified Block Diagram

**GATEWAY COMMUNICATION**

**SPI Interface**

The data collection and configuration command uses the SPI, which consists of four wires. The chip select ( $\overline{CS}$ ) signal activates the SPI interface, and the serial clock (SCLK) synchronizes the serial data lines. Input commands clock into the DIN pin, one bit at a time, on the SCLK rising edge. Output data clocks out of the DOUT pin on the SCLK falling edge. Because the ADIS16000 serves only as an SPI slave, the DOUT contents reflect the information requested using a DIN command.

**Register Organization**

The memory map for the ADIS16000 contains seven pages of user accessible registers, which enable simple organization of both local (gateway) and remote (sensor) functions. Each page has a page control register (PAGE\_ID), which is located at Address 0x00. The contents in this location contain the number that represents the active page. For example, if Address 0x00 has 0x05 in it, Page 5 is the active page. Change the active page assignment by writing a new value (between 0x00 and 0x06) to Address 0x00. For example, write 0x02 to Address 0x00 (DIN = 0x8002) to gain access to the registers in Page 2.

Each 16-bit register has its own unique bit assignment and two addresses: one for its upper byte and one for its lower byte. Table 10 and Table 11 provide more details on these memory maps, which list each register, along with its function and lower byte address.

**Table 7. ADIS16000 Register Map Page Organization**

| PAGE_ID | Function              | Reference |
|---------|-----------------------|-----------|
| 0x0000  | Gateway configuration | Table 10  |
| 0x0001  | Sensor Node 1         | Table 11  |
| 0x0002  | Sensor Node 2         | Table 11  |
| 0x0003  | Sensor Node 3         | Table 11  |
| 0x0004  | Sensor Node 4         | Table 11  |
| 0x0005  | Sensor Node 5         | Table 11  |
| 0x0006  | Sensor Node 6         | Table 11  |

**Dual Memory Structure**

The user registers provide addressing for all input/output operations in the SPI interface. The control registers use a dual memory structure (see Figure 11). The controller uses static random access memory (SRAM) registers for normal operation, including user configuration commands. The flash memory provides nonvolatile storage for control registers that have flash backup (see Table 10 and Table 11). When the device powers on or resets, the flash memory contents load into the SRAM, and the device starts producing data according to the configuration in the control registers. Storing configuration data in the flash memory requires a manual flash update command. For the ADIS16000, set DIN = 0x8000 (access Page 0), then set DIN = 0x9240 (set GLOB\_CMD\_S[6] = 1). For a remote ADIS16229, use the following steps to update its flash:

1. Turn to its page (for example, set DIN = 0x8001 to access Sensor Node 1).
2. Set DIN = 0xB640 (GLOB\_CMD\_S[6] = 1).
3. Set DIN = 0x8000 (turn to Page 0).
4. Set DIN = 0x9202 (GLOB\_CMD\_G[1] = 1).

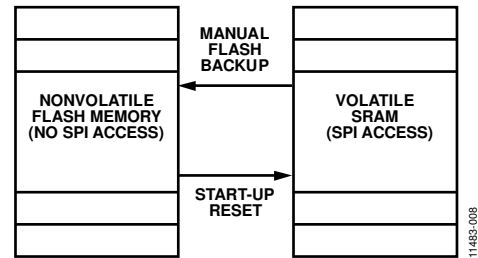


Figure 11. SRAM and Flash Memory Diagram

## BASIC OPERATION OF THE ADIS16000

When the ADIS16000 has appropriate power on the VDD pin, it automatically begins a self-initialization process. When this process is completed, the SPI interface is activated and provides access to its register structure. The SPI interface supports connectivity with most embedded processor platforms, using the connection diagram in Figure 12. The factory default configuration for DO1 provides a busy indicator signal that indicates when to avoid SPI communication requests.

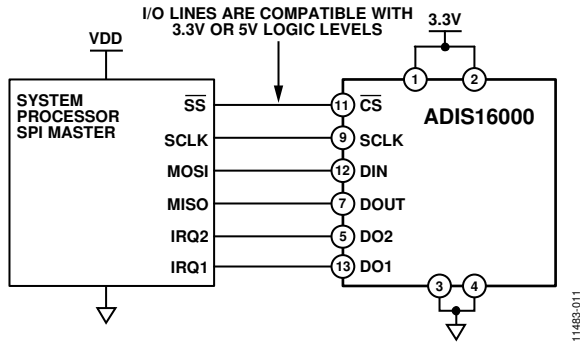


Figure 12. Electrical Hook-Up Diagram

Table 8. Generic Master Processor Pin Names and Functions

| Pin Name   | Function                            |
|------------|-------------------------------------|
| SS         | Slave select                        |
| SCLK       | Serial clock                        |
| MOSI       | Master output, slave input          |
| MISO       | Master input, slave output          |
| IRQ1, IRQ2 | Interrupt request inputs (optional) |

The ADIS16000 SPI interface supports full duplex serial communication (simultaneous transmit and receive) and uses the bit sequence shown in Figure 16. Table 9 provides a list of the most common settings that require attention to initialize a processor serial port for the ADIS16000 SPI interface.

Table 9. Generic Master Processor SPI Settings

| Processor Setting   | Description                               |
|---------------------|---|
| Master              | ADIS16000 operates as slave               |
| SCLK Rate ≤ 2.5 MHz | Bit rate setting                          |
| SPI Mode 3          | Clock polarity/phase (CPOL = 1, CPHA = 1) |
| MSB First           | Bit sequence                              |
| 16-Bit              | Shift register/data length                |

Table 10 and Table 11 provide lists of user registers with their lower byte addresses. Each register consists of two bytes, each of which has its own unique 7-bit address. Figure 13 relates the bits of each register to their upper and lower addresses.

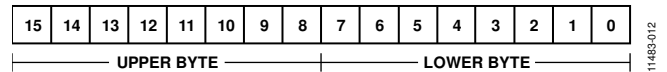


Figure 13. Generic Register Bit Definitions

## SPI WRITE COMMANDS

User control registers govern many internal operations. The DIN bit sequence in Figure 16 provides the ability to write to these registers, one byte at a time. Some configuration changes and functions require only one write cycle. For example, set PAGE\_ID[7:0] = 1 (DIN = 0x8001) to select Page 1 of the register map.

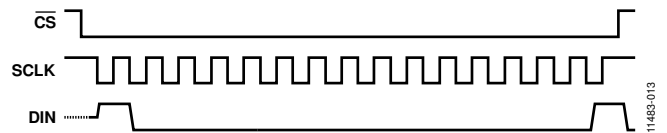


Figure 14. SPI Sequence for Selecting Page 1 for Access (DIN = 0x8001)

## SPI READ COMMANDS

A single register read requires two 16-bit SPI cycles that also use the bit assignments shown in Figure 16. The first sequence sets  $\bar{R}/W = 0$  and communicates the target address (Bits[A6:A0]). Bits[D7:D0] are don't care bits for a read DIN sequence. DOUT clocks out the requested register contents during the second sequence. The second sequence can also use DIN to set up the next read. Figure 15 provides a signal diagram for all four SPI signals while reading the PROD\_ID\_G. In this diagram, DIN = 0x1600 and DOUT reflects the decimal equivalent of 16,000.

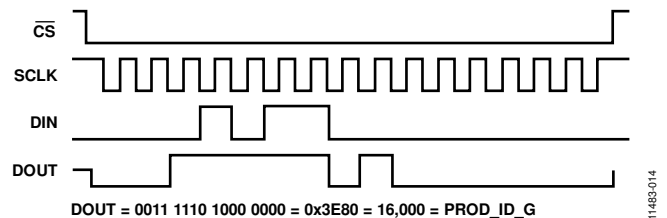
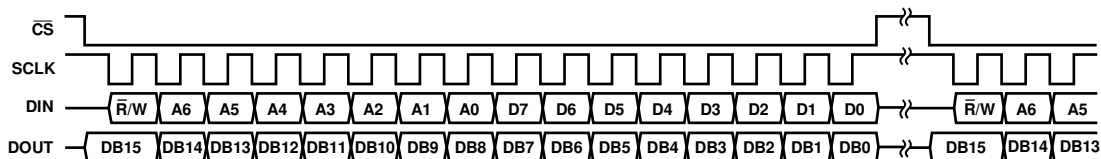


Figure 15. Example SPI Read, PROD\_ID\_G (Page 0), Second Sequence



NOTES

1. DOUT BITS ARE BASED ON THE PREVIOUS 16-BIT SEQUENCE ( $\bar{R}/W = 0$ ).

Figure 16. Example SPI Read Sequence

Table 10. User Register Memory Map, PAGE\_ID = 0x0000

| Register Name | Access <sup>1</sup> | Flash Backup <sup>1</sup> | Address | Default <sup>1</sup> | Function                                      | Reference |
|---------------|---------------------|---------------------------|---------|----------------------|---|-----------|
| PAGE_ID       | Read/write          | N/A                       | 0x00    | 0x0000               | Page identifier                               | Table 7   |
| NETWORK_ID    | Read/write          | Yes                       | 0x02    | 0x1234               | Network identifier, unique to a network       | Table 14  |
| FLASH_CNT_G   | Read only           | Yes                       | 0x04    | N/A                  | Flash update counter                          | Table 87  |
| NW_ERROR_STAT | Read only           | No                        | 0x06    | 0x0000               | Network error indicators                      | Table 26  |
| TX_PWR_CTRL_G | Read/write          | Yes                       | 0x08    | 0x0008               | Transmission power control, gateway           | Table 18  |
| RSSI_G        | Read only           | No                        | 0x0A    | N/A                  | Received signal strength                      | Table 16  |
| TEMP_OUT_G    | Read only           | No                        | 0x0C    | N/A                  | Output, temperature                           | Table 67  |
| SUPPLY_OUT_G  | Read only           | No                        | 0x0E    | N/A                  | Output, supply voltage                        | Table 64  |
| TEST_MODE     | Read/write          | Yes                       | 0x10    | 0x0000               | FCC test support modes                        | Table 23  |
| GLOB_CMD_G    | Write only          | No                        | 0x12    | N/A                  | System commands                               | Table 13  |
| CMD_DATA      | Read/write          | No                        | 0x14    | 0x0000               | Data to sensor nodes                          | Table 12  |
| PROD_ID_G     | Read only           | Yes                       | 0x16    | 0x3E80               | Product identifier, <a href="#">ADIS16000</a> | Table 80  |
| Reserved      | N/A                 | No                        | 0x18    | N/A                  | Reserved                                      |           |
| LOT_ID1_G     | Read only           | No                        | 0x1A    | N/A                  | Lot Identifier 1                              | Table 76  |
| LOT_ID2_G     | Read only           | No                        | 0x1C    | N/A                  | Lot Identifier 2                              | Table 78  |
| Reserved      | N/A                 | No                        | 0x1E    | N/A                  | Reserved                                      |           |
| Reserved      | N/A                 | No                        | 0x20    | N/A                  | Reserved                                      |           |
| Reserved      | N/A                 | No                        | 0x22    | N/A                  | Reserved                                      |           |
| SERIAL_NUM_G  | Read only           | No                        | 0x24    | N/A                  | Serial number, lot specific                   | Table 82  |
| Reserved      | N/A                 | No                        | 0x26    | N/A                  | Reserved                                      |           |
| Reserved      | N/A                 | No                        | 0x28    | N/A                  | Reserved                                      |           |
| GPO_CTRL      | Read/write          | Yes                       | 0x2A    | 0x0008               | General-purpose output control                | Table 84  |
| DIAG_STAT_G   | Read only           | No                        | 0x2C    | 0x0000               | Diagnostics, status flags                     | Table 85  |

<sup>1</sup> N/A = not applicable.Table 11. User Register Memory Map, PAGE\_ID ≥ 0x0001 (Registers Representing Remote [ADIS16229](#) Units)

| Register Name | Access <sup>1</sup> | Flash Backup <sup>1</sup> | Address | Default <sup>1,2</sup> | Function  | Reference |
|---------------|---------------------|---------------------------|---------|------------------------|---|-----------|
| PAGE_ID       | Read/write          | N/A                       | 0x00    | N/A                    | Page identifier   | Table 7   |
| SENS_ID       | Read only           | Yes                       | 0x02    | N/A                    | Sensor identifier   | Table 15  |
| FLASH_CNT_S   | Read only           | Yes                       | 0x04    | N/A                    | Status, flash memory write count                            | Table 88  |
| X_BUF         | Read only           | No                        | 0x06    | N/A                    | Output, buffer for x-axis acceleration data                 | Table 60  |
| Y_BUF         | Read only           | No                        | 0x08    | N/A                    | Output, buffer for y-axis acceleration data                 | Table 61  |
| TEMP_OUT_S    | Read only           | No                        | 0x0A    | N/A                    | Output, temperature during capture                          | Table 68  |
| SUPPLY_OUT_S  | Read only           | No                        | 0x0C    | N/A                    | Output, power supply during capture                         | Table 65  |
| FFT_AVG1      | Read/write          | Yes                       | 0x0E    | 0x0108                 | Control, FFT average, SR0 and SR1                           | Table 35  |
| FFT_AVG2      | Read/write          | Yes                       | 0x10    | 0x0101                 | Control, FFT average, SR2 and SR3                           | Table 36  |
| BUF_PNTR      | Read/write          | No                        | 0x12    | 0x0000                 | Control, buffer address pointer                             | Table 58  |
| REC_PNTR      | Read/write          | No                        | 0x14    | 0x0000                 | Control, record address pointer                             | Table 59  |
| X_SENS        | Read/write          | No                        | 0x16    | N/A                    | Control, x-axis scale correction factor                     | Table 33  |
| Y_SENS        | Read/write          | No                        | 0x18    | N/A                    | Control, y-axis scale correction factor                     | Table 34  |
| REC_CTRL1     | Read/write          | Yes                       | 0x1A    | 0x1102                 | Record control register                                     | Table 28  |
| REC_CTRL2     | Read/write          | Yes                       | 0x1C    | 0x00FF                 | Record control register                                     | Table 31  |
| Reserved      | N/A                 | No                        | 0x1E    | N/A                    | Reserved  |           |
| ALM_F_LOW     | Read/write          | Yes                       | 0x20    | 0x0000                 | Spectral alarm band, low frequency                          | Table 44  |
| ALM_F_HIGH    | Read/write          | Yes                       | 0x22    | 0x0000                 | Spectral alarm band, high frequency                         | Table 45  |
| ALM_X_MAG1    | Read/write          | Yes                       | 0x24    | 0x0000                 | Spectral alarm band, X-Axis Alarm Trigger Level 1 magnitude | Table 46  |
| ALM_Y_MAG1    | Read/write          | Yes                       | 0x26    | 0x0000                 | Spectral alarm band, Y-Axis Alarm Trigger Level 1 magnitude | Table 47  |
| ALM_X_MAG2    | Read/write          | Yes                       | 0x28    | 0x0000                 | Spectral alarm band, X-Axis Alarm Trigger Level 2 magnitude | Table 48  |

| Register Name  | Access <sup>1</sup> | Flash Backup <sup>1</sup> | Address | Default <sup>1, 2</sup> | Function  | Reference |
|----------------|---------------------|---------------------------|---------|-------------------------|---|-----------|
| ALM_Y_MAG2     | Read/write          | Yes                       | 0x2A    | 0x0000                  | Spectral alarm band, Y-Axis Alarm Trigger Level 2 magnitude | Table 49  |
| ALM_PNTR       | Read/write          | No                        | 0x2C    | 0x0000                  | Spectral alarm band pointer                                 | Table 43  |
| ALM_S_MAG      | Read/write          | Yes                       | 0x2E    | 0x0000                  | Alarm, system alarm trigger level                           | Table 50  |
| ALM_CTRL       | Read/write          | Yes                       | 0x30    | 0x0080                  | Alarm, control register                                     | Table 42  |
| AVG_CNT        | Read/write          | Yes                       | 0x32    | 0x9630                  | Sample rate control (average count)                         | Table 29  |
| DIAG_STAT_S    | Read only           | No                        | 0x34    | 0x0000                  | System status register                                      | Table 86  |
| GLOB_CMD_S     | Write only          | No                        | 0x36    | N/A                     | Global command register                                     | Table 75  |
| ALM_X_STAT     | Read only           | No                        | 0x38    | 0x0000                  | Alarm, x-axis status register                               | Table 51  |
| ALM_Y_STAT     | Read only           | No                        | 0x3A    | 0x0000                  | Alarm, y-axis status register                               | Table 52  |
| ALM_X_PEAK     | Read only           | No                        | 0x3C    | 0x0000                  | Alarm, x-axis peak level                                    | Table 53  |
| ALM_Y_PEAK     | Read only           | No                        | 0x3E    | 0x0000                  | Alarm, y-axis peak level                                    | Table 54  |
| TIME_STMP_L    | Read only           | No                        | 0x40    | 0x0000                  | Time stamp, low integer                                     | Table 73  |
| TIME_STMP_H    | Read only           | No                        | 0x42    | 0x0000                  | Time stamp, high integer                                    | Table 74  |
| ALM_X_FREQ     | Read only           | No                        | 0x44    | 0x0000                  | Alarm frequency of x-axis ALM_X_PEAK                        | Table 55  |
| ALM_Y_FREQ     | Read only           | No                        | 0x46    | 0x0000                  | Alarm frequency of y-axis ALM_Y_PEAK                        | Table 56  |
| PROD_ID_S      | Read only           | Yes                       | 0x48    | 0x3F65                  | Product identification register                             | Table 81  |
| REC_FLSH_CNT   | Read only           | No                        | 0x4A    | N/A                     | Flash write cycle count                                     | Table 40  |
| REC_INFO1      | Read only           | No                        | 0x4C    | 0x0008                  | Record Settings 1   | Table 71  |
| REC_INFO2      | Read only           | No                        | 0x4E    | 0x0000                  | Record Settings 2   | Table 72  |
| REC_CNTR       | Read only           | No                        | 0x50    | 0x0000                  | Record counter  | Table 38  |
| PKT_TIME_L     | Read only           | No                        | 0x52    | N/A                     | Received packet time stamp, low integer                     | Table 24  |
| PKT_TIME_H     | Read only           | No                        | 0x54    | N/A                     | Received packet time stamp, high integer                    | Table 25  |
| PKT_ERROR_STAT | Read only           | No                        | 0x56    | 0x0000                  | Missed packets/error indicator                              | Table 27  |
| TX_PWR_CTRL_S  | Read/write          | Yes                       | 0x58    | 0x0008                  | Transmission power control                                  | Table 19  |
| RSSI_S         | Read only           | No                        | 0x5A    | N/A                     | Received signal strength indicator                          | Table 17  |
| RF_MODE        | Read/write          | Yes                       | 0x5C    | 0x0000                  | Wireless communication configuration                        | Table 20  |
| UPDAT_INT      | Read/write          | Yes                       | 0x5E    | 0x0FA0                  | Update interval   | Table 21  |
| INT_SCL        | Read/write          | Yes                       | 0x60    | 0x0001                  | Update interval scale                                       | Table 22  |
| Reserved       | N/A                 | N/A                       | 0x62    | N/A                     | Reserved  |           |
| USER_SCR       | Read only           | Yes                       | 0x64    | 0x0000                  | User scratch register                                       | Table 83  |
| Reserved       | N/A                 | N/A                       | 0x66    | N/A                     | Reserved  |           |
| LOT_ID1_S      | Read only           | Yes                       | 0x68    | N/A                     | Lot Identification Code 1                                   | Table 77  |
| LOT_ID2_S      | Read only           | Yes                       | 0x6A    | N/A                     | Lot Identification Code 2                                   | Table 79  |
| Reserved       | N/A                 | N/A                       | 0x6C    | N/A                     | Reserved  |           |
| Reserved       | N/A                 | N/A                       | 0x6E    | N/A                     | Reserved  |           |

<sup>1</sup> N/A = not applicable.

<sup>2</sup> All registers in Page 1, Page 2, Page 3, Page 4, Page 5, and Page 6 read 0x0000 prior to connecting with the [ADIS16229](#).

## NETWORK MANAGEMENT

When the [ADIS16000](#) and the [ADIS16229](#) have an appropriate supply voltage across their VDD and GND pins, they both self-initialize and prepare themselves for connecting. After completing this process, the [ADIS16229](#) starts sending connection requests to any available [ADIS16000](#) devices within range. The system microcontroller manages the response of the [ADIS16000](#) to these requests, using the `CMD_DATA` (see Table 12) and `GLOB_CMD_G` registers (see Table 13), which are both in Page 0 of the [ADIS16000](#). Adding an [ADIS16229](#) network requires the following two steps:

1. Set `GLOB_CMD_G[0] = 1` (DIN = 0x9201, in Page 0).
2. Wait 500  $\mu$ s and then write the node number (between 0 and 6) to the `CMD_DATA` register.

After this second step, the connection process can take up to 10 seconds after writing this code. Removing a sensor from the network uses a similar two-step process: write the sensor node number to the `CMD_DATA` register, and then set `GLOB_CMD_G[8] = 1` (DIN = 0x9301, Page 0).

**Table 12. `CMD_DATA`,  
Page 0, Low Byte Address = 0x14, Read/Write**

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:4] | Not used   |
| [3:0]  | Sensor node for <code>GLOB_CMD_G[1]</code> and <code>GLOB_CMD_G[0]</code> commands, range = 000 (0) to 110 (6) |

**Table 13. `GLOB_CMD_G`,  
Page 0, Low Byte Address = 0x12, Write Only**

| Bits | Description (Default = Not Applicable)  |
|------|---|
| 15   | Remove the sensor node identified by the <code>CMD_DATA</code> register   |
| 14   | Not used  |
| 13   | Request current configuration and payload from the sensor node identified by the <code>CMD_DATA</code> register |
| 12   | Manual update of alarm registers for the sensor node identified by the <code>CMD_DATA</code> register           |
| 11   | Read alarm registers from the sensor node identified by the <code>CMD_DATA</code> register                      |
| 10   | Transfer alarm configuration from <a href="#">ADIS16000</a> page to remote sensor registers                     |
| 9    | Not used  |
| 8    | Remove sensor node in <code>CMD_DATA</code> from the network  |
| 7    | Software reset  |
| 6    | Save registers to flash memory  |
| 5    | Flash test, compare sum of flash memory with factory value  |
| 4    | Clear <code>DIAG_STAT_G</code> register   |
| 3    | Restore factory register settings, including capture buffer and alarm registers                                 |
| 2    | Not used  |
| 1    | Update sensor node in <code>CMD_DATA</code> register, in one of the manual modes                                |
| 0    | Add sensor node in <code>CMD_DATA</code> to the network   |

Set `GLOB_CMD_G[1] = 1` (DIN = 0x9202) to initialize an update of all of the registers, except those associated with the spectral alarms. Set `GLOB_CMD_G[12] = 1` (DIN = 0x9310) to update all of the alarm registers, after configuring them. Separating this function helps manage the flash memory endurance. The `NETWORK_ID` register (see Table 14) provides a user configurable identification number in its lower byte and provides a separate 8-bit number for application-specific information that does not influence the operation of the [ADIS16000](#).

**Table 14. `NETWORK_ID`,  
Page 0, Low Byte Address = 0x02, Read/Write**

| Bits   | Description (Default = 0x1234)                         |
|--------|--|
| [15:8] | User configurable (no internal function)               |
| [7:0]  | User configurable, 8-bit network identification number |

The `SENS_ID` register (see Table 15) contains the value 0x0000 when a particular page in the [ADIS16000](#) memory map is not managing a specific [ADIS16229](#) connection. When a page is managing a connection with an [ADIS16229](#), the lower byte indicates the assigned node number within the network.

**Table 15. `SENS_ID`,  
Page 1 to Page 6, Low Byte Address = 0x02, Read Only**

| Bits   | Description (Default = Not Applicable)                   |
|--------|--|
| [15:8] | When connected, it is 0xAD.                              |
| [7:0]  | Sensor node number. When connected, the range is 0 to 6. |

### Receiver Signal Strength

The `RSSI_G` and `RSSI_S` registers (see Table 16 and Table 17) provide tools for tuning the transmission power control at each location. Keep the transmission power high enough to maintain at least -92 dBm in these registers for best communication reliability.

**Table 16. `RSSI_G`,  
Page 0, Low Byte Address = 0x0A, Read Only**

| Bits   | Description (Default = Not Applicable)   |
|--------|--|
| [15:0] | Received signal strength. This is a 16-bit twos complement number, where 0x0000 represents 0 dBm and each LSB represents 1 dBm of change in the received signal strength. Examples include the following:<br>0x0001 = +1 dBm.<br>0xFFFF = -1 dBm.<br>0xFFA0 = -92 dBm. |

**Table 17. `RSSI_S`,  
Page 1 to Page 6, Low Byte Address = 0x5A, Read Only**

| Bits   | Description (Default = Not Applicable)   |
|--------|--|
| [15:0] | Received signal strength. This is a 16-bit twos complement number, where 0x0000 represents 0 dBm and each LSB represents 1 dBm of change in the received signal strength. Examples include the following:<br>0x0001 = +1 dBm.<br>0xFFFF = -1 dBm.<br>0xFFA0 = -92 dBm. |



## Transmission Power Control

Both the [ADIS16000](#) and [ADIS16229](#) units provide controls for transmission power in the TX\_PWR\_CTRL\_G (see Table 18) and TX\_PWR\_CTRL\_S (see Table 19) registers. The registers provide users with the ability to optimize the transmission power for battery optimization and to manage interference influence on other networks. Note that compliance with FCC Part 15.247 involves limiting the transmission power to -1 dBm.

**Table 18. TX\_PWR\_CTRL\_G, Page 0, Low Byte Address = 0x08, Read/Write**

| Bits    | Description (Default = 0x0008)   |
|---------|--|
| [15:14] | Not used (don't care).   |
| [13:8]  | Channel frequency. This is a 6-bit, offset binary number that selects one of 51 channel frequencies. The lowest setting, 000000 (binary for 0 LSB), represents 902.5 MHz, and each LSB represents an increase of 0.5 MHz. The maximum setting, 110010 (binary for 50 LSB), selects a channel frequency of 927.5 MHz.                               |
| [7:5]   | Not used (don't care).   |
| [4:0]   | Transmission power setting. This is a 5-bit, offset binary number that selects the transmission power in the gateway node. The lowest setting, 00000 (binary for 0 LSB), selects a transmission power of -15.5 dBm, and each LSB increases the transmission power by +1.7 dBm. The maximum setting, 01111, selects a transmission power of 10 dBm. |

**Table 19. TX\_PWR\_CTRL\_S, Page 1 to Page 6, Low Byte Address = 0x58, Read/Write**

| Bits    | Description (Default = 0x0008)   |
|---------|--|
| [15:14] | Not used (don't care).   |
| [13:8]  | Channel frequency. This is a 6-bit, offset binary number that selects one of 51 channel frequencies. The lowest setting, 000000 (binary for 0 LSB), represents 902.5 MHz, and each LSB represents an increase of 0.5 MHz. The maximum setting, 110010 (binary for 50 LSB), selects a channel frequency of 927.5 MHz.                               |
| [7:5]   | Not used (don't care).   |
| [4:0]   | Transmission power setting. This is a 5-bit, offset binary number that selects the transmission power in the gateway node. The lowest setting, 00000 (binary for 0 LSB), selects a transmission power of -15.5 dBm, and each LSB increases the transmission power by +1.7 dBm. The maximum setting, 01111, selects a transmission power of 10 dBm. |

## Wireless Configuration

The RF\_MODE register (see Table 20) provides a number of important wireless configuration parameters. Note that when the transmission power exceeds -1 dBm and the update period is less than 10 seconds, FCC Part 15.247 requires the use of frequency hopping.

**Table 20. RF\_MODE, Page 1 to Page 6, Low Byte Address = 0x5C, Read/Write**

| Bits    | Description (Default = 0x0000)   |
|---------|--|
| [15:12] | Not used (don't care)  |
| [11]    | Continuous transmission mode (single-channel, per TX_PWR_CTRL_S, see Table 19) |
| [10]    | Continuous frequency hopping mode  |
| [9:7]   | Not used (don't care)  |
| [6]     | Frequency hopping (0 = disable, 1 = enable)                                    |
| [5:2]   | Not used (don't care)  |
| [1]     | Update gateway on alarm only (0 = disable, 1 = enable)                         |
| [0]     | Not used (don't care)  |

The UPDAT\_INT and INT\_SCL registers (see Table 21 and Table 22) establish the time between wake-up events, where the remote [ADIS16229](#) captures data, analyzes it, and communicates the information.

**Table 21. UPDAT\_INT, Page 1 to Page 6, Low Byte Address = 0x5E, Read/Write**

| Bits   | Description (Default = 0x0FA0)                             |
|--------|--|
| [15:0] | Offset binary number, scale factor set by INT_SCL register |

**Table 22. INT\_SCL, Page 1 to Page 6, Low Byte Address = 0x60, Read/Write**

| Bits   | Description (Default = 0x0001)   |
|--------|--|
| [15:2] | Not used (don't care)  |
| [1:0]  | Scale factor<br>00 = 30.52 $\mu$ s/LSB, maximum = 2 seconds<br>01 = 0.488 ms/LSB, maximum = 31.98 seconds<br>10 = 1/128 sec/LSB, maximum = 512 seconds<br>11 = 1 sec/LSB, maximum = 18.2 hours |

The TEST\_MODE register (see Table 23) provides specific test modes for FCC testing.

**Table 23. TEST\_MODE, Page 0, Low Byte Address = 0x10, Read/Write**

| Bits    | Description (Default = 0x0000)   |
|---------|--|
| [15:12] | Not used   |
| 11      | Continuous transmission mode (single-channel, per TX_PWR_CTRL_G, see Table 18) |
| 10      | Continuous frequency hopping mode  |
| [9:0]   | Not used   |

**Communication Tools**

The PKT\_TIME\_H (upper word) and PKT\_TIME\_L (lower word) registers provide a 32-bit timer for tracking the relative times associated with packet transmission times. When the timer reaches its maximum value of 0xFFFFFFFF, it automatically starts over at 0x00000000.

**Table 24. PKT\_TIME\_L, Page 1 to Page 6, Low Byte Address = 0x52, Read Only**

| Bits   | Description (Default = Not Applicable)             |
|--------|--|
| [15:0] | Offset binary number, lower word, 1 LSB = 0.488 ms |

**Table 25. PKT\_TIME\_H, Page 1 to Page 6, Low Byte Address = 0x54, Read Only**

| Bits   | Description (Default = Not Applicable) |
|--------|--|
| [15:0] | Offset binary number, upper word       |

The NW\_ERROR\_STAT register (see Table 26) provides all of the error flags associated with the wireless communication.

**Table 26. NW\_ERROR\_STAT, Page 0, Low Byte Address = 0x06, Read Only**

| Bits    | Description (Default = 0x0000)   |
|---------|--|
| [15:11] | Not used   |
| 10      | Invalid packet received  |
| 9       | Received packet from an unknown device   |
| 8       | Packet synchronization failure from the most recent received packet  |
| [7:6]   | Not used   |
| 5       | Packet length mismatch   |
| 4       | Missing packet   |
| 3       | Packets received out of sync   |
| 2       | Failure to receive acknowledgment from a sensor node   |
| 1       | Low signal strength from a sensor node, read RSSI_S register for power level of this signal (see Table 17) |
| 0       | CRC mismatch error associated with the most recent packet from the sensor node packet                      |

**Table 27. PKT\_ERROR\_STAT, Page 1 to Page 6, Low Byte Address = 0x56, Read Only**

| Bits    | Description (Default = 0x0000)   |
|---------|--|
| [15:10] | Not used   |
| 9       | Received packet from an unknown device   |
| 8       | Packet synchronization failure from the most recent received packet  |
| [7:6]   | Not used   |
| 5       | Packet length mismatch   |
| 4       | Missing packet   |
| 3       | Packets received out of sync   |
| 2       | Failure to receive acknowledgment from a sensor node   |
| 1       | Low signal strength from a sensor node, read RSSI_S register for power level of this signal (see Table 17) |
| 0       | CRC mismatch error associated with the most recent packet from the sensor node packet                      |

## SENSOR NODE RECORDING MODE AND SIGNAL PROCESSING

The ADIS16229 provides a complete sensing system for recording and monitoring vibration data. Figure 17 provides a simplified block diagram for the signal processing associated with spectral record acquisition on both axes (x and y). User registers provide controls for data type (time or frequency), trigger mode (manual or automatic), collection mode (real time or capture), sample rates and filtering, windowing, FFT averaging, spectral alarms, and input/output management.

### RECORDING MODE

The recording mode selection establishes the data type (time or frequency domain), trigger type (manual or automatic), and data collection (captured or real time). The REC\_CTRL1[1:0] bits (see Table 28) provide four operating modes: manual FFT, automatic FFT, manual time capture, and real time. After REC\_CTRL1 is set, the manual FFT, automatic FFT, and manual time capture modes require a start command to start acquiring a spectral or time domain record. All of these modes automatically trigger when the sensor receives the configuration packet from the gateway. Set GLOB\_CMD\_S[11] = 1 to halt the operation and wait for further instructions from the ADIS16000.

#### Manual FFT Mode

Set REC\_CTRL1[1:0] = 00 to place the device in manual FFT mode, which triggers a single FFT cycle. When the spectral record is complete, the device transmits the data to the ADIS16000 and waits for another start command.

#### Automatic FFT Mode

Set REC\_CTRL1[1:0] = 01 to place the device in automatic FFT mode. Use the UPDAT\_INT and INT\_SCL registers to establish the period between wake-up times, which triggers data capture, FFT computation, and analysis.

#### Manual Time Capture Mode

Set REC\_CTRL1[1:0] = 10 to place the device into manual time capture mode, which results in triggering a single time domain data capture. When the device operates in this mode, 512 samples of time domain data are loaded into the buffer for each axis.

This data goes through all time domain signal processing, except the preFFT windowing, prior to loading into the data buffer for user access. When the data record is complete, the device transmits the data to the ADIS16000 and waits for another start command.

#### Real-Time Mode

Set REC\_CTRL1[1:0] = 11 to place the device into real-time mode. In this mode, the device samples only one axis, at a rate of 5 kSPS, and provides data on its output register at the SRO sample rate setting in AVG\_CNT[3:0] (see Table 29). Select the axis of measurement in this mode by reading its assigned register. For example, select the x-axis by reading X\_BUF, using DIN = 0x0600. See Table 60 or Table 61 for more information on the x\_BUF registers. No other ADIS16229 nodes are able to communicate with the ADIS16000 when one of the ADIS16229 nodes is in real-time mode.

Table 28. REC\_CTRL1, Page 1 to Page 6, Low Byte Address = 0x1A, Read/Write

| Bits    | Description (Default = 0x1102)  |
|---------|---|
| [15:14] | Not used (don't care)   |
| [13:12] | Window setting;<br>00 = rectangular, 01 = Hanning, 10 = flat top, 11 = N/A <sup>1</sup>                               |
| 11      | SR3: 1 = enabled for FFT, 0 = disabled;<br>Sample rate = $20,000 \div 2^{AVG\_CNT[15:12]}$ (see Table 29)             |
| 10      | SR2: 1 = enabled for FFT, 0 = disabled;<br>Sample rate = $20,000 \div 2^{AVG\_CNT[11:8]}$ (see Table 29)              |
| 9       | SR1: 1 = enabled for FFT, 0 = disabled;<br>Sample rate = $20,000 \div 2^{AVG\_CNT[7:4]}$ (see Table 29)               |
| 8       | SR0: 1 = enabled for FFT, 0 = disabled;<br>Sample rate = $20,000 \div 2^{AVG\_CNT[3:0]}$ (see Table 29)               |
| 7       | Power-down between each recording, 1 = enabled  |
| [6:4]   | Not used (don't care)   |
| [3:2]   | Storage method;<br>00 = none, 01 = alarm trigger, 10 = all, 11 = N/A <sup>1</sup>                                     |
| [1:0]   | Recording mode;<br>00 = manual FFT, 01 = automatic FFT, 10 = manual time capture, 11 = real-time sampling/data access |

<sup>1</sup> N/A = not applicable.

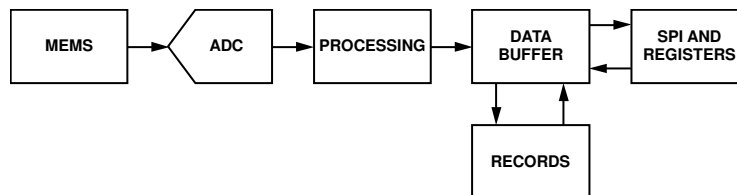


Figure 17. Simplified Block Diagram

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**SPECTRAL RECORD PRODUCTION**

The ADIS16229 produces a spectral record by taking a time record of data on both axes, then scaling, windowing, and performing an FFT process on each time record. This process is repeated for a programmable number of FFT averages, with the FFT result of each cycle accumulating in the data buffer. After completing the selected number of cycles, the FFT averaging process completes by scaling the data buffer contents. Then the data buffer contents are available to the SPI and output data registers.

**SAMPLE RATE AND FILTERING**

The sample rate for each axis is 20 kSPS. The internal ADC samples both axes in a time-interleaving pattern (x1, y1, x2, y2, and so on) that provides even distribution of data across the data record. The averaging/decimating filter provides a control for the final sample rate in the time record. By averaging and decimating the time domain data, this filter provides the ability to focus the spectral record on lower bandwidths, producing finer frequency resolution in each FFT frequency bin. The AVG\_CNT register (see

Table 29) provides the settings for the four different sample rate options in REC\_CTRL1[11:8] (SRx in Table 28). All four options are available when using the manual FFT, automatic FFT, and manual time capture modes. When more than one sample rate option is enabled while the device is in one of the manual modes, the device produces a spectral record for one SRx at a time, starting with the lowest number. After completing the spectral record for one SRx option, the device waits for another start command before producing a spectral record for the next SRx option that is enabled in REC\_CTRL1[11:8]. When more than one sample rate option is enabled while the device is in the automatic FFT mode, the device produces a spectral record for one SRx option and then waits for the next automatic trigger, which occurs based on the UPDAT\_INT and INT\_SCL registers (see Table 21 and Table 22). See Figure 19 for more details on how multiple SRx options influence data collection and spectral record production. When real-time mode is used, the output data rate reflects the SR0 setting.

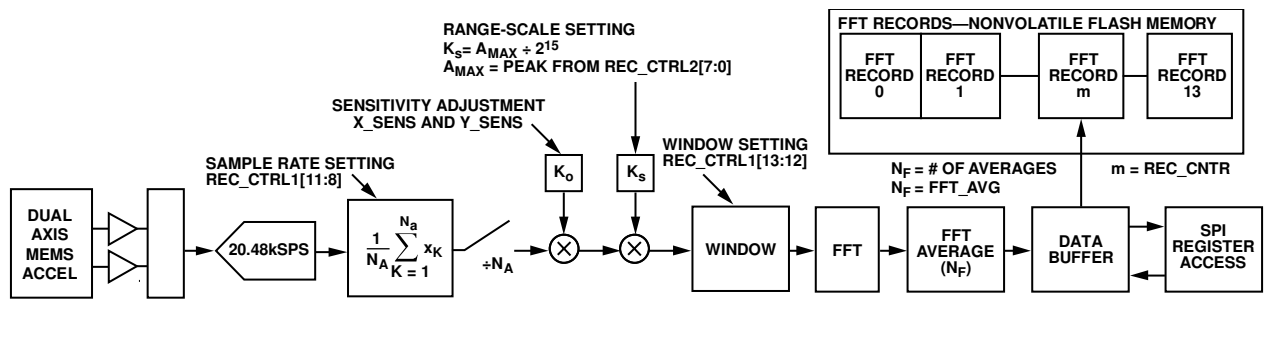


Figure 18. Signal Flow Diagram, REC\_CTRL1[1:0] = 00 or 01, FFT Analysis Modes

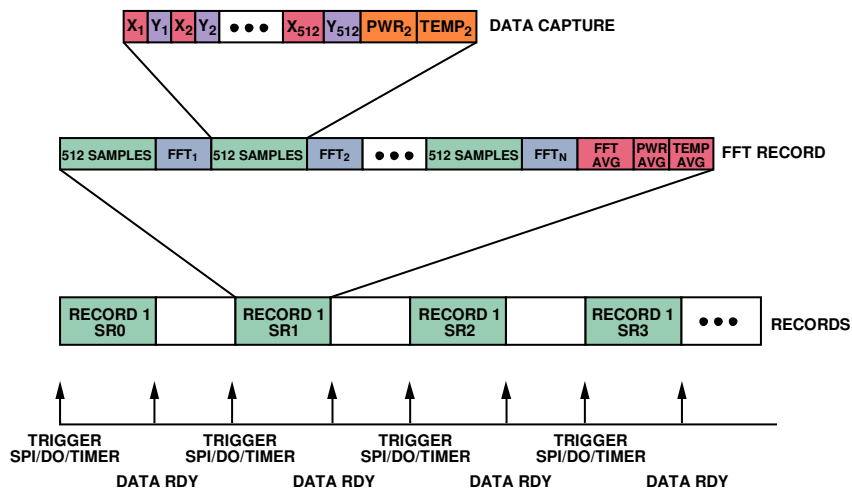


Figure 19. Spectral Record Production, with All SRx Settings Enabled

Table 30 provides a list of SRx settings available in the AVG\_CNT register (see Table 29), along with the resulting sample rates, FFT bin widths, bandwidth, and estimated total noise. Note that each SRx setting also has associated range settings in the REC\_CTRL2 register (see Table 31) and the FFT averaging settings that are shown in the FFT\_AVG1 and FFT\_AVG2 registers (see Table 35 and Table 36, respectively).

**Table 29. AVG\_CNT,**  
**Page 1 to Page 6, Low Byte Address = 0x32, Read/Write**

| Bits    | Description (Default = 0x9630)   |
|---------|--|
| [15:12] | Sample Rate Option 3 (SR3), binary (0 to 10), SR3 option sample rate = $20,000 \div 2^{AVG\_CNT[15:12]}$ |
| [11:8]  | Sample Rate Option 2 (SR2), binary (0 to 10), SR2 option sample rate = $20,000 \div 2^{AVG\_CNT[11:8]}$  |
| [7:4]   | Sample Rate Option 1 (SR1), binary (0 to 10), SR1 option sample rate = $20,000 \div 2^{AVG\_CNT[7:4]}$   |
| [3:0]   | Sample Rate Option 0 (SR0), binary (0 to 10), SR0 option sample rate = $20,000 \div 2^{AVG\_CNT[3:0]}$   |

**Table 30. Sample Rate Settings and Filter Performance**

| SRx Setting | Sample Rate, $f_s$ (SPS) | Bin Width (Hz) | Bandwidth (Hz) |
|-------------|--------------------------|----------------|----------------|
| 0           | 20,000                   | 39.1           | 10,000         |
| 1           | 10,000                   | 19.5           | 5,000          |
| 2           | 5,000                    | 9.8            | 2,500          |
| 3           | 2,500                    | 4.9            | 1,250          |
| 4           | 1,250                    | 2.4            | 625            |
| 5           | 625                      | 1.2            | 313            |
| 6           | 313                      | 0.6            | 156            |
| 7           | 156                      | 0.3            | 78             |
| 8           | 78                       | 0.2            | 39             |
| 9           | 39                       | 0.1            | 20             |
| 10          | 20                       | 0.0            | 10             |

## DYNAMIC RANGE AND SENSITIVITY

The range of the ADIS16229 accelerometers depends on the frequency of the vibration. The accelerometers have a self-resonant frequency of 5.5 kHz, and the signal conditioning circuit applies a single-pole, low-pass filter (2.5 kHz) to the response. The self-resonant behavior of the accelerometer influences the relationship between vibration frequency and dynamic range. Figure 20 displays the response to peak input amplitudes, assuming a sinusoidal vibration signature at each frequency. The accelerometer resonance and low-pass filter also influence the magnitude response, as shown in Figure 21.

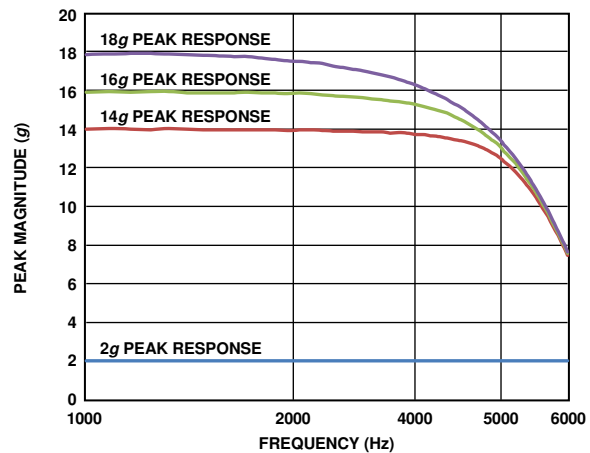


Figure 20. Peak Magnitude vs. Frequency

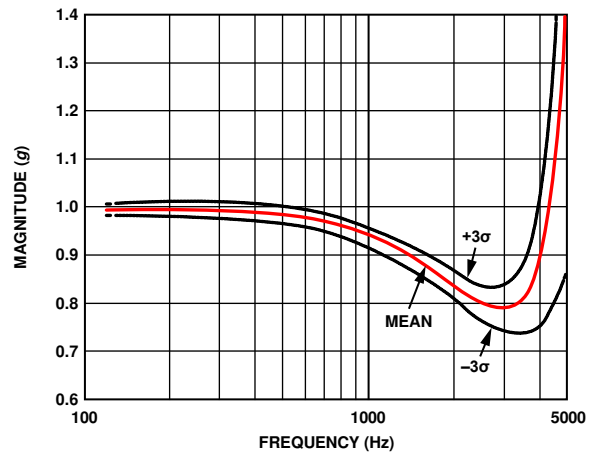


Figure 21. Magnitude/Frequency Response

## DYNAMIC RANGE SETTINGS

REC\_CTRL2 (see Table 31) provides four range settings that are associated with each sample rate option, SRx. The range options referenced in REC\_CTRL2 reflect the maximum dynamic range, which occurs at the lower part of the frequency range and does not account for the decrease in range (see Figure 20). For example, set REC\_CTRL2[5:4] = 10 (DIN = 0x9C20) to set the peak acceleration ( $A_{MAX}$ ) to 10 g on the SR2 sample rate option. These settings optimize FFT precision and sensitivity when monitoring lower magnitude vibrations. For each range setting in Table 31, this stage scales the time domain data so that the maximum value equates to  $2^{15}$  LSBs for time domain data and  $2^{16}$  LSBs for frequency domain data.

Note that the maximum range for each setting is 1 LSB smaller than the listed maximum. For example, the maximum number of codes in the frequency domain analysis is  $2^{16} - 1$ , or 65,535. When using a range setting of 1 g in one of the FFT modes, the maximum measurement is equal to 1 g times  $2^{16} - 1$ , divided by  $2^{16}$ . See Table 32 for the resolution associated with each setting and Figure 18 for the location of this operation in the signal flow diagram. The real-time mode automatically uses the 20 g range setting.

**Table 31. REC\_CTRL2,**  
Page 1 to Page 6, Low Byte Address = 0x1C, Read/Write

| Bits   | Description (Default = 0x00FF)                                      |
|--------|---|
| [15:8] | Not used (don't care)   |
| [7:6]  | Measurement range, SR3;<br>11 = 1 g, 10 = 5 g, 01 = 10 g, 00 = 20 g |
| [5:4]  | Measurement range, SR2;<br>11 = 1 g, 10 = 5 g, 01 = 10 g, 00 = 20 g |
| [3:2]  | Measurement range, SR1;<br>11 = 1 g, 10 = 5 g, 01 = 10 g, 00 = 20 g |
| [1:0]  | Measurement range, SR0;<br>11 = 1 g, 10 = 5 g, 01 = 10 g, 00 = 20 g |

**Table 32. Range Settings and LSB Weights**

| Range Setting (g) | Time Mode (mg/LSB) | FFT Mode (mg/LSB) |
|-------------------|--------------------|-------------------|
| 0 to 1            | 0.0305             | 0.0153            |
| 0 to 5            | 0.1526             | 0.0763            |
| 0 to 10           | 0.3052             | 0.1526            |
| 0 to 20           | 0.6104             | 0.3052            |

## Scale Adjustment

The x\_SENS registers (see Table 33 and Table 34) provide a fine-scale adjustment function for each axis. The following equation describes how to use measured and ideal values to calculate the scale factor for each register in LSBs:

$$SCFx = \left[ \frac{a_{XI}}{a_{XM}} - 1 \right] \times 2^{18}$$

where:

$a_{XI}$  is the ideal x-axis value.

$a_{XM}$  is the actual x-axis measurement.

These registers contain correction factors, which come from the factory calibration process. The calibration process records accelerometer output in four different orientations and computes the correction factors for each register.

These registers also provide write access for in-system adjustment. Gravity provides a common stimulus for this type of correction process. Use both +1 g and -1 g orientations to reduce the effect of offset on this measurement. In this case, the ideal measurement is 2 g, and the measured value is the difference of the accelerometer measurements at +1 g and -1 g orientations. The factory-programmed values are stored in flash memory and are restored by setting GLOB\_CMD\_S[3] = 1 (DIN = 0xB604). See Table 75.

**Table 33. X\_SENS,**  
Page 1 to Page 6, Low Byte Address = 0x16, Read/Write

| Bits   | Description (Default = Not Applicable)                 |
|--------|--|
| [15:0] | X-axis scale correction factor (SCFx), twos complement |

**Table 34. Y\_SENS,**  
Page 1 to Page 6, Low Byte Address = 0x18, Read/Write

| Bits   | Description (Default = Not Applicable)                 |
|--------|--|
| [15:0] | Y-axis scale correction factor (SCFy), twos complement |

## PREFFT WINDOWING

REC\_CTRL1[13:12] provides three options for preFFT windowing of time data. For example, set REC\_CTRL1[13:12] = 01 to use the Hanning window, which offers the best amplitude resolution of the peaks between frequency bins and minimal broadening of peak amplitudes. The rectangular and flat top windows are also available because they are common windowing options for vibration monitoring. The flat top window provides accurate amplitude resolution with a trade-off of broadening the peak amplitudes.

## FFT

The FFT process converts each 512-sample time record into a 256-point spectral record that provides magnitude vs. frequency data.

**FFT AVERAGING**

The FFT averaging function combines multiple FFT records to reduce the variation of the FFT noise floor, enabling detection of lower vibration levels. Each SRx option in the REC\_CTRL1 register has its own FFT average control, which establishes the number of FFT records to average into the final FFT record. To enable this function, write the number of averages for each SRx option that is enabled in the REC\_CTRL1 register to the FFT\_AVGx registers. For example, set FFT\_AVG2[15:8] = 0x10 (DIN = 0x9110) to set the number of FFT averages to 16 for the SR3 sample rate option.

**Table 35. FFT\_AVG1, Page 1 to Page 6, Low Byte Address = 0x0E, Read/Write**

| Bits   | Description (Default = 0x0108)   |
|--------|--|
| [15:8] | FFT averages for a single record, SR1 sample rate, N <sub>F</sub> in Figure 18; range = 1 to 255, binary |
| [7:0]  | FFT averages for a single record, SR0 sample rate, N <sub>F</sub> in Figure 18; range = 1 to 255, binary |

**Table 36. FFT\_AVG2, Page 1 to Page 6, Low Byte Address = 0x10, Read/Write**

| Bits   | Description (Default = 0x0101)   |
|--------|--|
| [15:8] | FFT averages for a single record, SR3 sample rate, N <sub>F</sub> in Figure 18; range = 1 to 255, binary |
| [7:0]  | FFT averages for a single record, SR2 sample rate, N <sub>F</sub> in Figure 18; range = 1 to 255, binary |

**RECORDING TIMES**

When using automatic FFT mode, the automatic recording period (UPDAT\_INT, see Table 21) must be greater than the total recording time. Use the following equations to calculate the recording time:

Manual time mode

$$t_R = t_S + t_{PT} + t_{ST} + t_{AST}$$

FFT modes

$$t_R = N_F \times (t_S + t_{PT} + t_{FFT}) + t_{ST} + t_{AST}$$

Table 37 provides a list of the processing times and settings used in these equations.

**Table 37. Typical Processing Times**

| Function                               | Time (ms)                        |
|--|----------------------------------|
| Sample Time, t <sub>S</sub>            | 1 ÷ f <sub>S</sub> , per AVG_CNT |
| Processing Time, t <sub>PT</sub>       | 18.7                             |
| Storage Time, t <sub>ST</sub>          | 120.0                            |
| Alarm Scan Time, t <sub>AST</sub>      | 2.21                             |
| Number of FFT Averages, N <sub>F</sub> | Per FFT_AVG1, FFT_AVG2           |
| FFT Time, t <sub>FFT</sub>             | 32.7                             |

The storage time (t<sub>ST</sub>) applies only when a storage method is selected in REC\_CTRL1[3:2] (see Table 28 for more details about the record storage settings). The alarm scan time (t<sub>AST</sub>)

applies only when the alarms are enabled in ALM\_CTRL[3:0] (see Table 42 for more information). For systems that cannot use DO1 to monitor the status of these operations, understanding the recording time helps predict when data is available. Note that when using automatic FFT mode, the automatic recording period (UPDAT\_INT, see Table 21) must be greater than the total recording time.

**DATA RECORDS**

After the ADIS16229 finishes processing the FFT data, it stores the data into the data buffer, where it is available for external access using the SPI and x\_BUF registers (see Table 60 and Table 61). REC\_CTRL1[3:2] (see Table 28) provides programmable conditions for writing buffer data into the FFT records, which are in nonvolatile flash memory locations. Set REC\_CTRL1[3:2] = 01 to store buffer data into the flash memory records only when an alarm condition is met. Set REC\_CTRL1[3:2] = 10 to store every set of FFT data into the flash memory locations. The flash memory record provides space for a total of 14 records. Each record stored in flash memory contains a header and frequency domain (FFT) data from both axes, x and y. When all 14 records are full, new records do not load into the flash memory. The REC\_CNTR register (see Table 38) provides a running count for the number of records that are stored. Set GLOB\_CMD\_S[8] = 1 (DIN = 0xB701) to clear all of the records in flash memory.

**Table 38. REC\_CNTR, Page 1 to Page 6, Low Byte Address = 0x50, Read Only**

| Bits   | Description (Default = 0x0000)                         |
|--------|--|
| [15:5] | Not used   |
| [4:0]  | Total number of records taken; range = 0 to 13, binary |

When used in conjunction with automatic trigger mode and record storage, FFT analysis for each sample rate option requires no additional inputs. Depending on the number of FFT averages, the time between each sample rate selection may be quite large. Note that selecting multiple sample rates reduces the number of records available for each sample rate setting, as shown in Table 39.

**Table 39. Available Records per Sample Rate Selected**

| Number of Sample Rates Selected | Available Records |
|---------------------------------|-------------------|
| 1                               | 14                |
| 2                               | 7                 |
| 3                               | 4                 |
| 4                               | 3                 |

**FFT RECORD FLASH ENDURANCE**

The REC\_FLSH\_CNT register (see Table 40) increments when all 14 records contain FFT data.

**Table 40. REC\_FLSH\_CNT, Page 1 to Page 6, Low Byte Address = 0x4A, Read Only**

| Bits   | Description (Default = Not Applicable)            |
|--------|---|
| [15:0] | Flash write cycle count; record data only, binary |

## SENSOR NODE SPECTRAL ALARMS

The alarm function offers six spectral bands for alarm detection. Each spectral band has high and low frequency definitions, along with two different trigger thresholds (Alarm 1 and Alarm 2) for each accelerometer axis. Table 41 provides a summary of each register used to configure the alarm function.

**Table 41. Alarm Function Register Summary**

| Register    | Address | Description                            |
|-------------|---------|--|
| ALM_F_LOW   | 0x20    | Alarm frequency band, lower limit      |
| ALM_F_HIGH  | 0x22    | Alarm frequency band, upper limit      |
| ALM_X_MAG1  | 0x24    | X-axis Alarm Trigger Level 1 (warning) |
| ALM_Y_MAG1  | 0x26    | Y-axis Alarm Trigger Level 1 (warning) |
| ALM_X_MAG2  | 0x28    | X-axis Alarm Trigger Level 2 (fault)   |
| ALM_Y_MAG2  | 0x2A    | Y-axis Alarm Trigger Level 2 (fault)   |
| ALM_PNTR    | 0x2C    | Alarm pointer                          |
| ALM_S_MAG   | 0x2E    | System alarm trigger level             |
| ALM_CTRL    | 0x30    | Alarm configuration                    |
| DIAG_STAT_S | 0x34    | Alarm status                           |
| ALM_X_STAT  | 0x38    | X-axis alarm status                    |
| ALM_Y_STAT  | 0x3A    | Y-axis alarm status                    |
| ALM_X_PEAK  | 0x3C    | X-axis alarm peak                      |
| ALM_Y_PEAK  | 0x3E    | Y-axis alarm peak                      |
| ALM_X_FREQ  | 0x44    | X-axis alarm frequency of peak alarm   |
| ALM_Y_FREQ  | 0x46    | Y-axis alarm frequency of peak alarm   |

The ALM\_CTRL register (see Table 42) provides control bits that enable the spectral alarms of each axis, configures the system alarm, sets the record delay for the spectral alarms, and configures the clearing function for the DIAG\_STAT\_S error flags (see Table 86).

**Table 42. ALM\_CTRL,**

**Page 1 to Page 6, Low Byte Address = 0x30, Read/Write**

| Bits    | Description (Default = 0x0080)   |
|---------|--|
| [15:12] | Not used.  |
| [11:8]  | Response delay; range = 0 to 15. Represents the number of spectral records for each spectral alarm before a spectral alarm flag is set high. |
| 7       | Latch DIAG_STAT_S error flags. Requires a clear status command (GLOB_CMD_S[4]) to reset the flags to 0. 1 = enabled, 0 = disabled.           |
| 6       | Enable DO1 as an Alarm 1 output indicator and enable DO2 as an Alarm 2 output indicator. 1 = enabled, 0 = disabled.                          |
| 5       | System alarm comparison polarity.<br>1 = trigger when less than ALM_S_MAG[15:0].<br>0 = trigger when greater than ALM_S_MAG[15:0].           |
| 4       | System alarm. 1 = temperature, 0 = power supply.   |
| 3       | Alarm S enable (ALM_S_MAG). 1 = enabled, 0 = disabled.   |
| 2       | Not used.  |
| 1       | Alarm Y enable (ALM_Y_MAG). 1 = enabled, 0 = disabled.   |
| 0       | Alarm X enable (ALM_X_MAG). 1 = enabled, 0 = disabled.   |

## ALARM DEFINITION

The alarm function provides six programmable spectral bands, as shown in Figure 22. Each spectral alarm band has lower and upper frequency definitions for all of the sample rate options (SRx). It also has two independent trigger level settings, which are useful for systems that value warning and fault condition indicators.

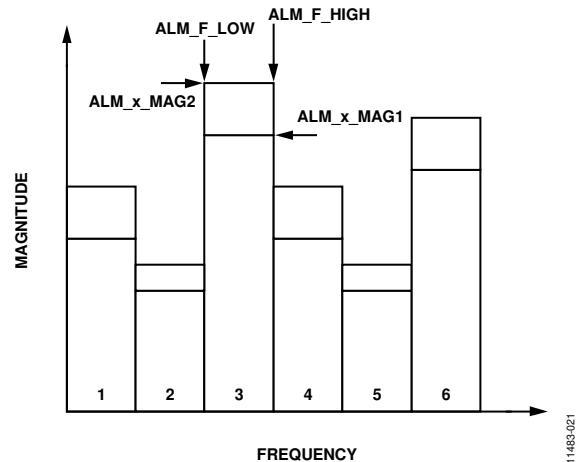


Figure 22. Spectral Band Alarm Setting Example, ALM\_PNTR = 0x03

Select the spectral band for configuration by writing its number (1 to 6) to ALM\_PNTR[2:0] (see Table 43). Then select the sample rate option using ALM\_PNTR[9:8]. This number represents a binary number, which corresponds to the x in the SRx sample rates option associated with REC\_CTRL1[11:8] (see Table 28). For example, set ALM\_PNTR[7:0] = 0x05 (DIN = 0xAC05) to select Alarm Spectral Band 5, and set ALM\_PNTR[15:8] = 0x02 (DIN = 0xAC02) to select the SR2 sample rate option.

**Table 43. ALM\_PNTR,**

**Pages 1 to 6, Low Byte Address = 0x2C, Read/Write**

| Bits    | Description (Default = 0x0000)                    |
|---------|---|
| [15:10] | Not used  |
| [9:8]   | Sample rate option; range = 0 to 3 for SR0 to SR3 |
| [7:3]   | Not used  |
| [2:0]   | Spectral band number; range = 1 to 6              |



## Alarm Band Frequency Definitions

After the spectral band and sample rate settings are set, program the lower and upper frequency boundaries by writing their bin numbers to the ALM\_F\_LOW register (see Table 44) and ALM\_F\_HIGH register (see Table 45). Use the bin width definitions listed in Table 30 to convert a frequency into a bin number for this definition. Calculate the bin number by dividing the frequency by the bin width associated with the sample rate setting. For example, if the sample rate is 5000 Hz and the lower band frequency is 400 Hz, divide that number by the bin width of 10 Hz to arrive at the 40<sup>th</sup> bin as the lower band setting. Then set ALM\_F\_LOW[7:0] = 0x28 (DIN = 0xA028) to establish 400 Hz as the lower frequency for the 5000 SPS sample rate setting.

**Table 44. ALM\_F\_LOW,**  
Page 1 to Page 6, Low Byte Address = 0x20, Read/Write

| Bits   | Description (Default = 0x0000)                |
|--------|---|
| [15:8] | Not used                                      |
| [7:0]  | Lower frequency, bin number; range = 0 to 255 |

**Table 45. ALM\_F\_HIGH,**  
Page 1 to Page 6, Low Byte Address = 0x22, Read/Write

| Bits   | Description (Default = 0x0000)                |
|--------|---|
| [15:8] | Not used                                      |
| [7:0]  | Upper frequency, bin number; range = 0 to 255 |

## Alarm Trigger Settings

The ALM\_x\_MAG1 and ALM\_x\_MAG2 registers (see Table 46 to Table 49) provide two independent trigger settings for both axes of acceleration data. They use the data format established by the range settings in the REC\_CTRL2 register (see Table 31) and recording mode in REC\_CTRL1[1:0] (see Table 28). For example, when using the 0 g to 1 g mode for FFT analysis, 32,768 LSB is the closest setting to 500 mg. Therefore, set ALM\_Y\_MAG2 = 0x8000 (DIN = 0xAB80, 0xAA00) to set the critical alarm to 500 mg, when using the 0 g to 1 g range option in REC\_CTRL2 for FFT records. See Table 31 and Table 32 for more information about formatting each trigger level. Note that the trigger settings associated with Alarm 2 must be greater than the trigger settings for Alarm 1. In other words, the alarm magnitude settings must meet the following criteria:

ALM\_X\_MAG2 > ALM\_X\_MAG1  
ALM\_Y\_MAG2 > ALM\_Y\_MAG1

**Table 46. ALM\_X\_MAG1,**  
Page 1 to Page 6, Low Byte Address = 0x24, Read/Write

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:0] | X-Axis Alarm Trigger Level 1, 16-bit unsigned (see Table 31 and Table 32 for the scale factor) |

**Table 47. ALM\_Y\_MAG1,**  
Page 1 to Page 6, Low Byte Address = 0x26, Read/Write

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:0] | Y-Axis Alarm Trigger Level 1, 16-bit unsigned (see Table 31 and Table 32 for the scale factor) |

**Table 48. ALM\_X\_MAG2,**  
Page 1 to Page 6, Low Byte Address = 0x28, Read/Write

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:0] | X-Axis Alarm Trigger Level 2, 16-bit unsigned (see Table 31 and Table 32 for the scale factor) |

**Table 49. ALM\_Y\_MAG2,**  
Page 1 to Page 6, Low Byte Address = 0x2A, Read/Write

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:0] | Y-Axis Alarm Trigger Level 2, 16-bit unsigned (see Table 31 and Table 32 for the scale factor) |

**Table 50. ALM\_S\_MAG,**  
Page 1 to Page 6, Low Byte Address = 0x2E, Read/Write

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:0] | System alarm trigger level, data format matches target from ALM_CTRL[4] (see Table 42) |

## Enable Alarm Settings

Before configuring the spectral alarm registers, clear their current contents by setting GLOB\_CMD\_S[9] = 1 (DIN = 0xB702). After completing the spectral alarm band definitions, save the settings by setting GLOB\_CMD\_S[12] = 1 (DIN = 0xB710). The device ignores the save command if any of these locations has already been written to.

## ALARM INDICATOR SIGNALS

GPO\_CTRL[5:0] (see Table 84) and ALM\_CTRL[6] (see Table 42) provide controls for establishing DO1 and DO2 as dedicated alarm output indicator signals. Use GPO\_CTRL[5:0] to select the alarm function for DO1 and/or DO2, then set ALM\_CTRL[6] = 1 to enable DO1 to serve as an Alarm 1 indicator and DO2 as an Alarm 2 indicator. This setting establishes DO1 to indicate Alarm 1 (warning) conditions and DO2 to indicate Alarm 2 (critical) conditions.

## ALARM FLAGS AND CONDITIONS

The FFT header (see Table 70) contains both generic alarm flags (DIAG\_STAT\_S, see Table 86) and spectral band-specific alarm flags (ALM\_x\_STAT, see Table 51 and Table 52). The FFT header also contains magnitude (ALM\_x\_PEAK, see Table 53 and Table 54) and frequency information (ALM\_x\_FREQ, see Table 55 and Table 56) associated with the highest magnitude of vibration content in the record.

**ALARM STATUS**

The ALM\_x\_STAT registers (see Table 51 and Table 52) provide alarm bits for each spectral band on the current sample rate option.

**Table 51. ALM\_X\_STAT,**  
Page 1 to Page 6, Low Byte Address = 0x38, Read Only

| Bits  | Description (Default = 0x0000)                               |
|-------|--|
| 15    | Alarm 2 on Band 6; 1 = alarm set, 0 = no alarm               |
| 14    | Alarm 1 on Band 6; 1 = alarm set, 0 = no alarm               |
| 13    | Alarm 2 on Band 5; 1 = alarm set, 0 = no alarm               |
| 12    | Alarm 1 on Band 5; 1 = alarm set, 0 = no alarm               |
| 11    | Alarm 2 on Band 4; 1 = alarm set, 0 = no alarm               |
| 10    | Alarm 1 on Band 4; 1 = alarm set, 0 = no alarm               |
| 9     | Alarm 2 on Band 3; 1 = alarm set, 0 = no alarm               |
| 8     | Alarm 1 on Band 3; 1 = alarm set, 0 = no alarm               |
| 7     | Alarm 2 on Band 2; 1 = alarm set, 0 = no alarm               |
| 6     | Alarm 1 on Band 2; 1 = alarm set, 0 = no alarm               |
| 5     | Alarm 2 on Band 1; 1 = alarm set, 0 = no alarm               |
| 4     | Alarm 1 on Band 1; 1 = alarm set, 0 = no alarm               |
| 3     | Not used   |
| [2:0] | Most critical alarm condition, spectral band; range = 1 to 6 |

**Table 52. ALM\_Y\_STAT,**  
Page 1 to Page 6, Low Byte Address = 0x3A, Read Only

| Bits  | Description (Default = 0x0000)                               |
|-------|--|
| 15    | Alarm 2 on Band 6; 1 = alarm set, 0 = no alarm               |
| 14    | Alarm 1 on Band 6; 1 = alarm set, 0 = no alarm               |
| 13    | Alarm 2 on Band 5; 1 = alarm set, 0 = no alarm               |
| 12    | Alarm 1 on Band 5; 1 = alarm set, 0 = no alarm               |
| 11    | Alarm 2 on Band 4; 1 = alarm set, 0 = no alarm               |
| 10    | Alarm 1 on Band 4; 1 = alarm set, 0 = no alarm               |
| 9     | Alarm 2 on Band 3; 1 = alarm set, 0 = no alarm               |
| 8     | Alarm 1 on Band 3; 1 = alarm set, 0 = no alarm               |
| 7     | Alarm 2 on Band 2; 1 = alarm set, 0 = no alarm               |
| 6     | Alarm 1 on Band 2; 1 = alarm set, 0 = no alarm               |
| 5     | Alarm 2 on Band 1; 1 = alarm set, 0 = no alarm               |
| 4     | Alarm 1 on Band 1; 1 = alarm set, 0 = no alarm               |
| 3     | Not used   |
| [2:0] | Most critical alarm condition, spectral band; range = 1 to 6 |

**WORST-CASE CONDITION MONITORING**

The ALM\_x\_PEAK registers (see Table 53 and Table 54) contain the peak magnitude for the worst-case alarm condition in each axis. The ALM\_x\_FREQ registers (see Table 55 and Table 56) contain the frequency bin number for the worst-case alarm condition.

**Table 53. ALM\_X\_PEAK,**  
Page 1 to Page 6, Low Byte Address = 0x3C, Read Only

| Bits   | Description (Default = 0x0000)                |
|--------|---|
| [15:0] | Alarm peak, x-axis, accelerometer data format |

**Table 54. ALM\_Y\_PEAK,**  
Page 1 to Page 6, Low Byte Address = 0x3E, Read Only

| Bits   | Description (Default = 0x0000)                |
|--------|---|
| [15:0] | Alarm peak, y-axis, accelerometer data format |

**Table 55. ALM\_X\_FREQ,**  
Page 1 to Page 6, Low Byte Address = 0x44, Read Only

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:8] | Not used   |
| [7:0]  | Alarm frequency of x-axis peak alarm level, FFT bin number; range = 0 to 255 |

**Table 56. ALM\_Y\_FREQ,**  
Page 1 to Page 6, Low Byte Address = 0x46, Read Only

| Bits   | Description (Default = 0x0000)   |
|--------|--|
| [15:8] | Not used   |
| [7:0]  | Alarm frequency of y-axis peak alarm level, FFT bin number; range = 0 to 255 |