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Digital Output, High Precision Angular Rate Sensor

Data Sheet

ADIS16130

FEATURES

Low noise density: 0.0125°/sec/√Hz
Industry-standard serial peripheral interface (SPI)
24-bit digital resolution
Dynamic range: ±250°/sec
Z-axis, yaw rate response
Bandwidth, adjustable: 300 Hz
Turn-on time: 35 ms
Digital self-test
High vibration rejection
High shock survivability
Embedded temperature sensor output
Precision voltage reference output
5 V single-supply operation
−40°C to +85°C

APPLICATIONS

Guidance and control
Instrumentation
Inertial measurement units (IMU)
Platform stabilization
Navigation

GENERAL DESCRIPTION

The ADIS16130 is a low noise, digital output angular rate sensor (gyroscope) that provides an output response over the complete dynamic range of ±250°/sec.

Its industry-standard serial interface and register structure provide a simple interface that is supported by most MCU, DSP, and FPGA platforms.

By implementing a unique design, the device provides superior stability over variations in temperature, voltage, linear acceleration, vibration, and next-level assembly. In addition, the surface-micro-machining technology used to manufacture the device is the same high volume BiMOS process used by Analog Devices, Inc., for its high reliability automotive sensor products.

Features include a temperature output that provides critical information for system-level calibrations and a digital self-test feature that exercises the mechanical structure of the sensor and enables system-level diagnostics.

The package configuration is a 36 mm × 44 mm × 16 mm module with a standard 24-lead connector interface.

FUNCTIONAL BLOCK DIAGRAM

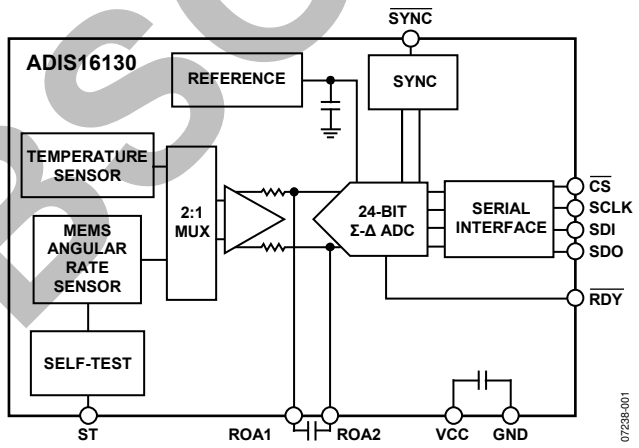

Figure 1.

Rev. C

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1/08—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, VCC = 5 V, angular rate = 0°/sec, C_{OUT} = 0 µF, ±1 *g*, unless otherwise noted.

Table 1.

Parameter	Conditions	Min[1]	Typ	Max[1]	Unit
SENSITIVITY	Clockwise rotation is positive output (see Figure 5)				
Dynamic Range[2]	Full-scale range over specified operating conditions	±250			°/sec
Initial	MODE[1] = 0, 16-bit RATEDATA	88	91.75	96	LSB/°/sec
	MODE[1] = 1, 24-bit RATEDATA	22,548	23,488	24,428	LSB/°/sec
Nonlinearity	Best-fit straight line		0.04		% of FS
NULL					
Zero Rotation Rate Output	MODE[1] = 0, 16-bit RATEDATA		32,768		LSB
	MODE[1] = 1, 24-bit RATEDATA		8,388,608		LSB
Initial Null	±1σ		±3		°/sec
In-Run Bias Stability	1σ		0.0016		°/sec
Angle Random Walk	1σ		0.56		°/√Hr
Turn-On Time	Power on to ±0.5°/sec of final value, 80 Hz bandwidth		35		ms
Linear Acceleration Effect	Any axis		0.05		°/sec/*g*
Voltage Sensitivity	VCC = 4.75 V to 5.25 V		0.2		°/sec/V
NOISE PERFORMANCE					
Rate Noise Density[3]			0.0125		°/sec/√Hz
FREQUENCY RESPONSE					
Bandwidth	−3 dB frequency with no external capacitance		300		Hz
Sensor Resonant Frequency			14		kHz
SELF-TEST INPUTS					
ST RATEOUT Response[4]	ST pins from Logic 0 to Logic 1	45	75	105	°/sec
Logic 1 Input Voltage	Standard high logic level definition	3.3			V
Logic 0 Input Voltage	Standard low logic level definition			1.7	V
Input Impedance	To GND		3.13		kΩ
TEMPERATURE SENSOR					
Output at 298 K (25°C)			8,388,608		LSB
Scale Factor			14,093		LSB/°C
DIGITAL OUTPUTS					
Output Low Voltage (V_{OL})				0.4	V
Output High Voltage (V_{OH})		4			V
DIGITAL INPUTS					
Input Current	$\overline{CS}$			10	µA
	All others			1	µA
Input Capacitance			5		pF
VT+		1.4		2	V
VT−		0.8		1.4	V
(VT+) – (VT−)		0.3		0.85	V
POWER SUPPLY					
Operating Voltage Range		4.75	5.00	5.25	V
Quiescent Supply Current	I_{OUT} = 0 mA, 5 V		73	85	mA
TEMPERATURE RANGE					
Operating Range		−40		+85	°C

[1] All minimum and maximum specifications are guaranteed. Typical specifications are not tested or guaranteed.
[2] Dynamic range is the maximum full-scale measurement range possible, including output swing range, initial offset, sensitivity, offset drift, and sensitivity drift at 4.75 V to 5.25 V supplies.
[3] Resulting bias stability is <0.01°/sec.
[4] Self-test response varies with temperature; see Figure 12.

TIMING SPECIFICATIONS

All input signals are specified with 10% to 90% rise and fall times of less than 5 ns.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
t_1	50			ns	$\overline{SYNC}$ pulse width
Read Operation					
t_4	0			ns	$\overline{CS}$ falling edge to SCLK falling edge setup time
t_5[1]					SCLK falling edge to data valid delay
	0		60	ns	DV_{DD} of 4.75 V to 5.25 V
t_{5A}[1, 2]					$\overline{CS}$ falling edge to data valid delay
	0		60	ns	DV_{DD} of 4.75 V to 5.25 V
t_6	50			ns	SCLK high pulse width
t_7	50			ns	SCLK low pulse width
t_8	0			ns	$\overline{CS}$ rising edge after SCLK rising edge hold time
t_9[3]	10		80	ns	Bus relinquish time after SCLK rising edge
Write Operation					
t_{11}	0			ns	$\overline{CS}$ falling edge to SCLK falling edge setup
t_{12}	30			ns	Data valid to SCLK rising edge setup time
t_{13}	25			ns	Data valid after SCLK rising edge hold time
t_{14}	50			ns	SCLK high pulse width
t_{15}	50			ns	SCLK low pulse width
t_{16}	0			ns	$\overline{CS}$ rising edge after SCLK rising edge hold time

[1] These numbers are measured with the load circuit shown in Figure 4 and defined as the time required for the output to cross the V_{OL} or V_{OH} limits.
[2] This specification is relevant only if $\overline{CS}$ goes low while SCLK is low.
[3] These numbers are derived from the measured time taken by the data output to change 0.5 V when loaded with the circuit shown in Figure 4. The measured number is then extrapolated back to remove effects of charging or discharging the 50 pF capacitor. Therefore, the times quoted are the true bus relinquish times of the part and as such are independent of external bus loading capacitances.

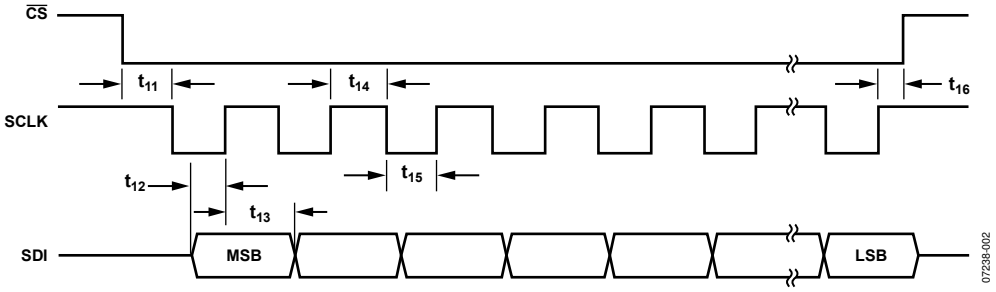

Figure 2. Input Timing for Write Operation

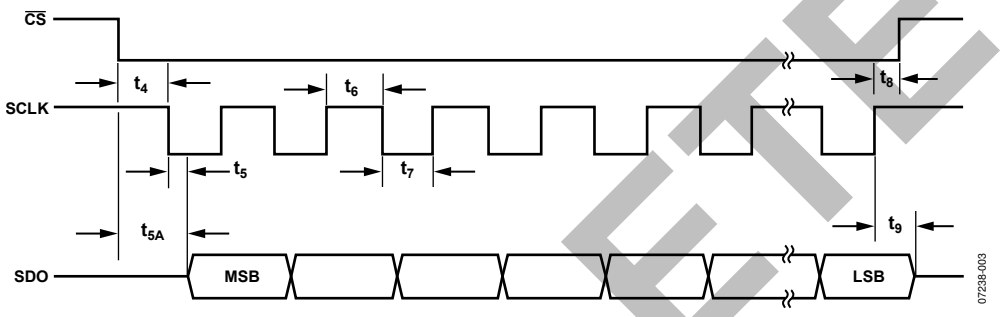

Figure 3. Output Timing for Read Operation

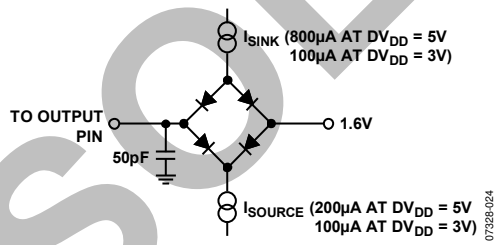

Figure 4. Load Circuit for Access Time and Bus Relinquish Time

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration (Any Axis, Unpowered, 0.5 ms)	2000 *g*
Acceleration (Any Axis, Powered, 0.5 ms)	2000 *g*
$+V_S$	−0.3 V to +6.0 V
Output Short-Circuit Duration (Any Pin to Common)	Indefinite
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Dropping the device onto a hard surface may cause a shock of greater than 2000 *g* and exceed the absolute maximum rating of the device. Care should be exercised when handling the device to avoid damage.

THERMAL RESISTANCE

The ADIS16130 provides a temperature output that is representative of the junction temperature. This can be used for system-level monitoring and power management/thermal characterization.

Table 4. Thermal Characteristics

Package Type[1]	θ_{JA}	θ_{JC}	Unit
24-Lead Module	15.7	1.48	°C/W

[1] Weight = 28.5 g typical.

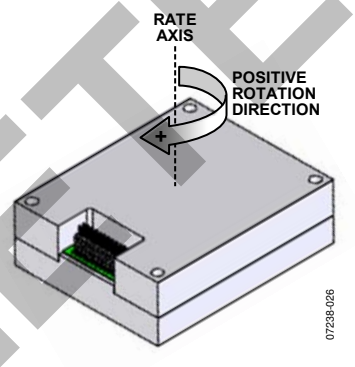

Figure 5. Rotational Measurement Orientation

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

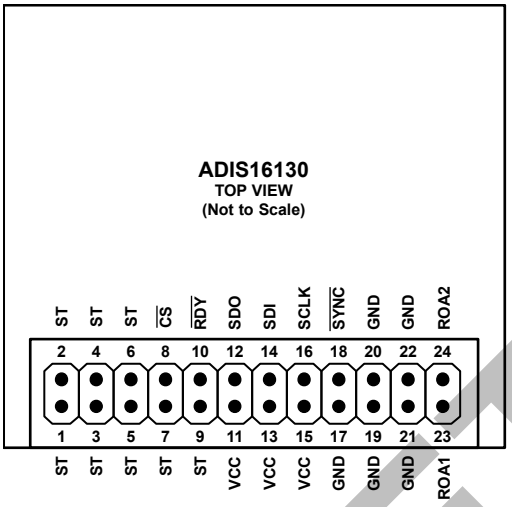

Figure 6. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1 to 7, 9	ST	Self-Test (see the Self-Test Function section)
8	$\overline{CS}$	Chip Select of the SPI
10	$\overline{RDY}$	Data Ready
11, 13, 15	VCC	Power Supply
12	SDO	Data Output of the SPI
14	SDI	Data Input of the SPI
16	SCLK	Serial Clock of the SPI
17, 19 to 22	GND	Power Supply Ground
18	$\overline{SYNC}$	Synchronization Input
23	ROA1	Analog Filter Node 1
24	ROA2	Analog Filter Node 2

TYPICAL PERFORMANCE CHARACTERISTICS

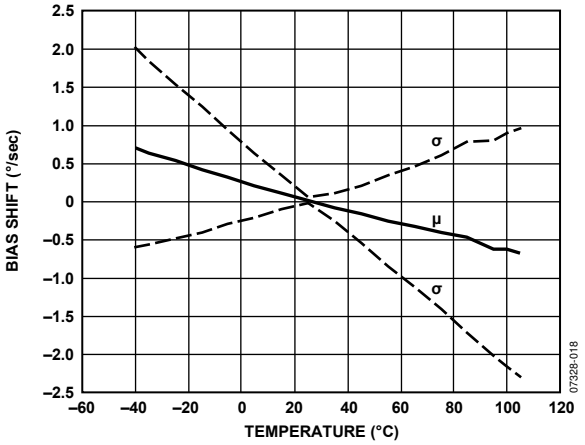

Figure 7. Bias Shift vs. Temperature, VCC = 5 V

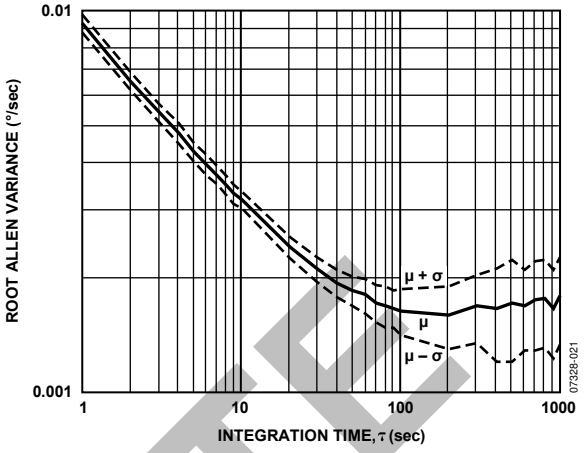

Figure 10. Root Allen Variance, VCC = 5 V, 25°C

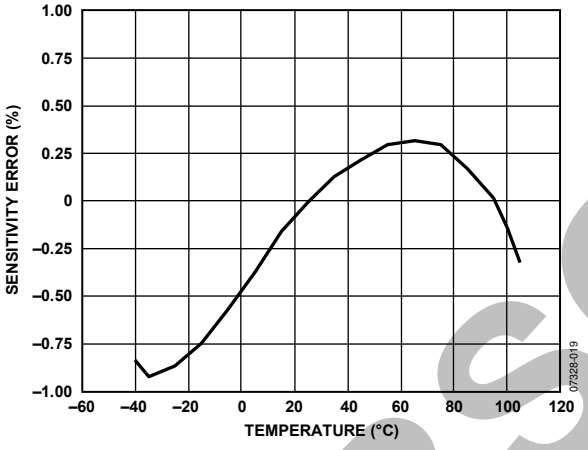

Figure 8. Sensitivity Error vs. Temperature, VCC = 5 V

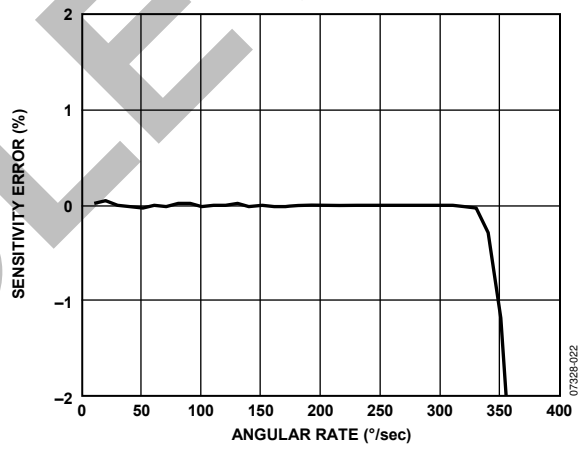

Figure 11. Sensitivity Error vs. Angular Rate, VCC = 5 V, 25°C

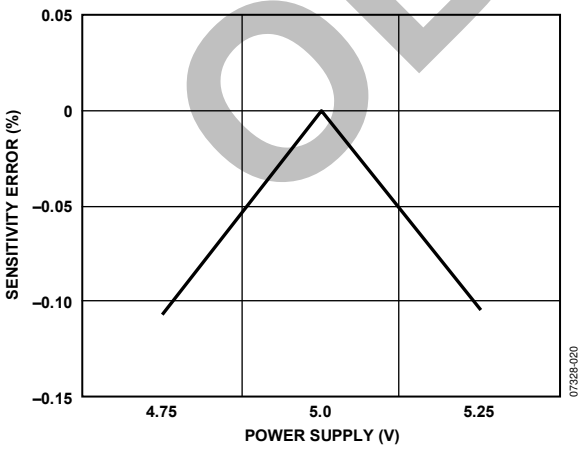

Figure 9. Sensitivity Error vs. Power Supply, 25°C

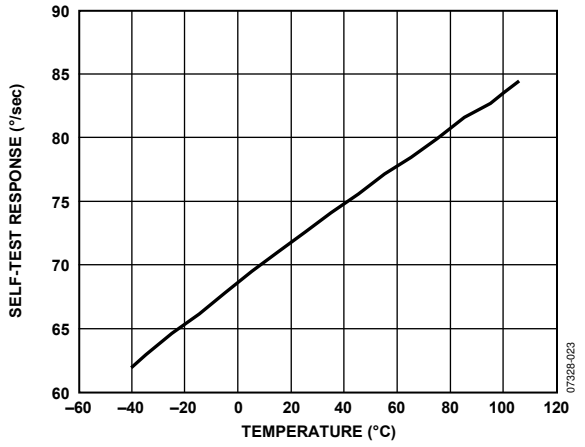

Figure 12. Self-Test Response vs. Temperature, VCC = 5 V

BASIC OPERATION

The ADIS16130 produces digital angular rate (RATE) and temperature (TEMP) data. The digital communication employs a simple 4-wire SPI that provides access to output data and several configuration features. A set of communication and configuration registers govern the operation in the ADIS16130. See Table 10 for a summary of these registers.

QUICK START

The ADIS16130 SPI operates in 8-bit segments. The first byte of a SPI sequence goes into the COM register, which contains the read/write control bit and the address of the target register. When writing information into control registers, the next byte contains the configuration information. When reading output data, the next one to three bytes contain the contents of the register selected.

Configuration Sequence

The sequence in Table 6 provides the recommended configuration sequence. Table 2 and Figure 2 provide the timing information for each segment of this configuration sequence.

For additional information on design and optimization with the ADIS16130, see the AN-1042 Application Note.

Table 6. Configuration Sequence

Step	SDI[1]	Register	Purpose
1	0x01	COM	Start a write sequence for IOP.
2	0x38	IOP	Configure the data-ready signal to pulse low when the RATEDATA and TEMPDATA output registers contain new data. The data-ready signal goes high after reading either of these registers.
3	0x28	COM	Start a write sequence for the RATECS register.
4	0x0A	RATECS	Enable and configure the gyroscope data channel.
5	0x30	COM	Start a write sequence for RATECONV register.
6	0x05	RATECONV	Initialize the RATE conversion.
7	0x2A	COM	Start a write sequence for the TEMPCS register.
8	0x0A	TEMPCS	Enable and configure the temperature data channel.
9	0x32	COM	Start a write sequence for TEMPCONV.
10	0x05	TEMPCONV	Initialize the TEMP conversion.
11	0x38	COM	Start a write sequence for the MODE register.
12	0x22	MODE	Establish the data output resolution to 24 bits and start the conversion process with the RATEDATA channel.

[1] The SDI column lists the hexadecimal code representation of the SDI bit input sequence.

Reading RATE Output Data

After the configuration sequence in Table 6 is complete, reading the output data is very simple. The ADIS16130 converts the RATE and TEMP data continuously. To better understand this process, Figure 13 provides an example read sequence, and Table 2 and Figure 3 provide critical timing details for the output signal. The first byte of the sequence uses SDI to establish a read of the RATE output register. This is accomplished by writing 0x48 to the COM register. The most significant byte is first in the SDO sequence, followed by the next significant, and then the least significant. When 16-bit resolution is in use, only two bytes are output from the SDO during the read sequence.

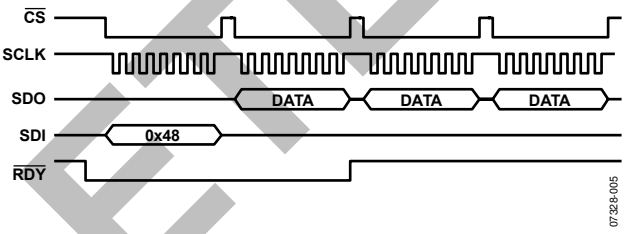

Figure 13. Read Sequence Example

The data-ready signal, $\overline{\text{RDY}}$, indicates that unread data is available on both RATE and TEMP output registers. After the RATE or TEMP channel is read, the signal returns high, as shown in Figure 13. The RATE and TEMP channels update sequentially, and each has a sample rate of 5.7 kSPS. The internal sample rate is not dependent on the SPI signals or read rates. Using the data-ready signal to drive data collection helps avoid losing data due to data collision, which is when a user-driven read cycle coincides with the internal update time. In this case, the old data remains and the new data is lost.

If a lower sample rate meets system-level requirements, the data-ready signal can still be useful in facilitating SPI read sequences. In this case, the data-ready signal pulses high for approximately 26 µs before returning low and then repeats this pattern at two times the internal sample rate. This signal can feed a counter circuit (or firmware), which drives a processor interrupt routine at a reduced sample rate.

Reading TEMP Output Data

Reading TEMP data requires a sequence that is very similar to that of Figure 13, except that the initial SDI sequence must be changed from 0x48 to 0x4A. If the TEMP data is not used, Step 7 to Step 10 of the configuration sequence are not required.

DATA FORMAT

The ADIS16130 uses the offset binary data format.

$$RATE = \left[\frac{Codes - 2^{23}}{23{,}488}\right] \quad TEMP = \left[\frac{Codes - 2^{23}}{14{,}093} + 25°\text{C}\right]$$

Table 7. Gyroscope Rate Output Data Format

24-Bit (Codes)	16-Bit (Codes)	Rate Output
14,260,608	55,706	+250°/sec
8,623,488	33,686	+10°/sec
8.388,612	32,769	+0.00017030°/sec
8,388,609		+0.000042575°/sec
8,388,608	32,768	0
8,388,607		−0.000042575°/sec
8,388,604	32,767	−0.00017030°/sec
8,153,728	31,850	−10°/sec
2,516,608	9,830	−250°/sec

Table 8. Gyroscope Temperature Output Data Format

24-Bit (Codes)	16-Bit (Codes)	Rate Output
9,516,048	37,172	+105°C
9,234,188	36,071	+85°C
8,402,701	32,823	+26°C
8,388,608	32,768	+25°C
8,036,283	31,392	+0°C
7,472,563	29,189	−40°C

CONFIGURATION OPTIONS

Synchronization Input

The $\overline{\text{SYNC}}$ pin can be used to synchronize the ADIS16130 with other devices in the system. When the $\overline{\text{SYNC}}$ bit in the I/O port register (IOP) is set and the $\overline{\text{SYNC}}$ pin is low, the ADIS16130 does not process any conversions. Instead, it waits until the $\overline{\text{SYNC}}$ pin goes high, and then starts the operation. This allows the conversion to start from a known point in time (for example, the rising edge of the $\overline{\text{SYNC}}$ pin).

Self-Test Function

The self-test function enables system-level diagnostic checks for the entire ADIS16130 sensor/signal conditioning circuit. To activate the self-test function, there must be a logic high signal on all ST pins (see Table 5). When activated, the self-test function results in a rate measurement shift. By comparing the observed shift with the limits specified in this data sheet, users can determine the pass/fail criteria for system-level diagnostic routines. For normal gyroscope operation, place a logic low input on all ST pins. For systems that do not require this feature, tie all ST pins to GND.

Analog Bandwidth

The typical −3 dB cutoff frequency for the ADIS16130 is 300 Hz, which is the combined response of two single-pole filters, as shown in Figure 14. Pin ROA1 and Pin ROA2 provide the opportunity for further bandwidth reduction in the first filter stage, as shown in the following relationship:

$$f_{-3dB} = \frac{1}{2 \times \pi \times R \times (C + C_{ext})}$$

where:
R = 25 kΩ.
C = 6800 pF.
C_{ext} is as defined in Figure 15 and Table 9.

The relationship between the −3 dB cutoff frequency and the external capacitance of the ADIS16130 is shown in Figure 15 and Table 9.

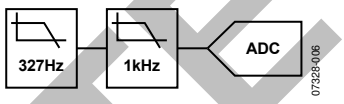

Figure 14. Frequency Response Block Diagram

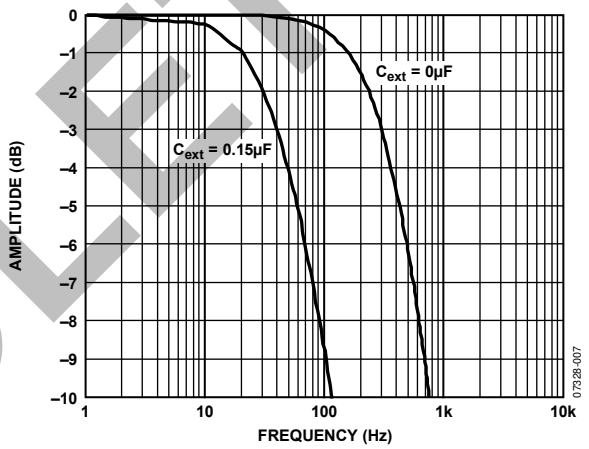

Figure 15. Frequency Response: C_{ext} = 0 µF vs. C_{ext} = 0.15 µF

Table 9. Nominal Bandwidth for Standard Capacitor Values

C_{ext} (pF)	BW (Hz)	C_{ext} (pF)	BW (Hz)	C_{ext} (pF)	BW (Hz)
1000	276.8	10,000	198.9	100,000	52.2
1200	274.4	12,000	187.2	120,000	44.8
1500	270.9	15,000	172.1	150,000	37.0
1800	267.5	18,000	159.2	180,000	31.5
2200	263.1	22,000	144.7	220,000	26.3
2700	257.7	27,000	129.9	270,000	21.8
3300	251.6	33,000	115.7	330,000	18.1
3900	245.8	39,000	104.4	390,000	15.5
4300	242.1	43,000	97.9	430,000	14.1
4700	238.4	47,000	92.3	470,000	12.9
5100	234.9	51,000	87.2	510,000	12.0
5600	230.7	56,000	81.6	560,000	10.9
6200	225.8	62,000	75.8	620,000	9.9
7500	215.8	75,000	65.6	750,000	8.2
8200	210.8	82,000	61.2	820,000	7.6
9100	204.7	91,000	56.3	910,000	6.8

CONTROL REGISTERS

Table 10. Register Descriptions

Name	Address	Type	Purpose
COM	0x00	W	Facilitate communications in the SPI port (see Table 11)
IOP	0x01	R/W	Data-ready and synchronization controls (see Table 12)
	0x02 to 0x07		Reserved
RATEDATA	0x08	R	Gyroscope output, rate of rotation
TEMPDATA	0x0A	R	Temperature output
	0x10 to 0x22		Reserved
RATECS	0x28	R/W	Gyroscope channel setup (see Table 13)
TEMPCS	0x2A	R/W	Temperature channel setup (see Table 14)
RATECONV	0x30	R/W	Gyroscope conversion time control (see Table 15)
TEMPCONV	0x32	R/W	Temperature conversion time control (see Table 15)
	0x33 to 0x37		Reserved
MODE	0x38	R/W	Resolution mode control (see Table 16)

CONTROL REGISTER DETAILS

Table 11. COM Register Bit Assignments

Bit	Description
[7]	0
[6]	1 = read; 0 = write
[5:0]	Register address

Table 12. IOP Register Bit Assignments

Bit	Description
[7:4]	0011
[3]	1 = data-ready signal low when unread data on all channels; 0 = data-ready signal low when unread data on one channel
[2:1]	00
[0]	0 = synchronization disabled; 1 = synchronization enabled

Table 13. RATECS Register Bit Assignments

Bit	Description
[7:4]	0000
[3]	1 = channel enable; 0 = channel disable
[2:0]	010

Table 14. TEMPCS Register Bit Assignments

Bit	Description
[7:4]	0000
[3]	1 = channel enable; 0 = channel disable
[2:0]	010

Table 15. RATECONV/TEMPCONV Bit Assignments

Bit	Description
[7:0]	00000101

Table 16. MODE Register Bit Assignments

Bit	Description
[7:2]	001000
[1]	1 = 24-bit resolution; 0 = 16-bit resolution
[0]	0

APPLICATIONS INFORMATION

ACHIEVING OPTIMAL NOISE PERFORMANCE

Several system-level considerations can have an impact on the noise and accuracy of the ADIS16130. Understanding and managing these factors can influence the behavior of any high performance system.

Supply and Common Considerations

The ADIS16130 provides approximately 1.8 µF of decoupling capacitance. This capacitance is distributed throughout the device and should be taken into account when considering potential noise threats on the power supply lines.

Bandwidth Setting

If C_{OUT} is applied to reduce the bandwidth of the ADIS16130 response, it should be placed close to the device. Long cable leads and PCB traces increase the risk of introducing noise into the system.

SECOND-LEVEL ASSEMBLY

The ADIS16130 package supports two mounting approaches: a bulkhead mount, where the interface is separate from the attachment surface, and a PCB mount that provides the mechanical and electrical connections on the same surface.

Figure 16 provides a suggested design for the ADIS16130's mechanical attachment. The hole pattern shown in Figure 16 can support either mounting approach and enables the integration of the mating socket layout that is illustrated in Figure 17.

The mating socket layout uses the Samtec CLM-112-02 family of connectors. The 24 holes that are inside the pad accommodate the pins on the ADIS16130, which can extend beyond the package body. The stress relief provided by these holes is important for maintaining reliability and optimal bias stability performance.

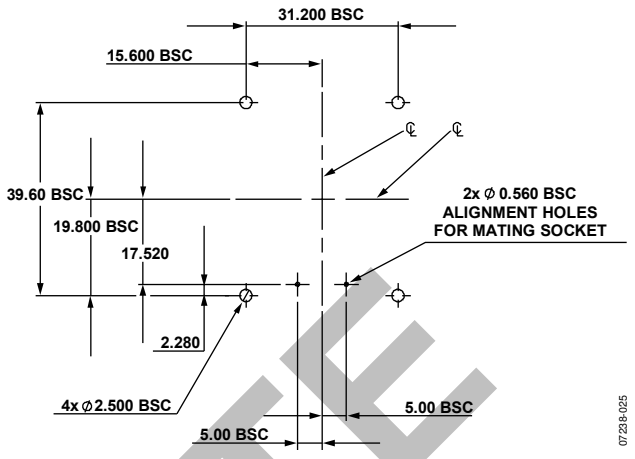

Figure 16. Suggested Hole Pattern for Mounting

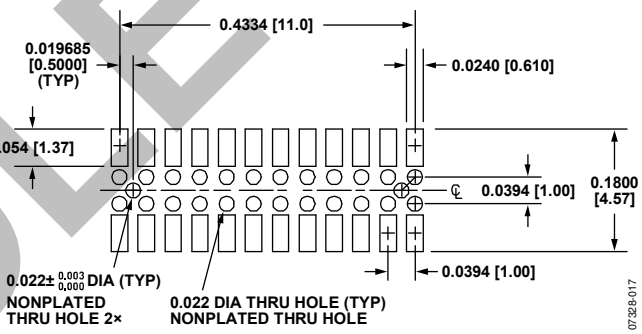

Figure 17. Mating Socket Recommended Pad Layout with Dimensions Shown in Inches and (Millimeters)

OUTLINE DIMENSIONS

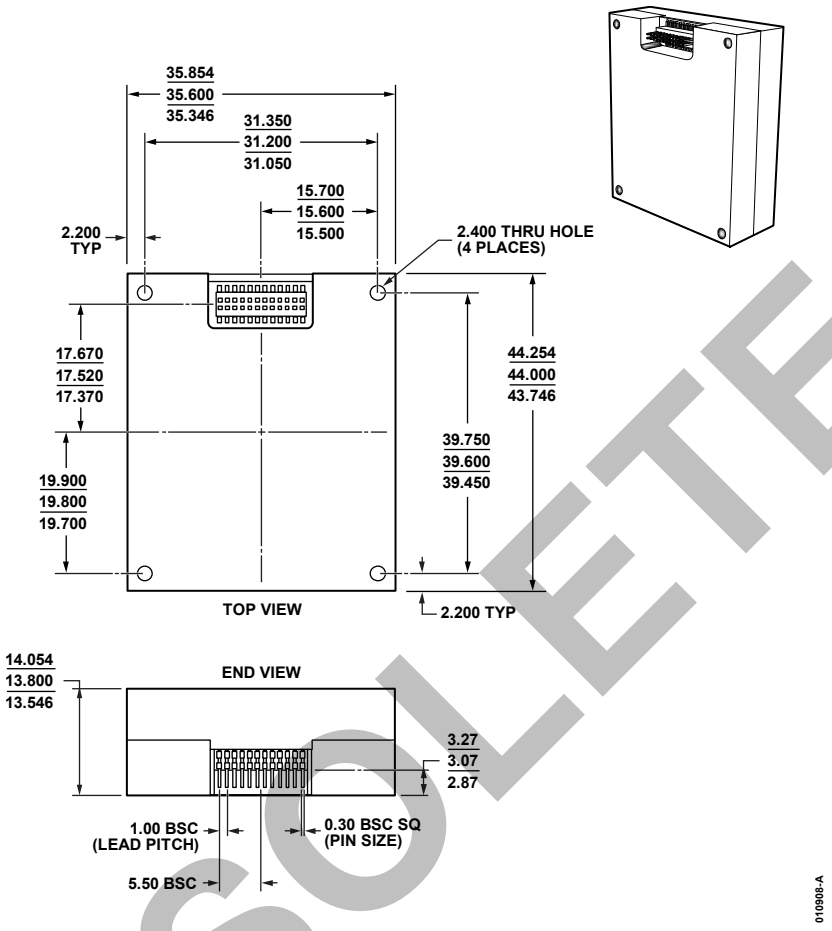

Figure 18. PCB Module with Connector Interface (ML-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Notes	Temperature Range	Package Description	Package Option
ADIS16130AMLZ		−40°C to +85°C	PCB Module with Connector Interface	ML-24-3
ADIS16130AMLZ-P	[2]	−40°C to +85°C	PCB Module with Connector Interface	ML-24-3

[1] Z = RoHS Compliant Part.
[2] Contact factory for more information.

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