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采购部

Digital Tri-Axial Vibration Sensor

ADIS16223

FEATURES

- **Tri-axial vibration sensing: ±70 *g* range**
- **Wide bandwidth: 14 kHz**
- **Programmable digital filters, low-pass/band-pass options**
- **Data capture function**
  - **3-channels, 1024 samples each, 72.9 kSPS sample rate**
- **Capture modes for managing machine life**
  - **Manual: early baseline characterization/validation**
  - **Automatic: periodic check for midlife performance shifts**
  - **Event: end-of-life monitoring for critical conditions**
  - **Extended: triple the record length for a single axis**
- **Digital temperature, power supply measurements**
- **Programmable operation and control**
  - **Capture mode and sample rate**
  - **I/O: data ready, alarm, capture trigger, general-purpose**
  - **Four alarm settings with threshold limits**
  - **Digitally activated self-test**
- **SPI-compatible serial interface**
- **Serial number and device ID**
- **Single-supply operation: 3.15 V to 3.6 V**
- **Operating temperature range: −40°C to +125°C**
- **15 mm × 15 mm × 15 mm package with flexible connector**

APPLICATIONS

- **Vibration analysis**
- **Shock detection and event capture**
- **Condition monitoring**
- **Machine health**
- **Instrumentation, diagnostics**
- **Safety, shutoff sensing**
- **Security sensing, tamper detection**

GENERAL DESCRIPTION

The ADIS16223 *i*Sensor® is a tri-axial, digital vibration sensor system that combines industry-leading *i*MEMS® sensing technology with signal processing, data capture, and a convenient serial peripheral interface (SPI). The SPI and data buffer structure provide convenient access to wide bandwidth sensor data. The 22 kHz sensor resonance and 72.9 kSPS sample rate provide a frequency response that is suitable for machine-health applications. The programmable digital filter offers low-pass and band-pass configuration options.

An internal clock drives the data sampling system during a data capture event, which eliminates the need for an external clock source. The data capture function has four different modes that offer several capture trigger options to meet the needs of many different applications.

The ADIS16223 also offers a digital temperature sensor, digital power supply measurements, and peak output capture.

The ADIS16223 is available in a 15 mm × 15 mm × 15 mm module with a threaded hole for stud mounting with a 10-32 UNF screw. The dual-row, 1 mm, 14-pin, flexible connector enables simple user interface and installation. It has an extended operating temperature range of −40°C to +125°C.

FUNCTIONAL BLOCK DIAGRAM

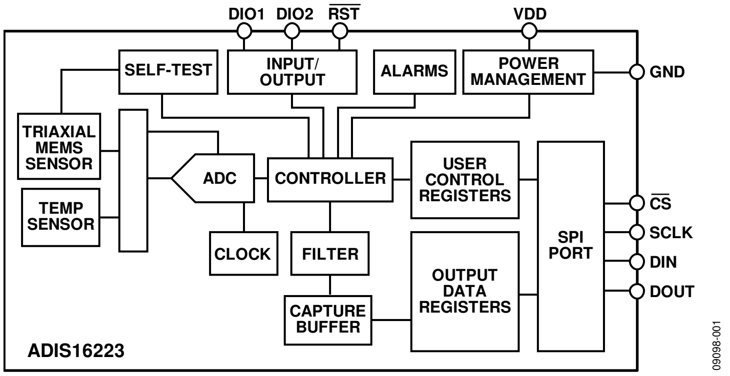

Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
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- ADIS16223 Daughter Board
- ADIS16ACL2 Breakout Board
- EVAL-ADIS2 Evaluation System

DOCUMENTATION

Data Sheet

- ADIS16223: Digital Tri-axial Vibration Sensor

DESIGN RESOURCES

- ADIS16223 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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REVISION HISTORY

6/10—Revision 0: Initial Version

SPECIFICATIONS

T_A = −40°C to +125°C, VDD = 3.3 V, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ACCELEROMETERS					
Measurement Range	T_A = 25°C	−70		+70	*g*
Sensitivity	T_A = 25°C		4.768		m*g*/LSB
Sensitivity Error	T_A = 25°C		±5		%
Nonlinearity	With respect to full scale		±0.2	±2	%
Cross Axis Sensitivity			2.6		%
Alignment Error	With respect to package		1.5		Degree
Offset Error	T_A = 25°C	−19.1		+19.1	*g*
Offset Temperature Coefficient			5		m*g*/°C
Output Noise	T_A = 25°C, Register AVG_CNT = 0x0000		477		m*g* rms
Output Noise Density	T_A = 25°C, 10 Hz to 1 kHz		3.3		m*g*/√Hz
Bandwidth	X/Y axes, ±5% flatness		7.75		kHz
	X/Y axes, ±10% flatness		9.0		kHz
	Z-axis, ±5% flatness		13		kHz
	Z-axis, ±10% flatness		14.25		kHz
Sensor Resonant Frequency			22		kHz
Self-Test Response		3669	5243	6815	LSB
LOGIC INPUTS[1]					
Input High Voltage, V_{INH}		2.0			V
Input Low Voltage, V_{INL}				0.8	V
Logic 1 Input Current, I_{INH}	V_{IH} = 3.3 V		±0.2	±1	µA
Logic 0 Input Current, I_{INL}	V_{IL} = 0 V				
All Except $\overline{\text{RST}}$			−40	−60	µA
$\overline{\text{RST}}$			−1		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[1]					
Output High Voltage, V_{OH}	I_{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1.6 mA			0.4	V
FLASH MEMORY					
Endurance[2]		10,000			Cycles
Data Retention[3]	T_J = 85°C	20			Years
START-UP TIME[4]					
Initial Startup			179		ms
Reset Recovery[5]	$\overline{\text{RST}}$ pulse low or Register GLOB_CMD[7] = 1		54		ms
Sleep Mode Recovery			2.5		ms
CONVERSION RATE	Register AVG_CNT = 0x0000		72.9		kSPS
Clock Accuracy			3		%
POWER SUPPLY	Operating voltage range, VDD	3.15	3.3	3.6	V
Power Supply Current	Capture mode, T_A = 25°C		43	52	mA
	Sleep mode, T_A = 25°C		230		µA

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[1] The digital I/O signals are 5 V tolerant.

[2] Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at −40°C, +25°C, +85°C, and +125°C.

[3] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22, Method A117. Retention lifetime decreases with junction temperature. See Figure 15.

[4] The start-up times presented do not include the data capture time, which is dependent on the AVG_CNT register settings.

[5] The $\overline{\text{RST}}$ pin must be held low for at least 15 ns.

TIMING SPECIFICATIONS

T_A = 25°C, VDD = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Description	Min[1]	Typ	Max	Unit
f_{SCLK}	SCLK frequency	0.01		2.25	MHz
t_{STALL}	Stall period between data, between 16th and 17th SCLK	15.4			μs
t_{CS}	Chip select to SCLK edge	48.8			ns
t_{DAV}	DOUT valid after SCLK edge			100	ns
t_{DSU}	DIN setup time before SCLK rising edge	24.4			ns
t_{DHD}	DIN hold time after SCLK rising edge	48.8			ns
t_{SR}	SCLK rise time			12.5	ns
t_{SF}	SCLK fall time			12.5	ns
t_{DF}, t_{DR}	DOUT rise/fall times		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	5			ns

[1] Guaranteed by design, not tested.

Timing Diagrams

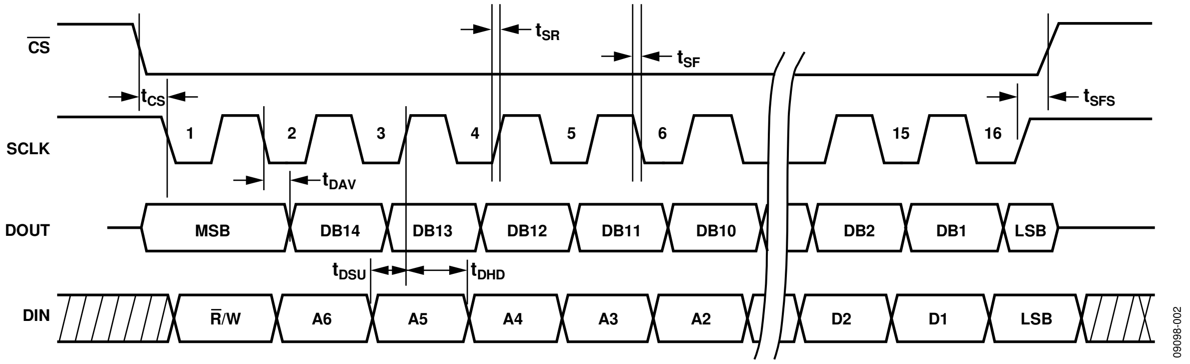


Figure 2. SPI Timing and Sequence

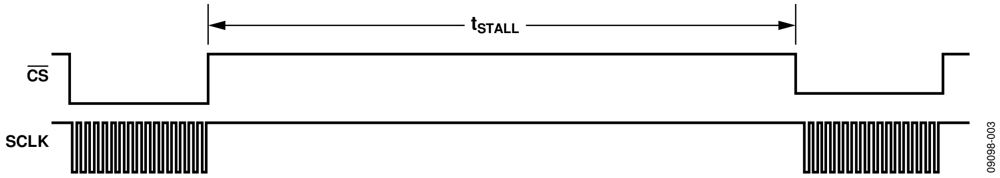


Figure 3. DIN Bit Sequence

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VDD to GND	−0.3 V to +6.0 V
Digital Input Voltage to GND	−0.3 V to +5.3 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.3 V
Analog Inputs to GND	−0.3 V to +3.6 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

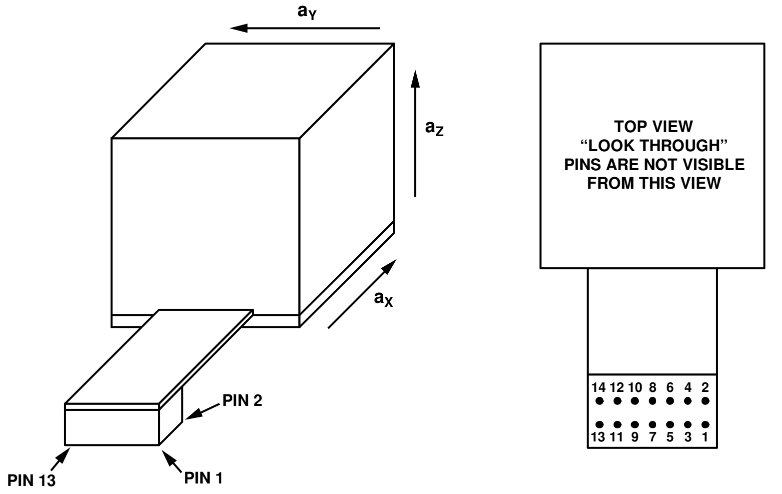
Table 4. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
14-Lead Module	31°C/W	11°C/W	6.5 grams

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



1. THE ARROWS ASSOCIATED WITH a_X, a_Y, AND a_Z DEFINE THE DIRECTION OF VELOCITY CHANGE THAT PRODUCES A POSITIVE OUTPUT IN ACCELERATION OUTPUT REGISTERS.
2. MATING CONNECTOR EXAMPLE: SAMTEC P/N CLM-107-02-LM-D-A.

Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1, 4, 9, 10	GND	S	Ground
2, 6	NC	I	No Connect
3	DIO2	I/O	Digital Input/Output Line 2
5	DIO1	I/O	Digital Input/Output Line 1
7	$\overline{\text{RST}}$	I	Reset, Active Low
8	VDD	S	Power Supply, 3.3 V
11	DIN	I	SPI, Data Input
12	DOUT	O[2]	SPI, Data Output
13	SCLK	I	SPI, Serial Clock
14	$\overline{\text{CS}}$	I	SPI, Chip Select

[1] S is supply, O is output, I is input, and I/O is input/output.

[2] DOUT is an output when $\overline{\text{CS}}$ is low. When $\overline{\text{CS}}$ is high, DOUT is in a three-state, high impedance mode.

THEORY OF OPERATION

The ADIS16223 is a tri-axial, wide bandwidth, digital acceleration sensor for vibration analysis. This sensing system collects data autonomously and makes it available to any processor system that supports a 4-wire serial peripheral interface (SPI).

SENSING ELEMENT

Digital vibration sensing in the ADIS16223 starts with a wide bandwidth MEMS accelerometer core on each axis, which provides a linear motion-to-electrical transducer function. Figure 5 provides a basic physical diagram of the sensing element and its response to linear acceleration. It uses a fixed frame and a moving frame to form a differential capacitance network that responds to linear acceleration. Tiny springs tether the moving frame to the fixed frame and govern the relationship between acceleration and physical displacement. A modulation signal on the moving plate feeds through each capacitive path into the fixed frame plates and into a demodulation circuit, which produces the electrical signal that is proportional to the acceleration acting on the device.

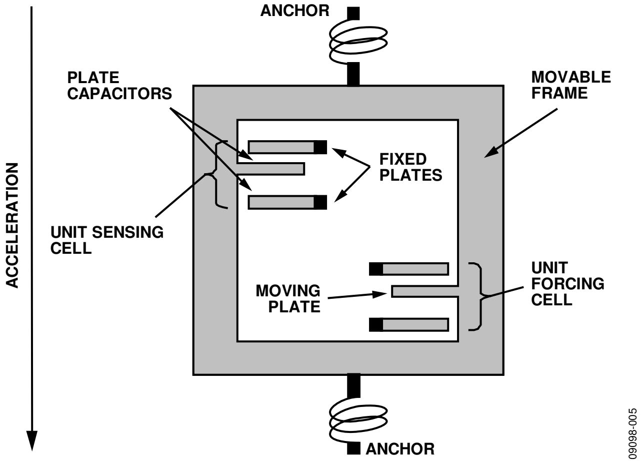


Figure 5. MEMS Sensor Diagram

DATA SAMPLING AND PROCESSING

The analog acceleration signal from each sensor feeds into an analog-to-digital (ADC) converter stage, which passes digitized data into the controller. The controller processes the acceleration data, stores it in the capture buffer, and manages access to it using the SPI/register user interface. Processing options include offset adjustment, filtering, and checking for preset alarm conditions.

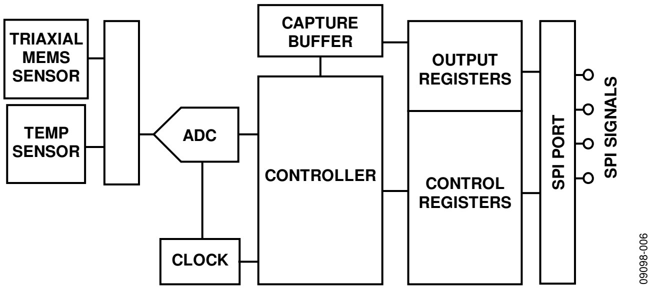


Figure 6. Simplified Sensor Signal Processing Diagram

USER INTERFACE

SPI Interface

The user registers manage user access to both sensor data and configuration inputs. Each 16-bit register has its own unique bit assignment and two addresses: one for its upper byte and one for its lower byte. Table 8 provides a memory map for each register, along with its function and lower byte address. Each data collection and configuration command both use the SPI, which consists of four wires. The chip select ($\overline{\text{CS}}$) signal activates the SPI interface and the serial clock (SCLK) synchronizes the serial data lines. Input commands clock into the DIN pin, one bit at a time, on the SCLK rising edge. Output data clocks out of the DOUT pin on the SCLK falling edge. As a SPI slave device, the DOUT contents reflect the information requested using a DIN command.

Dual Memory Structure

The user registers provide addressing for all input/output operations on the SPI interface. The control registers use a dual memory structure. The SRAM controls operation while the part is on and facilitates all user configuration inputs. The flash memory provides nonvolatile storage for control registers that have flash backup (see Table 8). Storing configuration data in the flash memory requires a manual, flash update command (GLOB_CMD[12] = 1, DIN = 0xBF10). When the device powers on or resets, the flash memory contents load into the SRAM, and then the device starts producing data according to the configuration in the control registers.

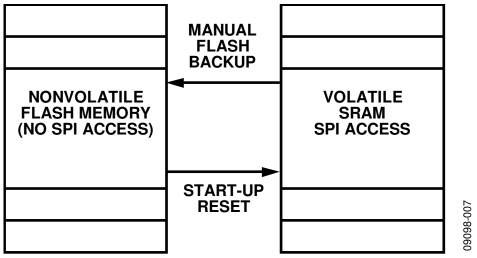


Figure 7. SRAM and Flash Memory Diagram

BASIC OPERATION

The ADIS16223 uses a SPI for communication, which enables a simple connection with a compatible, embedded processor platform, as shown in Figure 8. The factory default configuration for DIO1 provides a busy indicator signal that transitions low when a capture event completes and data is available for user access. Use the DIO_CTRL register in Table 28 to reconfigure DIO1 and DIO2, if necessary.

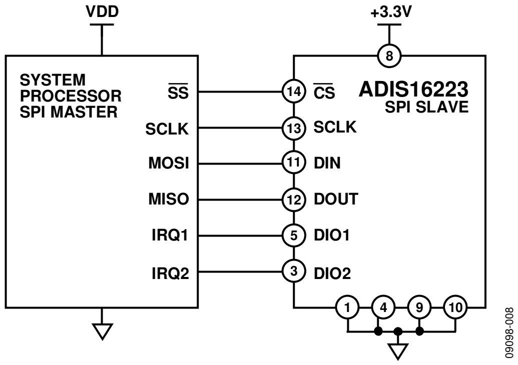


Figure 8. Electrical Hook-Up Diagram

Table 6. Generic Master Processor Pin Names and Functions

Pin Name	Function
$\overline{\text{SS}}$	Slave select
IRQ1, IRQ2	Interrupt request inputs (optional)
MOSI	Master output, slave input
MISO	Master input, slave output
SCLK	Serial clock

The ADIS16223 SPI interface supports full duplex serial communication (simultaneous transmit and receive) and uses the bit sequence shown in Figure 12. Table 7 provides a list of the most common settings that require attention to initialize a processor's serial port for the ADIS16223 SPI interface.

Table 7. Generic Master Processor SPI Settings

Processor Setting	Description
Master	ADIS16223 operates as a slave
SCLK Rate ≤ 2.25 MHz	Bit rate setting
SPI Mode 3	Clock polarity/phase (CPOL = 1, CPHA = 1)
MSB-First	Bit sequence
16-Bit	Shift register/data length

Table 8 provides a list of user registers with their lower byte addresses. Each register consists of two bytes that each have its own, unique 6-bit address. Figure 9 relates each register's bits to their upper and lower addresses.

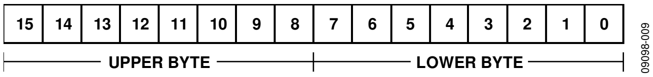


Figure 9. Generic Register Bit Definitions

SPI WRITE COMMANDS

User control registers govern many internal operations. The DIN bit sequence in Figure 12 provides the ability to write to these registers, one byte at a time. Some configuration changes and functions only require one write cycle. For example, set GLOB_CMD[11] = 1 (DIN = 0xBF08) to start a manual capture sequence. The manual capture starts immediately after the last bit clocks into DIN (16th SCLK rising edge). Other configurations may require writing to both bytes.

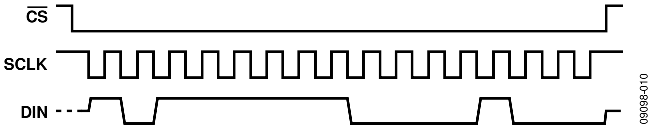


Figure 10. SPI Sequence for Manual Capture Start (DIN = 0xBF08)

SPI READ COMMANDS

A single register read requires two 16-bit SPI cycles that also use the bit assignments in Figure 12. The first sequence sets $\overline{\text{R}}$/W = 0 and communicates the target address (Bits[A6:A0]). Bits[D7:D0] are don't care bits for a read DIN sequence. DOUT clocks out the requested register contents during the second sequence. The second sequence can also use DIN to setup the next read. Figure 11 provides a signal diagram for all four SPI signals while reading the x-axis acceleration capture buffer (CAPT_BUFFX) in a repeating pattern. In this diagram, DIN = 0x1400 and DOUT reflects the CAPT_BUFFX register contents from the previous DIN read-request sequence.

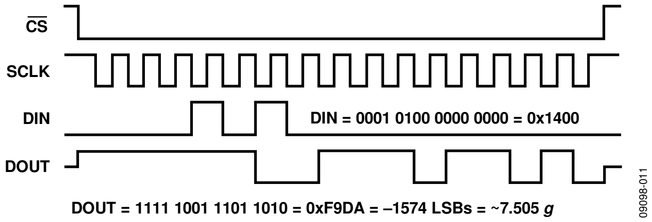
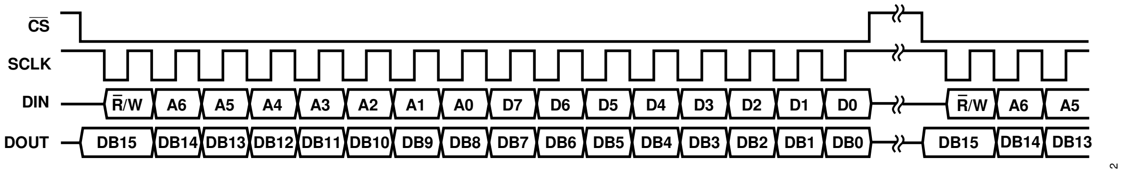


Figure 11. Example SPI Read, Second 16-Bit Sequence



NOTES
1. DOUT BITS ARE BASED ON THE PREVIOUS 16-BIT SEQUENCE ($\overline{\text{R}}$/W = 0).

Figure 12. Example SPI Read Sequence

Note that all registers in Table 8 consist of two bytes. All unused memory locations are reserved for future use.

Table 8. User Register Memory Map[1]

Register Name	Access	Flash Backup	Address[2]	Default	Function	Reference
FLASH_CNT	Read only	Yes	0x00	N/A	Status, flash memory write count	Table 35
NULL_X	Read/write	Yes	0x02	0x0000	Control, x-axis accelerometer offset correction	Table 40
NULL_Y	Read/write	Yes	0x04	0x0000	Control, y-axis accelerometer offset correction	Table 40
NULL_Z	Read/write	Yes	0x06	0x0000	Control, z-axis accelerometer offset correction	Table 40
Reserved	N/A	N/A	0x08 to 0x09	N/A	Reserved	N/A
CAPT_SUPPLY[3]	Read only	Yes	0x0A	0x8000	Output, power supply during capture	Table 10
CAPT_TEMP[3]	Read only	Yes	0x0C	0x8000	Output, temperature during capture	Table 10
CAPT_PEAKX[3]	Read only	Yes	0x0E	0x8000	Output, peak x-axis acceleration during capture	Table 10
CAPT_PEAKY[3]	Read only	Yes	0x10	0x8000	Output, peak y-axis acceleration during capture	Table 10
CAPT_PEAKZ[3]	Read only	Yes	0x12	0x8000	Output, peak z-axis acceleration during capture	Table 10
CAPT_BUFFX[3]	Read only	No	0x14	0x8000	Output, capture buffer for x-axis acceleration	Table 10
CAPT_BUFFY[3]	Read only	No	0x16	0x8000	Output, capture buffer for y-axis acceleration	Table 10
CAPT_BUFFZ[3]	Read only	No	0x18	0x8000	Output, capture buffer for z-axis acceleration	Table 10
CAPT_PNTR	Read/write	No	0x1A	0x0000	Control, capture buffer address pointer	Table 9
CAPT_CTRL	Read/write	Yes	0x1C	0x0020	Control, capture control register	Table 15
CAPT_PRD	Read/write	Yes	0x1E	0x0000	Control, capture period (automatic mode)	Table 17
ALM_MAGX	Read/write	Yes	0x20	0x0000	Alarm, trigger setting, x-axis acceleration	Table 22
ALM_MAGY	Read/write	Yes	0x22	0x0000	Alarm, trigger setting, y-axis acceleration	Table 22
ALM_MAGZ	Read/write	Yes	0x24	0x0000	Alarm, trigger setting, z-axis acceleration	Table 22
ALM_MAGS	Read/write	Yes	0x26	0x0000	Alarm, trigger setting, system	Table 23
ALM_CTRL	Read/write	Yes	0x28	0x0000	Alarm, control register	Table 21
Reserved	N/A	N/A	0x2A to 0x31	N/A	Reserved	N/A
GPIO_CTRL	Read/write	Yes	0x32	0x0000	Control, general-purpose I/O configuration	Table 29
MSC_CTRL	Read/write	No	0x34	0x0000	Control, manual self-test	Table 31
DIO_CTRL	Read/write	Yes	0x36	0x000F	Control, functional I/O configuration	Table 28
AVG_CNT	Read/write	Yes	0x38	0x0000	Control, low-pass filter (number of averages)	Table 37
Reserved	N/A	N/A	0x3A to 0x3B	N/A	Reserved	N/A
DIAG_STAT	Read only	Yes	0x3C	0x0000	Status, system error flags	Table 30
GLOB_CMD	Write only	No	0x3E	N/A	Control, global command register	Table 27
Reserved	N/A	N/A	0x40 to 0x51	N/A	Reserved	N/A
LOT_ID1	Read only	Yes	0x52	N/A	Lot identification code	Table 32
LOT_ID2	Read only	Yes	0x54	N/A	Lot identification code	Table 32
PROD_ID	Read only	Yes	0x56	0x3F5F	Product identifier; convert to decimal = 16,223	Table 33
SERIAL_NUM	Read only	Yes	0x58	N/A	Serial number	Table 34

[1] N/A is not applicable.
[2] Each register contains two bytes. The address of the lower byte is displayed. The address of the upper byte is equal to the address of the lower byte, plus 1.
[3] The default value in this register indicates that a no capture event has occurred.

DATA COLLECTION

The ADIS16223 samples and stores acceleration (vibration) data using capture events. A capture event involves several sampling/processing operations, as shown in Figure 13. First, the ADIS16223 produces and stores 1024 samples of acceleration data into the capture buffers. Second, the capture event takes a 5.12 ms record of power supply measurements at a sample rate of 50 kHz and loads the average of this record into the CAPT_SUPPLY register. Third, the capture event takes 64 samples of internal temperature data over a period of 1.7 ms and loads the average of this record into the CAPT_TEMP register.

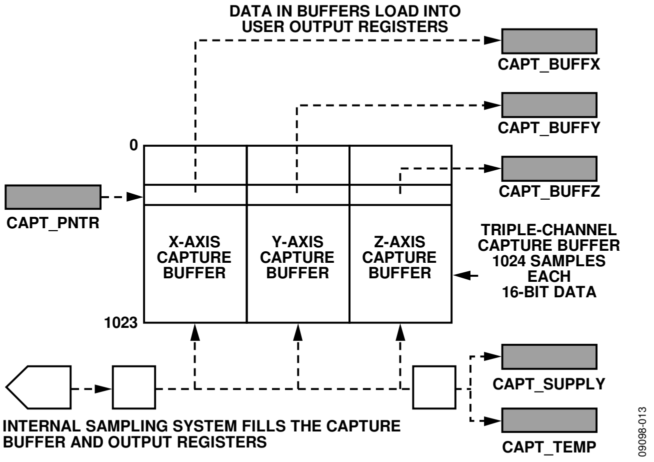


Figure 13. Capture Buffer Structure and Operation

READING DATA FROM THE CAPTURE BUFFER

When a capture is complete, the first data samples load into the CAPT_BUFFx registers and 0x0000 loads into the index pointer (CAPT_PNTR). The index pointer determines which data samples load into the CAPT_BUFFx registers. For example, writing 0x0138 to the CAPT_PNTR register (DIN = 0x9A38, DIN = 0x9B01) causes the 313th sample in each buffer memory to load into the CAPT_BUFFx registers.

Table 9. CAPT_PNTR Bits Descriptions

Bits	Description (Default = 0x0000)
[15:10]	Reserved
[9:0]	Data bits

The index pointer increments with every CAPT_BUFFx read command, which causes the next set of capture data to load into each capture buffer register, automatically.

OUTPUT DATA REGISTERS

The ADIS16223 output registers provide access to the following data taken during a capture event: acceleration data, peak acceleration data, power supply, and internal temperature. Table 10 provides a list of the output data and pointer registers, along with their lower byte addresses.

Table 10. Output Data/User Access Register Summary

Register Name	Lower Byte Address	Measurement	Format
CAPT_SUPPLY	0x0A	Power supply	Table 12
CAPT_TEMP	0x0C	Internal temperature	Table 13
CAPT_PEAKX	0x0E	Peak acceleration, X	Table 11
CAPT_PEAKY	0x10	Peak acceleration, Y	Table 11
CAPT_PEAKZ	0x12	Peak acceleration, Z	Table 11
CAPT_BUFFX	0x14	Acceleration, X	Table 11
CAPT_BUFFY	0x16	Acceleration, Y	Table 11
CAPT_BUFFZ	0x18	Acceleration, Z	Table 11
CAPT_PNTR	0x1A	Capture data pointer	Table 9

Output Data Format

The acceleration and peak acceleration output registers use a 16-bit, twos complement digital format, with a bit weight of 4.768 m*g*/LSB. The CAPT_PEAKx registers reflect the largest deviation from 0 *g*, assuming zero offset error, and can be either negative or positive. The CAPT_SUPPLY and CAPT_TEMP use a 12-bit, offset-binary digital format, with bit weights of +1.2207 mV/LSB and −0.47°C/LSB, respectively.

Output Data Format Examples

Table 11, Table 12, and Table 13 provide numerous digital coding examples for each output register data format.

Table 11. Acceleration Data Format Examples

Acceleration (*g*)	LSB	Hex	Binary
+70	+14681	0x3959	0011 1001 0101 1001
+1	+210	0x00D2	0000 0000 1101 0010
+0.004768	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−0.004768	−1	0xFFFF	1111 1111 1111 1111
−1	−210	0xFF2E	1111 1111 0010 1110
−70	−14681	0xC6A7	1100 0110 1010 0111

Table 12. Power Supply Data Format Examples

Supply Level (V)	LSB	Hex	Binary
3.6	2949	0xB85	1011 1000 0101
3.3 + 0.0012207	2704	0xA90	1010 1001 0000
3.3	2703	0xA8F	1010 1000 1111
3.3 – 0.0012207	2702	0xA8E	1010 1000 1110
3.15	2580	0xA14	1010 0001 0100

Table 13. Internal Temperature Data Format Examples

Temperature (°C)	LSB	Hex	Binary
125	1065	0x429	0100 0010 1001
25 + 0.47	1277	0x4FD	0100 1111 1101
25	1278	0x4FE	0100 1111 1110
25 – 0.047	1279	0x4FF	0100 1111 1111
0	1331	0x533	0101 0011 0011
−40	1416	0x588	0101 1000 1000

CAPTURE/ALARM CONFIGURATION

Table 14 provides a list of the control registers for the user configuration of the capture function. The address column in Table 14 represents the lower byte address for each register.

Table 14. Capture Configuration Register Summary

Register Name	Lower Byte Address	Description
CAPT_CTRL	0x1C	Capture configuration
CAPT_PRD	0x1E	Capture period (automatic mode)
ALM_MAGX	0x20	X-axis alarm threshold (event mode)
ALM_MAGY	0x22	Y-axis alarm threshold (event mode)
ALM_MAGZ	0x24	Z-axis alarm threshold (event mode)
ALM_S_MAG	0x26	System alarm
ALM_CTRL	0x28	Alarm control (event)
DIO_CTRL	0x36	Digital I/O configuration
GLOB_CMD	0x3E	Capture commands

The CAPT_CTRL register in Table 15 provides the primary user control for capture mode configuration. It provides four different modes of capture: manual, automatic, event, and extended. Configure the mode by writing to the CAPT_CTRL register, then use either GLOB_CMD[11] (see Table 27) or one of the digital I/O lines (DIO1 or DIO2) as a manual trigger to start operation. Use the DIO_CTRL register in Table 28 to configure either DIO1 or DIO2 as a manual trigger input line. The manual trigger can also stop a capture event that is processing and return the device to an idle state.

Table 15. CAPT_CTRL Bit Descriptions

Bits	Description (Default = 0x0020)
[15:10]	Reserved
[9:8]	Extended mode channel selection 00 = x-axis 01 = y-axis 10 = z-axis 11 = reserved
[7]	Band-pass filter, 1 = enabled
[6]	Automatically store capture buffers to flash upon alarm trigger, 1 = enabled
[5:4]	Pre-event capture length for event mode 00 = 64 samples 01 = 128 samples 10 = 256 samples 11 = 512 samples
[3:2]	Capture mode 00 = manual 01 = automatic 10 = event 11 = extended
[1]	Power-down between capture events, 1 = enabled
[0]	Reserved

MANUAL MODE

Table 16 provides an example configuration sequence for manual mode. When using the factory default configuration, the first step in this example is unnecessary. Use the manual trigger to start the data capture process.

Table 16. Manual Mode Configuration Example

DIN	Description
0x9C00	Set CAPT_CTRL[7:0] = 0x00 to select manual mode
0xBF08	Set GLOB_CMD[11] = 1 to start the data capture

AUTOMATIC MODE

Table 18 provides a configuration example for automatic mode, where the manual trigger results in a data capture and then begins a countdown sequence to start another data capture. This example also uses the option for shutting down the device to save power after the data capture completes. The CAPT_PRD register in Table 17 provides users with the ability to establish the countdown time in automatic mode.

Table 17. CAPT_PRD Register Bit Descriptions

Bits	Description (Default = 0x0000)
[15:10]	Reserved
[9:8]	Scale for data bits 00 = 1 second/LSB 01 = 1 minute/LSB 10 = 1 hour/LSB
[7:0]	Data bits, binary format

Table 18. Automatic Mode Configuration Example

DIN	Description
0x9F02 0x9E18	Set CAPT_PRD[15:8] = 0x02 to set time scale to hours Set CAPT_PRD[7:0] = 0x18 to set the period to 24 hours
0x9C06	Set CAPT_CTRL[7:0] = 0x06 to select automatic trigger mode and enable shutdown in between captures
0xBF08	Set GLOB_CMD[11] = 1 to execute a capture, shut down, and begin the 24-hour countdown for the next capture

EVENT MODE

In event mode, the manual trigger initiates the pre-event capture process that continuously samples data, monitors for the alarm trigger settings, and stores it in a circular buffer. CAPT_CTRL[5:4] establishes the circular buffer size as the pre-event capture length. When the data in the circular buffer exceeds one of the alarm's trigger settings, the remaining portion of the capture buffer fills up with post event data. Table 19 provides an example configuration sequence for this mode that sets all three acceleration alarms to trip when the magnitude exceeds ±20 *g*.

Table 19. Event Mode Configuration Example

DIN	Description
0xA063	Set ALM_MAGX = 0x1063, trigger threshold = ±20 *g*, 20 *g* ÷ 4.768 m*g*/LSB = 4195, LSB = 0x1063
0xA110	
0xA263	Set ALM_MAG Y = 0x1063, trigger threshold = ±20 *g*, 20 *g* ÷ 4.768 m*g*/LSB = 4195, LSB = 0x1063
0xA310	
0xA463	Set ALM_MAGZ = 0x1063, trigger threshold = ±20 *g*, 20 *g* ÷ 4.768 m*g*/LSB = 4195, LSB = 0x1063
0xA510	
0xA807	Set ALM_CTRL[2:0] = 0x07 to enable ALM_MAGX, ALM_MAGY, and ALM_MAGZ triggers
0xB61F	Set DIO_CTRL[7:0] = 0x1F to set DIO1 as a positive busy indicator and DIO2 as a positive alarm indicator
0x9C58	Set CAPT_CTRL[7:0] = 0x58 to select event mode, enable automatic capture store to flash and set the pre-event capture length to 128 samples
0xBF08	Set GLOB_CMD[11] = 1 to start the process of monitoring data for > +20 *g* or < −20 *g* (preset alarm trigger settings)

EXTENDED MODE

The extended capture mode option operates the same as the manual mode, except that it uses the three capture buffers for one axis of acceleration data. This 3× increase in the number of samples provides up to 4.5 dB improvement in the noise floor for applications that use FFT analysis techniques. In this mode, the x-axis capture buffer contains the first 1024 samples, the y-axis capture buffer contains the second 1024 samples, and the z-axis capture buffer contains the third 1024 samples. Set CAPT_CTRL[3:2] = 11 (DIN = 0x9C0C) to select extended mode, and use CAPT_CTRL[9:8] to select the accelerometer axis for this purpose.

POWER-DOWN CONTROL

Set CAPT_CTRL[1] = 1 (DIN = 0x9C02) to configure the ADIS16223 to go into sleep mode after a data capture event. Once the device shuts down and is in sleep mode, lowering the $\overline{CS}$ pin wakes it up. See Table 28 and Figure 14 for more information on the digital trigger input option that can also wake the device up from sleep mode. Allow at least 2.5 ms for the device to recover from sleep mode before trying to communicate with the SPI interface. Attempts to write to the DIN pin (lower $\overline{CS}$) during this time can cause invalid data. If this happens, raise $\overline{CS}$ high, and then lower it again to start collecting valid data. After the device recovers from sleep mode, it remains awake until after the next capture or until the device is manually put back to sleep. When data is extracted after a capture, the user can command the device to go back to sleep by setting GLOB_CMD[1] = 1 (DIN = 0xBE02). When waking multiple devices, $\overline{CS}$ must occur at different times to avoid conflicts on the DOUT line.

AUTOMATIC FLASH BACK-UP CONTROL

CAPT_CTRL[6] provides a flash based back-up function for capture data. When CAPT_CTRL[6] = 1, the capture buffer automatically loads into a mirror location in nonvolatile flash, immediately after the data capture sequence. Set GLOB_CMD[13] = 1 (DIN = 0xBF20) to recover this data from the flash memory back into the capture buffers.

CAPTURE TIMES

The capture time is dependent on two settings:

- the average count per sample setting in the AVG_CNT register (see Table 37)
- the flash back-up setting in CAPT_CTRL[6]:
  no flash: CAPT_CTRL[6] = 0
  with flash: CAPT_CTRL[6] = 1 (see Table 15)

Use the following equations to estimate capture times (t_C):

$$t_C = 0.014 + \frac{1}{70{,}700} \times 1024 \times 2^{AVG\_CNT} \text{ (no flash)}$$

$$t_C = 0.516 + \frac{1}{70{,}700} \times 1024 \times 2^{AVG\_CNT} \text{ (with flash)}$$

ALARMS

Table 20 provides a list of the control registers for the user configuration of the alarm function. The address column in Table 20 represents the lower byte address for each register.

Table 20. Alarm Configuration Register Summary

Register Name	Lower Byte Address	Description
CAPT_CTRL	0x1C	Capture configuration
CAPT_PRD	0x1E	Capture period (automatic mode)
ALM_MAGX	0x20	X-axis alarm threshold (event mode)
ALM_MAGY	0x22	Y-axis alarm threshold (event mode)
ALM_MAGZ	0x24	Z-axis alarm threshold (event mode)
ALM_S_MAG	0x26	System alarm
ALM_CTRL	0x28	Alarm control (event)
DIO_CTRL	0x36	Digital I/O configuration
GLOB_CMD	0x3E	Capture commands

The ALM_CTRL register provides on/off controls for four alarms that monitor all three accelerometers and a system alarm for monitoring either temperature or power supply. ALM_CTRL[5] provides a polarity control for the system alarm, whereas the accelerometer alarms do not require this.

Table 22 provides the bit assignment for ALM_MAGX, ALM_MAGY, and ALM_MAGZ, which use the same data format as the acceleration data registers (see Table 11). Table 23 provides the bit assignments for the system alarm, ALM_MAGS, which uses the same data format as the data source selection in ALM_CTRL[4]. ALM_MAGS can use either the power supply (see Table 12) or internal temperature register (see Table 13) formatting. All four alarms have error flags in DIAG_STAT[11:8] See Table 30 for more details on the conditions required to set an error flag to 1, which indicates an alarm state.

Table 21. ALM_CTRL Bit Descriptions

Bits	Description (Default = 0x0000)
[15:6]	Reserved
[5]	System alarm comparison polarity 1 = trigger when less than ALM_MAGS[11:0] 0 = trigger when greater than ALM_MAGS[11:0]
[4]	System alarm, 1 = temperature 0 = power supply
[3]	Alarm S enable (ALM_MAGS), 1 = enabled, 0 = disabled
[2]	Alarm Z enable (ALM_MAGZ), 1 = enabled, 0 = disabled
[1]	Alarm Y enable (ALM_MAGY), 1 = enabled, 0 = disabled
[0]	Alarm X enable (ALM_MAGZ), 1 = enabled, 0 = disabled

Table 22. ALM_MAGX, ALM_MAGY, and ALM_MAGZ

Bits	Description (Default = 0x0000)
[15:0]	Data bits for acceleration threshold setting; twos complement, 4.768 m*g*/LSB.

Table 23. ALM_MAGS Bit Descriptions

Bits	Description (Default = 0x0000)
[15:12]	Reserved.
[11:0]	Data bits for temperature or supply threshold setting. Binary format matches CAPT_TEMP or CAPT_SUPPLY format, depending on the ALM_CTRL[4] setting.

Table 24 and Table 25 provide configuration examples for using the ALM_CTRL and ALM_MAG to configure the system alarm function.

Table 24. System Alarm Configuration Example 1

DIN	Description
0xA808	Set ALM_CTRL[7:0] = 0x08 to set system alarm for a power supply too high condition.
0xA70B 0xA60A	Set ALM_MAGS = 0x0B0A for a trigger setting of 3.45 V. 3.45 V ÷ 0.0012207 = 2826 LSB = 0x0B0A. See Table 12 for more details on calculating digital codes for power supply measurements.

Table 25. System Alarm Configuration Example 2

DIN	Description
0xA838	Set ALM_CTRL[7:0] = 0x38 to set system alarm for a temperature too low condition.
0xA705 0xA673	Set ALM_MAGS = 0x0573 for a trigger setting of −30°C. For a temperature trigger setting of −30°C, use the sensitivity of −0.47°C/LSB and the reference TEMP_OUT reading for +25°C of 1278.

Use the following steps to calculate the settings for ALM_MAGS shown in Table 25:

1. T = −30°C.
2. ΔT = −30°C − 25°C = −55°C.
3. ΔLSB = −55°C ÷ −0.47°C/LSB = +117 LSB.
4. ALM_MAGS = 117 LSB + 1278 LSB (25°C setting).
5. ALM_MAGS = 1395 LSB (decimal)
6. ALM_MAGS = 0x0573 (hexadecimal)

See Table 13 for more details on calculating digital codes for internal temperature measurements.

SYSTEM TOOLS

Table 26 provides an overview of the control registers that provide support for the following system level functions: global commands, I/O control, status/error flags, device identification, MEMS self-test, and flash memory management.

Table 26. System Tool Register Addresses

Register Name	Address	Description
FLSH_CNT	0x00	Flash write cycle count
GPIO_CTRL	0x32	General-purpose I/O control
MSC_CTRL	0x34	Manual self-test controls
DIO_CTRL	0x36	Digital I/O configuration
DIAG_STAT	0x3C	Status, error flags
GLOB_CMD	0x3E	Global commands
LOT_ID1	0x52	Lot Identification Code 1
LOT_ID2	0x54	Lot Identification Code 2
PROD_ID	0x56	Product identification
SERIAL_NUM	0x58	Serial number

GLOBAL COMMANDS

The GLOB_CMD register provides an array of single-write commands for convenience. Setting the assigned bit in Table 27 to 1 activates each function. When the function completes, the bit restores itself to 0. For example, clear the capture buffers by setting GLOB_CMD[8] = 1 (DIN = 0xBF01). All of the commands in the GLOB_CMD register require the power supply to be within normal limits for the execution times listed in Table 27. Avoid communicating with the SPI interface during these execution times because it interrupts the process and causes data loss or corruption.

Table 27. GLOB_CMD Bit Descriptions

Bits	Description	Execution Time[1]
[15:14]	Reserved	Not applicable
[13]	Restore capture data and settings from flash memory	0.98 ms (no capture), 7.0 ms (with capture)
[12]	Copy capture data and settings to flash memory	339 ms (no capture), 509 (with capture)
[11]	Capture mode start/stop	Not applicable
[10]	Set CAPT_PNTR = 0x0000	0.035 ms
[9]	Reserved	Not applicable
[8]	Clear capture buffers	0.84 ms
[7]	Software reset	54 ms
[6]	Reserved	Not applicable
[5]	Flash test, compare sum of flash memory with factory value	10.5 ms
[4]	Clear DIAG_STAT register	0.035 ms
[3]	Restore factory register settings and clear the capture buffers	339 ms
[2]	Self-test, result in DIAG_STAT[5]	33 ms
[1]	Power-down	Not applicable
[0]	Autonull	936 ms

[1] This indicates the typical duration of time between the command write and the device returning to normal operation.

INPUT/OUTPUT FUNCTIONS

The DIO_CTRL register in Table 28 provides configuration control options for the two digital I/O lines.

Busy Indicator

The busy indicator is an output signal that indicates internal processor activity. This signal is active during data capture events, register write cycles, or internal processing, such as the functions in Table 27. The factory default setting for DIO_CTRL sets DIO1 as a positive, active high, busy indicator signal. When configured in this manner, use this signal to alert the master processor to read data from capture buffers.

Capture Trigger

The capture trigger function provides an input pin for starting trigger modes and capture events with a signal pulse. Set DIO_CTRL[7:0] = 0x2F (DIN = 0xB62F) to configure DIO2 as a positive trigger input and keep DIO1 as a busy indicator. To start a trigger, the trigger input signal must transition from low to high and then from high to low. The capture process starts on the high-to-low transition, as shown in Figure 14, and the pulse duration must be at least 2.6 µs to result in a trigger.

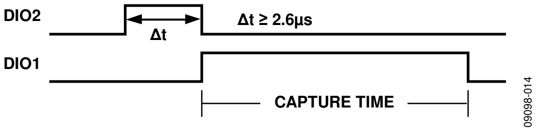


Figure 14. Manual Trigger/Busy Indicator Sequence Example

Alarm Indicator

Set DIO_CTRL[7:0] = 0x1F (DIN = 0xB61F) to configure DIO2 as an alarm indicator with an active high polarity. The alarm indicator transitions to its active state when the acceleration or system data exceeds the threshold settings in the ALM_MAGx registers. Set GLOB_CMD[4] = 1 (DIN = 0xBF10) to clear the DIAG_STAT error flags and restore the alarm indicator to its inactive state.

Table 28. DIO_CTRL Bit Descriptions

Bits	Description (Default = 0x000F)
[15:6]	Reserved
[5:4]	DIO2 function selection 00 = general-purpose I/O (use GPIO_CTRL) 01 = alarm indicator output (per ALM_CTRL) 10 = capture trigger input 11 = busy indicator output
[3:2]	DIO1 function selection 00 = general-purpose I/O (use GPIO_CTRL) 01 = alarm indicator output (per ALM_CTRL) 10 = capture trigger input 11 = busy indicator output
[1]	DIO2 line polarity; if [5:4] = 00, see GPIO_CTRL in Table 29 1 = active high 0 = active low
[0]	DIO1 line polarity; if [3:2] = 00, see GPIO_CTRL in Table 29 1 = active high 0 = active low

General Purpose I/O

If DIO_CTRL configures either DIO1 or DIO2 as a general-purpose digital line, use the GPIO_CTRL register in Table 29 to configure its input/output direction, set the output level when configured as an output, and monitor the status of an input.

Table 29. GPIO_CTRL Bit Descriptions

Bits	Description (Default = 0x0000)
[15:10]	Reserved
[9]	DIO2 output level 1 = high 0 = low
[8]	DIO1 output level 1 = high 0 = low
[7:2]	Reserved
[1]	DIO2 direction control 1 = output 0 = input
[0]	DIO1 direction control 1 = output 0 = input

Status/Error Flags

The DIAG_STAT register, in Table 30, provides a number of status/error flags that reflect the conditions observed during a capture, during SPI communication and diagnostic tests. A 1 indicates an error condition and all of the error flags are sticky, which means that they remain until they are reset by setting GLOB_CMD[4] = 1 (DIN = 0xBE10) or by starting a new capture event. DIAG_STAT[14:12], indicate the source of an event capture trigger. DIAG_STAT[11:8], indicate which ALM_MAGx thresholds were exceeded during a capture event. The capture period violation flag in DIAG_STAT[4] indicates user-driven SPI use while the most recent capture sequence was in progress. The flag in Register DIAG_STAT[3] indicates that the total number of SCLK clocks is not a multiple of 16.

Table 30. DIAG_STAT Bit Descriptions

Bits	Description (Default = 0x0000)
[15]	Reserved
[14]	Alarm Z, event-mode trigger indicator
[13]	Alarm Y, event-mode trigger indicator
[12]	Alarm X, event-mode trigger indicator
[11]	Alarm S, capture supply/temperature data > ALM_MAGS
[10]	Alarm Z, captured acceleration data > |ALM_MAGZ|
[9]	Alarm Y, captured acceleration data > |ALM_MAGY|
[8]	Alarm X, captured acceleration data > |ALM_MAGX|
[7]	Data ready, capture complete
[6]	Flash test result, checksum flag
[5]	Self-test diagnostic error flag
[4]	Capture period violation/interruption
[3]	SPI communications failure
[2]	Flash update failure
[1]	Power supply above 3.625 V
[0]	Power supply below 3.125 V

SELF-TEST

Set GLOB_CMD[2] = 1 (DIN = 0xBE02) to run an automatic self-test routine, which reports a pass/fail result to DIAG_STAT[5]. Set MSC_CTRL[8] = 1 (DIN = 0xB501) to manually activate the self-test function for all three axes, which results in an offset shift in captured accelerometer data. Compare this offset shift with the self-test response specification in Table 1. If the offset shift is inside of this specification, then the device is functional.

Table 31. MSC_CTRL Bit Descriptions

Bits	Description (Default = 0x0000)
[15:9]	Reserved
[8]	Manual self-test, 1: enabled
[7:0]	Reserved

DEVICE IDENTIFICATION

Table 32. LOT_ID1 and LOT_ID2 Bit Descriptions

Bits	Description
[15:0]	Lot identification code

Table 33. PROD_ID Bit Descriptions

Bits	Description
[15:0]	0x3F5F = 16,223

Table 34. SERIAL_NUM Bit Descriptions

Bits	Description
[15:0]	Serial number, lot specific

FLASH MEMORY MANAGEMENT

Set GLOB_CMD[5] = 1 (DIN = 0xBE20) to run an internal checksum test on the flash memory, which reports a pass/fail result to DIAG_STAT[6]. The FLASH_CNT register (see Table 35) provides a running count of flash memory write cycles. This is a tool for managing the endurance of the flash memory. Figure 15 quantifies the relationship between data retention and junction temperature.

Table 35. FLASH_CNT Bit Descriptions

Bits	Description
[15:0]	Binary counter for writing to flash memory

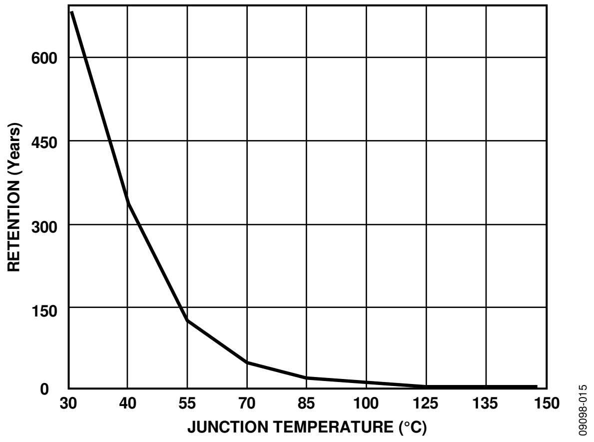


Figure 15. Flash/EE Memory Data Retention

DIGITAL SIGNAL PROCESSING

Figure 16 provides a block diagram of the sensor signal processing, and Table 36 provides a summary of the registers that control the low-pass filter, band-pass filter, and offset correction.

Table 36. Digital Signal Processing Register Summary

Register Name	Address	Description
NULL_X	0x02	Offset correction, X
NULL_Y	0x04	Offset correction, Y
NULL_Z	0x06	Offset correction, Z
CAPT_CTRL	0x1C	Band-pass filter enable
AVG_CNT	0x38	Low-pass filter, output sample rate
GLOB_CMD	0x3E	Autonull offset correction

LOW-PASS FILTER

The AVG_CNT register in Table 37 determines the rate at which the low-pass filter averages and decimates acceleration data. Table 38 provides the performance trade-offs associated with each setting.

Table 37. AVG_CNT Bit Descriptions

Bits	Description (Default = 0x0000)
[15:4]	Reserved
[3:0]	Power-of-two setting for number of averages, binary

Table 38. Low-Pass Filter Performance

D	N_D	f_{SC}	f_C (−3 dB)	Noise (m*g*)
0	1	72.9 kHz	22.5 kHz	465
1	2	36.5 kHz	14.2 kHz	386
2	4	18.2 kHz	7.78 kHz	302
3	8	9.11 kHz	3.99 kHz	227
4	16	4.56 kHz	2.01 kHz	164
5	32	2.28 kHz	1.01 kHz	117
6	64	1.14 kHz	504 Hz	83.0
7	128	570 Hz	252 Hz	58.8
8	256	285 Hz	126 Hz	41.6
9	512	142 Hz	62.7 Hz	29.7
10	1024	71.2 Hz	31.4 Hz	21.2

BAND-PASS FILTER

CAPT_CTRL[7], provide on/off control for the band-pass filter function. The band-pass filter stage combines a second-order, low-pass, IIR filter with a second-order, high-pass, IIR filter. The corner frequencies are dependent on the AVG_CNT register, which establishes the sample rate in this filter stage. Table 39 provides the corner frequencies for low-pass (F2) and high-pass (F1) filters for each AVG_CNT setting. Set CAPT_CTRL[7] = 1 (DIN = 0x9C80) to enable the band-pass filter stage.

Table 39. Band-Pass Filter Performance (CAPT_CTRL[7] = 1)

D	N_D	f_{SC}	F1 (Hz)	F2 (Hz)	Noise (m*g*)
0	1	72.9 kHz	2500	10,000	281
1	2	36.5 kHz	1250	5000	217
2	4	18.2 kHz	625	2500	158
3	8	9.11 kHz	313	1250	110
4	16	4.56 kHz	156	625	78.5
5	32	2.28 kHz	78.1	313	55.6
6	64	1.14 kHz	39.1	156	39.1
7	128	570 Hz	19.5	78.1	27.8
8	256	285 Hz	9.8	39.1	19.9
9	512	142 Hz	4.9	19.5	14.2
10	1024	71.2 Hz	2.4	9.8	10.2

OFFSET ADJUSTMENT

The NULL_X, NULL_Y, and NULL_Z registers provide a bias adjustment function. For example, setting NULL_X = 0x00D2 (DIN = 0x82D2) increases the acceleration bias by 210 LSB (~1 *g*). Set Register GLOB_CMD[0] = 1 (DIN = 0xBE01) to execute the auto-null function, which estimates the bias on each axis with an average of 65,536 samples, loads the offset registers with the opposite value, and then executes a flash update.

Table 40. NULL_X, NULL_Y, and NULL_Z Bit Descriptions

Bits	Description (Default = 0x0000)
[15:0]	Data bits, twos complement, 4.768 m*g*/LSB

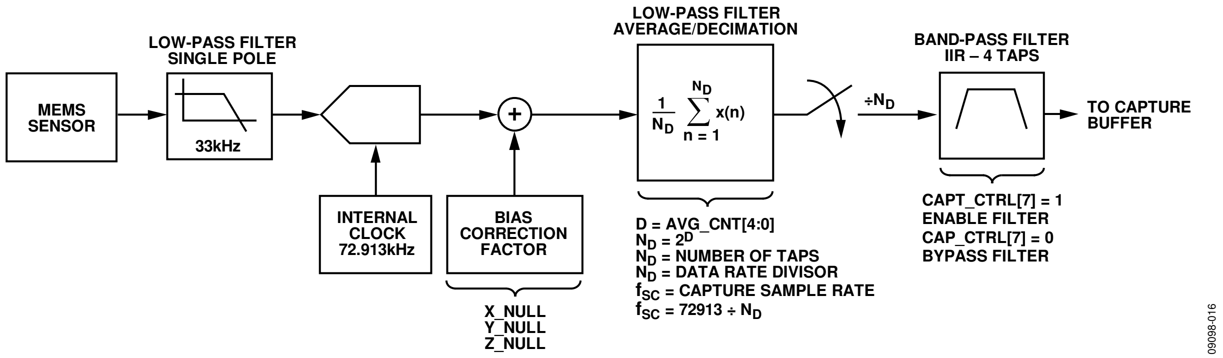


Figure 16. Sensor Signal Processing Diagram (Each Axis)

APPLICATIONS INFORMATION

GETTING STARTED

Once the power supply voltage of the ADIS16223 reaches 3.15 V, it executes a start-up sequence that places the device in manual capture mode. The following code example initiates a manual data capture by setting GLOB_CMD[11] = 1 (DIN = 0xBF08) and reads all 1024 samples in the x-axis acceleration capture buffer, using DIN = 0x1400. The data from the first spi_reg_read is not valid because this command is starting the process. The second spi_reg_read command (the first read inside the embedded for loop) produces the first valid data. This code sequence produces $\overline{\text{CS}}$, SCLK, and DIN signals similar to the ones shown in Figure 11.

```
spi_write(BF08h);
delay 30ms;
Data(0) = spi_reg_read(14h);
For n = 0 to 1023
Data(n) = spi_reg_read(14h);
n = n + 1;
end
```

INTERFACE BOARD

The ADIS16223/PCBZ provides the ADIS16223CMLZ on a small printed circuit board (PCB) that simplifies the connection to an existing processor system. A single 10-32 machine screw secures the ADIS16223CMLZ to the interface board. The first set of mounting holes on the interface boards are in the four corners of the PCB and provide clearance for 4-40 machine screws. The second set of mounting holes provides a pattern that matches the ADISUSBZ evaluation system, using M2 × 0.4 mm machine screws. These boards are made of IS410 material and are 0.063 inches thick. The J1 connector uses Pin 1 through Pin 12 in this pattern. Pin 13 and Pin 14 are for future expansion, but they also provide convenient probe points for the DIO1 and DIO2 signals. The connector is a dual row, 2 mm (pitch) connector that work with a number of ribbon cable systems, including 3M Part Number 152212-0100-GB (ribbon-crimp connector) and 3M Part Number 3625/12 (ribbon cable). The LEDs (D1 and D2) provide visual indication on the DIO1 and DIO2 signals.

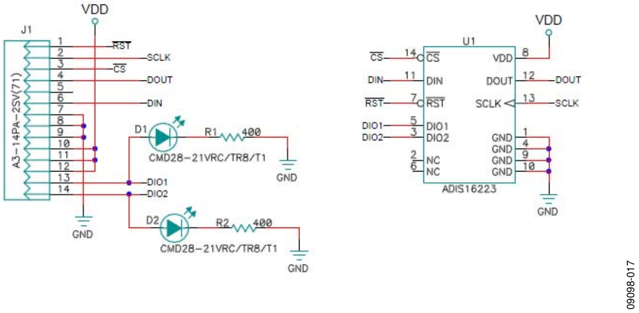


Figure 17. Electrical Schematic

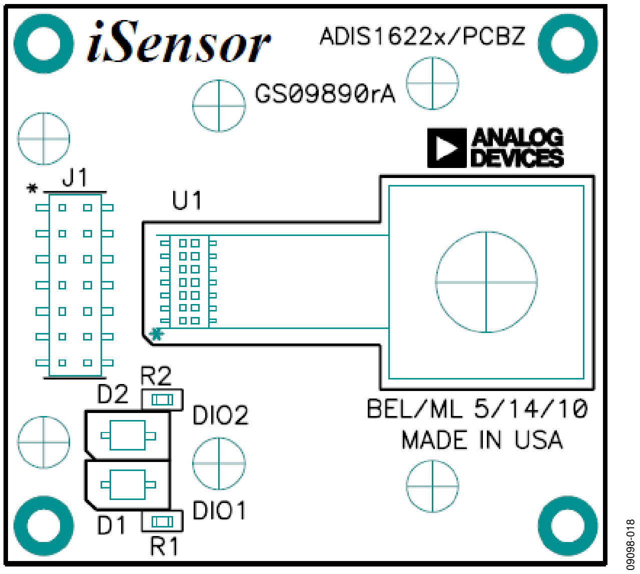


Figure 18. PCB Assembly View and Dimensions

OUTLINE DIMENSIONS

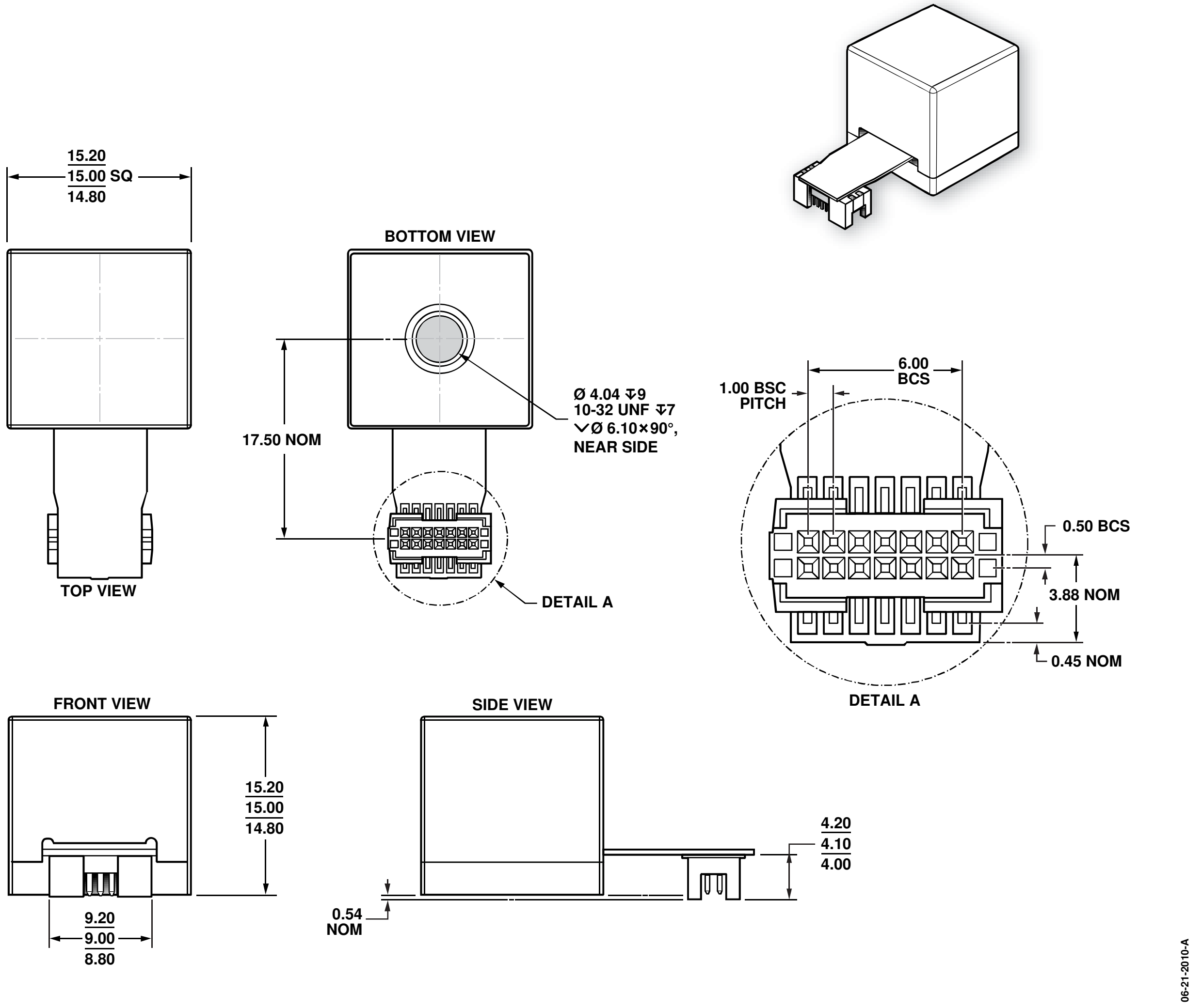


Figure 19. 14-Lead Module with Connector Interface
(ML-14-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16223CMLZ	−40°C to +125°C	14-Lead Module with Connector Interface	ML-14-2
ADIS16223/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

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