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FEATURES

Triaxis digital gyroscope with digital range scaling

$\pm 75^\circ/\text{sec}$, $\pm 150^\circ/\text{sec}$, $\pm 300^\circ/\text{sec}$ settings

Tight orthogonal alignment: $<0.05^\circ$

Triaxis digital accelerometer: $\pm 1.7 g$

Wide sensor bandwidth: 330 Hz

Autonomous operation and data collection

No external configuration commands required

Start-up time: 180 ms

Sleep mode recovery time: 4 ms

Factory-calibrated sensitivity, bias, and axial alignment

Calibration temperature range: -20°C to $+70^\circ\text{C}$

SPI-compatible serial interface

Embedded temperature sensor

Programmable operation and control

Automatic and manual bias correction controls

Bartlett window FIR filter length, number of taps

Digital I/O: data ready, alarm indicator, general-purpose

Alarms for condition monitoring

Sleep mode for power management

DAC output voltage

Enable external sample clock input: up to 1.2 kHz

Single-command self-test

Single-supply operation: 4.75 V to 5.25 V

2000 g shock survivability

Operating temperature range: -40°C to $+105^\circ\text{C}$

APPLICATIONS

Medical instrumentation

Robotics

Platform control

Navigation

GENERAL DESCRIPTION

The ADIS16362 iSensor[®] is a complete inertial system that includes a triaxis gyroscope and triaxis accelerometer. Each sensor in the ADIS16362 combines industry-leading iMEMS[®] technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyro bias). As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements over a temperature range of -20°C to $+70^\circ\text{C}$.

The ADIS16362 provides a simple, cost-effective method for integrating accurate, multiaxis, inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary

Rev. E

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FUNCTIONAL BLOCK DIAGRAM

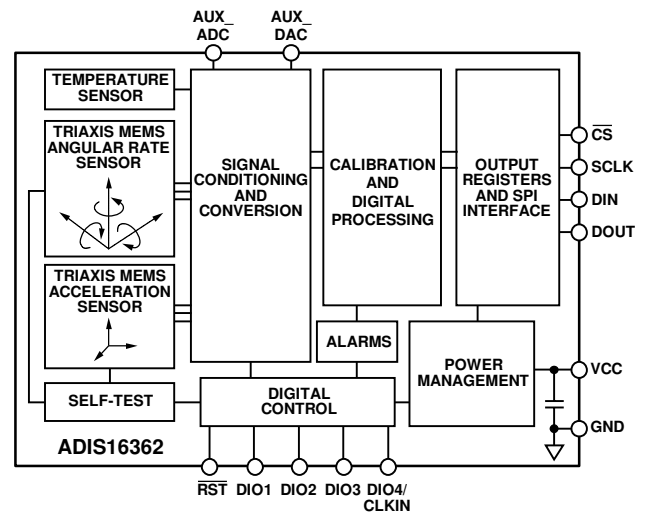


Figure 1.

08179-001

motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. An improved SPI interface and register structure provide faster data collection and configuration control. The ADIS16362 uses a compatible pinout and the same package as the ADIS1635x family. Therefore, systems that currently use the ADIS1635x family can upgrade their performance with minor firmware adjustments in their processor designs.

This compact module is approximately 23 mm × 23 mm × 23 mm and provides a flexible connector interface that enables multiple mounting orientation options.

ADIS16362* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADIS16IMU2 Breakout Board
- EVAL-ADIS2 Evaluation System

DOCUMENTATION

Application Notes

- AN-1041: iSensor® IMU Quick Start Guide and Bias Optimization Tips

Data Sheet

- ADIS16362: Six Degrees of Freedom Inertial Sensor Data Sheet

User Guides

- UG-363: ADISUSB User Guide

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADIS16400 IIO Inertial Measurement Unit Linux Driver
- ADIS16400 IIO Inertial Measurement Unit Linux Driver
- ADIS16334 and ADIS16360/2/4/5/7 Evaluation Software for the ADISUSB

REFERENCE MATERIALS

Customer Case Studies

- OrthAlign's KneeAlign® 2 System uses iSensor® MEMS technology to provide surgical precision

DESIGN RESOURCES

- ADIS16362 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADIS16362 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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2/11—Rev. C to Rev. D

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2/11—Rev. B to Rev. C

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| Changes to Table 30 and Table 31 | 16 |

12/09—Rev. A to Rev. B

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11/09—Rev. 0 to Rev. A

| | |
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| Changes to Table 8..... | 10 |
| Changes to Product Identification Section | 16 |

8/09—Revision 0: Initial Version

SPECIFICATIONS

$T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{ V}$, angular rate = $0^\circ/\text{sec}$, dynamic range = $\pm 300^\circ/\text{sec} \pm 1\text{ g}$, unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|-------------------------------------|---|-----------|------------|------------|--|
| GYROSCOPES | | | | | |
| Dynamic Range | | ± 300 | ± 350 | | $^\circ/\text{sec}$ |
| Initial Sensitivity | Dynamic range = $\pm 300^\circ/\text{sec}$ | 0.0495 | 0.05 | 0.0505 | $^\circ/\text{sec}/\text{LSB}$ |
| | Dynamic range = $\pm 150^\circ/\text{sec}$ | | 0.025 | | $^\circ/\text{sec}/\text{LSB}$ |
| | Dynamic range = $\pm 75^\circ/\text{sec}$ | | 0.0125 | | $^\circ/\text{sec}/\text{LSB}$ |
| Sensitivity Temperature Coefficient | $-20^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ | | ± 50 | | $\text{ppm}/^\circ\text{C}$ |
| Misalignment | Axis-to-axis | | ± 0.05 | | Degrees |
| | Axis-to-frame (package) | | ± 0.5 | | Degrees |
| Nonlinearity | Best fit straight line | | ± 0.1 | | % of FS |
| Initial Bias Error | $\pm 1\sigma$ | | ± 3 | | $^\circ/\text{sec}$ |
| In-Run Bias Stability | 1σ , SMPL_PRD = 0x0001 | | 0.007 | | $^\circ/\text{sec}$ |
| Angular Random Walk | 1σ , SMPL_PRD = 0x0001 | | 2.0 | | $^\circ/\sqrt{\text{hr}}$ |
| Bias Temperature Coefficient | $-20^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ | | ± 0.01 | | $^\circ/\text{sec}/^\circ\text{C}$ |
| Linear Acceleration Effect on Bias | Any axis, 1σ (MSC_CTRL[7] = 1) | | 0.05 | | $^\circ/\text{sec}/\text{g}$ |
| Bias Voltage Sensitivity | $V_{CC} = 4.75\text{ V}$ to 5.25 V | | ± 0.3 | | $^\circ/\text{sec}/\text{V}$ |
| Output Noise | $\pm 300^\circ/\text{sec}$ range, no filtering | | 0.8 | | $^\circ/\text{sec rms}$ |
| Rate Noise Density | $f = 25\text{ Hz}$, $\pm 300^\circ/\text{sec}$ range, no filtering | | 0.044 | | $^\circ/\text{sec}/\sqrt{\text{Hz rms}}$ |
| 3 dB Bandwidth | | | 330 | | Hz |
| Sensor Resonant Frequency | | | 14.5 | | kHz |
| Self-Test Change in Output Response | $\pm 300^\circ/\text{sec}$ range setting | ± 696 | ± 1400 | ± 2449 | LSB |
| ACCELEROMETERS | | | | | |
| Dynamic Range | Each axis | ± 1.7 | | | g |
| Initial Sensitivity | | 0.330 | 0.333 | 0.336 | mg/LSB |
| Sensitivity Temperature Coefficient | $-20^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ | | 40 | | $\text{ppm}/^\circ\text{C}$ |
| Misalignment | Axis-to-axis | | ± 0.2 | | Degrees |
| | Axis-to-frame (package) | | ± 0.5 | | Degrees |
| Nonlinearity | Best fit straight line | | ± 0.1 | | % of FS |
| Initial Bias Error | $\pm 1\sigma$ | | 6 | | mg |
| In-Run Bias Stability | 1σ | | 41 | | μg |
| Velocity Random Walk | 1σ | | 0.09 | | $\text{m}/\text{sec}/\sqrt{\text{hr}}$ |
| Bias Temperature Coefficient | $-20^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ | | ± 0.05 | | $\text{mg}/^\circ\text{C}$ |
| Bias Voltage Sensitivity | $V_{CC} = 4.75\text{ V}$ to 5.25 V | | ± 2.5 | | mg/V |
| Output Noise | No filtering | | 5 | | mg rms |
| Noise Density | No filtering | | 0.23 | | $\text{mg}/\sqrt{\text{Hz rms}}$ |
| 3 dB Bandwidth | | | 330 | | Hz |
| Sensor Resonant Frequency | | | 5.5 | | kHz |
| Self-Test Change in Output Response | X-axis and y-axis | 505 | | 1671 | LSB |
| TEMPERATURE SENSOR | | | | | |
| Scale Factor | Output = 0x0000 at 25°C ($\pm 5^\circ\text{C}$) | | 0.136 | | $^\circ\text{C}/\text{LSB}$ |
| ADC INPUT | | | | | |
| Resolution | | | 12 | | Bits |
| Integral Nonlinearity | | | ± 2 | | LSB |
| Differential Nonlinearity | | | ± 1 | | LSB |
| Offset Error | | | ± 4 | | LSB |
| Gain Error | | | ± 2 | | LSB |
| Input Range | | 0 | | 3.3 | V |
| Input Capacitance | During acquisition | | 20 | | pF |

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|---|------------------|------------------------|----------|--------------------------|
| DAC OUTPUT | 5 k Ω /100 pF to GND | | | | |
| Resolution | | | 12 | | Bits |
| Relative Accuracy | 101 LSB \leq input code \leq 4095 LSB | | ± 4 | | LSB |
| Differential Nonlinearity | | | ± 1 | | LSB |
| Offset Error | | | ± 5 | | mV |
| Gain Error | | | ± 0.5 | | % |
| Output Range | | 0 | | 3.3 | V |
| Output Impedance | | | 2 | | Ω |
| Output Settling Time | | | 10 | | μ s |
| LOGIC INPUTS ¹ | | | | | |
| Input High Voltage, V _{IH} | | 2.0 | | | V |
| Input Low Voltage, V _{IL} | | | | 0.8 | V |
| $\overline{\text{CS}}$ Wake-Up Pulse Width | $\overline{\text{CS}}$ signal to wake up from sleep mode | | | 0.55 | V |
| Logic 1 Input Current, I _{IH} | V _{IH} = 3.3 V | | ± 0.2 | ± 10 | μ A |
| Logic 0 Input Current, I _{IL} | V _{IL} = 0 V | | | | |
| All Pins Except $\overline{\text{RST}}$ | | | 40 | 60 | μ A |
| $\overline{\text{RST}}$ Pin | | | 1 | | mA |
| Input Capacitance, C _{IN} | | | 10 | | pF |
| DIGITAL OUTPUTS ¹ | | | | | |
| Output High Voltage, V _{OH} | I _{SOURCE} = 1.6 mA | 2.4 | | | V |
| Output Low Voltage, V _{OL} | I _{SINK} = 1.6 mA | | | 0.4 | V |
| FLASH MEMORY | | | | | |
| Data Retention ³ | Endurance ² T _J = 85°C | 10,000 20 | | | Cycles Years |
| FUNCTIONAL TIMES ⁴ | Time until data is available | | | | |
| Power-On Start-Up Time | Normal mode, SMPL_PRD \leq 0x09 Low power mode, SMPL_PRD \geq 0x0A | | 180 250 | | ms ms |
| Reset Recovery Time | Normal mode, SMPL_PRD \leq 0x09 Low power mode, SMPL_PRD \geq 0x0A | | 60 130 | | ms ms |
| Sleep Mode Recovery Time | Normal mode, SMPL_PRD \leq 0x09 Low power mode, SMPL_PRD \geq 0x0A | | 4 9 | | ms ms |
| Flash Memory Test Time | Normal mode, SMPL_PRD \leq 0x09 Low power mode, SMPL_PRD \geq 0x0A | | 17 90 | | ms ms |
| Automatic Self-Test Time | SMPL_PRD = 0x01 | | 12 | | ms |
| CONVERSION RATE | SMPL_PRD = 0x01 to 0xFF | 0.413 | | 819.2 | SPS |
| Clock Accuracy | | | | ± 3 | % |
| Sync Input Clock | | 0.8 ⁵ | | 1.2 | kHz |
| POWER SUPPLY | | | | | |
| Power Supply Current | Operating voltage range, VCC Low power mode Normal mode Sleep mode | 4.75 | 5.0 24 49 500 | 5.25 | V mA mA μ A |

¹ The digital I/O signals are driven by an internal 3.3 V supply, and the inputs are 5 V tolerant.

² Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at -40°C , $+25^{\circ}\text{C}$, $+85^{\circ}\text{C}$, and $+125^{\circ}\text{C}$.

³ The data retention lifetime equivalent is at a junction temperature (T_J) of 85°C as per JEDEC Standard 22, Method A117. Data retention lifetime decreases with junction temperature.

⁴ These times do not include thermal settling and internal filter response times (330 Hz bandwidth), which may affect overall accuracy.

⁵ The sync input clock functions below the specified minimum value, at reduced performance levels.

TIMING SPECIFICATIONS

T_A = 25°C, VCC = 5 V, unless otherwise noted.

Table 2.

| Parameter | Description | Normal Mode (SMPL_PRD ≤ 0x09) | | | Low Power Mode (SMPL_PRD ≥ 0x0A) | | | Burst Read | | | Unit |
|---|--|----------------------------------|-----|------|-------------------------------------|-----|------|---------------------|-----|------|------|
| | | Min ¹ | Typ | Max | Min ¹ | Typ | Max | Min ¹ | Typ | Max | |
| f _{SCLK} | Serial clock | 0.01 | | 2.0 | 0.01 | | 0.3 | 0.01 | | 1.0 | MHz |
| t _{STALL} | Stall period between data | 9 | | | 75 | | | 1/f _{SCLK} | | | μs |
| t _{READRATE} | Read rate | 40 | | | 100 | | | | | | μs |
| t _{CS} | Chip select to clock edge | 48.8 | | | 48.8 | | | 48.8 | | | ns |
| t _{DAV} | DOUT valid after SCLK edge | | | 100 | | | 100 | | | 100 | ns |
| t _{DSU} | DIN setup time before SCLK rising edge | 24.4 | | | 24.4 | | | 24.4 | | | ns |
| t _{DHD} | DIN hold time after SCLK rising edge | 48.8 | | | 48.8 | | | 48.8 | | | ns |
| t _{SCLKR} , t _{SCLKF} | SCLK rise/fall times | | 5 | 12.5 | | 5 | 12.5 | | 5 | 12.5 | ns |
| t _{DR} , t _{DF} | DOUT rise/fall times | | 5 | 12.5 | | 5 | 12.5 | | 5 | 12.5 | ns |
| t _{SFS} | CS high after SCLK edge | 5 | | | 5 | | | 5 | | | ns |
| t ₁ | Input sync positive pulse width | 5 | | | | | | 5 | | | μs |
| t _x | Input sync low time | 100 | | | | | | 100 | | | μs |
| t ₂ | Input sync to data ready output | | 600 | | | | | | 600 | | μs |
| t ₃ | Input sync period | 833 | | | | | | 833 | | | μs |

¹ Guaranteed by design and characterization, but not tested in production.

TIMING DIAGRAMS

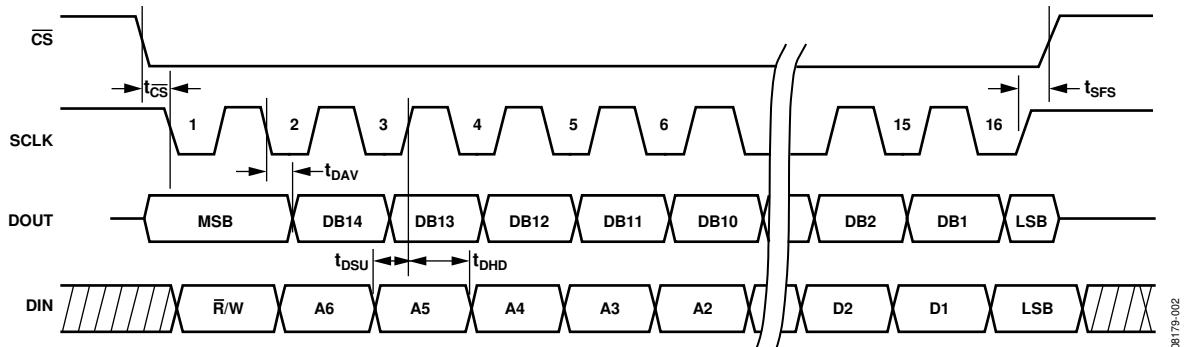


Figure 2. SPI Timing and Sequence

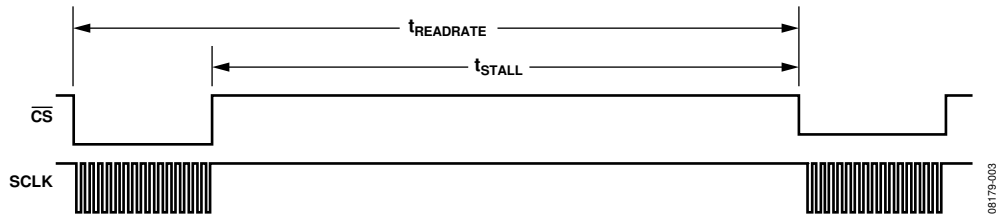


Figure 3. Stall Time and Data Rate

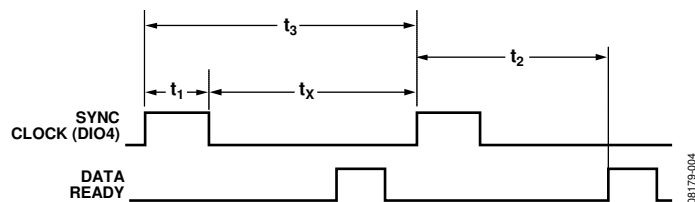


Figure 4. Input Clock Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

| Parameter | Rating |
|-------------------------------|--------------------------------|
| Acceleration | |
| Any Axis, Unpowered | 2000 <i>g</i> |
| Any Axis, Powered | 2000 <i>g</i> |
| VCC to GND | −0.3 V to +6.0 V |
| Digital Input Voltage to GND | −0.3 V to +5.3 V |
| Digital Output Voltage to GND | −0.3 V to VCC + 0.3 V |
| Analog Input to GND | −0.3 V to +3.6 V |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +125°C ^{1,2} |

¹ Extended exposure to temperatures outside the specified temperature range of −40°C to +105°C can adversely affect the accuracy of the factory calibration. For best accuracy, store the parts within the specified operating range of −40°C to +105°C.

² Although the device is capable of withstanding short-term exposure to 150°C, long-term exposure threatens internal mechanical integrity.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Package Characteristics

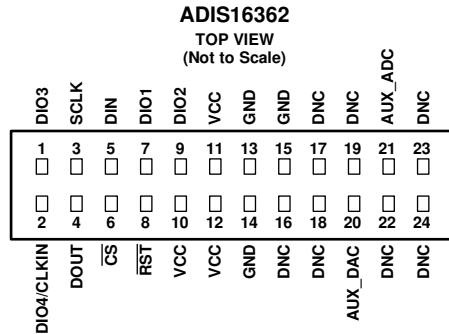
| Package Type | θ_{JA} | θ_{JC} | Device Weight |
|----------------|---------------|---------------|---------------|
| 24-Lead Module | 39.8°C/W | 14.2°C/W | 16 grams |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

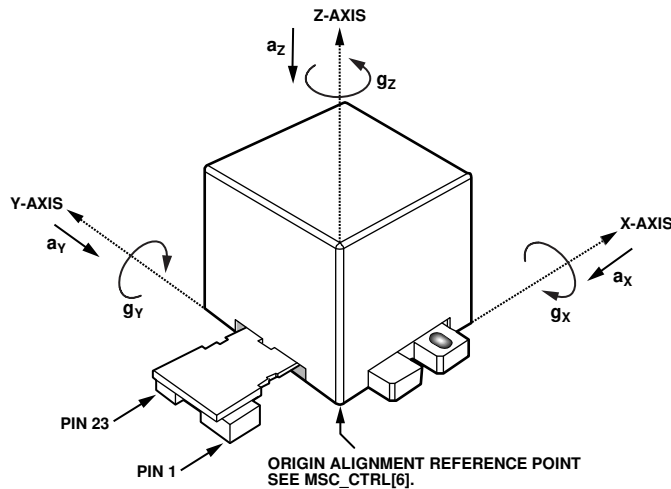
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
1. THIS REPRESENTATION DISPLAYS THE TOP VIEW PINOUT FOR THE MATING SOCKET CONNECTOR.
 2. THE ACTUAL CONNECTOR PINS ARE NOT VISIBLE FROM THE TOP VIEW.
 3. MATING CONNECTOR: SAMTEC CLM-112-02 OR EQUIVALENT.
 4. DNC = DO NOT CONNECT.

08179-005

Figure 5. Pin Configuration



- NOTES**
1. ACCELERATION (a_x, a_y, a_z) AND ROTATIONAL (g_x, g_y, g_z) ARROWS INDICATE THE DIRECTION OF MOTION THAT PRODUCES A POSITIVE OUTPUT.

08179-006

Figure 6. Axial Orientation

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Type ¹ | Description |
|----------------------------|------------------|-------------------|--|
| 1 | DIO3 | I/O | Configurable Digital Input/Output. |
| 2 | DIO4/CLKIN | I/O | Configurable Digital Input/Output or Sync Clock Input. |
| 3 | SCLK | I | SPI Serial Clock. |
| 4 | DOUT | O | SPI Data Output. Clocks output on SCLK falling edge. |
| 5 | DIN | I | SPI Data Input. Clocks input on SCLK rising edge. |
| 6 | \overline{CS} | I | SPI Chip Select. |
| 7, 9 | DIO1, DIO2 | I/O | Configurable Digital Input/Output. |
| 8 | \overline{RST} | I | Reset. |
| 10, 11, 12 | VCC | S | Power Supply. |
| 13, 14, 15 | GND | S | Power Ground. |
| 16, 17, 18, 19, 22, 23, 24 | DNC | N/A | Do Not Connect. |
| 20 | AUX_DAC | O | Auxiliary, 12-Bit DAC Output. |
| 21 | AUX_ADC | I | Auxiliary, 12-Bit ADC Input. |

¹ I/O is input/output, I is input, O is output, S is supply, N/A is not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

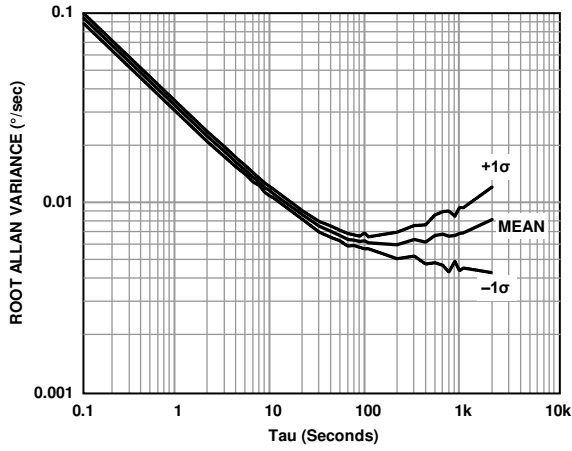


Figure 7. Gyroscope Allan Variance

08179-007

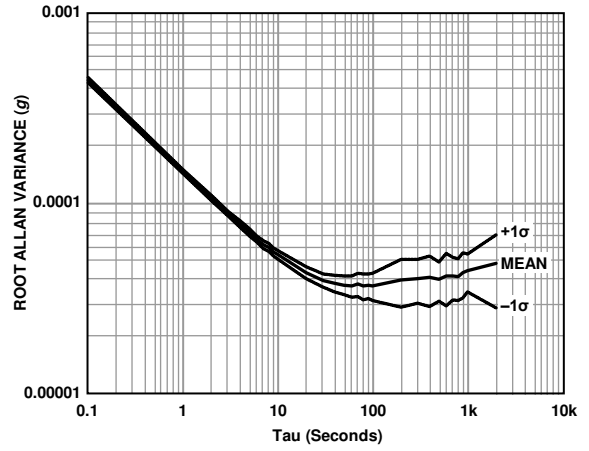


Figure 8. Accelerometer Allan Variance

08179-008

THEORY OF OPERATION

BASIC OPERATION

The ADIS16362 is an autonomous sensor system that starts up after it has a valid power supply voltage and begins producing inertial measurement data at the factory default sample rate setting of 819.2 SPS. After each sample cycle, the sensor data is loaded into the output registers, and DIO1 pulses high, which provides a new data ready control signal for driving system-level interrupt service routines. In a typical system, a master processor accesses the output data registers through the SPI interface, using the connection diagram shown in Figure 9. Table 6 provides a generic functional description for each pin on the master processor. Table 7 describes the typical master processor settings that are normally found in a configuration register and used for communicating with the ADIS16362.

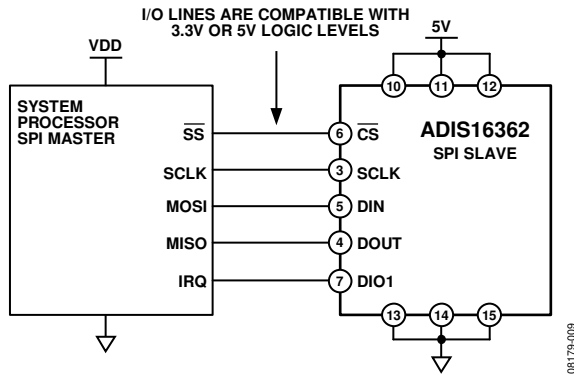


Figure 9. Electrical Connection Diagram

Table 6. Generic Master Processor Pin Names and Functions

| Pin Name | Function |
|----------|----------------------------|
| SS | Slave select |
| IRQ | Interrupt request |
| MOSI | Master output, slave input |
| MISO | Master input, slave output |
| SCLK | Serial clock |

Table 7. Generic Master Processor SPI Settings

| Processor Setting | Description |
|--------------------------------|---------------------------------------|
| Master | The ADIS16362 operates as a slave |
| SCLK Rate ≤ 2 MHz ¹ | Normal mode, SMPL_PRD[7:0] ≤ 0x09 |
| SPI Mode 3 | CPOL = 1 (polarity), CHPA = 1 (phase) |
| MSB First Mode | Bit sequence |
| 16-Bit Mode | Shift register/data length |

¹ For burst read, SCLK rate ≤ 1 MHz. For low power mode, SCLK rate ≤ 300 kHz.

The user registers provide addressing for all input/output operations on the SPI interface. Each 16-bit register has two 7-bit addresses: one for its upper byte and one for its lower byte. Table 8 lists the lower byte address for each register, and Figure 10 shows the generic bit assignments.

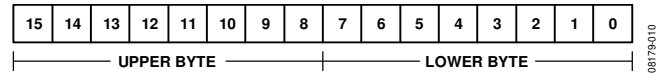


Figure 10. Generic Register Bit Assignments

READING SENSOR DATA

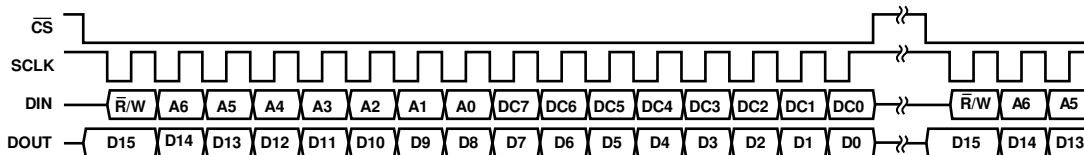
Although the ADIS16362 produces data independently, it operates as a SPI slave device that communicates with system (master) processors using the 16-bit segments displayed in Figure 11. Individual register reads require two of these 16-bit sequences. The first 16-bit sequence provides the read command bit ($\bar{R}/W = 0$) and the target register address (A6 to A0). The second sequence transmits the register contents (D15 to D0) on the DOUT line. For example, if DIN = 0x0A00, the contents of XACCL_OUT are shifted out on the DOUT line during the next 16-bit sequence.

The SPI operates in full-duplex mode, which means that the master processor can read the output data from DOUT while using the same SCLK pulses to transmit the next target address on DIN.

DEVICE CONFIGURATION

The user register memory map (see Table 8) identifies configuration registers with either a W or R/W. Configuration commands also use the bit sequence shown in Figure 11. If the MSB = 1, the last eight bits (DC7 to DC0) in the DIN sequence are loaded into the memory address associated with the address bits (A6 to A0). For example, if DIN = 0xA11F, 0x1F is loaded into Address 0x21 (XACCL_OFF, upper byte) at the conclusion of the data frame.

The master processor initiates the backup function by setting GLOB_CMD[3] = 1 (DIN = 0xBE08). This command copies the user registers into their assigned flash memory locations and requires the power supply to stay within its normal operating range for the entire 50 ms process. The FLASH_CNT register provides a running count of these events for monitoring the long-term reliability of the flash memory.



NOTES

1. DOUT BITS ARE PRODUCED ONLY WHEN THE PREVIOUS 16-BIT DIN SEQUENCE STARTS WITH $\bar{R}/W = 0$.

Figure 11. SPI Communication Bit Sequence

MEMORY MAP

Table 8. User Register Memory Map

| Name | R/W | Flash Backup | Address ¹ | Default | Register Description | Bit Function |
|------------|-----|--------------|----------------------|---------|--|--------------|
| FLASH_CNT | R | Yes | 0x00 | N/A | Flash memory write count | N/A |
| SUPPLY_OUT | R | No | 0x02 | N/A | Power supply measurement | See Table 9 |
| XGYRO_OUT | R | No | 0x04 | N/A | X-axis gyroscope output | See Table 9 |
| YGYRO_OUT | R | No | 0x06 | N/A | Y-axis gyroscope output | See Table 9 |
| ZGYRO_OUT | R | No | 0x08 | N/A | Z-axis gyroscope output | See Table 9 |
| XACCL_OUT | R | No | 0x0A | N/A | X-axis accelerometer output | See Table 9 |
| YACCL_OUT | R | No | 0x0C | N/A | Y-axis accelerometer output | See Table 9 |
| ZACCL_OUT | R | No | 0x0E | N/A | Z-axis accelerometer output | See Table 9 |
| XTEMP_OUT | R | No | 0x10 | N/A | X-axis gyroscope temperature measurement | See Table 9 |
| YTEMP_OUT | R | No | 0x12 | N/A | Y-axis gyroscope temperature measurement | See Table 9 |
| ZTEMP_OUT | R | No | 0x14 | N/A | Z-axis gyroscope temperature measurement | See Table 9 |
| AUX_ADC | R | No | 0x16 | N/A | Auxiliary ADC output | See Table 9 |
| Reserved | N/A | N/A | 0x18 | N/A | Reserved | N/A |
| XGYRO_OFF | R/W | Yes | 0x1A | 0x0000 | X-axis gyroscope bias offset factor | See Table 15 |
| YGYRO_OFF | R/W | Yes | 0x1C | 0x0000 | Y-axis gyroscope bias offset factor | See Table 15 |
| ZGYRO_OFF | R/W | Yes | 0x1E | 0x0000 | Z-axis gyroscope bias offset factor | See Table 15 |
| XACCL_OFF | R/W | Yes | 0x20 | 0x0000 | X-axis acceleration bias offset factor | See Table 16 |
| YACCL_OFF | R/W | Yes | 0x22 | 0x0000 | Y-axis acceleration bias offset factor | See Table 16 |
| ZACCL_OFF | R/W | Yes | 0x24 | 0x0000 | Z-axis acceleration bias offset factor | See Table 16 |
| ALM_MAG1 | R/W | Yes | 0x26 | 0x0000 | Alarm 1 amplitude threshold | See Table 27 |
| ALM_MAG2 | R/W | Yes | 0x28 | 0x0000 | Alarm 2 amplitude threshold | See Table 27 |
| ALM_SMPL1 | R/W | Yes | 0x2A | 0x0000 | Alarm 1 sample size | See Table 28 |
| ALM_SMPL2 | R/W | Yes | 0x2C | 0x0000 | Alarm 2 sample size | See Table 28 |
| ALM_CTRL | R/W | Yes | 0x2E | 0x0000 | Alarm control | See Table 29 |
| AUX_DAC | R/W | No | 0x30 | 0x0000 | Auxiliary DAC data | See Table 23 |
| GPIO_CTRL | R/W | No | 0x32 | 0x0000 | Auxiliary digital input/output control | See Table 21 |
| MSC_CTRL | R/W | Yes | 0x34 | 0x0006 | Miscellaneous control: data ready, self-test | See Table 22 |
| SMPL_PRD | R/W | Yes | 0x36 | 0x0001 | Internal sample period (rate) control | See Table 18 |
| SENS_AVG | R/W | Yes | 0x38 | 0x0402 | Dynamic range and digital filter control | See Table 20 |
| SLP_CNT | W | No | 0x3A | 0x0000 | Sleep mode control | See Table 19 |
| DIAG_STAT | R | No | 0x3C | 0x0000 | System status | See Table 26 |
| GLOB_CMD | W | N/A | 0x3E | 0x0000 | System command | See Table 17 |
| Reserved | N/A | N/A | 0x40 to 0x51 | N/A | Reserved | N/A |
| LOT_ID1 | R | Yes | 0x52 | N/A | Lot Identification Code 1 | See Table 32 |
| LOT_ID2 | R | Yes | 0x54 | N/A | Lot Identification Code 2 | See Table 32 |
| PROD_ID | R | Yes | 0x56 | 0x3FEA | Product identification | See Table 32 |
| SERIAL_NUM | R | Yes | 0x58 | N/A | Serial number | See Table 32 |

¹ Each register contains two bytes. The address of the lower byte is displayed. The address of the upper byte is equal to the address of the lower byte plus 1.

BURST READ DATA COLLECTION

Burst read data collection is a process-efficient method for collecting data from the ADIS16362. In burst read, all output registers are clocked out on DOUT, 16 bits at a time, in sequential data cycles (each separated by one SCLK period). To start a burst read sequence, set DIN = 0x3E00. The contents of each output register are then shifted out on DOUT, starting with SUPPLY_OUT and ending with AUX_ADC (see Figure 13). The addressing sequence shown in Table 8 determines the order of the outputs in burst read.

OUTPUT DATA REGISTERS

Each output data register uses the format in Figure 12 and Table 9. Figure 6 shows the positive direction for each inertial sensor. The ND bit is equal to 1 when the register contains unread data. The EA bit is high when any error/alarm flag in the DIAG_STAT register is equal to 1.

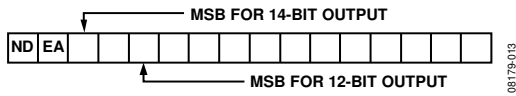


Figure 12. Output Register Bit Assignments

Table 9. Output Data Register Formats

| Register | Bits | Scale | Reference |
|------------------------|------|-----------|--------------|
| SUPPLY_OUT | 12 | 2.418 mV | See Table 10 |
| XGYRO_OUT ¹ | 14 | 0.05°/sec | See Table 11 |
| YGYRO_OUT ¹ | 14 | 0.05°/sec | See Table 11 |
| ZGYRO_OUT ¹ | 14 | 0.05°/sec | See Table 11 |
| XACCL_OUT | 14 | 0.333 mg | See Table 12 |
| YACCL_OUT | 14 | 0.333 mg | See Table 12 |
| ZACCL_OUT | 14 | 0.333 mg | See Table 12 |
| XTEMP_OUT ² | 12 | 0.136°C | See Table 13 |
| YTEMP_OUT ² | 12 | 0.136°C | See Table 13 |
| ZTEMP_OUT ² | 12 | 0.136°C | See Table 13 |
| AUX_ADC | 12 | 805.8 μV | See Table 14 |

¹ Assumes that the scaling is set to ±300°/sec. This factor scales with the range.
² 0x0000 = 25°C (±5°C).

Table 10. Power Supply, Offset Binary Format

| Supply Voltage | Decimal | Hex | Binary |
|----------------|----------|-------|---------------------|
| 5.25 V | 2171 LSB | 0x87B | XXXX 1000 0111 1011 |
| 5.002418 V | 2069 LSB | 0x815 | XXXX 1000 0001 0101 |
| 5 V | 2068 LSB | 0x814 | XXXX 1000 0001 0100 |
| 4.997582 V | 2067 LSB | 0x813 | XXXX 1000 0001 0011 |
| 4.75 V | 1964 LSB | 0x7AC | XXXX 0111 1010 1100 |

Table 11. Rotation Rate, Twos Complement Format

| Rotation Rate | Decimal | Hex | Binary |
|---------------|-----------|--------|---------------------|
| +300°/sec | +6000 LSB | 0x1770 | XX01 0111 0111 0000 |
| +0.1°/sec | +2 LSB | 0x0002 | XX00 0000 0000 0010 |
| +0.05°/sec | +1 LSB | 0x0001 | XX00 0000 0000 0001 |
| 0°/sec | 0 LSB | 0x0000 | XX00 0000 0000 0000 |
| -0.05°/sec | -1 LSB | 0x3FFF | XX11 1111 1111 1111 |
| -0.1°/sec | -2 LSB | 0x3FFE | XX11 1111 1111 1110 |
| -300°/sec | -6000 LSB | 0x2890 | XX10 1000 1001 0000 |

Table 12. Acceleration, Twos Complement Format

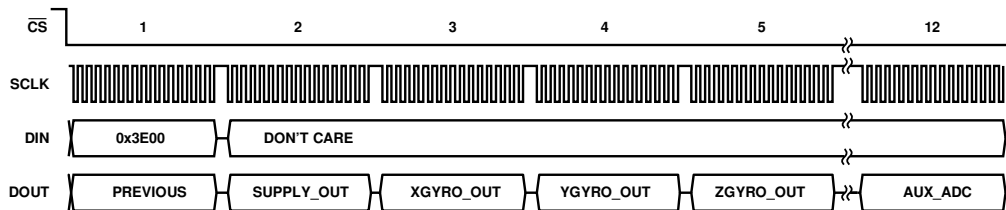
| Acceleration | Decimal | Hex | Binary |
|--------------|-----------|--------|---------------------|
| +1.7 g | +5105 LSB | 0x13F1 | XX01 0011 1111 0001 |
| +0.667 mg | +2 LSB | 0x0002 | XX00 0000 0000 0010 |
| +0.333 mg | +1 LSB | 0x0001 | XX00 0000 0000 0001 |
| 0 g | 0 LSB | 0x0000 | XX00 0000 0000 0000 |
| -0.333 mg | -1 LSB | 0x3FFF | XX11 1111 1111 1111 |
| -0.667 mg | -2 LSB | 0x3FFE | XX11 1111 1111 1110 |
| -1.7 g | -5105 LSB | 0x2C0F | XX10 1100 0000 1111 |

Table 13. Temperature, Twos Complement Format

| Temperature | Decimal | Hex | Binary |
|-------------|----------|-------|---------------------|
| +105°C | +588 LSB | 0x24C | XXXX 0010 0100 1100 |
| +85°C | +441 LSB | 0x1B9 | XXXX 0001 1011 1001 |
| +25.272°C | +2 LSB | 0x002 | XXXX 0000 0000 0010 |
| +25.136°C | +1 LSB | 0x001 | XXXX 0000 0000 0001 |
| +25°C | 0 LSB | 0x000 | XXXX 0000 0000 0000 |
| +24.864°C | -1 LSB | 0xFFF | XXXX 1111 1111 1111 |
| +24.728°C | -2 LSB | 0xFFE | XXXX 1111 1111 1110 |
| -40°C | -478 LSB | 0xE22 | XXXX 1110 0010 0010 |

Table 14. Analog Input, Offset Binary Format

| Input Voltage | Decimal | Hex | Binary |
|---------------|----------|--------|---------------------|
| 3.3 V | 4095 LSB | 0xFFFF | XXXX 1111 1111 1111 |
| 1 V | 1241 LSB | 0x4D9 | XXXX 0100 1101 1001 |
| 1.6116 mV | 2 LSB | 0x002 | XXXX 0000 0000 0010 |
| 805.8 μV | 1 LSB | 0x001 | XXXX 0000 0000 0001 |
| 0 V | 0 LSB | 0x000 | XXXX 0000 0000 0000 |



NOTES
 1. THE DOUT LINE HAS BEEN SIMPLIFIED FOR SPACE CONSTRAINTS BUT, IDEALLY, SHOULD INCLUDE ALL REGISTERS FROM SUPPLY_OUT THROUGH AUX_ADC.

Figure 13. Burst Read Sequence

CALIBRATION

Manual Bias Calibration

The bias offset registers in Table 15 and Table 16 provide a manual adjustment function for the output of each sensor. For example, if XGYRO_OFF = 0x1FF6 (DIN = 0x9B1F, 0x9AF6), the XGYRO_OUT offset shifts by -10 LSBs, or -0.125°/sec.

Table 15. XGYRO_OFF, YGYRO_OFF, ZGYRO_OFF

Bit Descriptions

| Bit | Description (Default = 0x0000) |
|---------|--|
| [15:13] | Not used. |
| [12:0] | Data bits. Twos complement, 0.0125°/sec per LSB. Typical adjustment range = ±50°/sec. |

Table 16. XACCL_OFF, YACCL_OFF, ZACCL_OFF

Bit Descriptions

| Bit | Description (Default = 0x0000) |
|---------|---|
| [15:12] | Not used. |
| [11:0] | Data bits. Twos complement, 0.333 mg/LSB. Typical adjustment range = ±0.3 g. |

Gyroscope Automatic Bias Null Calibration

Set GLOB_CMD[0] = 1 (DIN = 0xBE01) to execute the automatic bias null calibration function. This function measures all three gyroscope output registers and then loads each gyroscope offset register with the opposite value to provide a quick bias calibration. All sensor data is then reset to 0, and the flash memory is updated automatically within 50 ms (see Table 17).

Gyroscope Precision Automatic Bias Null Calibration

Set GLOB_CMD[4] = 1 (DIN = 0xBE10) to execute the precision automatic bias null calibration function. This function takes the sensor offline for 30 sec while it collects a set of data and calculates more accurate bias correction factors for each gyroscope. After this function is executed, the newly calculated correction factor is loaded into the gyroscope offset registers, all sensor data is reset to 0, and the flash memory is updated automatically within 50 ms (see Table 17).

Restoring Factory Calibration

Set GLOB_CMD[1] = 1 (DIN = 0xBE02) to execute the factory calibration restore function. This function resets each user calibration register to 0x0000 (see Table 15 and Table 16), resets all sensor data to 0, and automatically updates the flash memory within 50 ms (see Table 17).

Linear Acceleration Bias Compensation (Gyroscope)

Set MSC_CTRL[7] = 1 (DIN = 0xB486) to enable correction for low frequency acceleration influences on gyroscope bias. Note that the DIN sequence also preserves the factory default condition for the data ready function (see Table 22).

OPERATIONAL CONTROL

Global Commands

The GLOB_CMD register provides trigger bits for several useful functions. Setting the assigned bit to 1 starts each operation, which returns the bit to 0 after completion. For example, set GLOB_CMD[7] = 1 (DIN = 0xBE80) to execute a software reset, which stops the sensor operation and runs the device through its start-up sequence. This sequence includes loading the control registers with their respective flash memory locations prior to producing new data. Reading the GLOB_CMD register (DIN = 0x3E00) starts the burst read sequence.

Table 17. GLOB_CMD Bit Descriptions

| Bit | Description |
|--------|-------------------------------------|
| [15:8] | Not used |
| [7] | Software reset command |
| [6:5] | Not used |
| [4] | Precision autonull command |
| [3] | Flash update command |
| [2] | Auxiliary DAC data latch |
| [1] | Factory calibration restore command |
| [0] | Autonull command |

Internal Sample Rate

The SMPL_PRD register provides discrete sample rate settings using the bit assignments in Table 18 and the following equation:

$$t_s = t_b \times (N_s + 1)$$

For example, when SMPL_PRD[7:0] = 0x0A, the sample rate is 149 SPS.

Table 18. SMPL_PRD Bit Descriptions

| Bit | Description (Default = 0x0001) |
|--------|--|
| [15:8] | Not used |
| [7] | Time base (t_b) 0 = 0.61035 ms, 1 = 18.921 ms |
| [6:0] | Increment setting (N_s) Internal sample period = $t_s = t_b \times (N_s + 1)$ |

The default sample rate setting of 819.2 SPS preserves the sensor bandwidth and provides optimal performance. For systems that value slower sample rates, keep the internal sample rate at 819.2 SPS. Use the programmable filter (SENS_AVG) to reduce the bandwidth, which helps to prevent aliasing. The data ready function (MSC_CTRL) can drive an interrupt routine that uses a counter to help ensure data coherence at the reduced rates.

Power Management

Setting SMPL_PRD \geq 0x0A also sets the sensor to low power mode. For systems that require lower power dissipation, in-system characterization helps users to quantify the associated performance trade-offs. In addition to sensor performance, this mode affects SPI data rates (see Table 2). Set SLP_CNT[8] = 1 (DIN = 0xBB01) to start the indefinite sleep mode, which requires a \overline{CS} assertion (high to low), reset, or power cycle to wake up. Use SLP_CNT[7:0] to put the device into sleep mode for a specified period. For example, SLP_CNT[7:0] = 0x64 (DIN = 0xBA64) puts the ADIS16362 to sleep for 50 sec.

Table 19. SLP_CNT Bit Descriptions

| Bit | Description |
|--------|---|
| [15:9] | Not used |
| [8] | Indefinite sleep mode; set to 1 |
| [7:0] | Programmable sleep time bits, 0.5 sec/LSB |

Sensor Bandwidth

The signal chain for each MEMS sensor has several filter stages, which shape their frequency response. Figure 14 provides a block diagram for both gyroscope and accelerometer signal paths. Table 20 provides additional information for digital filter configuration.

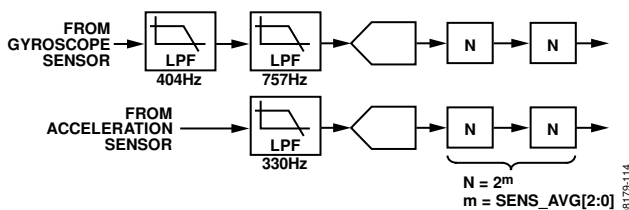


Figure 14. MEMS Analog and Digital Filters

Digital Filtering

The N blocks in Figure 14 are part of the programmable low-pass filter, which provides additional noise reduction on the inertial sensor outputs. This filter contains two cascaded averaging filters that provide a Bartlett window, FIR filter response (see Figure 15). For example, set SENS_AVG[2:0] = 100 (DIN = 0xB804) to set each stage to 16 taps. When used with the default sample rate of 819.2 SPS, this value reduces the sensor bandwidth to approximately 16 Hz.

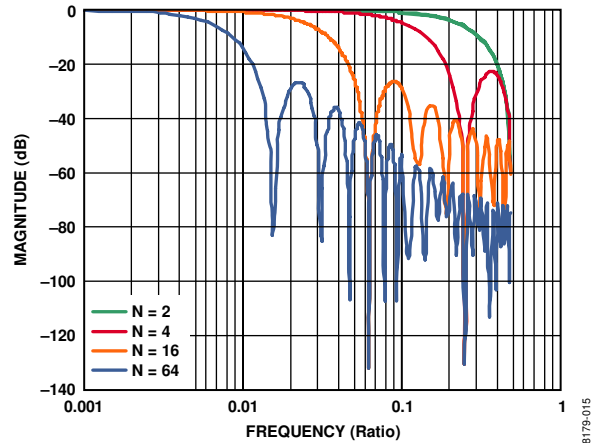


Figure 15. Bartlett Window, FIR Filter Frequency Response (Phase Delay = N Samples)

Dynamic Range

The SENS_AVG[10:8] bits provide three dynamic range settings for this gyroscope. The lower dynamic range settings ($\pm 75^\circ/\text{sec}$ and $\pm 150^\circ/\text{sec}$) limit the minimum filter tap sizes to maintain resolution. For example, set SENS_AVG[10:8] = 010 (DIN = 0xB902) for a measurement range of $\pm 150^\circ/\text{sec}$. Because this setting can influence the filter settings, program SENS_AVG[10:8] and then SENS_AVG[2:0] if more filtering is required.

Table 20. SENS_AVG Bit Descriptions

| Bit | Description |
|---------|---|
| [15:11] | Not used |
| [10:8] | Measurement range (sensitivity) selection 100 = $\pm 300^\circ/\text{sec}$ (default condition) 010 = $\pm 150^\circ/\text{sec}$, filter taps ≥ 4 (Bits[2:0] \geq 0x02) 001 = $\pm 75^\circ/\text{sec}$, filter taps ≥ 16 (Bits[2:0] \geq 0x04) |
| [7:3] | Not used |
| [2:0] | Number of taps in each stage, $N = 2^m$ |

INPUT/OUTPUT FUNCTIONS

General-Purpose I/O

DIO1, DIO2, DIO3, and DIO4 are configurable, general-purpose I/O lines that serve multiple purposes according to the following control register priority: MSC_CTRL, ALM_CTRL, and GPIO_CTRL. For example, set GPIO_CTRL = 0x080C (DIN = 0xB308, and then 0xB20C) to configure DIO1 and DIO2 as inputs and DIO3 and DIO4 as outputs, with DIO3 set low and DIO4 set high.

In this configuration, read GPIO_CTRL (DIN = 0x3200). The digital state of DIO1 and DIO2 is in GPIO_CTRL[9:8].

Table 21. GPIO_CTRL Bit Descriptions

| Bit | Description |
|---------|---|
| [15:12] | Not used |
| [11] | General-Purpose I/O Line 4 (DIO4) data level |
| [10] | General-Purpose I/O Line 3 (DIO3) data level |
| [9] | General-Purpose I/O Line 2 (DIO2) data level |
| [8] | General-Purpose I/O Line 1 (DIO1) data level |
| [7:4] | Not used |
| [3] | General-Purpose I/O Line 4 (DIO4) direction control (1 = output, 0 = input) |
| [2] | General-Purpose I/O Line 3 (DIO3) direction control (1 = output, 0 = input) |
| [1] | General-Purpose I/O Line 2 (DIO2) direction control (1 = output, 0 = input) |
| [0] | General-Purpose I/O Line 1 (DIO1) direction control (1 = output, 0 = input) |

Input Clock Configuration

The input clock function allows for external control oversampling in the ADIS16362. Set GPIO_CTRL[3] = 0 (DIN = 0x0B200) and SMPL_PRD[7:0] = 0x00 (DIN = 0xB600) to enable this function. See Table 2 and Figure 4 for timing information.

Data Ready I/O Indicator

The factory default sets DIO1 as a positive data ready indicator signal. The MSC_CTRL[2:0] bits provide configuration options for changing the default. For example, set MSC_CTRL[2:0] = 100 (DIN = 0xB404) to change the polarity of the data ready signal on DIO1 for interrupt inputs that require negative logic inputs for activation. The pulse width is between 100 μ s and 200 μ s over all conditions.

Table 22. MSC_CTRL Bit Descriptions

| Bit | Description |
|---------|--|
| [15:12] | Not used |
| [11] | Memory test (cleared upon completion) (1 = enabled, 0 = disabled) |
| [10] | Internal self-test enable (cleared upon completion) (1 = enabled, 0 = disabled) |
| [9] | Manual self-test, negative stimulus (1 = enabled, 0 = disabled) |
| [8] | Manual self-test, positive stimulus (1 = enabled, 0 = disabled) |
| [7] | Linear acceleration bias compensation for gyroscopes (1 = enabled, 0 = disabled) |
| [6] | Linear accelerometer origin alignment (1 = enabled, 0 = disabled) |
| [5:3] | Not used |
| [2] | Data ready enable (1 = enabled, 0 = disabled) |
| [1] | Data ready polarity (1 = active high, 0 = active low) |
| [0] | Data ready line select (1 = DIO2, 0 = DIO1) |

Auxiliary DAC

The 12-bit AUX_DAC line can drive its output to within 5 mV of the ground reference when it is not sinking current. As the output approaches 0 V, the linearity begins to degrade (~100 LSB beginning point). As the sink current increases, the nonlinear range increases. The DAC latch command moves the values of the AUX_DAC register into the DAC input register, enabling both bytes to take effect at the same time.

Table 23. AUX_DAC Bit Descriptions

| Bit | Description |
|---------|--|
| [15:12] | Not used |
| [11:0] | Data bits, scale factor = 0.8059 mV/LSB Offset binary format, 0 V = 0 LSB |

Table 24. Setting AUX_DAC = 1 V

| DIN | Description |
|--------|---|
| 0xB0D9 | AUX_DAC[7:0] = 0xD9 (217 LSB). |
| 0xB104 | AUX_DAC[15:8] = 0x04 (1024 LSB). |
| 0xBE04 | GLOB_CMD[2] = 1. Move values into the DAC input register, resulting in a 1 V output level. |

DIAGNOSTICS

Self-Test

The self-test function allows the user to verify the mechanical integrity of each MEMS sensor. It applies an electrostatic force to each sensor element, which results in mechanical displacement that simulates a response to actual motion. Table 1 lists the expected response for each sensor, which provides pass/fail criteria. Set MSC_CTRL[10] = 1 (DIN = 0xB504) to run the internal self-test routine, which exercises all inertial sensors, measures each response, makes pass/fail decisions, and reports them to error flags in the DIAG_STAT register. MSC_CTRL[10] resets itself to 0 after completing the routine. The MSC_CTRL[9:8] bits provide manual control over the self-test function for investigation of potential failures. Table 25 outlines an example test flow for using this option to verify the x-axis gyroscope function.

Table 25. Manual Self-Test Example Sequence

| DIN | Description |
|--------|---|
| 0xB601 | SMPL_PRD[7:0] = 0x01, sample rate = 819.2 SPS |
| 0xB904 | SENS_AVG[15:8] = 0x04, gyro range = $\pm 300^\circ/\text{sec}$ |
| 0xB802 | SENS_AVG[7:0] = 0x02, four-tap averaging filter Delay = 50 ms |
| 0x0400 | Read XGYRO_OUT |
| 0xB502 | MSC_CTRL[9] = 1, gyroscope negative self-test Delay = 50 ms |
| 0x0400 | Read XGYRO_OUT Determine whether the bias in the gyroscope output changed according to the self-test response specified in Table 1 |
| 0xB501 | MSC_CTRL[9:8] = 01, gyroscope/accelerometer positive self-test Delay = 50 ms |
| 0x0400 | Read XGYRO_OUT Determine whether the bias in the gyroscope output changed according to the self-test response specified in Table 1 |
| 0xB500 | MSC_CTRL[15:8] = 0x00 |

Zero motion provides results that are more reliable. The settings in Table 25 are flexible and allow for optimization around speed and noise influence. For example, using fewer filtering taps decreases delay times but increases the possibility of noise influence.

Memory Test

Setting MSC_CTRL[11] = 1 (DIN = 0xB508) performs a checksum verification of the flash memory locations. The pass/fail result is loaded into DIAG_STAT[6].

Status

The error flags provide indicator functions for common system level issues. All of the flags are cleared (set to 0) after each DIAG_STAT register read cycle. If an error condition remains, the error flag returns to 1 during the next sample cycle. The DIAG_STAT[1:0] bits do not require a read of this register to return to 0. If the power supply voltage goes back into range, these two flags are cleared automatically.

Table 26. DIAG_STAT Bit Descriptions

| Bit | Description |
|------|--|
| [15] | Z-axis accelerometer self-test failure (1 = fail, 0 = pass) |
| [14] | Y-axis accelerometer self-test failure (1 = fail, 0 = pass) |
| [13] | X-axis accelerometer self-test failure (1 = fail, 0 = pass) |
| [12] | Z-axis gyroscope self-test failure (1 = fail, 0 = pass) |
| [11] | Y-axis gyroscope self-test failure (1 = fail, 0 = pass) |
| [10] | X-axis gyroscope self-test failure (1 = fail, 0 = pass) |
| [9] | Alarm 2 status (1 = active, 0 = inactive) |
| [8] | Alarm 1 status (1 = active, 0 = inactive) |
| [7] | Not used |
| [6] | Flash test, checksum flag (1 = fail, 0 = pass) |
| [5] | Self-test diagnostic error flag (1 = fail, 0 = pass) |
| [4] | Sensor overrange (1 = fail, 0 = pass) |
| [3] | SPI communication failure (1 = fail, 0 = pass) |
| [2] | Flash update failure (1 = fail, 0 = pass) |
| [1] | Power supply > 5.25 V (1 = power supply > 5.25 V, 0 = power supply \leq 5.25 V) |
| [0] | Power supply < 4.75 V (1 = power supply < 4.75 V, 0 = power supply \geq 4.75 V) |

Alarm Registers

The alarm function provides monitoring for two independent conditions. The ALM_CTRL register provides control inputs for data source, data filtering (prior to comparison), static comparison, dynamic rate-of-change comparison, and output indicator configurations. The ALM_MAGx registers establish the trigger threshold and polarity configurations. Table 30 gives an example of how to configure a static alarm. The ALM_SMPLx registers provide the numbers of samples to use in the dynamic rate-of-change configuration. The period equals the number in the ALM_SMPLx register multiplied by the sample period time, which is established by the SMPL_PRD register. See Table 31 for an example of how to configure the sensor for this type of function.

Table 27. ALM_MAG1, ALM_MAG2 Bit Descriptions

| Bit | Description |
|--------|---|
| [15] | Comparison polarity (1 = greater than, 0 = less than) |
| [14] | Not used |
| [13:0] | Data bits that match the format of the trigger source selection |

Table 28. ALM_SMPL1, ALM_SMPL2 Bit Descriptions

| Bit | Description |
|--------|---|
| [15:8] | Not used |
| [7:0] | Data bits: number of samples (both 0x00 and 0x01 = 1) |

Table 29. ALM_CTRL Bit Descriptions

| Bit | Description |
|---------|--|
| [15:12] | Alarm 2 source selection 0000 = disable 0001 = power supply output 0010 = x-axis gyroscope output 0011 = y-axis gyroscope output 0100 = z-axis gyroscope output 0101 = x-axis accelerometer output 0110 = y-axis accelerometer output 0111 = z-axis accelerometer output 1000 = x-axis gyroscope temperature output 1001 = y-axis gyroscope temperature output 1010 = z-axis gyroscope temperature output 1011 = auxiliary ADC input |
| [11:8] | Alarm 1 source selection (same as Alarm 2) |
| [7] | Rate-of-change (ROC) enable for Alarm 2 (1 = rate of change, 0 = static level) |
| [6] | Rate-of-change (ROC) enable for Alarm 1 (1 = rate of change, 0 = static level) |
| [5] | Not used |
| [4] | Comparison data filter setting (1 = filtered data, 0 = unfiltered data) |
| [3] | Not used |
| [2] | Alarm output enable (1 = enabled, 0 = disabled) |
| [1] | Alarm output polarity (1 = active high, 0 = active low) |
| [0] | Alarm output line select (1 = DIO2, 0 = DIO1) |

Table 30. Alarm Configuration Example 1

| DIN | Description |
|-------------------|---|
| 0xAF55, 0xAE17 | ALM_CTRL = 0x5517 Alarm 1 input = XACCL_OUT Alarm 2 input = XACCL_OUT Static level comparison, filtered data DIO2 output indicator, positive polarity |
| 0xA785, 0xA6DE | ALM_MAG1 = 0x85DE Alarm 1 is true if XACCL_OUT > +0.5 g |
| 0xA93A, 0xA822 | ALM_MAG2 = 0x3A22 Alarm 2 is true if XACCL_OUT < -0.5 g |

Table 31. Alarm Configuration Example 2

| DIN | Description |
|-------------------|---|
| 0xAF76, 0xAE87 | ALM_CTRL = 0x7687 Alarm 1 input = YACCL_OUT Alarm 2 input = ZACCL_OUT Rate-of-change comparison, unfiltered data DIO2 output indicator, positive polarity |
| 0xB601 | SMPL_PRD = 0x0001 Sample rate = 819.2 SPS |
| 0xAA08 | ALM_SMPL1 = 0x0008 Alarm 1 rate-of-change period = 9.77 ms |
| 0xAC50 | ALM_SMPL2 = 0x0050 Alarm 2 rate-of-change period = 97.7 ms |
| 0xA785, 0xA6DE | ALM_MAG1 = 0x85DE Alarm 1 is true if XACCL_OUT > +0.5 g |
| 0xA93A, 0xA822 | ALM_MAG2 = 0x3A22 Alarm 2 is true if XACCL_OUT < -0.5 g |

PRODUCT IDENTIFICATION

Table 32 provides a summary of the registers that identify the product: PROD_ID, which identifies the product type; LOT_ID1 and LOT_ID2, the 32-bit lot identification code; and SERIAL_NUM, which displays the 12-bit serial number. All four registers are two bytes in length. When using the SERIAL_NUM value to calculate the serial number, mask off the upper four bits and convert the remaining 12 bits to a decimal number.

Table 32. Identification Registers

| Register Name | Address | Description |
|---------------|---------|--|
| LOT_ID1 | 0x52 | Lot Identification Code 1 |
| LOT_ID2 | 0x54 | Lot Identification Code 2 |
| PROD_ID | 0x56 | Product identification = 0x3FEA (hexadecimal number for 16,362) |
| SERIAL_NUM | 0x58 | Serial number, 0 to 4095 |

APPLICATIONS INFORMATION

INSTALLATION/HANDLING

For ADIS16362 installation, use the following two-step process:

1. Secure the baseplate using machine screws.
2. Press the connector into its mate.

For removal,

1. Gently pry the connector from its mate using a small slot screwdriver.
2. Remove the screws and lift the part up.

Never attempt to unplug the connector by pulling on the plastic case or baseplate. Although the flexible connector is very reliable in normal operation, it can break when subjected to unreasonable handling. When broken, the flexible connector cannot be repaired. The AN-1041 Application Note provides more information about developing an appropriate mechanical interface design.

GYROSCOPE BIAS OPTIMIZATION

The factory calibration addresses initial bias errors along with temperature-dependent bias behaviors. Installation and certain environmental conditions can introduce modest bias errors. The precision autonull command (GLOB_CMD[4]) provides a simple predeployment method for correcting these errors to an accuracy of approximately 0.008°/sec, using an average of 30 sec. Averaging the sensor output data for 100 sec can provide incremental performance gains, as well. Controlling device rotation, power supply, and temperature during these averaging times helps to ensure optimal accuracy during this process. Refer to the AN-1041 Application Note for more information about optimizing performance.

INPUT ADC CHANNEL

The AUX_ADC register provides access to the auxiliary ADC input channel. The ADC is a 12-bit successive approximation converter that has an input circuit equivalent to the one shown in Figure 16. The maximum input is 3.3 V. The ESD protection diodes can handle 10 mA without causing irreversible damage. The on resistance (R1) of the switch has a typical value of 100 Ω. The sampling capacitor, C2, has a typical value of 16 pF.

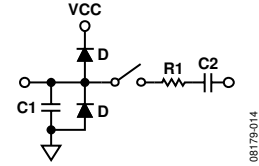
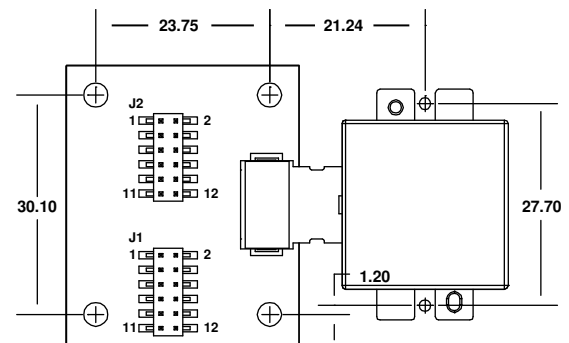


Figure 16. Equivalent Analog Input Circuit (Conversion Phase: Switch Open, Track Phase: Switch Closed)

INTERFACE PRINTED CIRCUIT BOARD (PCB)

The ADIS16362/PCBZ includes one ADIS16362BLMZ and one interface PCB. The interface PCB simplifies the process of integrating the ADIS16362BMLZ into an existing processor system.

J1 and J2 are dual-row, 2 mm (pitch) connectors that work with a number of ribbon cable systems, including 3M Part Number 152212-0100-GB (ribbon crimp connector) and 3M Part Number 3625/12 (ribbon cable). Figure 17 provides a hole pattern design for installing the ADIS16362BMLZ and the interface PCB onto the same surface. Figure 18 provides the pin assignments for each connector. The pin descriptions match those listed in Table 5. The ADIS16362 does not require external capacitors for normal operation, so the interface PCB does not use the C1/C2 pads (not shown in Figure 17).



NOTES
1. DIMENSIONS IN MILLIMETERS.

Figure 17. Physical Diagram for the ADIS16362/PCBZ

| J1 | | | | J2 | | | |
|-----|----|----|------|---------|----|----|------|
| RST | 1 | 2 | SCLK | AUX_ADC | 1 | 2 | GND |
| CS | 3 | 4 | DOUT | AUX_DAC | 3 | 4 | DIO3 |
| DNC | 5 | 6 | DIN | GND | 5 | 6 | DIO4 |
| GND | 7 | 8 | GND | DNC | 7 | 8 | DNC |
| GND | 9 | 10 | VCC | DNC | 9 | 10 | DNC |
| VCC | 11 | 12 | VCC | DIO2 | 11 | 12 | DIO1 |

Figure 18. J1/J2 Pin Assignments

OUTLINE DIMENSIONS

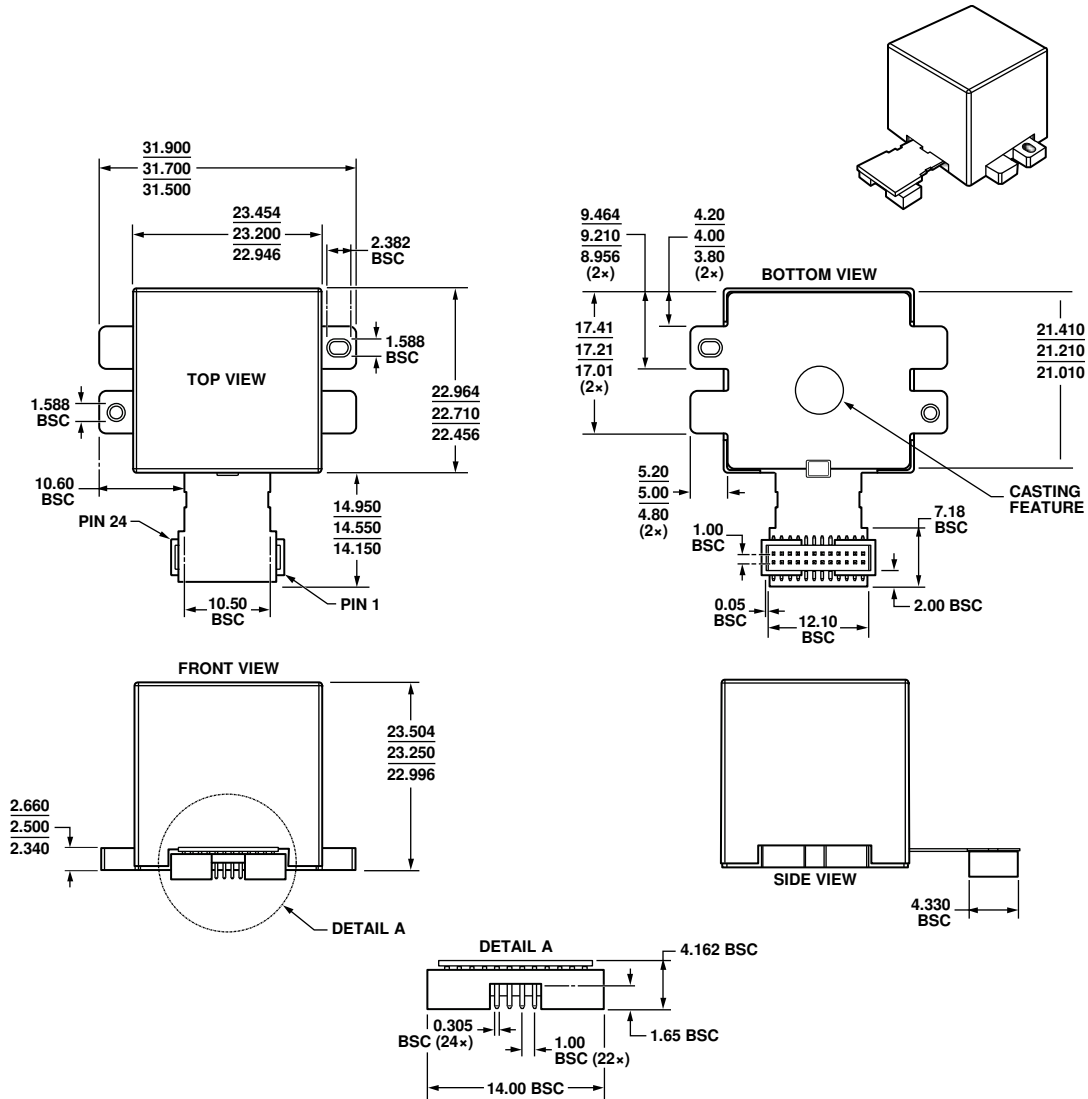


Figure 19. 24-Lead Module with Connector Interface (ML-24-2)
Dimensions shown in millimeters

122208-C

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option |
|--------------------|-------------------|---|----------------|
| ADIS16362BMLZ | -40°C to +105°C | 24-Lead Module with Connector Interface | ML-24-2 |
| ADIS16362/PCBZ | | Interface Board | |

¹ Z = RoHS Compliant Part.

NOTES

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