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Tactical Grade, Six Degrees of Freedom Inertial Sensor

Data Sheet **ADIS16485**

FEATURES

Triaxial, digital gyroscope, ±450°/sec dynamic range
- **±0.05° orthogonal alignment error**
- **6°/hr in-run bias stability**
- **0.3°/√hr angular random walk**
- **0.01% nonlinearity**

Triaxial, digital accelerometer, ±5 *g*
Triaxial, delta angle, and delta velocity outputs
Fast start-up time, ~500 ms
Factory calibrated sensitivity, bias, and axial alignment
- **Calibration temperature range: −40°C to +85°C**

SPI-compatible serial interface
Embedded temperature sensor
Programmable operation and control
- **Automatic and manual bias correction controls**
- **4 FIR filter banks, 120 configurable taps**
- **Digital I/O: data-ready alarm indicator, external clock**
- **Alarms for condition monitoring**
- **Power-down/sleep mode for power management**
- **Optional external sample clock input: up to 2.4 kHz**
- **Single command self test**

Single-supply operation: 3.0 V to 3.6 V
2000 *g* shock survivability
Operating temperature range: −40°C to +105°C

APPLICATIONS

Platform stabilization and control
Navigation
Personnel tracking
Instruments
Robotics

GENERAL DESCRIPTION

The ADIS16485 *i*Sensor® device is a complete inertial system that includes a triaxial gyroscope and a triaxial accelerometer. Each inertial sensor in the ADIS16485 combines industry-leading *i*MEMS® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyroscope bias). As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements.

The ADIS16485 provides a simple, cost-effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The SPI and register structure provide a simple interface for data collection and configuration control.

The ADIS16485 uses the same footprint and connector system as the ADIS16375, ADIS16488, and ADIS16488A, which greatly simplifies the upgrade process. It comes in a module that is approximately 47 mm × 44 mm × 14 mm and has a standard connector interface.

FUNCTIONAL BLOCK DIAGRAM

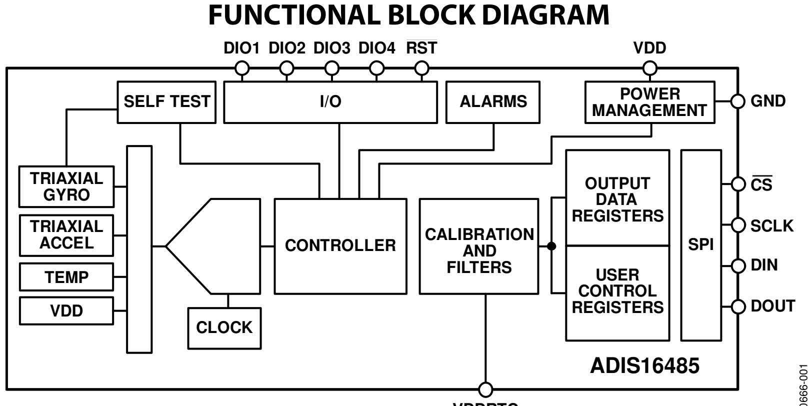

Figure 1.

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EVALUATION KITS

- Breakout Board for the ADIS1613x, ADIS1637x, ADIS1648x and ADIS1649x
- EVAL-ADIS Evaluation System

DOCUMENTATION

Application Notes

- AN-1295: Mechanical Design Tips for ADIS16375, ADIS16480, ADIS16485, and ADIS16488

Data Sheet

- ADIS16485: Tactical Grade, Six Degrees of Freedom Inertial Sensor Data Sheet

User Guides

- ADIS1648x Evaluation on the EVAL-ADIS System

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADIS16480 IIO Inertial Measurement Unit Linux Driver
- IMU Evaluation Software for the EVAL-ADISx Platforms
- USB Driver File for EVAL-ADISx Platforms (v2.2.95.68, 3/9/2016)

REFERENCE MATERIALS

Customer Case Studies

- Trusted Positioning Inc. Integrates iSensor MEMS IMU into Continuous, Accurate, Affordable Positioning and Navigation Platform Solutions

Press

- 10-DoF MEMS IMU Incorporates Sensor Fusion Algorithm for Exceptionally Precise Orientation Sensing in Industrial, Defense and Avionics Applications

Technical Articles

- Designing For Low Noise Feedback Control With Mems Gyroscopes
- INS Faceoff: MEMS vs FOGs, InsideGNSS, July/Aug 2012
- MS-2432 The Battle Between MEMS and FOGs for Precision Guidance
- MS-2694: Enabling Next-Generation Avionics Systems

DESIGN RESOURCES

- ADIS16485 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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TABLE OF CONTENTS

REVISION HISTORY

SPECIFICATIONS

T_A = 25°C, VDD = 3.3 V, angular rate = 0°/sec, dynamic range = ±450°/sec ± 1 *g*, 300 mbar to 1100 mbar, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±450		±480	°/sec
Sensitivity	x_GYRO_OUT and x_GYRO_LOW (32-bit)		3.052×10^{-7}		°/sec/LSB
Repeatability[1]	−40°C ≤ T_A ≤ +85°C			±1	%
Sensitivity Temperature Coefficient	−40°C ≤ T_A ≤ +85°C, 1 σ		±35		ppm/°C
Misalignment	Axis-to-axis		±0.05		Degrees
	Axis-to-frame (package)		±1.0		Degrees
Nonlinearity	Best fit straight line, FS = 450°/sec		0.01		% of FS
Bias Repeatability[1, 2]	−40°C ≤ T_A ≤ +85°C, 1 σ		±0.2		°/sec
In-Run Bias Stability	1 σ		6.25		°/hr
Angular Random Walk	1 σ		0.3		°/√hr
Bias Temperature Coefficient	−40°C ≤ T_A ≤ +85°C, 1 σ		±0.0025		°/sec/°C
Linear Acceleration Effect on Bias	Any axis, 1 σ (CONFIG[7] = 1)		0.009		°/sec/*g*
Output Noise	No filtering		0.16		°/sec rms
Rate Noise Density	f = 25 Hz, no filtering		0.0066		°/sec/√Hz rms
3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			18		kHz
ACCELEROMETERS	Each axis				
Dynamic Range		±5			*g*
Sensitivity	x_ACCL_OUT and x_ACCL_LOW (32-bit)		3.815×10^{-9}		*g*/LSB
Repeatability[1]	−40°C ≤ T_A ≤ +85°C			±0.5	%
Sensitivity Temperature Coefficient	−40°C ≤ T_A ≤ +85C, 1 σ		±10		ppm/°C
Misalignment	Axis-to-axis		±0.035		Degrees
	Axis-to-frame (package)		±1.0		Degrees
Nonlinearity	Best-fit straight line, ±5 *g*		0.1		% of FS
Bias Repeatability[1, 2]	−40°C ≤ T_A ≤ +85°C, 1 σ		±3		m*g*
In-Run Bias Stability	1 σ		32		μ*g*
Velocity Random Walk	1 σ		0.023		m/sec/√hr
Bias Temperature Coefficient	−40°C ≤ T_A ≤ +85°C		±0.03		m*g*/°C
Output Noise	No filtering		1.25		m*g* rms
Noise Density	f = 25 Hz, no filtering		0.055		m*g*/√Hz rms
3 dB Bandwidth			330		Hz
Sensor Resonant Frequency			5.5		kHz
TEMPERATURE SENSOR					
Scale Factor	Output = 0x0000 at 25°C (±5°C)		0.00565		°C/LSB
LOGIC INPUTS[3]					
Input High Voltage, V_{IH}		2.0			V
Input Low Voltage, V_{IL}				0.8	V
$\overline{CS}$ Wake-Up Pulse Width		20			μs
Logic 1 Input Current, I_{IH}	V_{IH} = 3.3 V			10	μA
Logic 0 Input Current, I_{IL}	V_{IL} = 0 V				
All Pins Except $\overline{RST}$				10	μA
$\overline{RST}$ Pin			0.33		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{SOURCE} = 0.5 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 2.0 mA			0.4	V

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FLASH MEMORY	Endurance[4]	100,000			Cycles
Data Retention[5]	T_J = 85°C	20			Years
FUNCTIONAL TIMES[6]	Time until data is available				
Power-On, Start-Up Time			400 ± 160		ms
Reset Recovery Time[7]			400 ± 160		ms
Sleep Mode Recovery Time			500		µs
Flash Memory Update Time			900		ms
Flash Memory Test Time			66		ms
Automatic Self Test Time	Using internal clock, 100 SPS		12		ms
CONVERSION RATE			2.46		kSPS
Initial Clock Accuracy			0.02		%
Temperature Coefficient			40		ppm/°C
Sync Input Clock[8]		0.7		2.4	kHz
POWER SUPPLY, VDD	Operating voltage range	3.0		3.6	V
Power Supply Current[9]	Normal mode, VDD = 3.3 V, µ ± σ		197		mA
	Sleep mode, VDD = 3.3 V		12.2		mA
	Power-down mode, VDD = 3.3 V		37		µA
POWER SUPPLY, VDDRTC	Operating voltage range	3.0		3.6	V
Real-Time Clock Supply Current	Normal mode, VDDRTC = 3.3 V		13		µA

[1] The repeatability specifications represent analytical projections that are based off of the following drift contributions and conditions: temperature hysteresis (−40°C to +85°C), electronics drift (high temperature operating life test: +110°C, 500 hours), drift from temperature cycling (JESD22, Method A104-C, Method N, 500 cycles, −40°C to +85°C), rate random walk (10 year projection), and broadband noise
[2] Bias repeatability describes a long-term behavior over a variety of conditions. Short-term repeatability is related to the in-run bias stability and noise density specifications.
[3] The digital I/O signals use a 3.3 V system.
[4] Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at −40°C, +25°C, +85°C, and +125°C.
[5] The data retention specification assumes a junction temperature (T_J) of 85°C as per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T_J.
[6] These times do not include thermal settling and internal filter response times, which can affect overall accuracy.
[7] The $\overline{\text{RST}}$ line must be in a low state for at least 10 µs to assure a proper reset initiation and recovery.
[8] The device functions at clock rates below 0.7 kHz but at reduced performance levels.
[9] Supply current transients can reach 600 mA during start-up and reset recovery.

TIMING SPECIFICATIONS

T_A = 25°C, VDD = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Description	Normal Mode Min[1]	Typ	Max[1]	Unit
f_{SCLK}	Serial clock	0.01		15	MHz
t_{STALL}[2]	Stall period between data communication cycles	2			μs
t_{CLS}	Serial clock low period	31			ns
t_{CHS}	Serial clock high period	31			ns
$t_{\overline{CS}}$	Chip select to clock edge	32			ns
t_{DAV}	DOUT valid after SCLK edge			10	ns
t_{DSU}	DIN setup time before SCLK rising edge	2			ns
t_{DHD}	DIN hold time after SCLK rising edge	2			ns
t_{DR}, t_{DF}	DOUT rise/fall times, ≤100 pF loading		3	8	ns
t_{DSOE}	$\overline{CS}$ assertion to data out active	0		11	ns
t_{HD}	SCLK edge to data out invalid	0			ns
t_{SFS}	Last SCLK edge to $\overline{CS}$ deassertion	32			ns
t_{DSHI}	$\overline{CS}$ deassertion to data out high impedance	0		9	ns
t_1	Input sync pulse width	5			μs
t_2	Input sync to data invalid		510		μs
t_3	Input sync period	417			μs

[1] Guaranteed by design and characterization, but not tested in production.
[2] See Table 3 for exceptions to the stall time rating.

Table 3. Register Specific Stall Times

Register	Function	Minimum Stall Time (μs)
FNCTIO_CTRL	Configure DIOx functions	60
FLTR_BNK0	Enable/select FIR filter banks	320
FLTR_BNK1	Enable/select FIR filter banks	320
NULL_CFG	Configure autonull bias function	10
GLOB_CMD[1]	Self test	12,000
GLOB_CMD[2]	Memory test	50,000
GLOB_CMD[3]	Flash memory update	375,000
GLOB_CMD[6]	Flash memory test	75,000
GLOB_CMD[7]	Software reset	12,000

Timing Diagrams

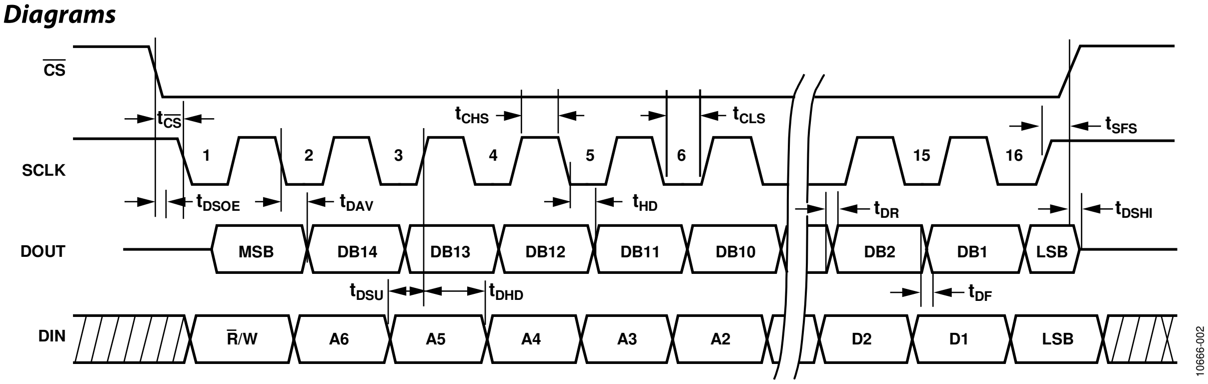


Figure 2. SPI Timing and Sequence

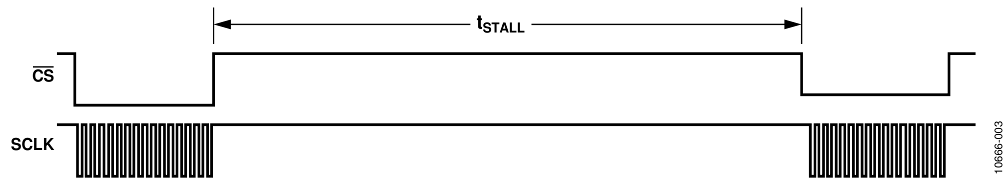


Figure 3. Stall Time and Data Rate

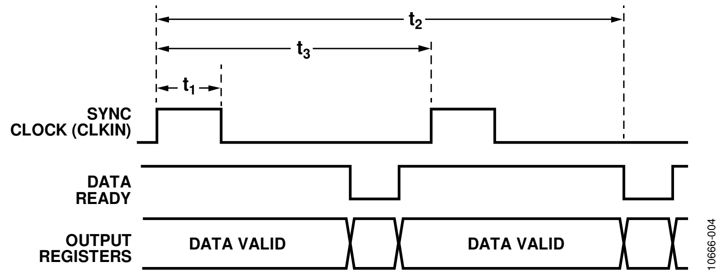


Figure 4. Input Clock Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VDD to GND	−0.3 V to +3.6 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.2 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.2 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C[1]

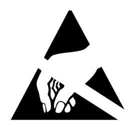
[1] Extended exposure to temperatures that are lower than −40°C or higher than +105°C can adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 5. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
24-Lead Module (ML-24-6)	22.8°C/W	10.1°C/W	48 *g*

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

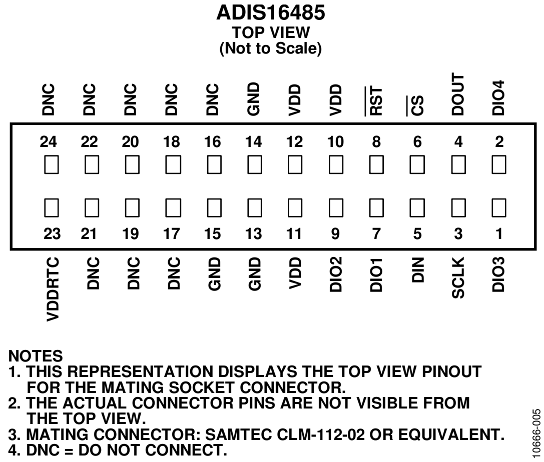


Figure 5. Mating Connector Pin Assignments

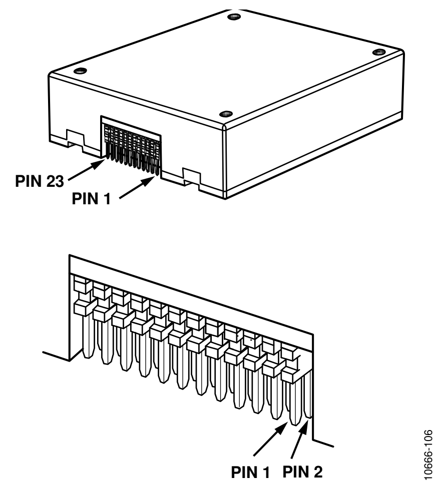


Figure 6. Axial Orientation (Top Side Facing Up)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	DIO3	Input/output	Configurable Digital Input/Output.
2	DIO4	Input/output	Configurable Digital Input/Output.
3	SCLK	Input	SPI Serial Clock.
4	DOUT	Output	SPI Data Output. Clocks output on SCLK falling edge.
5	DIN	Input	SPI Data Input. Clocks input on SCLK rising edge.
6	$\overline{\text{CS}}$	Input	SPI Chip Select.
7	DIO1	Input/output	Configurable Digital Input/Output.
8	$\overline{\text{RST}}$	Input	Reset.
9	DIO2	Input/output	Configurable Digital Input/Output.
10, 11, 12	VDD	Supply	Power Supply.
13, 14, 15	GND	Supply	Power Ground.
16 to 22, 24	DNC	Not applicable	Do Not Connect to These Pins.
23	VDDRTC	Supply	Real-Time Clock Power Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

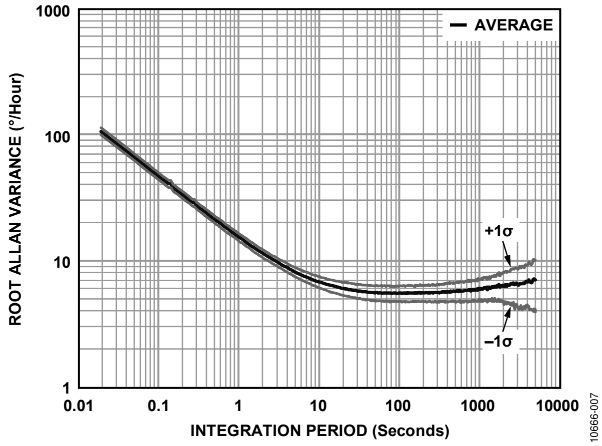


Figure 7. Gyroscope Allan Variance, 25°C

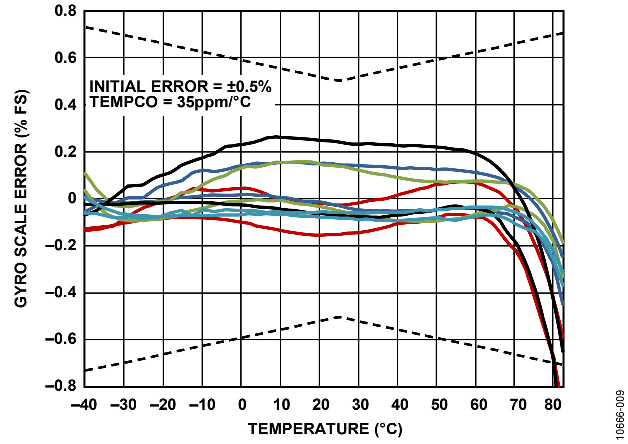


Figure 9. Gyroscope Scale (Sensitivity) Error and Hysteresis vs. Temperature

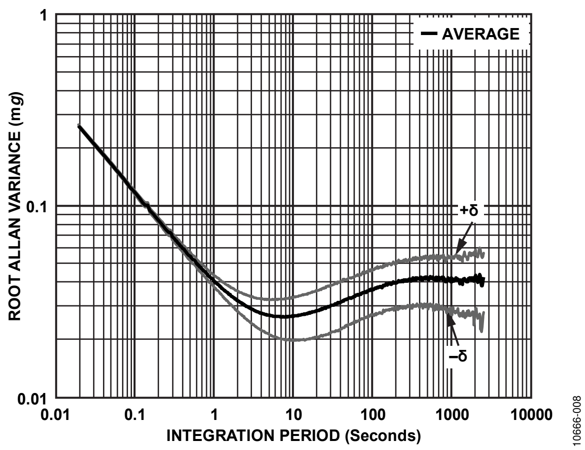


Figure 8. Accelerometer Allan Variance, 25°C

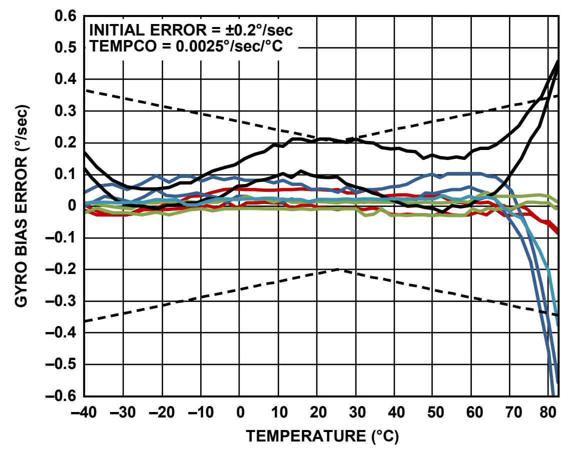


Figure 10. Gyroscope Bias Error and Hysteresis vs. Temperature

BASIC OPERATION

The ADIS16485 is an autonomous sensor system that starts up on its own when it has a valid power supply. After running through its initialization process, it begins sampling, processing, and loading calibrated sensor data into the output registers, which are accessible using the SPI port. The SPI port typically connects to a compatible port on an embedded processor, using the connection diagram in Figure 11. The four SPI signals facilitate synchronous, serial data communication. Connect $\overline{RST}$ (Pin 8, see Table 6) to VDD or leave $\overline{RST}$ open for normal operation. The factory default configuration provides users with a data-ready signal on the DIO2 pin, which pulses high when new data is available in the output data registers.

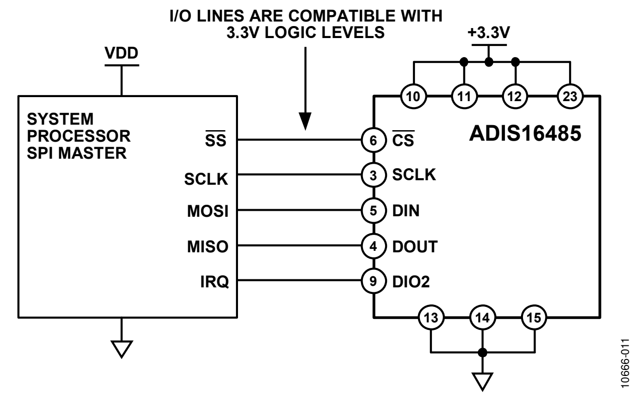


Figure 11. Electrical Connection Diagram

Table 7. Generic Master Processor Pin Names and Functions

Mnemonic	Function
$\overline{SS}$	Slave select
IRQ	Interrupt request
MOSI	Master output, slave input
MISO	Master input, slave output
SCLK	Serial clock

Embedded processors typically use control registers to configure their serial ports for communicating with SPI slave devices such as the ADIS16485. Table 8 provides a list of settings, which describe the SPI protocol of the ADIS16485. The initialization routine of the master processor typically establishes these settings using firmware commands to write them into its serial control registers.

Table 8. Generic Master Processor SPI Settings

Processor Setting	Description
Master	ADIS16485 operates as slave
SCLK ≤ 15 MHz	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), and CPHA = 1 (phase)
MSB-First Mode	Bit sequence
16-Bit Mode	Shift register/data length

REGISTER STRUCTURE

The register structure and SPI port provide a bridge between the sensor processing system and an external, master processor. It contains both output data and control registers. The output data registers include the latest sensor data, a real-time clock, error flags, alarm flags, and identification data. The control registers include sample rate, filtering, input/output, alarms, calibration, and diagnostic configuration options. All communication between the ADIS16485 and an external processor involves either reading or writing to one of the user registers.

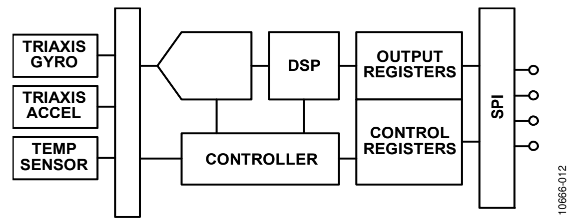


Figure 12. Basic Operation

The register structure uses a paged addressing scheme that is composed of 13 pages, with each one containing 64 register locations. Each register is 16 bits wide, with each byte having its own unique address within the memory map of that page. The SPI port has access to one page at a time, using the bit sequence in Figure 17. Select the page to activate for SPI access by writing its code to the PAGE_ID register. Read the PAGE_ID register to determine which page is currently active. Table 9 displays the PAGE_ID contents for each page, together with their basic functions. The PAGE_ID register is located at Address 0x00 on every page.

Table 9. User Register Page Assignments

Page	PAGE_ID	Function
0	0x00	Output data, clock, identification
1	0x01	Reserved
2	0x02	Calibration
3	0x03	Control: sample rate, filtering, I/O, alarms
4	0x04	Serial number
5	0x05	FIR Filter Bank A Coefficient 0 to Coefficient 59
6	0x06	FIR Filter Bank A, Coefficient 60 to Coefficient 119
7	0x07	FIR Filter Bank B, Coefficient 0 to Coefficient 59
8	0x08	FIR Filter Bank B, Coefficient 60 to Coefficient 119
9	0x09	FIR Filter Bank C, Coefficient 0 to Coefficient 59
10	0x0A	FIR Filter Bank C, Coefficient 60 to Coefficient 119
11	0x0B	FIR Filter Bank D, Coefficient 0 to Coefficient 59
12	0x0C	FIR Filter Bank D, Coefficient 60 to Coefficient 119

SPI COMMUNICATION

The SPI port supports full duplex communication, as shown in Figure 17, which enables external processors to write to DIN while reading DOUT, when the previous command was a read request. Figure 17 provides a guideline for the bit coding on both DIN and DOUT.

DEVICE CONFIGURATION

The SPI provides write access to the control registers, one byte at a time, using the bit assignments shown in Figure 17. Each register has 16 bits, where Bits[7:0] represent the lower address (listed in Table 10) and Bits[15:8] represent the upper address. Write to the lower byte of a register first, followed by a write to its upper byte. The only register that changes with a single write to its lower byte is the PAGE_ID register. For a write command, the first bit in the DIN sequence is set to 1. Address Bits[A6:A0] represent the target address, and Data Command Bits[DC7:DC0] represent the data being written to the location. Figure 13 provides an example of writing 0x03 to Address 0x00 (PAGE_ID [7:0]), using DIN = 0x8003. This write command activates the control page for SPI access.

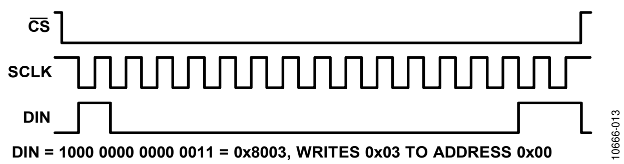


Figure 13. SPI Sequence for Activating the Control Page (DIN = 0x8003)

Dual Memory Structure

Writing configuration data to a control register updates its SRAM contents, which are volatile. After optimizing each relevant control register setting in a system, use the manual flash update command, which is located in GLOB_CMD[3] on Page 3 of the register map. Activate the manual flash update command by turning to Page 3 (DIN = 0x8003) and setting GLOB_CMD[3] = 1 (DIN = 0x8208, then DIN = 0x8300). Make sure that the power supply is within specification for the entire 375 ms processing time for a flash memory update. Table 10 provides a memory map for all of the user registers, which includes a column of flash backup information. A yes in this column indicates that a register has a mirror location in flash and, when backed up properly, automatically restores itself during startup or after a reset. Figure 14 provides a diagram of the dual memory structure used to manage operation and store critical user settings.

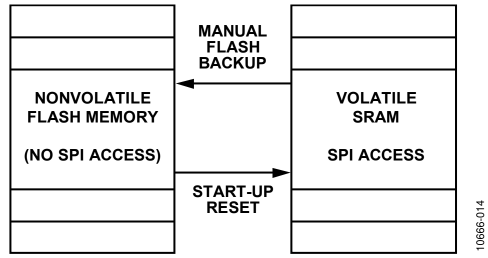


Figure 14. SRAM and Flash Memory Diagram

READING SENSOR DATA

The ADIS16485 automatically starts up and activates Page 0 for data register access. Write 0x00 to the PAGE_ID register (DIN = 0x8000) to activate Page 0 for data access after accessing any other page. A single register read requires two 16-bit SPI cycles. The first cycle requests the contents of a register using the bit assignments in Figure 17, and then the register contents follow DOUT during the second sequence. The first bit in a DIN command is zero, followed by either the upper or the lower address for the register. The last eight bits are don't care, but the SPI requires the full set of 16 SCLKs to receive the request. Figure 15 includes two register reads in succession, which starts with DIN = 0x1A00 to request the contents of the Z_GYRO_OUT register and follows with 0x1800 to request the contents of the Z_GYRO_LOW register.

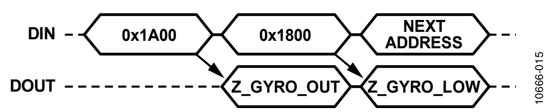


Figure 15. SPI Read Example

Figure 16 provides an example of the four SPI signals when reading PROD_ID in a repeating pattern. This is a good pattern to use for troubleshooting the SPI interface setup and communications because the contents of PROD_ID are predefined and stable.

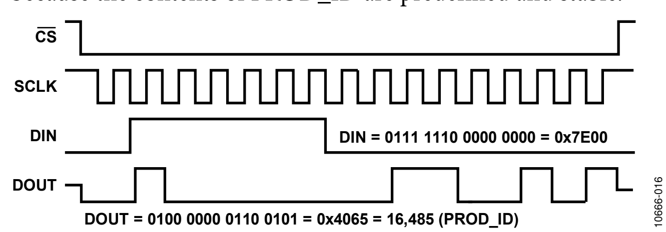


Figure 16. SPI Read Example, Second 16-Bit Sequence

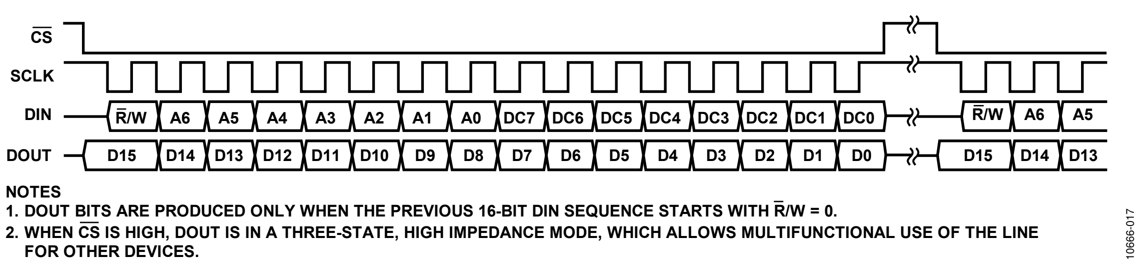


Figure 17. SPI Communication Bit Sequence

USER REGISTERS

Table 10. User Register Memory Map (N/A Means Not Applicable)

Name	R/W	Flash	PAGE_ID	Address	Default	Register Description	Format
PAGE_ID	R/W	No	0x00	0x00	0x00	Page identifier	N/A
Reserved	N/A	N/A	0x00	0x02 to 0x06	N/A	Reserved	N/A
SYS_E_FLAG	R	No	0x00	0x08	0x0000	Output, system error flags	Table 41
DIAG_STS	R	No	0x00	0x0A	0x0000	Output, self test error flags	Table 42
ALM_STS	R	No	0x00	0x0C	0x0000	Output, alarm error flags	Table 43
TEMP_OUT	R	No	0x00	0x0E	N/A	Output, temperature	Table 39
X_GYRO_LOW	R	No	0x00	0x10	N/A	Output, x-axis gyroscope, low word	Table 15
X_GYRO_OUT	R	No	0x00	0x12	N/A	Output, x-axis gyroscope, high word	Table 11
Y_GYRO_LOW	R	No	0x00	0x14	N/A	Output, y-axis gyroscope, low word	Table 16
Y_GYRO_OUT	R	No	0x00	0x16	N/A	Output, y-axis gyroscope, high word	Table 12
Z_GYRO_LOW	R	No	0x00	0x18	N/A	Output, z-axis gyroscope, low word	Table 17
Z_GYRO_OUT	R	No	0x00	0x1A	N/A	Output, z-axis gyroscope, high word	Table 13
X_ACCL_LOW	R	No	0x00	0x1C	N/A	Output, x-axis accelerometer, low word	Table 22
X_ACCL_OUT	R	No	0x00	0x1E	N/A	Output, x-axis accelerometer, high word	Table 18
Y_ACCL_LOW	R	No	0x00	0x20	N/A	Output, y-axis accelerometer, low word	Table 23
Y_ACCL_OUT	R	No	0x00	0x22	N/A	Output, y-axis accelerometer, high word	Table 19
Z_ACCL_LOW	R	No	0x00	0x24	N/A	Output, z-axis accelerometer, low word	Table 24
Z_ACCL_OUT	R	No	0x00	0x26	N/A	Output, z-axis accelerometer, high word	Table 20
Reserved	N/A	N/A	0x00	0x28 to 0x3E	N/A	Reserved	N/A
X_DELTANG_LOW	R	No	0x00	0x40	N/A	Output, x-axis delta angle, low word	Table 29
X_DELTANG_OUT	R	No	0x00	0x42	N/A	Output, x-axis delta angle, high word	Table 25
Y_DELTANG_LOW	R	No	0x00	0x44	N/A	Output, y-axis delta angle, low word	Table 30
Y_DELTANG_OUT	R	No	0x00	0x46	N/A	Output, y-axis delta angle, high word	Table 26
Z_DELTANG_LOW	R	No	0x00	0x48	N/A	Output, z-axis delta angle, low word	Table 31
Z_DELTANG_OUT	R	No	0x00	0x4A	N/A	Output, z-axis delta angle, high word	Table 27
X_DELTVEL_LOW	R	No	0x00	0x4C	N/A	Output, x-axis delta velocity, low word	Table 36
X_DELTVEL_OUT	R	No	0x00	0x4E	N/A	Output, x-axis delta velocity, high word	Table 32
Y_DELTVEL_LOW	R	No	0x00	0x50	N/A	Output, y-axis delta velocity, low word	Table 37
Y_DELTVEL_OUT	R	No	0x00	0x52	N/A	Output, y-axis delta velocity, high word	Table 33
Z_DELTVEL_LOW	R	No	0x00	0x54	N/A	Output, z-axis delta velocity, low word	Table 38
Z_DELTVEL_OUT	R	No	0x00	0x56	N/A	Output, z-axis delta velocity, high word	Table 34
Reserved	N/A	N/A	0x00	0x58 to 0x76	N/A	Reserved	N/A
TIME_MS_OUT	R	Yes	0x00	0x78	N/A	Factory configuration time: minutes/seconds	Table 96
TIME_DH_OUT	R	Yes	0x00	0x7A	N/A	Factory configuration date/time: day/hour	Table 97
TIME_YM_OUT	R	Yes	0x00	0x7C	N/A	Factory configuration date: year/month	Table 98
PROD_ID	R	Yes	0x00	0x7E	0x4065	Output, product identification (16,485)	Table 47
Reserved	N/A	N/A	0x01	0x00 to 0x7E	N/A	Reserved	N/A
PAGE_ID	R/W	No	0x02	0x00	0x00	Page identifier	N/A
Reserved	N/A	N/A	0x02	0x02	N/A	Reserved	N/A
X_GYRO_SCALE	R/W	Yes	0x02	0x04	0x0000	Calibration, scale, x-axis gyroscope	Table 64
Y_GYRO_SCALE	R/W	Yes	0x02	0x06	0x0000	Calibration, scale, y-axis gyroscope	Table 65
Z_GYRO_SCALE	R/W	Yes	0x02	0x08	0x0000	Calibration, scale, z-axis gyroscope	Table 66
X_ACCL_SCALE	R/W	Yes	0x02	0x0A	0x0000	Calibration, scale, x-axis accelerometer	Table 74
Y_ACCL_SCALE	R/W	Yes	0x02	0x0C	0x0000	Calibration, scale, y-axis accelerometer	Table 75
Z_ACCL_SCALE	R/W	Yes	0x02	0x0E	0x0000	Calibration, scale, z-axis accelerometer	Table 76

Name	R/W	Flash	PAGE_ID	Address	Default	Register Description	Format
XG_BIAS_LOW	R/W	Yes	0x02	0x10	0x0000	Calibration, offset, gyroscope, x-axis, low word	Table 60
XG_BIAS_HIGH	R/W	Yes	0x02	0x12	0x0000	Calibration, offset, gyroscope, x-axis, high word	Table 57
YG_BIAS_LOW	R/W	Yes	0x02	0x14	0x0000	Calibration, offset, gyroscope, y-axis, low word	Table 61
YG_BIAS_HIGH	R/W	Yes	0x02	0x16	0x0000	Calibration, offset, gyroscope, y-axis, high word	Table 58
ZG_BIAS_LOW	R/W	Yes	0x02	0x18	0x0000	Calibration, offset, gyroscope, z-axis, low word	Table 62
ZG_BIAS_HIGH	R/W	Yes	0x02	0x1A	0x0000	Calibration, offset, gyroscope, z-axis, high word	Table 59
XA_BIAS_LOW	R/W	Yes	0x02	0x1C	0x0000	Calibration, offset, accelerometer, x-axis, low word	Table 71
XA_BIAS_HIGH	R/W	Yes	0x02	0x1E	0x0000	Calibration, offset, accelerometer, x-axis, high word	Table 68
YA_BIAS_LOW	R/W	Yes	0x02	0x20	0x0000	Calibration, offset, accelerometer, y-axis, low word	Table 72
YA_BIAS_HIGH	R/W	Yes	0x02	0x22	0x0000	Calibration, offset, accelerometer, y-axis, high word	Table 69
ZA_BIAS_LOW	R/W	Yes	0x02	0x24	0x0000	Calibration, offset, accelerometer, z-axis, low word	Table 73
ZA_BIAS_HIGH	R/W	Yes	0x02	0x26	0x0000	Calibration, offset, accelerometer, z-axis, high word	Table 70
Reserved	N/A	N/A	0x02	0x28 to 0x72	N/A	Reserved	N/A
USER_SCR_1	R/W	Yes	0x02	0x74	0x0000	User Scratch Register 1	Table 92
USER_SCR_2	R/W	Yes	0x02	0x76	0x0000	User Scratch Register 2	Table 93
USER_SCR_3	R/W	Yes	0x02	0x78	0x0000	User Scratch Register 3	Table 94
USER_SCR_4	R/W	Yes	0x02	0x7A	0x0000	User Scratch Register 4	Table 95
FLSHCNT_LOW	R	Yes	0x02	0x7C	N/A	Diagnostic, flash memory count, low word	Table 87
FLSHCNT_HIGH	R	Yes	0x02	0x7E	N/A	Diagnostic, flash memory count, high word	Table 88
PAGE_ID	R/W	No	0x03	0x00	0x0000	Page identifier	N/A
GLOB_CMD	W	No	0x03	0x02	N/A	Control, global commands	Table 86
Reserved	N/A	N/A	0x03	0x04	N/A	Reserved	N/A
FNCTIO_CTRL	R/W	Yes	0x03	0x06	0x000D	Control, I/O pins, functional definitions	Table 89
GPIO_CTRL	R/W	Yes	0x03	0x08	0x00X0[1]	Control, I/O pins, general purpose	Table 90
CONFIG	R/W	Yes	0x03	0x0A	0x00C0	Control, clock, and miscellaneous correction	Table 67
DEC_RATE	R/W	Yes	0x03	0x0C	0x0000	Control, output sample rate decimation	Table 49
NULL_CNFG	R/W	Yes	0x03	0x0E	0x070A	Control, automatic bias correction configuration	Table 63
SLP_CNT	R/W	No	0x03	0x10	N/A	Control, power-down/sleep mode	Table 91
Reserved	N/A	N/A	0x03	0x12 to 0x14	N/A	Reserved	N/A
FILTR_BNK_0	R/W	Yes	0x03	0x16	0x0000	Filter selection	Table 50
FILTR_BNK_1	R/W	Yes	0x03	0x18	0x0000	Filter selection	Table 51
Reserved	N/A	N/A	0x03	0x1A to 0x1E	N/A	Reserved	N/A
ALM_CNFG_0	R/W	Yes	0x03	0x20	0x0000	Alarm configuration	Table 83
ALM_CNFG_1	R/W	Yes	0x03	0x22	0x0000	Alarm configuration	Table 84
Reserved	N/A	N/A	0x03	0x24 to 0x26	N/A	Reserved	N/A
XG_ALM_MAGN	R/W	Yes	0x03	0x28	0x0000	Alarm, x-axis gyroscope threshold setting	Table 77
YG_ALM_MAGN	R/W	Yes	0x03	0x2A	0x0000	Alarm, y-axis gyroscope threshold setting	Table 78
ZG_ALM_MAGN	R/W	Yes	0x03	0x2C	0x0000	Alarm, z-axis gyroscope threshold setting	Table 79
XA_ALM_MAGN	R/W	Yes	0x03	0x2E	0x0000	Alarm, x-axis accelerometer threshold	Table 80
YA_ALM_MAGN	R/W	Yes	0x03	0x30	0x0000	Alarm, y-axis accelerometer threshold	Table 81
ZA_ALM_MAGN	R/W	Yes	0x03	0x32	0x0000	Alarm, z-axis accelerometer threshold	Table 82
Reserved	N/A	N/A	0x03	0x34 to 0x76	N/A	Reserved	N/A
FIRM_REV	R	Yes	0x03	0x78	N/A	Firmware revision	Table 44
FIRM_DM	R	Yes	0x03	0x7A	N/A	Firmware programming date: day/month	Table 45
FIRM_Y	R	Yes	0x03	0x7C	N/A	Firmware programming date: year	Table 46
Reserved	N/A	N/A	0x03	0x7E	N/A	Reserved	N/A
Reserved	N/A	N/A	0x04	0x00 to 0x18	N/A	Reserved	N/A
SERIAL_NUM	R	Yes	0x04	0x20	N/A	Serial number	Table 48
Reserved	N/A	N/A	0x04	0x22 to 0x7F	N/A	Reserved	N/A

Name	R/W	Flash	PAGE_ID	Address	Default	Register Description	Format
PAGE_ID	R/W	No	0x05	0x00	0x0000	Page identifier	N/A
FIR_COEF_Axxx	R/W	Yes	0x05	0x02 to 0x7E	N/A	FIR Filter Bank A, Coefficients 0 through 59	Table 52
PAGE_ID	R/W	No	0x06	0x00	0x0000	Page identifier	N/A
FIR_COEF_Axxx	R/W	Yes	0x06	0x02 to 0x7E	N/A	FIR Filter Bank A, Coefficients 60 through 119	Table 52
PAGE_ID	R/W	No	0x07	0x00	0x0000	Page identifier	N/A
FIR_COEF_Bxxx	R/W	Yes	0x07	0x02 to 0x7E	N/A	FIR Filter Bank B, Coefficients 0 through 59	Table 53
PAGE_ID	R/W	No	0x08	0x00	0x0000	Page identifier	N/A
FIR_COEF_Bxxx	R/W	Yes	0x08	0x02 to 0x7E	N/A	FIR Filter Bank B, Coefficients 60 through 119	Table 53
PAGE_ID	R/W	No	0x09	0x00	0x0000	Page identifier	N/A
FIR_COEF_Cxxx	R/W	Yes	0x09	0x02 to 0x7E	N/A	FIR Filter Bank C, Coefficients 0 through 59	Table 54
PAGE_ID	R/W	No	0x0A	0x00	0x0000	Page identifier	N/A
FIR_COEF_Cxxx	R/W	Yes	0x0A	0x02 to 0x7E	N/A	FIR Filter Bank C, Coefficients 60 through 119	Table 54
PAGE_ID	R/W	No	0x0B	0x00	0x0000	Page identifier	N/A
FIR_COEF_Dxxx	R/W	Yes	0x0B	0x02 to 0x7E	N/A	FIR Filter Bank D, Coefficients 0 through 59	Table 55
PAGE_ID	R/W	No	0x0C	0x00	0x0000	Page identifier	N/A
FIR_COEF_Dxxx	R/W	Yes	0x0C	0x02 to 0x7E	N/A	FIR Filter Bank D, Coefficients 60 through 119	Table 55

[1] The GPIO_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

OUTPUT DATA REGISTERS

After the ADIS16485 completes its start-up process, the PAGE_ID register contains 0x0000, which sets Page 0 as the active page for SPI access. Page 0 contains the output data, real-time clock, status, and product identification registers.

INERTIAL SENSOR DATA FORMAT

The gyroscope, accelerometer, delta angle, and delta velocity output data registers use a 32-bit, twos complement format. Each output uses two registers to support this resolution. Figure 18 provides an example of how each register contributes to each inertial measurement. In this case, X_GYRO_OUT is the most significant word (upper 16 bits), and X_GYRO_LOW is the least significant word (lower 16 bits). In many cases, using the most significant word registers alone provide sufficient resolution for preserving key performance metrics.

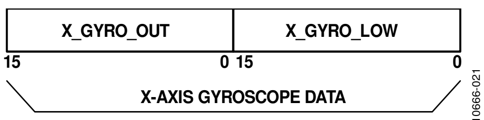


Figure 18. Gyroscope Output Format Example, DEC_RATE > 0

The arrows in Figure 19 describe the direction of the motion, which produces a positive output response in each output register of the sensor. The accelerometers respond to both dynamic and static forces associated with acceleration, including gravity. When lying perfectly flat, as shown in Figure 19, the z-axis accelerometer output is 1 *g*, and the x and y accelerometers are 0 *g*.

ROTATION RATE (GYROSCOPE)

The registers that use the x_GYRO_OUT format are the primary registers for the gyroscope measurements (see Table 11, Table 12, and Table 13). When processing data from these registers, use a 16-bit, twos complement data format. Table 14 provides x_GYRO_OUT digital coding examples.

Table 11. X_GYRO_OUT (Page 0, Base Address = 0x12)

Bits	Description
[15:0]	X-axis gyroscope data; twos complement, ±450°/sec range, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 12. Y_GYRO_OUT (Page 0, Base Address = 0x16)

Bits	Description
[15:0]	Y-axis gyroscope data; twos complement, ±450°/sec range, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 13. Z_GYRO_OUT (Page 0, Base Address = 0x1A)

Bits	Description
[15:0]	Z-axis gyroscope data; twos complement, ±450°/sec range, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 14. x_GYRO_OUT Data Format Examples

Rotation Rate	Decimal	Hex	Binary
+450°/sec	+22,500	0x57E4	0101 0111 1110 0100
+0.04/sec	+2	0x0002	0000 0000 0000 0010
+0.02°/sec	+1	0x0001	0000 0000 0000 0001
0°/sec	0	0x0000	0000 0000 0000 0000
−0.02°/sec	−1	0xFFFF	1111 1111 1111 1111
−0.04°/sec	−2	0xFFFE	1111 1111 1111 1110
−450°/sec	−22,500	0xA81C	1010 1000 0001 1100

The registers that use the x_GYRO_LOW naming format provide additional resolution for the gyroscope measurements (see Table 15, Table 16, and Table 17). The MSB has a weight of 0.01°/sec, and each subsequent bit has ½ the weight of the previous one.

Table 15. X_GYRO_LOW (Page 0, Base Address = 0x10)

Bits	Description
[15:0]	X-axis gyroscope data; additional resolution bits

Table 16. Y_GYRO_LOW (Page 0, Base Address = 0x14)

Bits	Description
[15:0]	Y-axis gyroscope data; additional resolution bits

Table 17. Z_GYRO_LOW (Page 0, Base Address = 0x18)

Bits	Description
[15:0]	Z-axis gyroscope data; additional resolution bits

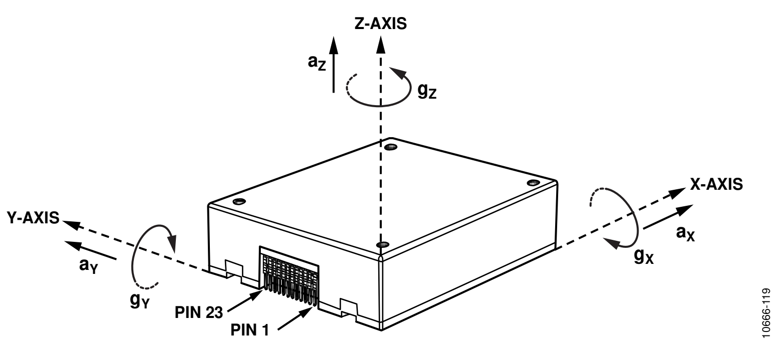


Figure 19. Inertial Sensor Direction Reference Diagram

ACCELERATION

The registers that use the x_ACCL_OUT format are the primary registers for the accelerometer measurements (see Table 18, Table 19, and Table 20). When processing data from these registers, use a 16-bit, twos complement data format. Table 21 provides x_ACCL_OUT digital coding examples.

Table 18. X_ACCL_OUT (Page 0, Base Address = 0x1E)

Bits	Description
[15:0]	X-axis accelerometer data; twos complement, ±5 *g* range, 0 *g* = 0x0000, 1 LSB = 0.25 m*g*

Table 19. Y_ACCL_OUT (Page 0, Base Address = 0x22)

Bits	Description
[15:0]	Y-axis accelerometer data; twos complement, ±5 *g* range, 0 *g* = 0x0000, 1 LSB = 0.25 m*g*

Table 20. Z_ACCL_OUT (Page 0, Base Address = 0x26)

Bits	Description
[15:0]	Z-axis accelerometer data; twos complement, ±5 *g* range, 0 *g* = 0x0000, 1 LSB = 0.25 m*g*

Table 21. x_ACCL_OUT Data Format Examples

Acceleration	Decimal	Hex	Binary
+5 *g*	+20,000	0x4E20	0100 1110 0010 0000
+0.5 m*g*	+2	0x0002	0000 0000 0000 0010
+0.25 m*g*	+1	0x0001	0000 0000 0000 0001
0 m*g*	0	0x0000	0000 0000 0000 0000
−0.25 m*g*	−1	0xFFFF	1111 1111 1111 1111
−0.5 m*g*	−2	0xFFFE	1111 1111 1111 1110
−5 *g*	−20,000	0xB1E0	1011 0001 1110 0000

The registers that use the x_ACCL_LOW naming format provide additional resolution for the accelerometer measurements (see Table 22, Table 23, and Table 24). The MSB has a weight of 0.125 m*g*, and each subsequent bit has ½ the weight of the previous one.

Table 22. X_ACCL_LOW (Page 0, Base Address = 0x1C)

Bits	Description
[15:0]	X-axis accelerometer data; additional resolution bits

Table 23. Y_ACCL_LOW (Page 0, Base Address = 0x20)

Bits	Description
[15:0]	Y-axis accelerometer data; additional resolution bits

Table 24. Z_ACCL_LOW (Page 0, Base Address = 0x24)

Bits	Description
[15:0]	Z-axis accelerometer data; additional resolution bits

DELTA ANGLES

The x_DELTANG_OUT registers are the primary output registers for the delta angle calculations. When processing data from these registers, use a 16-bit, twos complement data format (see Table 25, Table 26, and Table 27). Table 28 shows x_DELTANG_OUT digital coding examples.

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta_{x,nD} = \frac{1}{2f_S} \times \sum_{d=0}^{D-1}\left(\omega_{x,nD+d} + \omega_{x,nD+d-1}\right)$$

where:
D is the decimation rate = DEC_RATE + 1.
f_S is the sample rate.
d is the incremental variable in the summation formula.
ω_x is the x-axis rate of rotation (gyroscope).
n is the sample time, prior to the decimation filter.

When using the internal sample clock, fS is equal to 2460 SPS. When using the external clock option, fS is equal to the frequency of the external clock, which is limited to a minimum of 2 kHz, to prevent overflow in the x_DELTANG_xxx registers at high rotation rates. See Table 49 and Figure 20 for more information on the DEC_RATE register (decimation filter).

The x_DELTANG_LOW registers (see Table 29, Table 30, and Table 31) provide additional resolution bits for the delta angle and combine with the x_DELTANG_OUT registers to provide a 32-bit, twos complement number. The MSB in the x_DELTANG_LOW registers have a weight of ~0.011° (720°/216), and each subsequent bit carries a weight of ½ of the previous one.

Table 25. X_DELTANG_OUT (Page 0, Base Address = 0x42)

Bits	Description
[15:0]	X-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = $720°/2^{15}$ = ~0.022°

Table 26. Y_DELTANG_OUT (Page 0, Base Address = 0x46)

Bits	Description
[15:0]	Y-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = $720°/2^{15}$ = ~0.022°

Table 27. Z_DELTANG_OUT (Page 0, Base Address = 0x4A)

Bits	Description
[15:0]	Z-axis delta angle data; twos complement, ±720° range, 0° = 0x0000, 1 LSB = $720°/2^{15}$ = ~0.022°

Table 28. x_DELTANG_OUT Data Format Examples

Angle (°)	Decimal	Hex	Binary
$+720 \times (2^{15} - 1)/2^{15}$	+32,767	0x7FFF	0111 1111 1111 1111
$+1440/2^{15}$	+2	0x0002	0000 0000 0000 0010
$+720/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-720/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-1440/2^{15}$	−2	0xFFFE	1111 1111 1111 1110
−720	−32,768	0x8000	1000 0000 0000 0000

The x_DELTANG_LOW registers (see Table 29, Table 30, and Table 31) provide additional resolution for the angle measurement and combine with the x_DELTANT_OUT registers to provide a 32-bit, twos complement number. The MSBs in the x_DELTANG_LOW registers have a weight of ~0.011° ($720°/2^{16}$), and each subsequent bit carries a weight of ½ of the previous one.

Table 29. X_DELTANG_LOW (Page 0, Base Address = 0x40)

Bits	Description
[15:0]	X-axis delta angle data; additional resolution bits

Table 30. Y_DELTANG_LOW (Page 0, Base Address = 0x44)

Bits	Description
[15:0]	Y-axis delta angle data; additional resolution bits

Table 31. Z_DELTANG_LOW (Page 0, Base Address = 0x48)

Bits	Description
[15:0]	Z-axis delta angle data; additional resolution bits

DELTA VELOCITY

The registers that use the x_DELTVEL_OUT format are the primary registers for the delta velocity calculations. When processing data from these registers, use a 16-bit, twos complement data format (see Table 32, Table 33, and Table 34). Table 35 provides x_DELTVEL_OUT digital coding examples.

The delta velocity outputs represent an integration of the accelerometer measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta V_{x,nD} = \frac{1}{2f_S} \times \sum_{d=0}^{D-1} \left(a_{x,nD+d} + a_{x,nD+d-1} \right)$$

where:
a_x is the x-axis linear acceleration.
f_S is the sample rate.
n is the sample time, prior to the decimation filter.
D is the decimation rate = DEC_RATE + 1.
d is the incremental variable in the summation formula.

When using the internal sample clock, f_S is equal to 2460 SPS. When using the external clock option, f_S is equal to the frequency of the external clock, which is limited to a minimum of 2 kHz, to prevent overflow in the x_DELTVEL_xxx registers at high rotation rates. See Table 49 and Figure 20 for more information on the DEC_RATE register (decimation filter).

Table 32. X_DELTVEL_OUT (Page 0, Base Address = 0x4E)

Bits	Description
[15:0]	X-axis delta velocity data; twos complement, ±50 m/sec range, 0 m/sec = 0x0000, 1 LSB = 50 m/sec ÷ (2^{15} – 1) = ~1.526 mm/sec

Table 33. Y_DELTVEL_OUT (Page 0, Base Address = 0x52)

Bits	Description
[15:0]	Y-axis delta velocity data; twos complement, ±50 m/sec range, 0 m/sec = 0x0000, 1 LSB = 50 m/sec ÷ (2^{15} – 1) = ~1.526 mm/sec

Table 34. Z_DELTVEL_OUT (Page 0, Base Address = 0x56)

Bits	Description
[15:0]	Z-axis delta velocity data; twos complement, ±50 m/sec range, 0 m/sec = 0x0000, 1 LSB = 50 m/sec ÷ (2^{15} – 1) = ~1.526 mm/sec

Table 35. x_DELTVEL_OUT, Data Format Examples

Velocity (m/sec)	Decimal	Hex	Binary
$+50 \times (2^{15} - 1)/2^{15}$	+32,767	0x7FFF	0111 1111 1111 1111
$+100/2^{15}$	+2	0x0002	0000 0000 0000 0010
$+50/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-50/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-100/2^{15}$	−2	0xFFFE	1111 1111 1111 1110
−50	−32,768	0x8000	1000 0000 0000 0000

The x_DELTVEL_LOW registers (see Table 36, Table 37, and Table 38) provide additional resolution bits for the delta-velocity measurement and combine with the x_DELTVEL_OUT registers to provide a 32-bit, twos complement number. The MSBs in the x_DELTVEL_LOW registers have a weight of ~0.7629 mm/sec (50 m/sec ÷ 2^{16}), and each subsequent bit carries a weight of ½ of the previous one.

Table 36. X_DELTVEL_LOW (Page 0, Base Address = 0x4C)

Bits	Description
[15:0]	X-axis delta velocity data; additional resolution bits

Table 37. Y_DELTVEL_LOW (Page 0, Base Address = 0x50)

Bits	Description
[15:0]	Y-axis delta velocity data; additional resolution bits

Table 38. Z_DELTVEL_LOW (Page 0, Base Address = 0x54)

Bits	Description
[15:0]	Z-axis delta velocity data; additional resolution bits

INTERNAL TEMPERATURE

The TEMP_OUT register provides an internal temperature measurement that can be useful for observing relative temperature changes inside of the ADIS16485 (see Table 39). Table 40 provides TEMP_OUT digital coding examples. Note that this temperature reflects a higher temperature than ambient, due to self heating.

Table 39. TEMP_OUT (Page 0, Base Address = 0x0E)

Bits	Description
[15:0]	Temperature data; twos complement, 0.00565°C per LSB, 25°C = 0x0000

Table 40. TEMP_OUT Data Format Examples

Temperature (°C)	Decimal	Hex	Binary
+85	+10,619	0x297B	0010 1001 0111 1011
+25 + 0.0113	+2	0x0002	0000 0000 0000 0010
+25 + 0.00565	+1	0x0001	0000 0000 0000 0001
+25	0	0x0000	0000 0000 0000 0000
+25 − 0.00565	−1	0xFFFF	1111 1111 1111 1111
+25 − 0.0113	−2	0xFFFE	1111 1111 1111 1110
−40	−11,504	0xD310	1101 0011 0001 0000

STATUS/ALARM INDICATORS

The SYS_E_FLAG register in Table 41 provides the system error flags for a variety of conditions (see Table 41). Reading the SYS_E_FLAG register clears all of its error flags and returns each bit to a zero value, with the exception of Bit[7]. If SYS_E_FLAG[7] is high, use the software reset (GLOB_CMD[7], see Table 86) to clear this condition and restore normal operation. If any bit in the SYS_E_FLAG register is associated with an error condition that remains after reading this register, this bit automatically returns to an alarm value as 1.

Table 41. SYS_E_FLAG (Page 0, Base Address = 0x08)

Bits	Description (Default = 0x0000)
15	Watch dog timer flag (1 = timed out)
[14:8]	Not used
7	Processing overrun (1 = error)
6	Flash memory update, result of GLOB_CMD[3] = 1 (1 = failed update, 0 = update successful)
5	Inertial self test failure (1 = DIAG_STS ≠ 0x0000)
4	Sensor overrange (1 = at least one sensor overranged)
3	SPI communication error (1 = error condition, when the number of SCLK pulses is not equal to a multiple of 16)
[2:1]	Not used
0	Alarm status flag (1 = ALM_STS ≠ 0x0000)

The DIAG_STS register in Table 42 provides the flags for the internal self test function, which is from GLOB_CMD[1] (see Table 86). Note that reading DIAG_STS also resets it to 0x0000.

Table 42. DIAG_STS (Page 0, Base Address = 0x0A)

Bits	Description (Default = 0x0000)
[15:6]	Not used
5	Self test failure, z-axis accelerometer (1 = failure)
4	Self test failure, y-axis accelerometer (1 = failure)
3	Self test failure, x-axis accelerometer (1 = failure)
2	Self test failure, z-axis gyroscope (1 = failure)
1	Self test failure, y-axis gyroscope (1 = failure)
0	Self test failure, x-axis gyroscope (1 = failure)

The ALM_STS register in Table 43 provides the alarm bits for the programmable alarm levels of each sensor. Note that reading ALM_STS also resets its value to 0x0000.

Table 43. ALM_STS (Page 0, Base Address = 0x0C)

Bits	Description (Default = 0x0000)
[15:6]	Not used
5	Z-axis accelerometer alarm flag (1 = alarm is active)
4	Y-axis accelerometer alarm flag (1 = alarm is active)
3	X-axis accelerometer alarm flag (1 = alarm is active)
2	Z-axis gyroscope alarm flag (1 = alarm is active)
1	Y-axis gyroscope alarm flag (1 = alarm is active)
0	X-axis gyroscope alarm flag (1 = alarm is active)

FIRMWARE REVISION

The FIRM_REV register (see Table 44) provides the firmware revision for the internal processor. Each nibble represents a digit in this revision code. For example, if FIRM_REV = 0x0102, the firmware revision is 1.02.

Table 44. FIRM_REV (Page 3, Base Address = 0x78)

Bits	Description
[15:12]	Binary, revision, 10s digit
[11:8]	Binary, revision, 1s digit
[7:4]	Binary, revision, tenths digit
[3:0]	Binary, revision, hundredths digit

The FIRM_DM register (see Table 45) contains the month and day of the factory configuration date. FIRM_DM[15:12] and FIRM_DM[11:8] contain digits that represent the month of factory configuration. For example, November is the 11th month in a year and represented by FIRM_DM[15:8] = 0x11. FIRM_DM[7:4] and FIRM_DM[3:0] contain digits that represent the day of factory configuration. For example, the 27th day of the month is represented by FIRM_DM[7:0] = 0x27.

Table 45. FIRM_DM (Page 3, Base Address = 0x7A)

Bits	Description
[15:12]	Binary, month 10s digit, range: 0 to 1
[11:8]	Binary, month 1s digit, range: 0 to 9
[7:4]	Binary, day 10s digit, range: 0 to 3
[3:0]	Binary, day 1s digit, range: 0 to 9

The FIRM_Y register (see Table 46) contains the year of the factory configuration date. For example, the year of 2013 is represented by FIRM_Y = 0x2013.

Table 46. FIRM_Y (Page 3, Base Address = 0x7C)

Bits	Description
[15:12]	Binary, year 1000s digit, range: 0 to 9
[11:8]	Binary, year 100s digit, range: 0 to 9
[7:4]	Binary, year 10s digit, range: 0 to 9
[3:0]	Binary, year 1s digit, range: 0 to 9

PRODUCT IDENTIFICATION

The PROD_ID register (see Table 47) contains the binary equivalent of the device number (16,485 = 0x4065), and the SERIAL_NUM register (see Table 48) contains a lot-specific serial number.

Table 47. PROD_ID (Page 0, Base Address = 0x7E)

Bits	Description (Default = 0x4065)
[15:0]	Product identification = 0x4065 (16,485)

Table 48. SERIAL_NUM (Page 4, Base Address = 0x20)

Bits	Description
[15:0]	Lot specific serial number

DIGITAL SIGNAL PROCESSING

GYROSCOPES/ACCELEROMETERS

Figure 20 provides a signal flow diagram for all the components and settings that influence the frequency response for the accelerometers and gyroscopes. The sample rate for each accelerometer and gyroscope is 9.84 kHz. Each sensor has its own averaging/decimation filter stage that reduces the update rate to 2.46 kSPS. When using the external sync clock option (FNCTIO_CTRL[7:4], see Table 89), the input clock drives a 4-sample burst at a sample rate of 9.84 kSPS, which feeds into the 4× averaging/decimation filter. This results in a data rate that is equal to the input clock frequency.

AVERAGING/DECIMATION FILTER

The DEC_RATE register (see Table 49) provides user control for the final filter stage (see Figure 20), which averages and decimates the accelerometers, gyroscopes, delta angle, and delta velocity data. The output sample rate is equal to 2460/(DEC_RATE + 1). When using the external sync clock option (FNCTIO_CTRL[7:4], see Table 89), replace the 2460 number in this relationship with the input clock frequency. For example, turn to Page 3 (DIN = 0x8003), and set DEC_RATE = 0x18 (DIN = 0x8C18, then DIN = 0x8D00) to reduce the output sample rate to 98.4 SPS (2460 ÷ 25).

Table 49. DEC_RATE (Page 3, Base Address = 0x0C)

Bits	Description (Default = 0x0000)
[15:11]	Don't care
[10:0]	Decimation rate, binary format, maximum = 2047, see Figure 20 for impact on sample rate

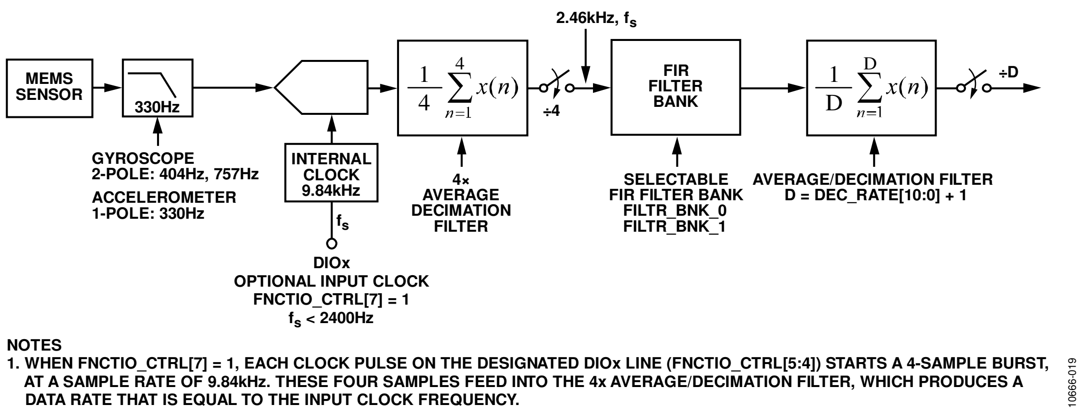


Figure 20. Sampling and Frequency Response Signal Flow

FIR FILTER BANKS

The ADIS16485 provides four configurable, 120-tap FIR filter banks. Each coefficient is 16 bits wide and occupies its own register location with each page. When designing a FIR filter for these banks, use a sample rate of 2.46 kHz and scale the coefficients so that their sum equals 32,768. For filter designs that have less than 120 taps, load the coefficients into the lower portion of the filter and start with Coefficient 1. Make sure that all unused taps are equal to zero, so that they do not add phase delay to the response. The FILTR_BNK_x registers provide three bits per sensor, which configure the filter bank (A, B, C, D) and turn filtering on and off. For example, turn to Page 3 (DIN = 0x8003), then write 0x002F to FILTR_BNK_0 (DIN = 0x962F, DIN = 0x9700) to set the x-axis gyroscope to use the FIR filter in Bank D, to set the y-axis gyroscope to use the FIR filter in Bank B, and to enable these FIR filters in both x- and y-axis gyroscopes. Note that the filter settings update after writing to the upper byte; therefore, always configure the lower byte first. In cases that require configuration to only the lower byte of either FILTR_BNK_0 or FILTR_BNK_1, complete the process by writing 0x00 to the upper byte.

Table 50. FILTR_BNK_0 (Page 3, Base Address = 0x16)

Bits	Description (Default = 0x0000)
15	Don't care
14	Y-axis accelerometer filter enable (1 = enabled)
[13:12]	Y-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
11	X-axis accelerometer filter enable (1 = enabled)
[10:9]	X-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
8	Z-axis gyroscope filter enable (1 = enabled)
[7:6]	Z-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
5	Y-axis gyroscope filter enable (1 = enabled)
[4:3]	Y-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D
2	X-axis gyroscope filter enable (1 = enabled)
[1:0]	X-axis gyroscope filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D

Table 51. FILTR_BNK_1 (Page 3, Base Address = 0x18)

Bits	Description (Default = 0x0000)
[15:3]	Don't care
2	Z-axis accelerometer filter enable (1 = enabled)
[1:0]	Z-axis accelerometer filter bank selection: 00 = Bank A, 01 = Bank B, 10 = Bank C, 11 = Bank D

Filter Memory Organization

Each filter bank uses two pages of the user register structure. See Table 52, Table 53, Table 54 and Table 55 for the register addresses in each filter bank.

Table 52. Filter Bank A Memory Map, FIR_COEF_Axxx

Page	PAGE_ID	Address	Register
5	0x05	0x00	PAGE_ID
5	0x05	0x02 to 0x07	Not used
5	0x05	0x08	FIR_COEF_A000
5	0x05	0x0A	FIR_COEF_A001
5	0x05	0x0C to 0x7C	FIR_COEF_A002 to FIR_COEF_A058
5	0x05	0x7E	FIR_COEF_A059
6	0x06	0x00	PAGE_ID
6	0x06	0x02 to 0x07	Not used
6	0x06	0x08	FIR_COEF_A060
6	0x06	0x0A	FIR_COEF_A061
6	0x06	0x0C to 0x7C	FIR_COEF_A062 to FIR_COEF_A118
6	0x06	0x7E	FIR_COEF_A119

Table 53. Filter Bank B Memory Map, FIR_COEF_Bxxx

Page	PAGE_ID	Address	Register
7	0x07	0x00	PAGE_ID
7	0x07	0x02 to 0x07	Not used
7	0x07	0x08	FIR_COEF_B000
7	0x07	0x0A	FIR_COEF_B001
7	0x07	0x0C to 0x7C	FIR_COEF_B002 to FIR_COEF_B058
7	0x07	0x7E	FIR_COEF_B059
8	0x08	0x00	PAGE_ID
8	0x08	0x02 to 0x07	Not used
8	0x08	0x08	FIR_COEF_B060
8	0x08	0x0A	FIR_COEF_B061
8	0x08	0x0C to 0x7C	FIR_COEF_B062 to FIR_COEF_B118
8	0x08	0x7E	FIR_COEF_B119

Table 54. Filter Bank C Memory Map, FIR_COEF_Cxxx

Page	PAGE_ID	Address	Register
9	0x09	0x00	PAGE_ID
9	0x09	0x02 to 0x07	Not used
9	0x09	0x08	FIR_COEF_C000
9	0x09	0x0A	FIR_COEF_C001
9	0x09	0x0C to 0x7C	FIR_COEF_C002 to FIR_COEF_C058
9	0x09	0x7E	FIR_COEF_C059
10	0x0A	0x00	PAGE_ID
10	0x0A	0x02 to 0x07	Not used
10	0x0A	0x08	FIR_COEF_C060
10	0x0A	0x0A	FIR_COEF_C061
10	0x0A	0x0C to 0x7C	FIR_COEF_C062 to FIR_COEF_C118
10	0x0A	0x7E	FIR_COEF_C119

Table 55. Filter Bank D Memory Map, FIR_COEF_Dxxx

Page	PAGE_ID	Address	Register
11	0x0B	0x00	PAGE_ID
11	0x0B	0x02 to 0x07	Not used
11	0x0B	0x08	FIR_COEF_D000
11	0x0B	0x0A	FIR_COEF_D001
11	0x0B	0x0C to 0x7C	FIR_COEF_D002 to FIR_COEF_D058
11	0x0B	0x7E	FIR_COEF_D059
12	0x0C	0x00	PAGE_ID
12	0x0C	0x02 to 0x07	Not used
12	0x0C	0x08	FIR_COEF_D060
12	0x0C	0x0A	FIR_COEF_D061
12	0x0C	0x0C to 0x7C	FIR_COEF_D062 to FIR_COEF_D118
12	0x0C	0x7E	FIR_COEF_D119

Default Filter Performance

The FIR filter banks have factory programmed filter designs. They are all low-pass filters that have unity dc gain. Table 56 provides a summary of each filter design, and Figure 21 shows the frequency response characteristics. The phase delay is equal to ½ of the total number of taps.

Table 56. FIR Filter Descriptions, Default Configuration

FIR Filter Bank	Taps	−3 dB Frequency (Hz)
A	120	310
B	120	55
C	32	275
D	32	63

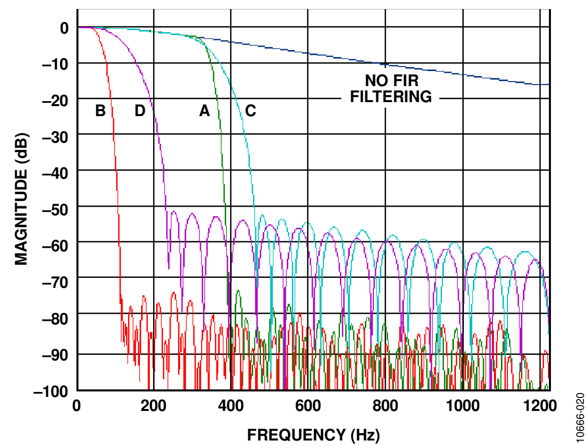


Figure 21. FIR Filter Frequency Response Curves

CALIBRATION

The ADIS16485 factory calibration produces correction formulas for the gyroscopes and the accelerometers and then programs them into the flash memory. In addition, there are a series of user-configurable calibration registers for in-system tuning.

GYROSCOPES

The user calibration for the gyroscopes includes registers for adjusting bias and sensitivity, as shown in Figure 22.

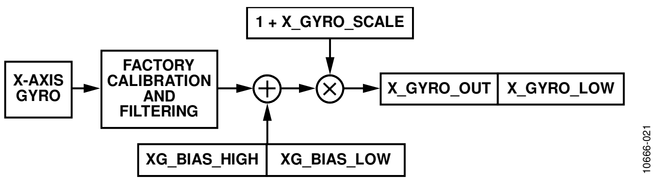


Figure 22. User Calibration Signal Path, Gyroscopes

Manual Bias Correction

The xG_BIAS_HIGH registers (see Table 57, Table 58, and Table 59) and xG_BIAS_LOW registers (see Table 60, Table 61, and Table 62) provide a bias adjustment function for the output of each gyroscope sensor.

Table 57. XG_BIAS_HIGH (Page 2, Base Address = 0x12)

Bits	Description (Default = 0x0000)
[15:0]	X-axis gyroscope offset correction, upper word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 58. YG_BIAS_HIGH (Page 2, Base Address = 0x16)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis gyroscope offset correction, upper word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 59. ZG_BIAS_HIGH (Page 2, Base Address = 0x1A)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis gyroscope offset correction, upper word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec

Table 60. XG_BIAS_LOW (Page 2, Base Address = 0x10)

Bits	Description (Default = 0x0000)
[15:0]	X-axis gyroscope offset correction, lower word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec ÷ 2^{16} = ~0.000000305°/sec

Table 61. YG_BIAS_LOW (Page 2, Base Address = 0x14)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis gyroscope offset correction, lower word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec ÷ 2^{16} = ~0.000000305°/sec

Table 62. ZG_BIAS_LOW (Page 2, Base Address = 0x18)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis gyroscope offset correction, lower word; twos complement, 0°/sec = 0x0000, 1 LSB = 0.02°/sec ÷ 2^{16} = ~0.000000305°/sec

Bias Null Command

The continuous bias estimator (CBE) accumulates and averages data in a 64-sample FIFO. The average time (t_A) for the bias estimates relies on the sample time base setting in NULL_CNFG[3:0] (see Table 63). Users can load the correction factors of the CBE into the gyroscope offset correction registers (see Table 57, Table 58, Table 59, Table 60, Table 61, and Table 62) using the bias null command in GLOB_CMD[0] (see Table 86). NULL_CNFG[13:8] provide on/off controls for the sensors that update when issuing a bias null command. The factory default configuration for NULL_CNFG enables the bias null command for the gyroscopes, disables the bias null command for the accelerometers, and establishes the average time to ~26.64 seconds. For best results, make sure the ADIS16485 is stationary for this entire time.

Table 63. NULL_CNFG (Page 3, Base Address = 0x0E)

Bits	Description (Default = 0x070A)
[15:14]	Not used
13	Z-axis acceleration bias correction enable (1 = enabled)
12	Y-axis acceleration bias correction enable (1 = enabled)
11	X-axis acceleration bias correction enable (1 = enabled)
10	Z-axis gyroscope bias correction enable (1 = enabled)
9	Y-axis gyroscope bias correction enable (1 = enabled)
8	X-axis gyroscope bias correction enable (1 = enabled)
[7:4]	Not used
[3:0]	Time base control (TBC), range: 0 to 13 (default = 10); $t_B = 2^{TBC}/2460$, time base, $t_A = 64 \times t_B$, average time

Turn to Page 3 (DIN = 0x8003) and set GLOB_CMD[0] = 1 (DIN = 0x8201, then DIN = 0x8300) to update the user offset registers with the correction factors of the CBE.

Manual Sensitivity Correction

The x_GYRO_SCALE registers enable sensitivity adjustment (see Table 64, Table 65, and Table 66).

Table 64. X_GYRO_SCALE (Page 2, Base Address = 0x04)

Bits	Description (Default = 0x0000)
[15:0]	X-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Table 65. Y_GYRO_SCALE (Page 2, Base Address = 0x06)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Table 66. Z_GYRO_SCALE (Page 2, Base Address = 0x08)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis gyroscope scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Linear Acceleration on Effect on Gyroscope Bias

MEMS gyroscopes typically have a bias response to linear acceleration that is normal to their axes of rotation. The ADIS16485 offers an optional compensation function for this effect; the factory default setting (0x00C0) for the CONFIG register enables this function. To turn it off, turn to Page 3 (DIN = 0x8003) and set CONFIG[7] = 0 (DIN = 0x8A20, DIN = 0x8B00). Note that this also keeps the point of percussion alignment function enabled.

Table 67. CONFIG (Page 3, Base Address = 0x0A)

Bits	Description (Default = 0x00C0)
[15:8]	Not used
7	Linear-*g* compensation for gyroscopes (1 = enabled)
6	Point of percussion alignment (1 = enabled)
[5:2]	Not used
1	Real-time clock, daylight savings time (1: enabled, 0: disabled)
0	Real-time clock control (1: relative/elapsed timer mode, 0: calendar mode)

ACCELEROMETERS

The user calibration for the accelerometers includes registers for adjusting bias and sensitivity, as shown in Figure 23.

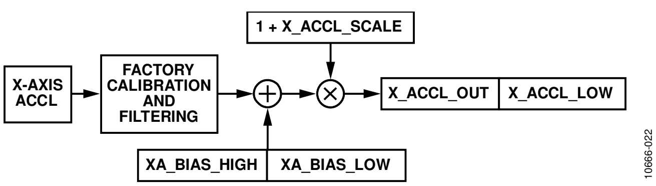


Figure 23. User Calibration Signal Path, Gyroscopes

Manual Bias Correction

The xA_BIAS_HIGH (see Table 68, Table 69, and Table 70) and xA_BIAS_LOW (see Table 71, Table 72, and Table 73) registers provide a bias adjustment function for the output of each accelerometer sensor. The xA_BIAS_HIGH registers use the same format as x_ACCL_OUT registers. The xA_BIAS_LOW registers use the same format as x_ACCL_LOW registers.

Table 68. XA_BIAS_HIGH (Page 2, Base Address = 0x1E)

Bits	Description (Default = 0x0000)
[15:0]	X-axis accelerometer offset correction, high word; twos complement, 0 *g* = 0x0000, 1 LSB = 0.25 m*g*

Table 69. YA_BIAS_HIGH (Page 2, Base Address = 0x22)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis accelerometer offset correction, high word; twos complement, 0 *g* = 0x0000, 1 LSB = 0.25 m*g*

Table 70. ZA_BIAS_HIGH (Page 2, Base Address = 0x26)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis accelerometer offset correction, high word; twos complement, 0 *g* = 0x0000, 1 LSB = 0.25 m*g*

Table 71. XA_BIAS_LOW (Page 2, Base Address = 0x1C)

Bits	Description (Default = 0x0000)
[15:0]	X-axis accelerometer offset correction, low word; twos complement, 0 *g* = 0x0000, 1 LSB = 0.25 m*g* ÷ 2^{16} = ~0.000003815 m*g*

Table 72. YA_BIAS_LOW (Page 2, Base Address = 0x20)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis accelerometer offset correction, low word; twos complement, 0 *g* = 0x0000, 1 LSB = 0.25 m*g* ÷ 2^{16} = ~0.000003815 m*g*

Table 73. ZA_BIAS_LOW (Page 2, Base Address = 0x24)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis accelerometer offset correction, low word; twos complement, 0 *g* = 0x0000, 1 LSB = 0.25 m*g* ÷ 2^{16} = ~0.000003815 m*g*

Manual Sensitivity Correction

The x_ACCL_SCALE registers enable sensitivity adjustment (see Table 74, Table 75, Table 76).

Table 74. X_ACCL_SCALE (Page 2, Base Address = 0x0A)

Bits	Description (Default = 0x0000)
[15:0]	X-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Table 75. Y_ACCL_SCALE (Page 2, Base Address = 0x0C)

Bits	Description (Default = 0x0000)
[15:0]	Y-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%

Table 76. Z_ACCL_SCALE (Page 2, Base Address = 0x0E)

Bits	Description (Default = 0x0000)
[15:0]	Z-axis accelerometer scale correction; twos complement, 0x0000 = unity gain, 1 LSB = 1 ÷ 2^{15} = ~0.003052%