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Tactical Grade, Six Degrees of Freedom Inertial Sensor

Data Sheet

ADIS16495

FEATURES

Triaxial, digital gyroscope
- **±125°/sec, ±450°/sec, ±2000°/sec range options**
- **±0.05° axis to axis misalignment error**
- **±0.25° (maximum) axis to package misalignment error**
- **0.8°/hr in-run bias stability**
- **0.09°/√hr angular random walk**

Triaxial, digital accelerometer, ±8 *g*
- **3.2 µ*g* in run bias stability**

Triaxial, delta angle and delta velocity outputs
Factory calibrated sensitivity, bias, and axial alignment
- **Calibration temperature range: −40°C to +85°C**

SPI compatible
Programmable operation and control
- **Automatic and manual bias correction controls**
- **Configurable FIR filters**
- **Digital I/O: data ready, external clock**
- **Sample clock options: internal, external, or scaled**
- **On demand self test of inertial sensors**

Single-supply operation: 3.0 V to 3.6 V
1500 *g* mechanical shock survivability
Operating temperature range: −40°C to +105°C

APPLICATIONS

Precision instrumentation, stabilization
Guidance, navigation, control
Avionics, unmanned vehicles
Precision autonomous machines, robotics

GENERAL DESCRIPTION

The ADIS16495 is a complete inertial system that includes a triaxis gyroscope and a triaxis accelerometer. Each inertial sensor in the ADIS16495 combines industry leading *i*MEMS® technology with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, alignment, and linear acceleration (gyroscope bias). As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements.

The ADIS16495 provides a simple, cost effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment simplifies inertial frame alignment in navigation systems. The serial peripheral interface (SPI) and register structure provide a simple interface for data collection and configuration control.

The footprint and connector system of the ADIS16495 enable a simple upgrade from the ADIS16375, ADIS16480, ADIS16485, ADIS16488A, and ADIS16490. The ADIS16495 is available in an aluminum package that is approximately 47 mm × 44 mm × 14 mm and includes a standard connector interface.

FUNCTIONAL BLOCK DIAGRAM

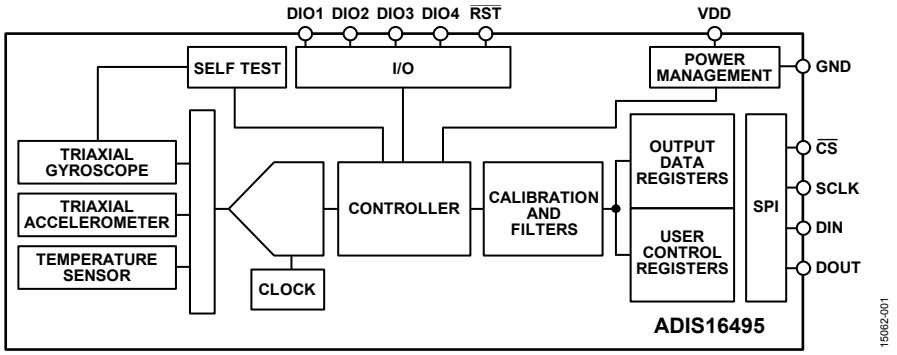

Figure 1.

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Technical Support
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REVISION HISTORY

11/2017—Rev. 0 to Rev. A

Changes to Table 1 ... 3
Added Endnote 2, Table 1; Renumbered Sequentially ... 4
Changes to t_2 Parameter, Table 2 ... 5
Changes to Table 3 ... 5

10/2017—Revision 0: Initial Version

SPECIFICATIONS

T_C = 25°C, VDD = 3.3 V, angular rate = 0°/sec, ADIS16495-1BMLZ model, ±1 *g*, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range	ADIS16495-1BMLZ	±125			°/sec
	ADIS16495-2BMLZ	±450		±480	°/sec
	ADIS16495-3BMLZ	±2000			°/sec
Sensitivity	ADIS16495-1BMLZ, 32-bit		10485760		LSB/°/sec
	ADIS16495-2BMLZ, 32-bit		2621440		LSB/°/sec
	ADIS16495-3BMLZ, 32-bit		655360		LSB/°/sec
Error Over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.2		%
Misalignment	Axis to axis, −40°C ≤ T_C ≤+85°C, 1 σ		±0.05		Degrees
	Axis to package, −40°C ≤ T_C ≤+85°C			±0.25	Degrees
Nonlinearity[1]	1 σ, ADIS16495-1BMLZ, FS = 125°/sec		0.2		% FS
	1 σ, ADIS16495-2BMLZ, FS = 450°/sec		0.2		% FS
	1 σ, ADIS16495-3BMLZ, FS = 2000°/sec		0.25		% FS
Bias					
Repeatability[2]	−40°C ≤ T_C ≤+85°C, 1 σ		0.07		°/sec
In Run Bas Stability	1 σ, ADIS16495-1BMLZ		0.8		°/hr
	1 σ, ADIS16495-2BMLZ		1.6		°/hr
	1 σ, ADIS16495-3BMLZ		3.3		°/hr
Angular Random Walk	1 σ, ADIS16495-1BMLZ		0.09		°/√hr
	1 σ, ADIS16495-2BMLZ		0.1		°/√hr
	1 σ, ADIS16495-3BMLZ		0.18		°/√hr
Error over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.1		°/sec
Linear Acceleration Effect	Any axis, 1 σ (CONFIG register, Bit 7 = 1)		0.006		°/sec/*g*
	Any axis, 1 σ (CONFIG register, Bit 7 = 0)		0.015		°/sec/*g*
Vibration Rectification Error	1 σ, ADIS16495-1BMLZ		0.0003		°/sec/g^2
Noise					
Output Noise	No filtering, ADIS16495-1BMLZ		0.051		°/sec rms
	No filtering, ADIS16495-2BMLZ		0.058		°/sec rms
	No filtering, ADIS16495-3BMLZ		0.112		°/sec rms
Rate Noise Density[3]	1 σ, ADIS16495-1BMLZ		0.002		°/sec/√Hz rms
	1 σ, ADIS16495-2BMLZ		0.0022		°/sec/√Hz rms
	1 σ, ADIS16495-3BMLZ		0.0042		°/sec/√Hz rms
−3 dB Bandwidth	ADIS16495-1BMLZ		480		Hz
	ADIS16495-2BMLZ, ADIS16495-3BMLZ		550		Hz
Sensor Resonant Frequency			65		kHz
ACCELEROMETERS[4]	Each axis				
Dynamic Range		±8			*g*
Sensitivity	x_ACCL_OUT and x_ACCL_LOW (32-bit)		262144000		*g*/LSB
Error Over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.01		%
Misalignment	Axis to axis, −40°C ≤ T_C ≤+85°C, 1 σ		±0.035		Degrees
	Axis to package, −40°C ≤ T_C ≤+85°C			±0.25	Degrees
Nonlinearity	Best fit straight line, ±2 *g*, FS = 8 *g*		0.25		% FS
	Best fit straight line, ±4 *g*, FS = 8 *g*		0.5		% FS
	Best fit straight line, ±8 *g*, FS = 8 *g*		1.5		% FS
Bias					
In Run Stability	1 σ		3.2		µ*g*
Velocity Random Walk	1 σ		0.008		m/sec/√hr
Error over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.5		m*g*

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Noise					
Output Noise	No filtering		0.5		m*g* rms
Noise Density	10 Hz to 40 Hz, no filtering		17		μ*g*/√Hz rms
−3 dB Bandwidth			750		Hz
Sensor Resonant Frequency			2.5		kHz
TEMPERATURE SENSOR					
Scale Factor	Output = 0x0000 at 25°C (±5°C)		0.0125		°C/LSB
LOGIC INPUTS[5]					
Input Voltage					
High, V_{IH}		2.0			V
Low, V_{IL}				0.8	V
$\overline{RST}$ Pulse Width		1			μs
$\overline{CS}$ Wake-Up Pulse Width		20			μs
Input Current					
Logic 1, I_{IH}	V_{IH} = 3.3 V			10	μA
Logic 0, I_{IL}	V_{IL} = 0 V				
All Pins Except $\overline{RST}$, $\overline{CS}$				10	μA
$\overline{RST}$, $\overline{CS}$ Pins[6]			0.33		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[5]					
Output Voltage					
High, V_{OH}	I_{SOURCE} = 0.5 mA	2.4			V
Low, V_{OL}	I_{SINK} = 2.0 mA			0.4	V
FLASH MEMORY	Endurance[7]	100,000			Cycles
Data Retention[8]	T_J = 85°C	20			Years
FUNCTIONAL TIMES[9]	Time until data is available				
Power-On Start-Up Time			250		ms
Reset Recovery Time[10]	GLOB_CMD register, Bit 7 = 1 (see Table 142)		210		ms
	$\overline{RST}$ pulled low, then restored to high		250		Ms
Flash Memory					
Update Time	GLOB_CMD register, Bit 3 = 1 (see Table 142)		1120		ms
Clear User Calibration	GLOB_CMD register, Bit 6 = 1 (see Table 142)		350		μs
Self Test Time[11]	GLOB_CMD register, Bit 1 = 1 (see Table 142)		20		ms
CONVERSION RATE			4.25		kSPS
Initial Clock Accuracy			0.02		%
Temperature Coefficient			40		ppm/°C
Sync Input Clock		3.0		4.5	kHz
Pulse Per Second (PPS) Mode		1		128	Hz
POWER SUPPLY, VDD	Operating voltage range	3.0		3.6	V
Power Supply Current[12]	Normal mode, VDD = 3.3 V, μ + σ		89		mA

[1] FS means full scale, FS = 125°/sec (ADIS16495-1BMLZ), FS = 450°/sec (ADIS16495-2BMLZ), FS = 2000°/sec (ADIS16495-3BMLZ).
[2] Bias repeatability provides an estimate for long-term drift in the bias, as observed during 500 hours of High-Temperature Operating Life (HTOL) at +105°C.
[3] Magnitude between 10 Hz and 40 Hz, sample rate is 4250 SPS (nominal), no digital filtering.
[4] All specifications associated with the accelerometers relate to the full-scale range of ±5 *g*.
[5] The digital I/O signals use a 3.3 V system.
[6] $\overline{RST}$ and $\overline{CS}$ pins are connected to the VDD pin through 10kΩ pull-up resistors.
[7] Endurance is qualified as per JEDEC Standard 22, Method A117, measured at −40°C, +25°C, +85°C, and +125°C.
[8] The data retention specification assumes a junction temperature (T_J) of 85°C per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T_J.
[9] These times do not include thermal settling and internal filter response times, which can affect overall accuracy.
[10] The $\overline{RST}$ line must be in a low state for at least 10 μs to ensure a proper reset initiation and recovery.
[11] Self test time can extend when using external clock rates that are lower than 4000 Hz.
[12] Supply current transients can reach 250 mA during initial startup or reset recovery.

TIMING SPECIFICATIONS

T_C = 25°C, VDD = 3.3 V, unless otherwise noted.

Table 2.

		Normal Mode			Burst Read Function			
Parameter	**Description**	**Min[1]**	**Typ**	**Max[1]**	**Min**	**Typ**	**Max[1]**	**Unit**
f_{SCLK}	SCLK frequency	0.01		15			6.5	MHz
t_{STALL}[2]	Stall period between data	2				N/A		µs
t_{CLS}	SCLK low period	31			31			ns
t_{CHS}	SCLK high period	31			31			ns
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	32			32			ns
t_{DAV}	DOUT valid after SCLK edge			10			10	ns
t_{DSU}	DIN setup time before SCLK rising edge	2			2			ns
t_{DHD}	DIN hold time after SCLK rising edge	2			2			ns
t_{DR}, t_{DF}	DOUT rise/fall times, ≤100 pF loading		3	8		3	8	ns
t_{DSOE}	$\overline{CS}$ assertion to DOUT active	0		11	0		11	ns
t_{HD}	SCLK edge to DOUT invalid	0			0			ns
t_{SFS}	Last SCLK edge to $\overline{CS}$ deassertion	32			32			ns
t_{DSHI}	$\overline{CS}$ deassertion to DOUT high impedance	0		9	0		9	ns
t_{NV}	Data invalid time		20			20		µs
t_1	Input sync pulse width	5			5			µs
t_2	Input sync to data invalid		306			306		µs
t_3	Input sync period[3]	222.2			222.2			µs

[1] Guaranteed by design and characterization, but not tested in production.
[2] See Table 3 for exceptions to the stall time rating.
[3] This measurement represents the inverse of the maximum frequency for the input sample clock: 4500 Hz.

Register Specific Stall Times

Table 3.

Parameter	**Description**	**Min[1]**	**Typ**	**Max**	**Unit**
STALL TIME					
FNCTIO_CTRL	Configure the DIOx functions	340			µs
FILTR_BNK_0	Enable/select finite impulse response (FIR) filter banks	65			µs
FILTR_BNK_1	Enable/select FIR filter banks	65			µs
NULL_CNFG	Configure autonull bias function	71			µs
SYNC_SCALE	Configure input clock scale factor	340			µs
DEC_RATE	Configure decimation rate	340			µs
GPIO_CTRL	Configure general-purpose input/output (I/O) lines	45			µs
CONFIG	Configure miscellaneous functions	45			µs
GLOB_CMD, Bit 1	On demand self test	20			ms
GLOB_CMD, Bit 3	Flash memory update	1120			ms
GLOB_CMD, Bit 6	Factory calibration restore	350			µs
GLOB_CMD, Bit 7	Software reset	210			ms

[1] Monitoring the data ready signal (see Table 144 for FNCTIO_CTRL configuration) for the return of regular pulsing can help minimize system wait times.

Timing Diagrams

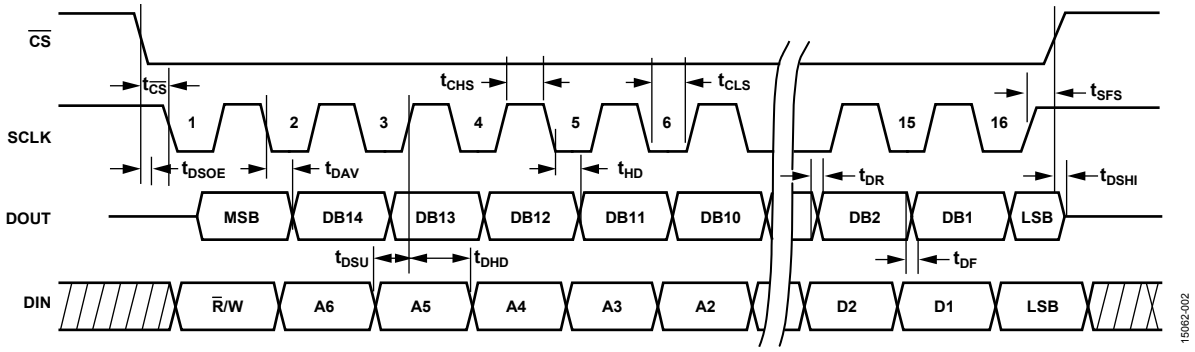

Figure 2. SPI Timing and Sequence

Figure 3. Stall Time and Data Rate

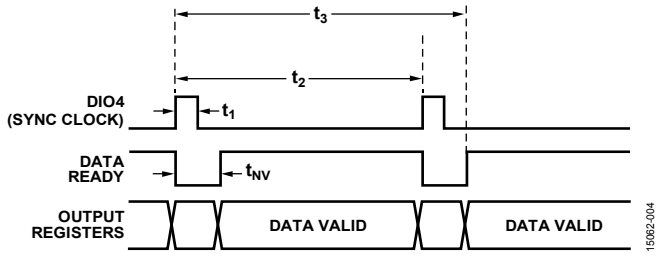

Figure 4. Input Clock Timing Diagram, FNCTIO_CTRL, Bits[7:4] = 0xFD

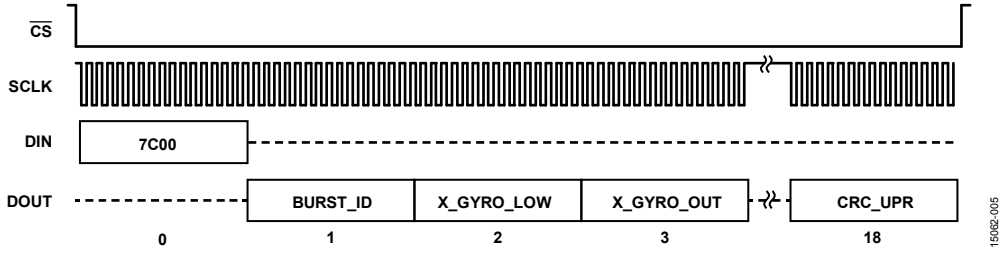

Figure 5. Burst Read Function Sequence Diagram, 19 Segments

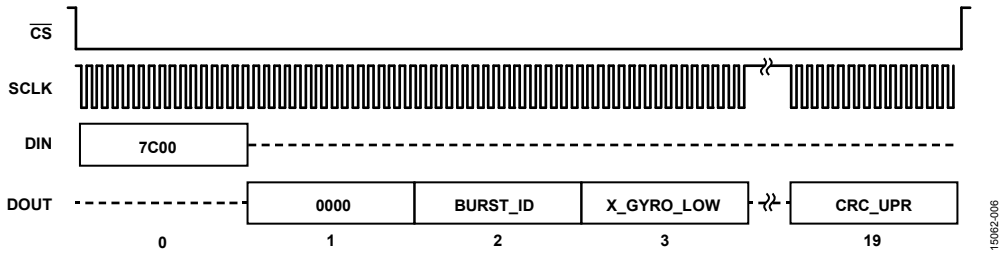

Figure 6. Burst Read Function Sequence Diagram, 20 Segments

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Mechanical Shock Survivability	
Any Axis, Unpowered	1500 *g*
Any Axis, Powered	1500 *g*
VDD to GND	−0.3 V to +3.6 V
Digital Input Voltage to GND	−0.3 V to VDD + 0.2 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.2 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range[1]	−55°C to +150°C
Barometric Pressure	2 bar

[1] Extended exposure to temperatures that are lower than −40°C or higher than +105°C can adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Pay careful attention to PCB thermal design.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

The ADIS16495 is a multichip module, which includes many active components. The values in Table 5 identify the thermal response of the hottest component inside of the ADIS16495, with respect to the overall power dissipation of the module. This approach enables a simple method for predicting the temperature of the hottest junction, based on either ambient or case temperature.

For example, when the T_A = 70°C, the hottest junction inside of the ADIS16495 is 76.7°C.

$$T_J = \theta_{JA} \times V_{DD} \times I_{DD} + 70°C$$

$$T_J = 22.8°C/W \times 3.3\ V \times 0.089\ A + 70°C$$

$$T_J = 76.7°C$$

Table 5. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
ML-24-9[1]	30.7°C/W	20.9°C/W	42 g

[1] Thermal impedance simulated values come from a case when 4 M2 × 0.4 mm machine screws (torque = 20 inch ounces) secure the ADIS16495 to the PCB.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

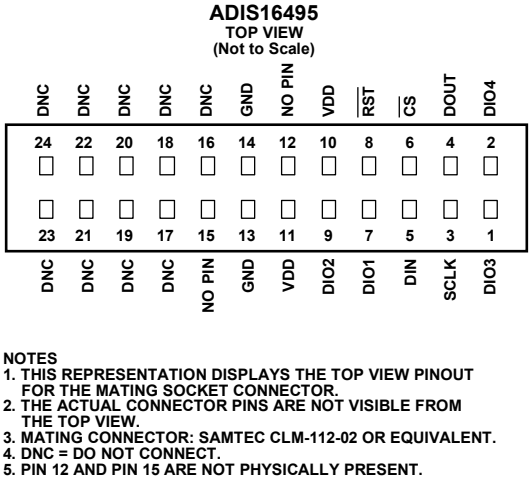

Figure 7. Pin Configuration

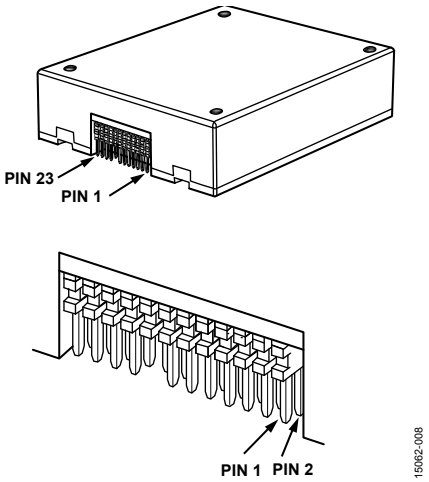

Figure 8. Axial Orientation (Top Side Facing Up)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	DIO3	Input/output	Configurable Digital Input/Output 3.
2	DIO4	Input/output	Configurable Digital Input/Output 4.
3	SCLK	Input	SPI Serial Clock.
4	DOUT	Output	SPI Data Output. Clocks output on the SCLK falling edge.
5	DIN	Input	SPI Data Input. Clocks input on the SCLK rising edge.
6	$\overline{CS}$	Input	SPI Chip Select.
7	DIO1	Input/output	Configurable Digital Input/Output 1.
8	$\overline{RST}$	Input	Reset.
9	DIO2	Input/output	Configurable Digital Input/Output 2.
10, 11	VDD	Supply	Power Supply.
12, 15	NO PIN	Not applicable	No Pin. These pins are not physically present.
13, 14	GND	Supply	Power Ground.
16 to 24	DNC	Not applicable	Do Not Connect. Do not connect to these pins.

TYPICAL PERFORMANCE CHARACTERISTICS

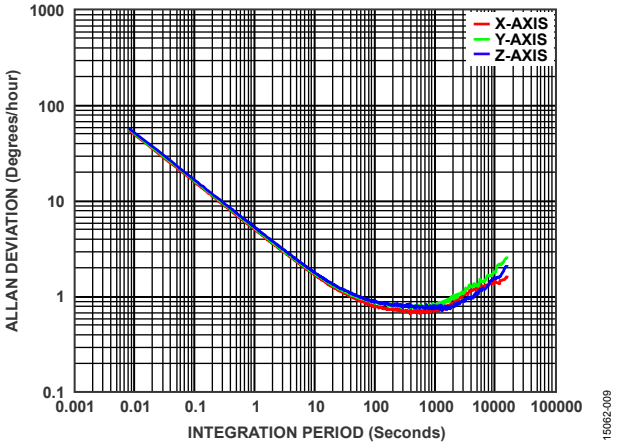

Figure 9. Gyroscope Allan Deviation, ADIS16495-1

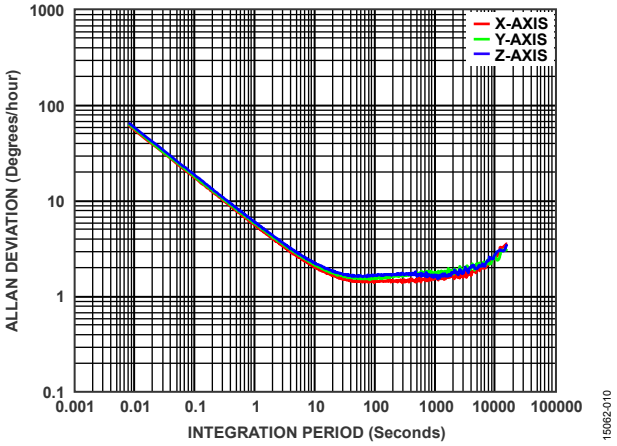

Figure 10. Gyroscope Allan Deviation, ADIS16495-2

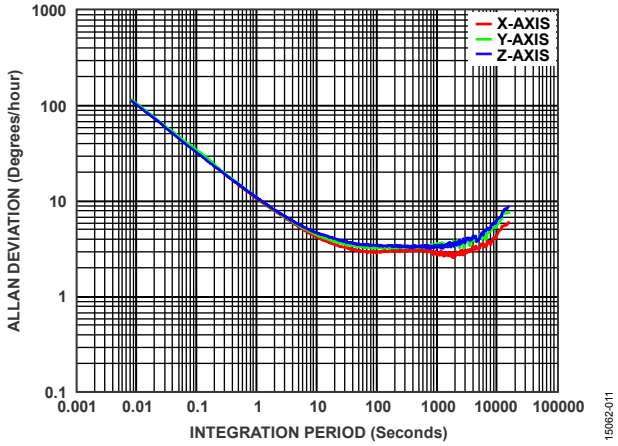

Figure 11. Gyroscope Allan Deviation, ADIS16495-3

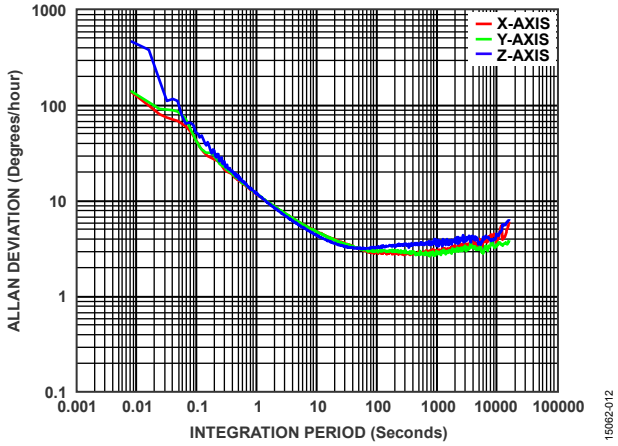

Figure 12. Accelerometer Allan Deviation

THEORY OF OPERATION

The ADIS16495 is an autonomous sensor system that starts up on its own when it has a valid power supply. After running through its initialization process, it begins sampling, processing, and loading calibrated sensor data into the output registers, which are accessible using the SPI port.

INERTIAL SENSOR SIGNAL CHAIN

Figure 13 shows the basic signal chain for the inertial sensors in the ADIS16495, which processes data at a rate of 4250 SPS when using the internal sample clock. Using one of the external clock options in FNCTIO_CTRL, Bits[7:4] (see Table 144) can provide some flexibility in selecting this rate.

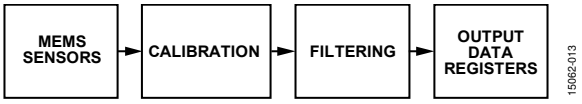

Figure 13. Signal Processing Diagram, Inertial Sensors

Gyroscope Data Sampling

The ADIS16495 produces angular rate measurements around three orthogonal axes (x, y, and z). Figure 14 shows the basic signal flow for the production of x-axis gyroscope data (same as y-axis and z-axis). This signal chain contains two digital MEMS gyroscopes (X_{G1} and X_{G2}), which have their own ADC and sample clocks (f_{SGX1} and f_{SGX2} = 4100 Hz) that produce data independently from each other. The sensor to sensor tolerance on this sample rate is ±200 samples per second (SPS). Processing this data starts with combining (summation and rescale) the most recent sample from each gyroscope together by using an independent sample master frequency (f_{SM}) clock (f_{SM} = 4250 Hz, see Figure 14), which drives the rest of the digital signal processing (calibration, alignment, and filtering) for the gyroscopes and accelerometers.

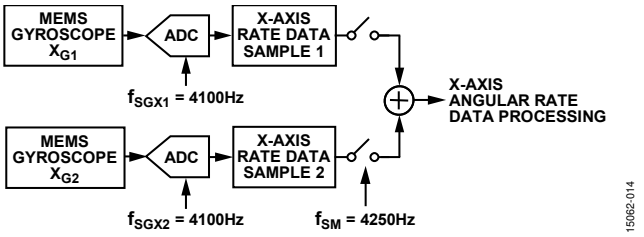

Figure 14. Gyroscope Data Sampling

Accelerometer Data Sampling

The ADIS16495 produces linear acceleration measurements along the same orthogonal axes (x, y, and z) as the gyroscopes, using the same clock (f_{SM}, see Figure 14 and Figure 15) that triggers data acquisition and subsequent processing of the gyroscope data.

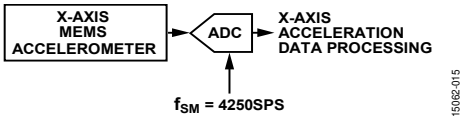

Figure 15. Accelerometer Data Sampling

External Clock Options

The ADIS16495 offers two modes of operation to control data production with an external clock: sync mode and PPS mode. In sync mode, the external clock directly controls the data sampling and production clock (f_{SM} in Figure 14 and Figure 15). In PPS mode the user can provide a lower input clock rate (1 Hz to 128 Hz) and use a scale factor (SYNC_SCALE register, see Table 154) to establish a data collection and processing rate that is between 3000 Hz and 4250 Hz for best performance.

Inertial Sensor Calibration

The calibration function for the gyroscopes and the accelerometers has two components: factory calibration and user calibration (see Figure 16).

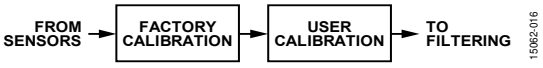

Figure 16. Gyroscope Calibration Processing

Gyroscope Factory Calibration

Gyroscope factory calibration applies the following correction formula to the data of each gyroscope:

$$\begin{bmatrix} \omega_{XC} \\ \omega_{YC} \\ \omega_{ZC} \end{bmatrix} = \begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix} \times \begin{bmatrix} \omega_X \\ \omega_Y \\ \omega_Z \end{bmatrix} + \begin{bmatrix} b_X \\ b_Y \\ b_Z \end{bmatrix} + \begin{bmatrix} g_{11} & g_{12} & g_{13} \\ g_{21} & g_{22} & g_{23} \\ g_{31} & g_{32} & g_{33} \end{bmatrix} \times \begin{bmatrix} a'_X \\ a'_Y \\ a'_Z \end{bmatrix} \quad (1)$$

where:

ω_{XC}, ω_{YC}, and ω_{ZC} are the postcalibration gyroscope data.
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} are the scale and alignment correction factors.
ω_X, ω_Y, and ω_Z are the precalibration gyroscope data.
b_X, b_Y, and b_Z are the bias correction factors.
g_{11}, g_{12}, g_{13}, g_{21}, g_{22}, g_{23}, g_{31}, g_{32}, and g_{33} are the linear g correction factors.
a'_X, a'_Y, and a'_Z are the postcalibration accelerometer data.

All the correction factors in each matrix/array are derived from direct observation of the response of each gyroscope to a variety of rotation rates at multiple temperatures across the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the flash memory bank, but they are not available for observation. Bit 7 in the CONFIG register provides an on/off control for the linear g compensation (see Table 148). See Figure 37 for more details on the user calibration options that are available for the gyroscopes.

Accelerometer Factory Calibration

The accelerometer factory calibration applies the following correction formulas to the data of each accelerometer:

$$\begin{bmatrix} a'_X \\ a'_Y \\ a'_Z \end{bmatrix} = \begin{bmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{bmatrix} \times \begin{bmatrix} a_X \\ a_Y \\ a_Z \end{bmatrix} + \begin{bmatrix} b_X \\ b_Y \\ b_Z \end{bmatrix} + \begin{bmatrix} 0 & p_{12} & p_{13} \\ p_{21} & 0 & p_{23} \\ p_{31} & p_{32} & 0 \end{bmatrix} \times \begin{bmatrix} \omega^2_{XC} \\ \omega^2_{YC} \\ \omega^2_{ZC} \end{bmatrix} \quad (2)$$

where:

a'_X, a'_Y, and a'_Z are the postcalibration accelerometer data.

m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} are the scale and alignment correction factors.

a_X, a_Y, and a_Z are the precalibration accelerometer data.

b_X, b_Y, and b_Z are the bias correction factors.

0, p_{12}, p_{13}, p_{21}, p_{23}, p_{31}, and p_{32} are the point of percussion correction factors

ω^2_{XC}, ω^2_{YC}, and ω^2_{ZC} are the postcalibration gyroscope data (squared).

All the correction factors in each matrix/array are derived from direct observation of the response of each accelerometer to a variety of inertial test conditions at multiple temperatures across the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the flash memory bank, but they are not available for observation. Bit 6 in the CONFIG register provides an on/off control for the point of percussion alignment (see Table 148). See Figure 38 for more details on the user calibration options that are available for the accelerometers.

Filtering

After calibration, the data of each inertial sensor passes through two digital filters, both of which have user configurable attributes: FIR and decimation (see Figure 17).

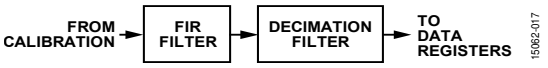

Figure 17. Inertial Sensor Filtering

The FIR filter includes four banks of coefficients that have 120 taps each. Register FILTR_BNK_0 (see Table 158) and Register FILTR_BNK_1 (see Table 160) provide the configuration options for the use of the FIR filters of each inertial sensor. Each FIR filter bank includes a preconfigured filter, but the user can design their own filters and write over these values using the register of each coefficient. For example, Table 163 provides the details for the FIR_COEF_A071 register, which contains Coefficient 71 in FIR Bank A. Refer to Figure 41 for the frequency response of the factory default filters. These filters do not represent any specific application environment; they are only examples.

The decimation filter averages multiple samples together to produce each register update. In this type of filter structure, the number of samples in the average is equal to the reduction in the update rate for the output data registers. See the DEC_RATE register for the user controls for this filter (see Table 150).

REGISTER STRUCTURE

All communication with the ADIS16495 involves accessing its user registers. The register structure contains both output data and control registers. The output data registers include the latest sensor data, error flags, and identification data. The control registers include sample rate, filtering, I/O, calibration, and diagnostic configuration options. All com-munication between the ADIS16495 and an external processor involves either reading or writing to one of the user registers.

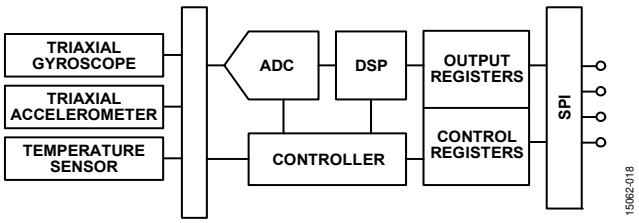

Figure 18. Basic Operation

The register structure uses a paged addressing scheme that contains 13 pages, with each page containing 64 register locations. Each register is 16 bits wide, with each byte having its own unique address within the memory map of that page. The SPI port has access to one page at a time, using the bit sequence in Figure 19. Select the page to activate for SPI access by writing its code to the PAGE_ID register. Read the PAGE_ID register to determine which page is currently active. Table 7 displays the PAGE_ID contents for each page and their basic functions. The PAGE_ID register is located at Address 0x00 on every page.

Table 7. User Register Page Assignments

Page	PAGE_ID	Function
0	0x00	Output data, clock, identification
1	0x01	Reserved
2	0x02	Calibration
3	0x03	Control: sample rate, filtering, I/O
4	0x04	Serial number, cyclic redundancy check (CRC) values
5	0x05	FIR Filter Bank A, Coefficient 0 to Coefficient 59
6	0x06	FIR Filter Bank A, Coefficient 60 to Coefficient 119
7	0x07	FIR Filter Bank B, Coefficient 0 to Coefficient 59
8	0x08	FIR Filter Bank B, Coefficient 60 to Coefficient 119
9	0x09	FIR Filter Bank C, Coefficient 0 to Coefficient 59
10	0x0A	FIR Filter Bank C, Coefficient 60 to Coefficient 119
11	0x0B	FIR Filter Bank D, Coefficient 0 to Coefficient 59
12	0x0C	FIR Filter Bank D, Coefficient 60 to Coefficient 119

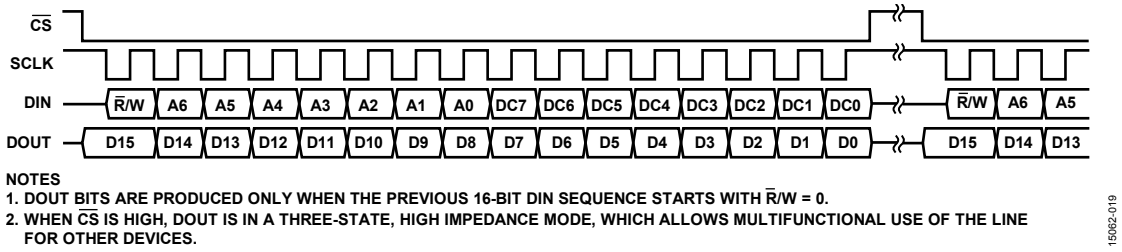

Figure 19. SPI Communication Bit Sequence

SERIAL PERIPHERAL INTERFACE

The SPI provides access to all of the user accessible registers (see Table 8) and typically connects to a compatible port on an embedded processor platform. See Figure 20 for a diagram that provides the most common connections between the ADIS16495 and an embedded processor.

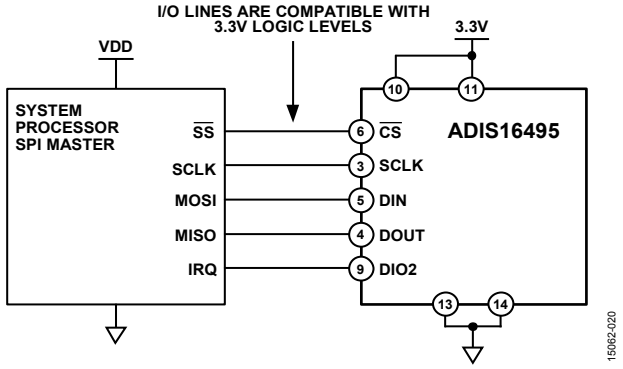

Figure 20. Electrical Connection Diagram

Table 8. Generic Master Processor Pin Names and Functions

Mnemonic	Function
$\overline{SS}$	Slave select
IRQ	Interrupt request
MOSI	Master output, slave input
MISO	Master input, slave output
SCLK	Serial clock

Embedded processors typically use control registers to configure their serial ports for communicating with SPI slave devices such as the ADIS16495. Table 9 provides a list of settings that describe the SPI protocol of the ADIS16495. The initialization routine of the master processor typically establishes these settings using firmware commands to write them into its serial control registers.

Table 9. Generic Master Processor SPI Settings

Processor Setting	Description
Master	ADIS16495 operates as slave
SCLK ≤ 15 MHz	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence, see Figure 19 for coding
16-Bit Mode	Shift register/data length

DATA READY

The factory default configuration provides users with a data ready (DR) signal on the DIO2 pin, which pulses low when the output data registers are updating (see Figure 21). In this configuration, connect DIO2 to an interrupt service pin on the embedded processor, which triggers data collection, when this signal pulses high. Register FNCTIO_CTRL, Bits[3:0] (see Table 144) provide some user configuration options for this function.

Figure 21. Data Ready, when FNCTIO_CTRL, Bits[3:0] = 1101 (Default)

During the start-up and reset recovery processes, the DR signal can exhibit some transient behavior before data production begins. Figure 22 provides an example of the DR behavior during startup, and Figure 23 and Figure 24 provide examples of the DR behavior during recovery from reset commands.

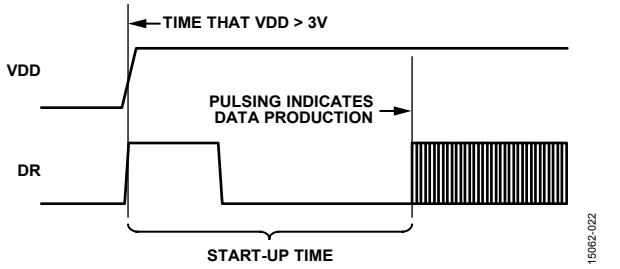

Figure 22. Data Ready Response During Startup

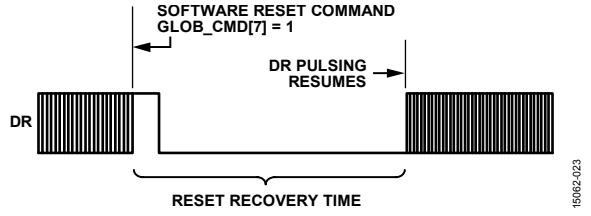

Figure 23. Data Ready Response During Reset (Register GLOB_CMD, Bit 7 = 1) Recovery

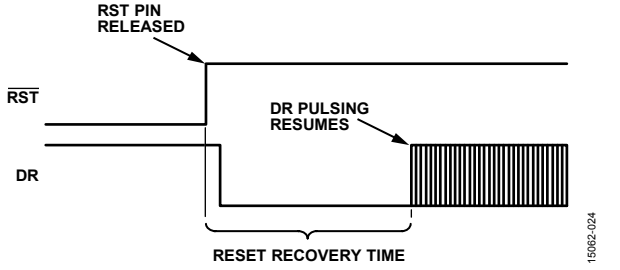

Figure 24. Data Ready Response During Reset ($\overline{RST}$ = 0) Recovery

READING SENSOR DATA

Reading a single register requires two 16-bit cycles on the SPI: one to request the contents of a register and another to receive those contents. The 16-bit command code (see Figure 19) for a read request on the SPI has three parts: the read bit ($\overline{R}/W = 0$), the 7-bit address code for either address (upper or lower) of the register, Bits[A6:A0], and eight don't care bits, Bits[DC7:DC0]. Figure 25 provides an example that includes two register reads in succession. This example starts with DIN = 0x1A00, to request the contents of the Z_GYRO_OUT register, and follows with 0x1800, to request the contents of the Z_GYRO_LOW register (assuming PAGE_ID already equals 0x0000). The sequence in Figure 25 also shows full duplex mode of operation, which means that the ADIS16495 can receive requests on DIN while also transmitting data out on DOUT within the same 16-bit SPI cycle.

Figure 25. SPI Read Example

Figure 26 provides an example of the four SPI signals when reading the PROD_ID register (see Table 92) in a repeating pattern. This pattern can be helpful when troubleshooting the SPI interface setup and communications.

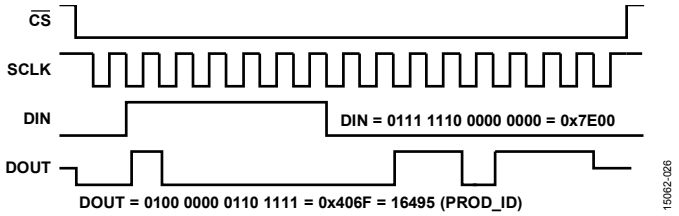

Figure 26. SPI Read Example, Second 16-Bit Sequence

Burst Read Function

The burst read function (BRF) provides a method for reading a batch of data (status, temperature, gyroscopes, accelerometers, time stamp/data counter, and CRC code), which does not require a stall time between each 16-bit segment and only requires one command on the DIN line to initiate. System processors can execute this mode by reading the BURST_CMD register (DIN = 0x7C00) and then reading each segment of data in the response, while holding the $\overline{CS}$ line in a low state, until after reading the last 16-bit segment of data. If the $\overline{CS}$ line goes high before the completion of all data acquisition, the data from that read request is lost.

The BRF contains either 19 or 20 different data segments (16-bits each), depending on the SCLK rate. When using a SCLK rate that is less than 3 MHz, the BRF response uses the sequencing diagram in Figure 5 and the data format that is in Table 10. When using a SCLK rate that is greater than 3.6 MHz, the BRF response uses the sequencing diagram in Figure 6 and the data format in Table 11. When using an SCLK rate that is in between 3 MHz and 3.6 MHz, the ADIS16495 can use either format.

To manage that variation, use the BURST_ID code (0xA5A5 in Table 10 and Table 11) as an identifier for when the ADIS16495 BRF response is starting.

Table 10. BRF Data Format (f_{SCLK} < 3 MHz)[1]

Segment	DIN	DOUT
0	0x7C00	N/A
1	N/A	0xA5A5 (BURST_ID)
2	N/A	SYS_E_FLAG
3	N/A	TEMP_OUT
4	N/A	X_GYRO_LOW
5	N/A	X_GYRO_OUT
6	N/A	Y_GYRO_LOW
7	N/A	Y_GYRO_OUT
8	N/A	Z_GYRO_LOW
9	N/A	Z_GYRO_OUT
10	N/A	X_ACCL_LOW
11	N/A	X_ACCL_OUT
12	N/A	Y_ACCL_LOW
13	N/A	Y_ACCL_OUT
14	N/A	Z_ACCL_LOW
15	N/A	Z_ACCL_OUT
16	N/A	DATA_CNT (FNCTIO_CTRL, Bits[8:7] ≠ 11)
		TIME_STAMP (FNCTIO_CTRL, Bits[8:7] = 11)
17	N/A	CRC_LWR
18	N/A	CRC_UPR

[1] N/A means not applicable.

Table 11. BRF Data Format (f_{SCLK} > 3.6 MHz)[1]

Segment	DIN	DOUT
0	0x7C00	N/A
1	N/A	0x0000
2	N/A	0xA5A5 (BURST_ID)
3	N/A	SYS_E_FLAG
4	N/A	TEMP_OUT
5	N/A	X_GYRO_LOW
6	N/A	X_GYRO_OUT
7	N/A	Y_GYRO_LOW
8	N/A	Y_GYRO_OUT
9	N/A	Z_GYRO_LOW
10	N/A	Z_GYRO_OUT
11	N/A	X_ACCL_LOW
12	N/A	X_ACCL_OUT
13	N/A	Y_ACCL_LOW
14	N/A	Y_ACCL_OUT
15	N/A	Z_ACCL_LOW
16	N/A	Z_ACCL_OUT
17	N/A	DATA_CNT (FNCTIO_CTRL, Bits[8:7] ≠ 11)
		TIME_STAMP (FNCTIO_CTRL, Bits[8:7] = 11)
18	N/A	CRC_LWR
19	N/A	CRC_UPR

[1] N/A means not applicable.

DEVICE CONFIGURATION

Each register contains 16 bits (two bytes); Bits[7:0] contain the low byte and Bits[15:8] contain the high byte. Each byte has its own unique address in the user register map (see Table 12). Updating the contents of a register requires writing to its low byte first and its high byte second. There are three parts to coding a SPI command (see Figure 19), which writes a new byte of data to a register: the write bit ($\overline{R}/W = 1$), the 7-bit address code for the byte that this command is updating, and the new data for that location, Bits[DC7:DC0]. Figure 27 provides a coding example for writing 0xFEDC to the XG_BIAS_LOW register (see Table 106), assuming that PAGE_ID already equals 0x0002.

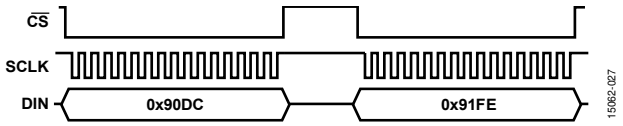

Figure 27. SPI Sequence for Writing 0xFEDC to XG_BIAS_LOW

Dual Memory Structure

The ADIS16495 uses a dual memory structure (see Figure 28), with static random access memory (SRAM) supporting real-time operation and flash memory storing operational code, calibration coefficients, and user configurable register settings. The manual flash update command (GLOB_CMD, Bit 3, see Table 142) provides a single-command method for storing user configuration settings into flash memory, for automatic recall during the next power-on or reset recovery process.

This portion of the flash memory bank has two independent banks that operate in a ping pong manner, alternating with every flash update. During power-on or reset recovery, the ADIS16495 performs a CRC on the SRAM and compares it to a CRC computation from the same memory locations in flash memory. If this memory test fails, the ADIS16495 resets and boots up from the other flash memory location. SYS_E_FLAG, Bit 2 (see Table 18) provides an error flag for detecting when the backup flash memory supported the last power-on or reset recovery. Table 12 provides a memory map for the user registers in the ADIS16495, which includes flash backup support (indicated by yes or no in the flash column).

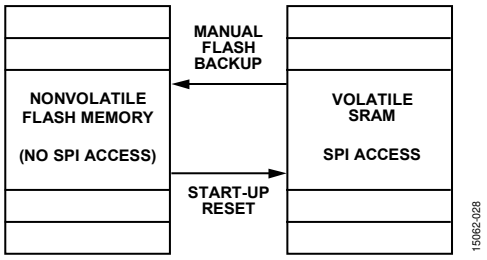

Figure 28. SRAM and Flash Memory Diagram

USER REGISTER MEMORY MAP

Table 12. User Register Memory Map[1]

Register Name	R/W	Flash Backup	PAGE_ID	Address	Default	Register Description
PAGE_ID	R/W	No	0x00	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x00	0x02, 0x03	N/A	Reserved
DATA_CNT	R	No	0x00	0x04, 0x05	N/A	Data counter
Reserved	N/A	N/A	0x00	0x06, 0x07	N/A	Reserved
SYS_E_FLAG	R	No	0x00	0x08, 0x09	0x0000	Output, system error flags
DIAG_STS	R	No	0x00	0x0A, 0x0B	0x0000	Output, self test error flags
Reserved	N/A	N/A	0x00	0x0C, 0x0D	N/A	Reserved
TEMP_OUT	R	No	0x00	0x0E, 0x0F	N/A	Output, temperature
X_GYRO_LOW	R	No	0x00	0x10, 0x11	N/A	Output, x-axis gyroscope, low word
X_GYRO_OUT	R	No	0x00	0x12, 0x13	N/A	Output, x-axis gyroscope, high word
Y_GYRO_LOW	R	No	0x00	0x14, 0x15	N/A	Output, y-axis gyroscope, low word
Y_GYRO_OUT	R	No	0x00	0x16, 0x17	N/A	Output, y-axis gyroscope, high word
Z_GYRO_LOW	R	No	0x00	0x18, 0x19	N/A	Output, z-axis gyroscope, low word
Z_GYRO_OUT	R	No	0x00	0x1A, 0x1B	N/A	Output, z-axis gyroscope, high word
X_ACCL_LOW	R	No	0x00	0x1C, 0x1D	N/A	Output, x-axis accelerometer, low word
X_ACCL_OUT	R	No	0x00	0x1E, 0x1F	N/A	Output, x-axis accelerometer, high word
Y_ACCL_LOW	R	No	0x00	0x20, 0x21	N/A	Output, y-axis accelerometer, low word
Y_ACCL_OUT	R	No	0x00	0x22, 0x23	N/A	Output, y-axis accelerometer, high word
Z_ACCL_LOW	R	No	0x00	0x24, 0x25	N/A	Output, z-axis accelerometer, low word
Z_ACCL_OUT	R	No	0x00	0x26, 0x27	N/A	Output, z-axis accelerometer, high word
TIME_STAMP	R	No	0x00	0x28, 0x29	N/A	Output, time stamp
CRC_LWR	R	No	0x00	0x2A, 0x2B	N/A	Output, CRC-32 (32 bits), lower word
CRC_UPR	R	No	0x00	0x2C, 0x2D	N/A	Output, CRC-32, upper word
Reserved	N/A	N/A	0x00	0x2A to 0x3F	N/A	Reserved
X_DELTANG_LOW	R	No	0x00	0x40, 0x41	N/A	Output, x-axis delta angle, low word
X_DELTANG_OUT	R	No	0x00	0x42, 0x43	N/A	Output, x-axis delta angle, high word
Y_DELTANG_LOW	R	No	0x00	0x44, 0x45	N/A	Output, y-axis delta angle, low word
Y_DELTANG_OUT	R	No	0x00	0x46, 0x47	N/A	Output, y-axis delta angle, high word
Z_DELTANG_LOW	R	No	0x00	0x48, 0x49	N/A	Output, z-axis delta angle, low word
Z_DELTANG_OUT	R	No	0x00	0x4A, 0x4B	N/A	Output, z-axis delta angle, high word
X_DELTVEL_LOW	R	No	0x00	0x4C, 0x4D	N/A	Output, x-axis delta velocity, low word
X_DELTVEL_OUT	R	No	0x00	0x4E, 0x4F	N/A	Output, x-axis delta velocity, high word
Y_DELTVEL_LOW	R	No	0x00	0x50, 0x51	N/A	Output, y-axis delta velocity, low word
Y_DELTVEL_OUT	R	No	0x00	0x52, 0x53	N/A	Output, y-axis delta velocity, high word
Z_DELTVEL_LOW	R	No	0x00	0x54, 0x55	N/A	Output, z-axis delta velocity, low word
Z_DELTVEL_OUT	R	No	0x00	0x56, 0x57	N/A	Output, z-axis delta velocity, high word
Reserved	N/A	N/A	0x00	0x58 to 0x7B	N/A	Reserved
BURST_CMD	R	No	0x00	0x7C, 0x7D	N/A	Burst read command
PROD_ID	R	Yes	0x00	0x7E, 0x7F	0x4071	Output, product identification (16,495)
Reserved	N/A	N/A	0x01	0x00 to 0x7F	N/A	Reserved
PAGE_ID	R/W	No	0x02	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x02	0x02, 0x03	N/A	Reserved
X_GYRO_SCALE	R/W	Yes	0x02	0x04, 0x05	0x0000	Calibration, scale, x-axis gyroscope
Y_GYRO_SCALE	R/W	Yes	0x02	0x06, 0x07	0x0000	Calibration, scale, y-axis gyroscope
Z_GYRO_SCALE	R/W	Yes	0x02	0x08, 0x09	0x0000	Calibration, scale, z-axis gyroscope
X_ACCL_SCALE	R/W	Yes	0x02	0x0A, 0x0B	0x0000	Calibration, scale, x-axis accelerometer
Y_ACCL_SCALE	R/W	Yes	0x02	0x0C, 0x0D	0x0000	Calibration, scale, y-axis accelerometer
Z_ACCL_SCALE	R/W	Yes	0x02	0x0E, 0x0F	0x0000	Calibration, scale, z-axis accelerometer
XG_BIAS_LOW	R/W	Yes	0x02	0x10, 0x11	0x0000	Calibration, bias, gyroscope, x-axis, low word

Register Name	R/W	Flash Backup	PAGE_ID	Address	Default	Register Description
XG_BIAS_HIGH	R/W	Yes	0x02	0x12, 0x13	0x0000	Calibration, bias, gyroscope, x-axis, high word
YG_BIAS_LOW	R/W	Yes	0x02	0x14, 0x15	0x0000	Calibration, bias, gyroscope, y-axis, low word
YG_BIAS_HIGH	R/W	Yes	0x02	0x16, 0x17	0x0000	Calibration, bias, gyroscope, y-axis, high word
ZG_BIAS_LOW	R/W	Yes	0x02	0x18, 0x19	0x0000	Calibration, bias, gyroscope, z-axis, low word
ZG_BIAS_HIGH	R/W	Yes	0x02	0x1A, 0x1B	0x0000	Calibration, bias, gyroscope, z-axis, high word
XA_BIAS_LOW	R/W	Yes	0x02	0x1C, 0x1D	0x0000	Calibration, bias, accelerometer, x-axis, low word
XA_BIAS_HIGH	R/W	Yes	0x02	0x1E, 0x1F	0x0000	Calibration, bias, accelerometer, x-axis, high word
YA_BIAS_LOW	R/W	Yes	0x02	0x20, 0x21	0x0000	Calibration, bias, accelerometer, y-axis, low word
YA_BIAS_HIGH	R/W	Yes	0x02	0x22, 0x23	0x0000	Calibration, bias, accelerometer, y-axis, high word
ZA_BIAS_LOW	R/W	Yes	0x02	0x24, 0x25	0x0000	Calibration, bias, accelerometer, z-axis, low word
ZA_BIAS_HIGH	R/W	Yes	0x02	0x26, 0x27	0x0000	Calibration, bias, accelerometer, z-axis, high word
Reserved	N/A	N/A	0x02	0x28 to 0x73	0x0000	Reserved
USER_SCR_1	R/W	Yes	0x02	0x74, 0x75	0x0000	User Scratch Register 1
USER_SCR_2	R/W	Yes	0x02	0x76, 0x77	0x0000	User Scratch Register 2
USER_SCR_3	R/W	Yes	0x02	0x78, 0x79	0x0000	User Scratch Register 3
USER_SCR_4	R/W	Yes	0x02	0x7A, 0x7B	0x0000	User Scratch Register 4
FLSHCNT_LOW	R	Yes	0x02	0x7C, 0x7D	N/A	Diagnostic, flash memory count, low word
FLSHCNT_HIGH	R	Yes	0x02	0x7E, 07F	N/A	Diagnostic, flash memory count, high word
PAGE_ID	R/W	No	0x03	0x00, 0x01	0x0000	Page identifier
GLOB_CMD	W	No	0x03	0x02, 0x03	N/A	Control, global commands
Reserved	N/A	N/A	0x03	0x04, 0x05	N/A	Reserved
FNCTIO_CTRL	R/W	Yes	0x03	0x06, 0x07	0x000D	Control, I/O pins, functional definitions
GPIO_CTRL	R/W	Yes	0x03	0x08, 0x09	0x00X0[2]	Control, I/O pins, general-purpose
CONFIG	R/W	Yes	0x03	0x0A, 0x0B	0x00C0	Control, clock, and miscellaneous correction
DEC_RATE	R/W	Yes	0x03	0x0C, 0x0D	0x0000	Control, output sample rate decimation
NULL_CNFG	R/W	Yes	0x03	0x0E, 0x0F	0x070A	Control, automatic bias correction configuration
SYNC_SCALE	R/W	Yes	0x03	0x10, 0x11	0x109A	Control, input clock scaling (PPS mode)
RANG_MDL	R	N/A	0x03	0x12, 0x13	N/A	Measurement range (model-specific) Identifier
Reserved	N/A	N/A	0x03	0x14, 0x15	N/A	Reserved
FILTR_BNK_0	R/W	Yes	0x03	0x16, 0x17	0x0000	Filter selection
FILTR_BNK_1	R/W	Yes	0x03	0x18, 0x19	0x0000	Filter selection
Reserved	N/A	N/A	0x03	0x1A to 0x77	N/A	Reserved
FIRM_REV	R	Yes	0x03	0x78, 0x79	N/A	Firmware revision
FIRM_DM	R	Yes	0x03	0x7A, 0x7B	N/A	Firmware programming date (day/month)
FIRM_Y	R	Yes	0x03	0x7C, 0x7D	N/A	Firmware programming date (year)
BOOT_REV	R	Yes	0x03	0x7E, 0x7F	N/A	Boot loader revision
PAGE_ID	R/W	No	0x04	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x04	0x02, 0x03	N/A	Reserved
CAL_SIGTR_LWR	R	Yes	0x04	0x04, 0x05	N/A	Signature CRC, calibration coefficients, low word
CAL_SIGTR_UPR	R	Yes	0x04	0x06, 0x07	N/A	Signature CRC, calibration coefficients, high word
CAL_DRVTN_LWR	R	No	0x04	0x08, 0x09	N/A	Real-time CRC, calibration coefficients, low word
CAL_DRVTN_UPR	R	No	0x04	0x0A, 0x0B	N/A	Real-time CRC, calibration coefficients, high word
CODE_SIGTR_LWR	R	Yes	0x04	0x0C, 0x0D	N/A	Signature CRC, program code, low word
CODE_SIGTR_UPR	R	Yes	0x04	0x0E, 0x0F	N/A	Signature CRC, program code, high word
CODE_DRVTN_LWR	R	No	0x04	0x10, 0x11	N/A	Real-time CRC, program code, low word
CODE_DRVTN_UPR	R	No	0x04	0x12, 0x13	N/A	Real-time CRC, program code, high word
Reserved	N/A	N/A	0x04	0x1C to 0x1F	N/A	Reserved
SERIAL_NUM	R	Yes	0x04	0x20, 0x21	N/A	Serial number
Reserved	N/A	N/A	0x04	0x22 to 0x7F	N/A	Reserved
PAGE_ID	R/W	No	0x05	0x00, 0x01	0x0000	Page identifier
Reserved	N/A	N/A	0x05	0x02 to 0x07	N/A	Reserved
FIR_COEF_Axxx[3]	R/W	Yes	0x05	0x08 to 0x7F	N/A	FIR Filter Bank A: Coefficient 0 through Coefficient 59

Register Name	R/W	Flash Backup	PAGE_ID	Address	Default	Register Description
PAGE_ID	R/W	No	0x06	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x06	0x02 to 0x07	N/A	Reserved
FIR_COEF_Axxx[3]	R/W	Yes	0x06	0x08 to 0x7F	N/A	FIR Filter Bank A: Coefficient 60 through Coefficient 119
PAGE_ID	R/W	No	0x07	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x07	0x02 to 0x07	N/A	Reserved
FIR_COEF_Bxxx[4]	R/W	Yes	0x07	0x08 to 0x7F	N/A	FIR Filter Bank B: Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x08	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x08	0x02 to 0x07	N/A	Reserved
FIR_COEF_Bxxx[4]	R/W	Yes	0x08	0x08 to 0x7F	N/A	FIR Filter Bank B: Coefficient 60 through Coefficient 119
PAGE_ID	R/W	No	0x09	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x09	0x02 to 0x07	N/A	Reserved
FIR_COEF_Cxxx[5]	R/W	Yes	0x09	0x08 to 0x7F	N/A	FIR Filter Bank C: Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x0A	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x0A	0x02 to 0x07	N/A	Reserved
FIR_COEF_Cxxx[5]	R/W	Yes	0x0A	0x08 to 0x7F	N/A	FIR Filter Bank C: Coefficient 60 through Coefficient 119
PAGE_ID	R/W	No	0x0B	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x0B	0x02 to 0x07	N/A	Reserved
FIR_COEF_Dxxx[6]	R/W	Yes	0x0B	0x08 to 0x7F	N/A	FIR Filter Bank D: Coefficient 0 through Coefficient 59
PAGE_ID	R/W	No	0x0C	0x00	0x0000	Page identifier
Reserved	N/A	N/A	0x0C	0x02 to 0x07	N/A	Reserved
FIR_COEF_Dxxx[6]	R/W	Yes	0x0C	0x08 to 0x7F	N/A	FIR Filter Bank D: Coefficient 60 through Coefficient 119

[1] N/A means not applicable.
[2] The GPIO_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.
[3] See the FIR Filter Bank A, FIR_COEF_A000 to FIR_COEF_A119 section for additional information.
[4] See the FIR Filter Bank B, FIR_COEF_B000 to FIR_COEF_B119 section for additional information.
[5] See the FIR Filter Bank C, FIR_COEF_C000 to FIR_COEF_C119 section for additional information.
[6] See the FIR Filter Bank D, FIR_COEF_D000 to FIR_COEF_D119 section for additional information.

USER REGISTER DEFINTIONS

PAGE NUMBER (PAGE_ID)

The contents in the PAGE_ID register (see Table 13 and Table 14) contain the current page setting, and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 for SPI-based user access. See Table 12 for the page assignments associated with each user accessible register.

Table 13. PAGE_ID Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x00, 0x01	0x0000	R/W	No

Table 14. PAGE_ID Bit Descriptions

Bits	Description
[15:0]	Page number, binary numerical format

DATA/SAMPLE COUNTER (DATA_CNT)

The DATA_CNT register (see Table 15 and Table 16) is a continuous, real-time, sample counter. It starts at 0x0000, increments every time the output data registers update, and wraps around from 0xFFFF (65,535 decimal) to 0x0000 (0 decimal).

Table 15. DATA_CNT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x04, 0x05	Not applicable	R	No

Table 16. DATA_CNT Bit Descriptions

Bits	Description
[15:0]	Data counter, binary format

STATUS/ERROR FLAG INDICATORS (SYS_E_FLAG)

The SYS_E_FLAG register (see Table 17 and Table 18) provides various error flags. Reading this register causes all of its bits to return to 0, with the exception of Bit 7. If an error condition persists, its flag (bit) automatically returns to an alarm value of 1.

Table 17. SYS_E_FLAG Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x08, 0x09	0x0000	R	No

Table 18. SYS_E_FLAG Bit Descriptions

Bits	Description
15	Watchdog timer flag. A 1 indicates the ADIS16495 automatically resets itself to clear an issue.
[14:9]	Not used.
8	Sync error. A 1 indicates the sample timing is not scaling correctly, when operating in PPS mode (FNCTIO_CTRL, Bit 8 = 1, see Table 144). When this error occurs, verify that the input sync frequency is correct and that SYNC_SCALE (see Table 154) has the correct value.
7	Processing overrun. A 1 indicates the occurrence of a processing overrun. Initiate a reset to recover. Replace the ADIS16495 if this error persists.
6	Flash memory update failure. A 1 indicates that the most recent flash memory update failed (GLOB_CMD, Bit 3, see Table 142). Repeat the test and replace the ADIS16495 if this error persists.
5	Sensor failure. A 1 indicates failure in at least one of the inertial sensors. Read the DIAG_STS register (see Table 20) to determine which sensor is failing. Replace the ADIS16495 if the error persists, when it is operating in static inertial conditions.
4	Not used.
3	SPI communication error. A 1 indicates that the total number of SCLK cycles is not equal to an integer multiple of 16. Repeat the previous communication sequence to recover. Persistence in this error can indicate a weakness in the SPI service from the master processor.
2	SRAM error condition. A 1 indicates a failure in the CRC (period = 20 ms) between the SRAM and flash memory. Initiate a reset to recover. Replace the ADIS16495 if this error persists.
1	Boot memory failure. A 1 indicates that the device booted up using code from the backup memory bank. Replace the ADIS16495 if this error occurs.
0	Not used.

SELF TEST ERROR FLAGS (DIAG_STS)

SYS_E_FLAG, Bit 5 (see Table 18) contains the pass/fail result (0 = pass) for the on demand self test (ODST) operations, whereas the DIAG_STS register (see Table 19 and Table 20) contains pass/fail flags (0 = pass) for each inertial sensor. Reading the DIAG_STS register causes all of its bits to restore to 0. The bits in DIAG_STS return to 1 if the error conditions persists.

Table 19. DIAG_STS Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x0A, 0x0B	0x0000	R	No

Table 20. DIAG_STS Bit Descriptions

Bits	Description (Default = 0x0000)
[15:6]	Not used
5	Self test failure, z-axis accelerometer (1 means failure)
4	Self test failure, y-axis accelerometer (1 means failure)
3	Self test failure, x-axis accelerometer (1 means failure)
2	Self test failure, z-axis gyroscope (1 means failure)
1	Self test failure, y-axis gyroscope (1 means failure)
0	Self test failure, x-axis gyroscope (1 means failure)

INTERNAL TEMPERATURE (TEMP_OUT)

The TEMP_OUT register (see Table 21 and Table 22) provides a coarse measurement of the temperature inside of the ADIS16495. This data is useful for monitoring relative changes in the thermal environment. Table 23 provides several examples of the data format for the TEMP_OUT register.

Table 21. TEMP_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x0E, 0x0F	Not applicable	R	No

Table 22. TEMP_OUT Bit Descriptions

Bits	Description
[15:0]	Temperature data; twos complement, 1°C per 80 LSB, 25°C = 0x0000

Table 23. TEMP_OUT Data Format Examples

Temperature (°C)	Decimal	Hex	Binary
+85	+4800	0x12C0	0001 0010 1100 0000
+25 + 2/80	+2	0x0002	0000 0000 0000 0010
+25 + 1/80	+1	0x0001	0000 0000 0000 0001
+25	0	0x0000	0000 0000 0000 0000
+25 – 1/80	−1	0xFFFF	1111 1111 1111 1111
+25 – 2/80	−2	0xFFFE	1111 1111 1111 1110
−40	−5200	0xEBB0	1110 1011 1011 0000

GYROSCOPE DATA

The gyroscopes in the ADIS16495 measure the angular rate of rotation around three orthogonal axes (x, y, and z). Figure 30 shows the orientation of each gyroscope axis, which defines the direction of rotation that produces a positive response in each of the angular rate measurements.

Each gyroscope has two output data registers. Figure 29 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis gyroscope measurements. This format also applies to the y-axis and z-axis as well.

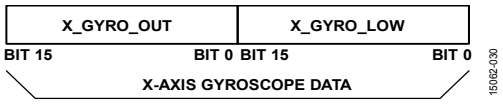

Figure 29. Gyroscope Output Data Structure

Gyroscope Measurement Range/Scale Factor

Table 24 provides the range and scale factor (K_G) for the angular rate (gyroscope) measurements in each ADIS16495 model.

Table 24. Gyroscope Measurement Range and Scale Factors

Model	Range	Scale Factor, K_G
ADIS16495-1BMLZ	±125°/sec	0.00625°/sec/LSB
ADIS16495-2BMLZ	±450°/sec	0.025°/sec/LSB
ADIS16495-3BMLZ	±2000°/sec	0.1°/sec/LSB

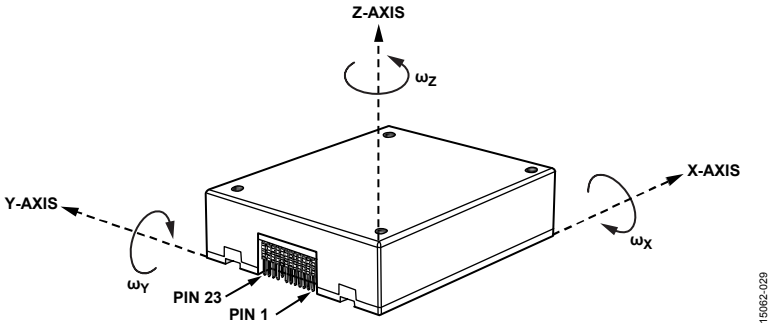

Figure 30. Gyroscope Axis and Polarity Assignments

Gyroscope Data Formatting

Table 25 and Table 26 offer various numerical examples that demonstrate the format of the rotation rate data in both 16-bit and 32-bit formats. See Table 24 for the scale factor (K_G) associated with each ADIS16495 model.

Table 25. 16-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hex	Binary
+10000 K_G	+10,000	0x2710	0010 0111 0001 0000
+2 K_G	+2	0x0002	0000 0000 0000 0010
+K_G	+1	0x0001	0000 0000 0000 0001
0°/sec	0	0x0000	0000 0000 0000 0000
−K_G	−1	0xFFFF	1111 1111 1111 1111
−2 K_G	−2	0xFFFE	1111 1111 1111 1110
−10000 K_G	−10,000	0xD8F0	1101 1000 1111 0000

Table 26. 32-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hexadecimal
+10000 K_G	+655,360,000	0x27100000
+$K_G/2^{15}$	+2	0x00000002
+$K_G/2^{16}$	+1	0x00000001
0	0	0x0000000
−K_G /2^{16}	−1	0xFFFFFFFF
−K_G /2^{15}	−2	0xFFFFFFFE
−10000 K_G	−655,360,000	0xD8F00000

X-Axis Gyroscope (X_GYRO_LOW, X_GRYO_OUT)

The X_GYRO_LOW (see Table 27 and Table 28) and X_GRYO_OUT (see Table 29 and Table 30) registers contain the gyroscope data for the x-axis.

Table 27. X_GYRO_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x10, 0x11	Not applicable	R	No

Table 28. X_GYRO_LOW Bit Descriptions

Bits	Description
[15:0]	X-axis gyroscope data; low word

Table 29. X_GYRO_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x12, 0x13	Not applicable	R	No

Table 30. X_GYRO_OUT Bit Descriptions

Bits	Description
[15:0]	X-axis gyroscope data; high word; twos complement, 0°/sec = 0x0000, see Table 24 for scale factor

Y-Axis Gyroscope (Y_GYRO_LOW, Y_GYRO_OUT)

The Y_GYRO_LOW (see Table 31 and Table 32) and Y_GRYO_OUT (see Table 33 and Table 34) registers contain the gyroscope data for the y-axis.

Table 31. Y_GYRO_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x14, 0x15	Not applicable	R	No

Table 32. Y_GYRO_LOW Bit Descriptions

Bits	Description
[15:0]	Y-axis gyroscope data; low word

Table 33. Y_GYRO_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x16, 0x17	Not applicable	R	No

Table 34. Y_GYRO_OUT Bit Descriptions

Bits	Description
[15:0]	Y-axis gyroscope data; high word; twos complement, 0°/sec = 0x0000, see Table 24 for scale factor

Z-Axis Gyroscope (Z_GYRO_LOW, Z_GYRO_OUT)

The Z_GYRO_LOW (see Table 35 and Table 36) and Z_GRYO_OUT (see Table 37 and Table 38) registers contain the gyroscope data for the z-axis.

Table 35. Z_GYRO_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x18, 0x19	Not applicable	R	No

Table 36. Z_GYRO_LOW Bit Descriptions

Bits	Description
[15:0]	Z-axis gyroscope data; additional resolution bits

Table 37. Z_GYRO_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1A, 0x1B	Not applicable	R	No

Table 38. Z_GYRO_OUT Bit Descriptions

Bits	Description
[15:0]	Z-axis gyroscope data; high word; twos complement, 0°/sec = 0x0000, see Table 24 for scale factor

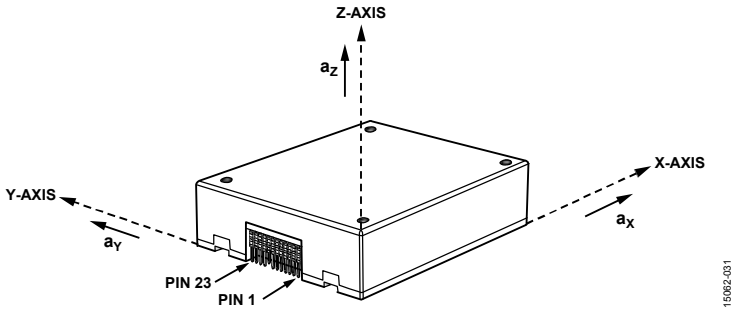

Figure 31. Accelerometer Axis and Polarity Assignments

ACCELERATION DATA

The accelerometers in the ADIS16495 measure both dynamic and static (response to gravity) acceleration along three orthogonal axes (x, y, and z). Figure 31 shows the orientation of each accelerometer axis, which defines the direction of linear acceleration that produces a positive response in each of the angular rate measurements.

Each accelerometer has two output data registers. Figure 32 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis accelerometer measurements. This format also applies to the y-axis and z-axis.

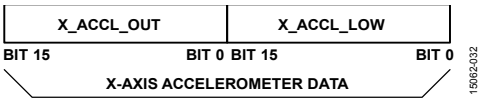

Figure 32. Accelerometer Output Data Structure

X-Axis Accelerometer (X_ACCL_LOW, X_ACCL_OUT)

The X_ACCL_LOW (see Table 39 and Table 40) and X_ACCL_OUT (see Table 41 and Table 42) registers contain the accelerometer data for the x-axis.

Table 39. X_ACCL_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1C, 0x1D	Not applicable	R	No

Table 40. X_ACCL_LOW Bit Descriptions

Bits	Description
[15:0]	X-axis accelerometer data; low word

Table 41. X_ACCL_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1E, 0x1F	Not applicable	R	No

Table 42. X_ACCL_OUT Descriptions

Bits	Description
[15:0]	X-axis accelerometer data, high word; twos complement, ±8 *g* range; 0 *g* = 0x0000, 1 LSB = 0.25 m*g*

Y-Axis Accelerometer (Y_ACCL_LOW, Y_ACCL_OUT)

The Y_ACCL_LOW (see Table 43 and Table 44) and Y_ACCL_OUT (see Table 45 and Table 46) registers contain the accelerometer data for the y-axis.

Table 43. Y_ACCL_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x20, 0x21	Not applicable	R	No

Table 44. Y_ACCL_LOW Bit Descriptions

Bits	Description
[15:0]	Y-axis accelerometer data; low word

Table 45. Y_ACCL_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x22, 0x23	Not applicable	R	No

Table 46. Y_ACCL_OUT Bit Descriptions

Bits	Description
[15:0]	Y-axis accelerometer data, high word; twos complement, ±8 *g* range, 0 *g* = 0x0000, 1 LSB = 0.25 m*g*

Z-Axis Accelerometer (Z_ACCL_LOW, Z_ACCL_OUT)

The Z_ACCL_LOW (see Table 47 and Table 48) and Z_ACCL_OUT (see Table 49 and Table 50) registers contain the accelerometer data for the z-axis.

Table 47. Z_ACCL_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x24, 0x25	Not applicable	R	No

Table 48. Z_ACCL_LOW Bit Descriptions

Bits	Description
[15:0]	Z-axis accelerometer data; low word

Table 49. Z_ACCL_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x26, 0x27	Not applicable	R	No

Table 50. Z_ACCL_OUT Bit Descriptions

Bits	Description
[15:0]	Z-axis accelerometer data, high word; twos complement, ±8 *g* range, 0 *g* = 0x0000, 1 LSB = 0.25 m*g*

Accelerometer Resolution

Table 51 and Table 52 offer various numerical examples that demonstrate the format of the linear acceleration data in both 16-bit and 32-bit formats.

Table 51. 16-Bit Accelerometer Data Format Examples

Acceleration	Decimal	Hex	Binary
+8 *g*	+32,000	0x7D00	0111 1101 0000 0000
+0.5 m*g*	+2	0x0002	0000 0000 0000 0010
+0.25 m*g*	+1	0x0001	0000 0000 0000 0001
0 m*g*	0	0x0000	0000 0000 0000 0000
−0.25 m*g*	−1	0xFFFF	1111 1111 1111 1111
−0.5 m*g*	−2	0xFFFE	1111 1111 1111 1110
−8 *g*	−32,000	0x8300	1000 0011 0000 0000

Table 52. 32-Bit Accelerometer Data Format Examples

Acceleration	Decimal	Hexadecimal
+8 *g*	+2,097,152,000	0x7D000000
+0.25/2^{15} m*g*	+2	0x00000002
+0.25/2^{16} m*g*	+1	0x00000001
0 m*g*	0	0x00000000
−0.25/2^{16} m*g*	−1	0xFFFFFFFF
−0.25/2^{15} m*g*	−2	0xFFFFFFFE
−8 *g*	−2,097,152,000	0x83000000

TIME STAMP

When using PPS mode (FNCTIO_CTRL, Bits[8:7] = 11 (binary), see Table 144), the TIME_STAMP register (see Table 53 and Table 54) provides the time between the most recent pulse on the input clock signal and the most recent data update.

Table 53. TIME_STAMP Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x28, 0x29	Not applicable	R	No

Table 54. TIME_STAMP Bit Descriptions

Bits	Description
[15:0]	Time stamp, binary format. 1 LSB = 1/f_{SM} (see Figure 14, Figure 15, and Table 154). The leading edge of the input clock pulse resets the value in this register to 0x0000.

When using the decimation filter (DEC_RATE > 0x0000), the value in the TIME_STAMP register represents the time of the first sample (taken at the rate of f_{SM}, per Figure 14 and Figure 15).

For example, when DEC_RATE = 0x0003, the decimation filter reduces the update by a factor of four and the TIME_STAMP register updates to 1 (decimal) during the first data update, then to 5 on the second update, 9 on the third update, for example, until the next clock signal pulse.

CYCLICAL REDUNDANDCY CHECK (CRC-32)

The ADIS16495 performs a CRC-32 computation, using the data registers that are shown in Table 55.

Table 55. CRC-32 Source Data and Example Values

Register	Example Value
SYS_E_FLAG	0x0000
TEMP_OUT	0x083A
X_GYRO_LOW	0x0000
X_GYRO_OUT	0xFFF7
Y_GYRO_LOW	0x0000
Y_GYRO_OUT	0xFFFE
Z_GYRO_LOW	0x0000
Z_GYRO_OUT	0x0001
X_ACCL_LOW	0x5001
X_ACCL_OUT	0x0003
Y_ACCL_LOW	0xE00A
Y_ACCL_OUT	0x0015
Z_ACCL_LOW	0xC009
Z_ACCL_OUT	0x0320
TIME_STAMP	0x8A54

The CRC_LWR (see Table 56 and Table 57) and CRC_UPR (see Table 58 and Table 59) registers contain the result of the CRC-32 computation. For the example, the register values from Table 55 are,

CRC_LWR = 0x15B4

CRC_UPR = 0xB6C8

Table 56. CRC_LWR Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x2A, 0x2B	Not applicable	R	No

Table 57. CRC_LWR Bit Definitions

Bits	Description
[15:0]	CRC-32 code from most recent BRF, lower word

Table 58. CRC_UPR Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x2C, 0x2D	Not applicable	R	No

Table 59. CRC_UPR Bit Definitions

Bits	Description
[15:0]	CRC-32 code from most recent BRF, upper word

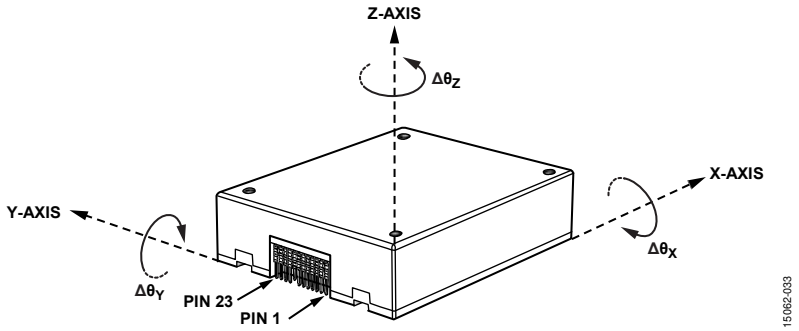

Figure 33. Delta Angle Axis and Polarity Assignments

DELTA ANGLES

In addition to the angular rate of rotation (gyroscope) measurements around each axis (x, y, and z), the ADIS16495 also provides delta angle measurements that represent a computation of angular displacement between each sample update. Figure 33 shows the orientation of each delta angle output, which defines the direction of rotation that produces a positive response in each of the angular displacement (delta angle) measurements.

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\Theta_{x,nD} = \frac{1}{2f_S} \times \sum_{d=0}^{D-1} \left(\omega_{x,nD+d} + \omega_{x,nD+d-1} \right)$$

where:
$\Delta\Theta_x$ is the delta angle measurement for the x-axis.
D is the decimation rate = DEC_RATE + 1 (see Table 150).
f_S is the sample rate.
d is the incremental variable in the summation formula.
ω_x is the x-axis rate of rotation (gyroscope).
n is the sample time, prior to the decimation filter.

When using the internal sample clock, f_S is equal to 4250 SPS. When using the external clock option, f_S is equal to the frequency of the external clock. The range in the delta angle registers accommodates the maximum rate of rotation (100°/sec), the nominal sample rate (4250 SPS), and an update rate of 1 Hz (DEC_RATE = 0x1099; divide by 4249 plus 1, see Table 150), all at the same time. When using an external clock that is higher than 4250 SPS, reduce the DEC_RATE setting to avoid overranging the delta angle registers.

Each axis of the delta angle measurements has two output data registers. Figure 34 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis delta angle measurements. This format also applies to the y-axis and z-axis.

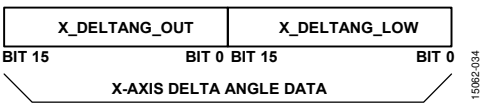

Figure 34. Delta Angle Output Data Structure

Delta Angle Measurement Range

Table 60 offers the measurement range and scale factor for each ADIS16470 model.

Table 60. Delta Angle Measurement Range and Scale Factor

Model	Measurement Range, $\pm\Delta\Theta_{MAX}$
ADIS16495-1AMLZ	±360°
ADIS16495-2AMLZ	±720°
ADIS16495-3AMLZ	±2160°

X-Axis Delta Angle (X_DELTANG_LOW, X_DELTANG_OUT)

The X_DELTANG_LOW (see Table 61 and Table 62) and X_DELTANG_OUT (see Table 63 and Table 64) registers contain the delta angle data for the x-axis.

Table 61. X_DELTANG_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x40, 0x41	Not applicable	R	No

Table 62. X_DELTANG_LOW Bit Descriptions

Bits	Description
[15:0]	X-axis delta angle data; low word

Table 63. X_DELTANG_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x42, 0x43	Not applicable	R	No

Table 64. X_DELTANG_OUT Bit Descriptions

Bits	Description
[15:0]	X-axis delta angle data; twos complement, 0° = 0x0000, 1 LSB = $\Delta\Theta_{MAX}/2^{15}$ (see Table 60 for $\Delta\Theta_{MAX}$)

Y-Axis Delta Angle (Y_DELTANG_LOW, Y_DELTANG_OUT)

The Y_DELTANG_LOW (see Table 65 and Table 66) and Y_DELTANG_OUT (see Table 67 and Table 68) registers contain the delta angle data for the y-axis.

Table 65. Y_DELTANG_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x44, 0x45	Not applicable	R	No

Table 66. Y_DELTANG_LOW Bit Descriptions

Bits	Description
[15:0]	Y-axis delta angle data; low word

Table 67. Y_DELTANG_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x46, 0x47	Not applicable	R	No

Table 68. Y_DELTANG_OUT Bit Descriptions

Bits	Description
[15:0]	Y-axis delta angle data; twos complement, 0° = 0x0000, 1 LSB = $\Delta\Theta_{MAX}/2^{15}$ (see Table 60 for $\Delta\Theta_{MAX}$)

Z-Axis Delta Angle (Z_DELTANG_LOW, Z_DELTANG_OUT)

The Z_DELTANG_LOW (see Table 69 and Table 70) and Z_DELTANG_OUT (see Table 71 and Table 72) registers contain the delta angle data for the z-axis.

Table 69. Z_DELTANG_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x48, 0x49	Not applicable	R	No

Table 70. Z_DELTANG_LOW Bit Descriptions

Bits	Description
[15:0]	Z-axis delta angle data; low word

Table 71. Z_DELTANG_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4A, 0x4B	Not applicable	R	No

Table 72. Z_DELTANG_OUT Bit Descriptions

Bits	Description
[15:0]	Z-axis delta angle data; twos complement, 0° = 0x0000, 1 LSB = $\Delta\Theta_{MAX}/2^{15}$ (see Table 60 for $\Delta\Theta_{MAX}$)

Delta Angle Resolution

Table 73 and Table 74 shows various numerical examples that demonstrate the format of the delta angle data in both 16-bit and 32-bit formats.

Table 73. 16-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex	Binary
$\Delta\Theta_{MAX} \times (2^{15}-1)/2^{15}$	+32,767	0x7FFF	0111 1111 1110 1111
$+\Delta\Theta_{MAX}/2^{14}$	+2	0x0002	0000 0000 0000 0010
$+\Delta\Theta_{MAX}/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-\Delta\Theta_{MAX}/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-\Delta\Theta_{MAX}/2^{14}$	−2	0xFFFE	1111 1111 1111 1110
$-\Delta\Theta_{MAX}$	−32,768	0x8000	1000 0000 0000 0000

Table 74. 32-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hex
$+\Delta\Theta_{MAX} \times (2^{31}-1)/2^{31}$	+2,147,483,647	0x7FFFFFFF
$+\Delta\Theta_{MAX}/2^{30}$	+2	0x00000002
$+\Delta\Theta_{MAX}2000/2^{31}$	+1	0x00000001
0	0	0x00000000
$-\Delta\Theta_{MAX}/2^{31}$	−1	0xFFFFFFFF
$-\Delta\Theta_{MAX}/2^{30}$	−2	0xFFFFFFFE
$-\Delta\Theta_{MAX}$	−2,147,483,648	0x80000000

DELTA VELOCITY

In addition to the linear acceleration measurements along each axis (x, y, and z), the ADIS16495 also provides delta velocity measurements that represent a computation of linear velocity change between each sample update. Figure 36 shows the orientation of each delta-velocity measurement, which defines the direction of linear velocity increase that produces a positive response in each of the delta velocity rate measurements.

The delta velocity outputs represent an integration of the acceleration measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta V_{x,nD} = \frac{1}{2f_S} \times \sum_{d=0}^{D-1} \left(a_{x,nD+d} + a_{x,nD+d-1} \right)$$

where:
ΔV_X is the delta velocity measurement for the x-axis.
D is the decimation rate = DEC_RATE + 1 (see Table 150).
f_S is the sample rate.
d is the incremental variable in the summation formula.
a_x is the x-axis rate of rotation (gyroscope).
n is the sample time, prior to the decimation filter.

When using the internal sample clock, f_S is equal to 4250 SPS. When using the external clock option, f_S is equal to the frequency of the external clock. The range in the delta velocity registers accommodates the maximum linear acceleration (8 *g*), the nominal sample rate (4250 SPS), and an update rate of 1 Hz (DEC_RATE = 0x1099; divide by 4249 plus 1, see Table 150), all at the same time. When using an external clock that is higher than 4250 SPS, reduce the DEC_RATE setting to avoid overranging the delta velocity registers.

Each axis of the delta velocity measurements has two output data registers. Figure 35 shows how these two registers combine to support 32-bit, twos complement data format for the delta velocity measurements along the x-axis. This format also applies to the y-axis and x-axis.

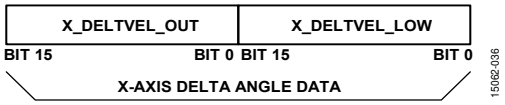

Figure 35. Delta Angle Output Data Structure

X-Axis Delta Velocity (X_DELTVEL_LOW, X_DELTVEL_OUT)

The X_DELTVEL_LOW (see Table 75 and Table 76) and X_DELTVEL_OUT (see Table 77 and Table 78) registers contain the delta velocity data for the x-axis.

Table 75. X_DELTVEL_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4C, 0x4D	Not applicable	R	No

Table 76. X_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	X-axis delta angle data; low word

Table 77. X_DELTVEL_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4E, 0x4F	Not applicable	R	No

Table 78. X_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	X-axis delta velocity data, high word; twos complement, ±100 m/sec range, 0 m/sec = 0x0000; 1 LSB = 100 m/sec ÷ 2^{15} = ~3.052 mm/sec

Y-Axis Delta Velocity (Y_DELTVEL_LOW, Y_DELTVEL_OUT)

The Y_DELTVEL_LOW (see Table 79 and Table 80) and Y_DELTVEL_OUT (see Table 81 and Table 82) registers contain the delta velocity data for the y-axis.

Table 79. Y_DELTVEL_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x50, 0x51	Not applicable	R	No

Table 80. Y_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	Y-axis delta angle data; low word

Table 81. Y_DELTVEL_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x52, 0x53	Not applicable	R	No

Table 82. Y_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	Y-axis delta velocity data, high word; twos complement, ±100 m/sec range, 0 m/sec = 0x0000; 1 LSB = 100 m/sec ÷ 2^{15} = ~3.052 mm/sec

Z-Axis Delta Velocity (Z_DELTVEL_LOW, Z_DELTVEL_OUT)

The Z_DELTVEL_LOW (see Table 83and Table 84) and Z_DELTVEL_OUT (see Table 85 and Table 86) registers contain the delta velocity data for the z-axis.

Table 83. Z_DELTVEL_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x54, 0x55	Not applicable	R	No

Table 84. Z_DELTVEL_LOW Bit Definitions

Bits	Description
[15:0]	Z-axis delta angle data; low word

Table 85. Z_DELTVEL_OUT Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x56, 0x57	Not applicable	R	No

Table 86. Z_DELTVEL_OUT Bit Definitions

Bits	Description
[15:0]	Z-axis delta velocity data, high word; twos complement, ±100 m/sec range, 0 m/sec = 0x0000; 1 LSB = 100 m/sec ÷ 2^{15} = ~3.052 mm/sec