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### FEATURES

- Dual independent, digitally controlled VGAs
- 11.5 dB to +20 dB gain range
- 0.5 dB  $\pm$ 0.1 dB step size
- 150  $\Omega$  differential input and output
- 7.5 dB noise figure at maximum gain
- OIP3 > 47.5 dBm at 200 MHz
- 3 dB upper frequency bandwidth of 700 MHz
- Multiple control interface options
- Parallel 6-bit control interface (with latch)
- Serial peripheral interface (SPI) (with fast attack)
- Gain up/down mode
- Wide input dynamic range
- Low power mode option
- Power-down control
- Single 5 V supply operation
- 40-lead, 6 mm  $\times$  6 mm LFCSP package

### APPLICATIONS

- Differential ADC drivers
- High IF sampling receivers
- High output power IF amplification
- Instrumentation

### GENERAL DESCRIPTION

The **ADL5202** is a digitally controlled, variable gain, wide bandwidth amplifier that provides precise gain control, high output IP3, and low noise figure. The excellent distortion performance and high signal bandwidth make the **ADL5202** an excellent gain control device for a variety of receiver applications. The **ADL5202** also incorporates a low power mode option that lowers the supply current.

For wide input dynamic range applications, the **ADL5202** provides a broad 31.5 dB gain range with 0.5 dB resolution. The gain is adjustable through multiple gain control interface options: parallel, serial peripheral interface, and up/down.

Incorporating proprietary distortion cancellation techniques, the **ADL5202** achieves a better than 47.5 dBm output IP3 at frequencies approaching 200 MHz for most gain settings.

### FUNCTIONAL BLOCK DIAGRAM

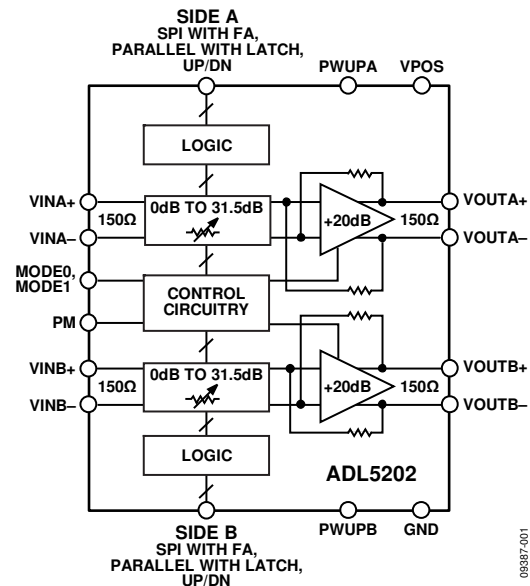


Figure 1.

The **ADL5202** is powered on by applying the appropriate logic level to the PWUPx pins. The quiescent current of the **ADL5202** is typically 160 mA in low power mode. When configured in high performance mode for more demanding applications, the quiescent current is 210 mA. When powered down, the **ADL5202** consumes less than 14 mA and offers excellent input-to-output isolation. The gain setting is preserved during power-down.

Fabricated on an Analog Devices, Inc., high speed SiGe process, the **ADL5202** provides precise gain adjustment capabilities with good distortion performance and low phase error. The **ADL5202** amplifier comes in a compact, thermally enhanced 40-lead, 6 mm  $\times$  6 mm LFCSP package and operates over a temperature range of -40°C to +85°C.

# ADL5202\* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- ADL5202 Evaluation Board

## DOCUMENTATION

### Data Sheet

- ADL5202: Wide Dynamic Range, High Speed, Digitally Controlled VGA Data Sheet

## SOFTWARE AND SYSTEMS REQUIREMENTS

- ADL5201 and ADL5202 Evaluation Board Software

## TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF
- ADL5202 S-Parameters

## REFERENCE DESIGNS

- CN0242

## REFERENCE MATERIALS

### Press

- Analog Devices Introduces High-Performance RF ICs for Multi-band Base Stations and Microwave Point-to-Point Radios

### Product Selection Guide

- RF Source Booklet

## DESIGN RESOURCES

- ADL5202 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all ADL5202 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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## REVISION HISTORY

### 1/2017—Rev. C to Rev. D

|  |   |
|--|---|
| Change to Features Section and General Description Section ..... | 1 |
| Changes to Noise/Harmonic Performance Parameter, Table 1 .....   | 4 |

### 1/2015—Rev. B to Rev. C

|                         |   |
|-------------------------|---|
| Changes to Table 1..... | 4 |
| Change to Table 3 ..... | 6 |

### 9/2013—Rev. A to Rev. B

|  |   |
|--|---|
| Changed Logic Pins Absolute Maximum Rating from 3.6 V to<br>–0.3 V to +3.6 V (not to exceed  VPOS – 0.5 V  at any time) .... | 5 |
|--|---|

### 12/2012—Rev. 0 to Rev. A

|  |    |
|--|----|
| Changes to Layout Consideration Section..... | 21 |
|--|----|

### 10/2011—Revision 0: Initial Version

## SPECIFICATIONS

$V_S = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_S = R_L = 150\ \Omega$  at 100 MHz, high performance mode, 2 V p-p differential output, unless otherwise noted.

Table 1.

| Parameter                          | Test Conditions/Comments  | Min | Typ        | Max | Unit     |
|------------------------------------|---|-----|------------|-----|----------|
| <b>DYNAMIC PERFORMANCE</b>         |   |     |            |     |          |
| –3 dB Bandwidth                    | $V_{OUT} < 2\text{ V p-p}$ (5.2 dBm)                                    |     | 700        |     | MHz      |
| Slew Rate                          |   |     | 5.5        |     | V/ns     |
| Input Return Loss (S11)            | 100 MHz   |     | –17.7      |     | dB       |
| Output Return Loss (S22)           | 100 MHz   |     | –16.5      |     | dB       |
| <b>INPUT STAGE</b>                 |   |     |            |     |          |
| Maximum Input Swing (Differential) | VINA+, VINB+ and VINA–, VINB– pins<br>Gain code = 111111                |     | 10.8       |     | V p-p    |
| Differential Input Resistance      |   |     | 150        |     | $\Omega$ |
| Common-Mode Input Voltage          |   |     | 1.5        |     | V        |
| CMRR                               | Gain code = 000000  |     | 40         |     | dB       |
| <b>GAIN</b>                        |   |     |            |     |          |
| Maximum Voltage Gain               | Gain code = 000000  |     | 20         |     | dB       |
| Minimum Voltage Gain               | Gain code = 111111  |     | –11.5      |     | dB       |
| Gain Step Size                     |   |     | 0.5        |     | dB       |
| Gain Flatness                      | $30\text{ MHz} < f_c < 200\text{ MHz}$                                  |     | 0.285      |     | dB       |
| Gain Temperature Sensitivity       | Gain code = 000000  |     | 0.012      |     | dB/°C    |
| Gain Step Response                 | For $V_{IN} = 0.2\text{ V}$ , gain code = 111111 to 000000              |     | 15         |     | ns       |
| Gain Conformance Error             | Over 10 dB gain range   |     | $\pm 0.03$ |     | dB       |
| Phase Conformance Error            | Over 10 dB gain range   |     | 1.0        |     | Degrees  |
| <b>OUTPUT STAGE</b>                |   |     |            |     |          |
| Output Voltage Swing               | VOUTx+ and VOUTx– pins<br>At P1dB, gain code = 000000                   |     | 10         |     | V p-p    |
| Differential Output Resistance     | Differential  |     | 150        |     | $\Omega$ |
| <b>NOISE/HARMONIC PERFORMANCE</b>  |   |     |            |     |          |
| 46 MHz                             |   |     |            |     |          |
| Second Harmonic                    | Gain code = 000000, high performance mode<br>$V_{OUT} = 2\text{ V p-p}$ |     | –92        |     | dBc      |
| Third Harmonic                     | $V_{OUT} = 2\text{ V p-p}$  |     | –105       |     | dBc      |
| Output IP3                         | $V_{OUT} = 2\text{ V p-p}$ composite                                    |     | 47.5       |     | dBm      |
| 70 MHz                             |   |     |            |     |          |
| Second Harmonic                    | Gain code = 000000, high performance mode<br>$V_{OUT} = 2\text{ V p-p}$ |     | –96        |     | dBc      |
| Third Harmonic                     | $V_{OUT} = 2\text{ V p-p}$  |     | –105       |     | dBc      |
| Output IP3                         | $V_{OUT} = 2\text{ V p-p}$ composite                                    |     | 47.5       |     | dBm      |
| 140 MHz                            |   |     |            |     |          |
| Noise Figure                       | Gain code = 000000, high performance mode                               |     | 7.5        |     | dB       |
| Second Harmonic                    | $V_{OUT} = 2\text{ V p-p}$  |     | –86        |     | dBc      |
| Third Harmonic                     | $V_{OUT} = 2\text{ V p-p}$  |     | –105       |     | dBc      |
| Output IP3                         | $V_{OUT} = 2\text{ V p-p}$ composite                                    |     | 47.5       |     | dBm      |
| Output 1 dB Compression Point      |   |     | 19.5       |     | dBm      |
| 300 MHz                            |   |     |            |     |          |
| Second Harmonic                    | Gain code = 000000, high performance mode<br>$V_{OUT} = 2\text{ V p-p}$ |     | –77        |     | dBc      |
| Third Harmonic                     | $V_{OUT} = 2\text{ V p-p}$  |     | –91        |     | dBc      |
| Output IP3                         | $V_{OUT} = 2\text{ V p-p}$ composite                                    |     | 45         |     | dBm      |

| Parameter                         | Test Conditions/Comments                 | Min              | Typ | Max | Unit    |
|-----------------------------------|--|------------------|-----|-----|---------|
| POWER-UP INTERFACE                | PWUPA, PWUPB pins                        |                  |     |     |         |
| Power-Up Threshold                | Minimum voltage to enable the device     | 1.4              |     |     | V       |
| PWUPx Input Bias Current          | Maximum voltage to enable the device     |                  | 1   | 3.3 | $\mu$ A |
| GAIN CONTROL INTERFACE            |  |                  |     |     |         |
| V <sub>IH</sub>                   | Minimum/Maximum voltage for a logic high | 1.4 <sup>1</sup> |     | 3.3 | V       |
| V <sub>IL</sub>                   | Maximum voltage for a logic low          |                  |     | 0.8 | V       |
| Maximum Input Bias Current        |  |                  | 1   |     | $\mu$ A |
| SPI TIMING                        | LATCHA and LATCHB, SCLK, SDIO, data pins |                  |     |     |         |
| f <sub>SCLK</sub>                 | 1/t <sub>SCLK</sub>                      |                  | 20  |     | MHz     |
| t <sub>DH</sub>                   | Data hold time                           |                  | 5   |     | ns      |
| t <sub>DS</sub>                   | Data setup time                          |                  | 5   |     | ns      |
| t <sub>PW</sub>                   | SCLK high pulse width                    |                  | 5   |     | ns      |
| POWER INTERFACE                   |  |                  |     |     |         |
| Supply Voltage                    |  | 4.5              |     | 5.5 | V       |
| Quiescent Current, Both Channels  | High performance mode                    |                  | 210 |     | mA      |
|                                   | T <sub>A</sub> = 85°C                    |                  |     | 250 | mA      |
|                                   | Low power mode                           |                  | 160 |     | mA      |
|                                   | T <sub>A</sub> = 85°C                    |                  |     | 180 | mA      |
| Power-Down Current, Both Channels | PWUPx low                                |                  | 14  |     | mA      |

<sup>1</sup> The minimum value for a logic high on the PM pin is 2.8 V.

Timing Diagrams

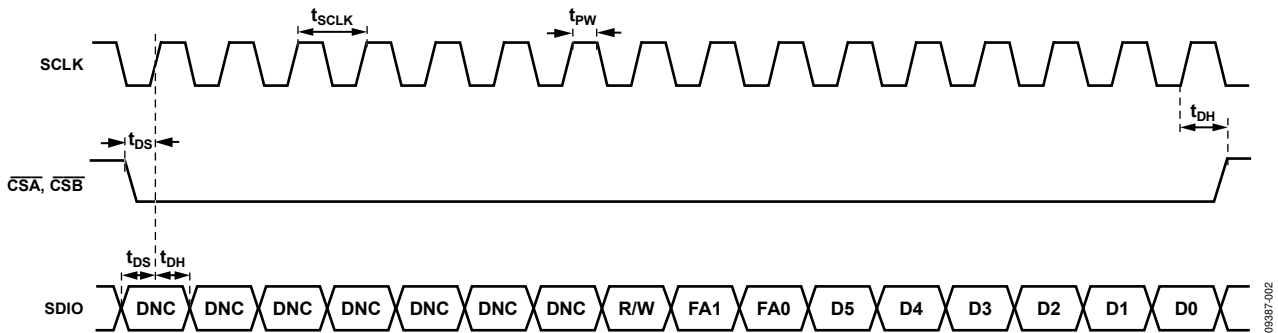


Figure 2. SPI Interface Read/Write Mode Timing Diagram

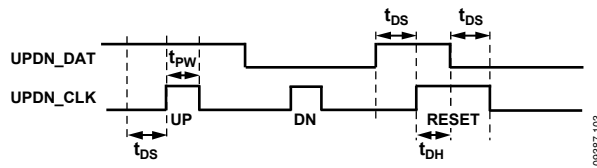


Figure 3. Up/Down Mode Timing Diagram

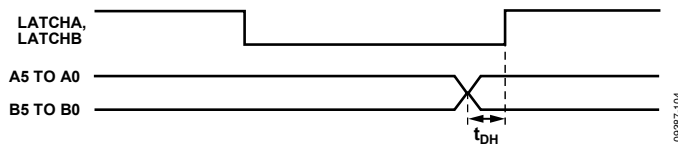


Figure 4. Parallel Mode Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter   | Rating  |
|---|---|
| Supply Voltage, $V_{POS}$   | 5.5   |
| PWUPA, PWUPB, A0 to A5, B0 to B5,<br>MODE0, MODE1, PM, LATCHA, LATCHB | -0.3 V to +3.6 V<br>(not to exceed $ V_{POS} - 0.5 V $ at any time) |
| Input Voltage, $V_{IN+}$ , $V_{IN-}$                                  | +3.6 V to -1.2 V  |
| Internal Power Dissipation  | 1.6 W   |
| $\theta_{JA}$ (Exposed Paddle Soldered Down)                          | 34.6°C/W  |
| $\theta_{JC}$ (At Exposed Paddle)                                     | 3.6°C/W   |
| Maximum Junction Temperature  | 140°C   |
| Operating Temperature Range   | -40°C to +85°C  |
| Storage Temperature Range   | -65°C to +150°C   |
| Lead Temperature (Soldering, 60 sec)                                  | 240°C   |

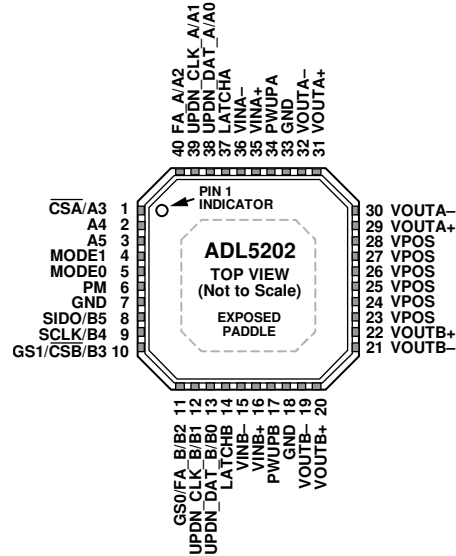
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES
1. THE EXPOSED PADDLE (EP) MUST BE CONNECTED TO A LOW IMPEDANCE GROUND PAD.

09387-003

Figure 5. Pin Configuration

Table 3. Pin Function Descriptions

| Pin No.       | Mnemonic                         | Description  |
|---------------|----------------------------------|--|
| 1             | CSA/A3                           | Channel A Select ( $\overline{\text{CSA}}$ ). When serial mode is enabled, a logic low ( $0\text{ V} \leq \overline{\text{CSA}} \leq 0.8\text{ V}$ ) selects Channel A. Bit 3 for Channel A Parallel Gain Control Interface (A3).  |
| 2             | A4                               | Bit 4 for Channel A Parallel Gain Control Interface.   |
| 3             | A5                               | Bit 5 (MSB) for Channel A Parallel Gain Control Interface.   |
| 4             | MODE1                            | MSB for Mode Control. With the MODE0 pin, selects parallel, SPI, or up/down interface mode.  |
| 5             | MODE0                            | LSB for Mode Control. With the MODE1 pin, selects parallel, SPI, or up/down interface mode.  |
| 6             | PM                               | Performance Mode. A logic low ( $0\text{ V} \leq \text{PM} \leq 0.8\text{ V}$ ) enables high performance mode. A logic high ( $2.8\text{ V} \leq \text{PM} \leq 3.3\text{ V}$ ) enables low power mode.  |
| 7, 18, 33, EP | GND                              | Ground. The exposed paddle (EP) must be connected to a low impedance ground pad.   |
| 8             | SDIO/B5                          | Serial Data Input/Output (SDIO). When $\overline{\text{CSA}}$ or $\overline{\text{CSB}}$ is pulled low, SDIO is used for reading and writing to the SPI port. Bit 5 for Channel B Parallel Gain Control Interface (B5).  |
| 9             | SCLK/B4                          | Serial Clock Input in SPI Mode (SCLK). Bit 4 for Channel B Parallel Gain Control Interface (B4).   |
| 10            | GS1/ $\overline{\text{CSB}}$ /B3 | MSB for Gain Step Size Control in Up/Down Mode (GS1). Channel B Select ( $\overline{\text{CSB}}$ ). When serial mode is enabled, a logic low ( $0\text{ V} \leq \overline{\text{CSB}} \leq 0.8\text{ V}$ ) selects Channel B. Bit 3 for Channel B Parallel Gain Control Interface (B3).  |
| 11            | GS0/FA_B/B2                      | LSB for Gain Step Size Control in Up/Down Mode (GS0). Fast Attack (FA_B). In serial mode, a logic high ( $1.4\text{ V} \leq \text{FA}_B \leq 3.3\text{ V}$ ) attenuates Channel B according to the FA setting in the SPI word. Bit 2 for Channel B Parallel Gain Control Interface (B2). |
| 12            | UPDN_CLK_B/B1                    | Clock Interface for Channel B Up/Down Function (UPDN_CLK_B). Bit 1 for Channel B Parallel Gain Control Interface (B1).   |
| 13            | UPDN_DAT_B/B0                    | Data Pin for Channel B Up/Down Function (UPDN_DAT_B). Bit 0 for Channel B Parallel Gain Control Interface (B0).  |
| 14            | LATCHB                           | Channel B Latch. A logic low ( $0\text{ V} \leq \text{LATCHB} \leq 0.8\text{ V}$ ) allows gain changes on Channel B. A logic high ( $1.4\text{ V} \leq \text{LATCHB} \leq 3.3\text{ V}$ ) prevents gain changes on Channel B.  |



| Pin No.                   | Mnemonic      | Description   |
|---------------------------|---------------|---|
| 15                        | VINB-         | Channel B Negative Input.   |
| 16                        | VINB+         | Channel B Positive Input.   |
| 17                        | PWUPB         | Channel B Power-Up. A logic high ( $1.4\text{ V} \leq \text{PWUPB} \leq 3.3\text{ V}$ ) enables Channel B.  |
| 19, 21                    | VOUTB-        | Channel B Negative Output.  |
| 20, 22                    | VOUTB+        | Channel B Positive Output.  |
| 23, 24, 25,<br>26, 27, 28 | VPOS          | Positive Power Supply.  |
| 29, 31                    | VOUTA+        | Channel A Positive Output.  |
| 30, 32                    | VOUTA-        | Channel A Negative Output.  |
| 34                        | PWUPA         | Channel A Power-Up. A logic high ( $1.4\text{ V} \leq \text{PWUPA} \leq 3.3\text{ V}$ ) enables Channel A.  |
| 35                        | VINA+         | Channel A Positive Input.   |
| 36                        | VINA-         | Channel A Negative Input.   |
| 37                        | LATCHA        | Channel A Latch. A logic low ( $0\text{ V} \leq \text{LATCHA} \leq 0.8\text{ V}$ ) allows gain changes on Channel A. A logic high ( $1.4\text{ V} \leq \text{LATCHA} \leq 3.3\text{ V}$ ) prevents gain changes on Channel A.     |
| 38                        | UPDN_DAT_A/A0 | Data Pin for Channel A Up/Down Function (UPDN_DAT_A).<br>Bit 0 for Channel A Parallel Gain Control Interface (A0).  |
| 39                        | UPDN_CLK_A/A1 | Clock Interface for Channel A Up/Down Function (UPDN_CLK_A).<br>Bit 1 for Channel A Parallel Gain Control Interface (A1).   |
| 40                        | FA_A/A2       | Fast Attack (FA_A). In serial mode, a logic high ( $1.4\text{ V} \leq \text{FA}_A \leq 3.3\text{ V}$ ) attenuates Channel A according to FA setting in the SPI word.<br>Bit 2 for Channel A Parallel Gain Control Interface (A2). |

### TYPICAL PERFORMANCE CHARACTERISTICS

$V_s = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ ,  $R_s = R_L = 150\ \Omega$  at 200 MHz, high performance mode, 2 V p-p differential output, unless otherwise noted.

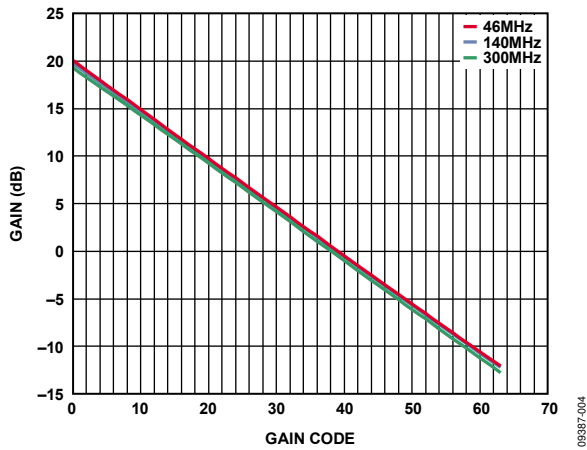


Figure 6. Gain vs. Gain Code at 46 MHz, 140 MHz, and 300 MHz

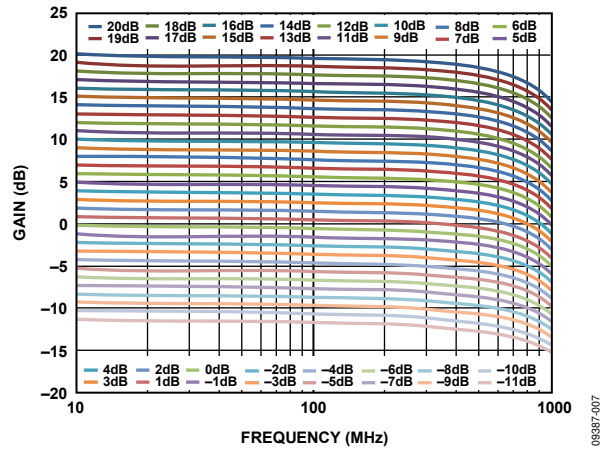


Figure 9. Gain vs. Frequency Response (Every 1 dB Step)

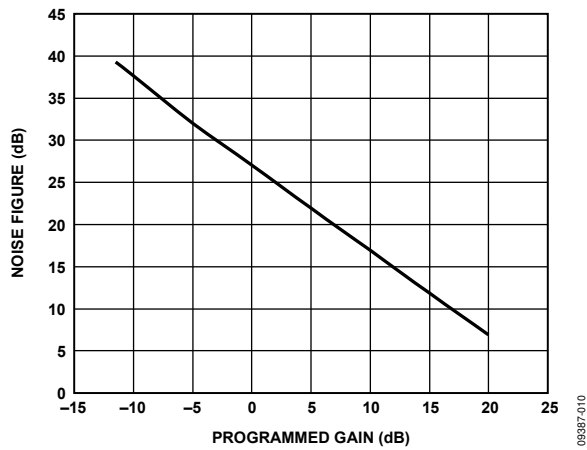


Figure 7. Noise Figure vs. Programmed Gain at 140 MHz

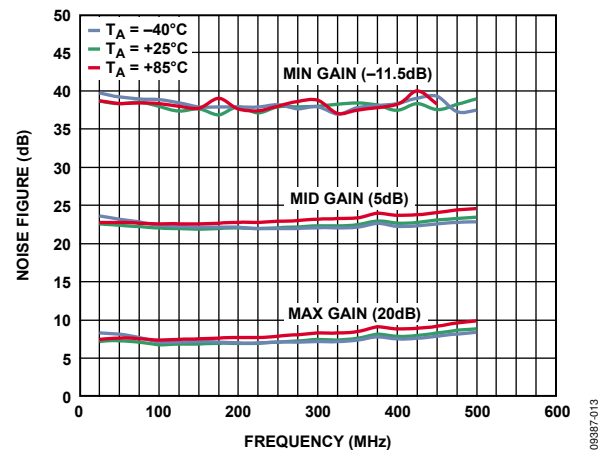


Figure 10. Noise Figure vs. Frequency at Max, Mid, and Min Gain Outputs

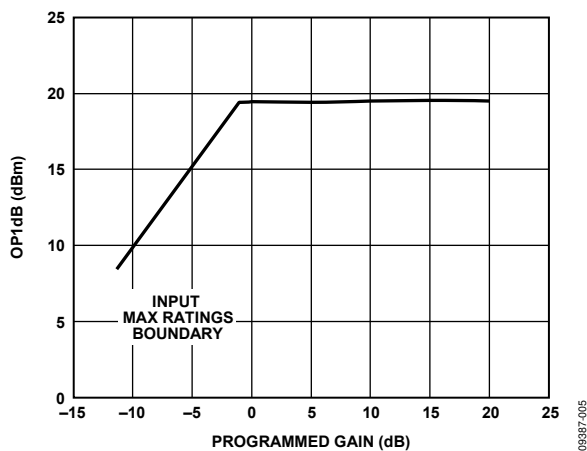


Figure 8. OP1dB vs. Programmed Gain at 140 MHz

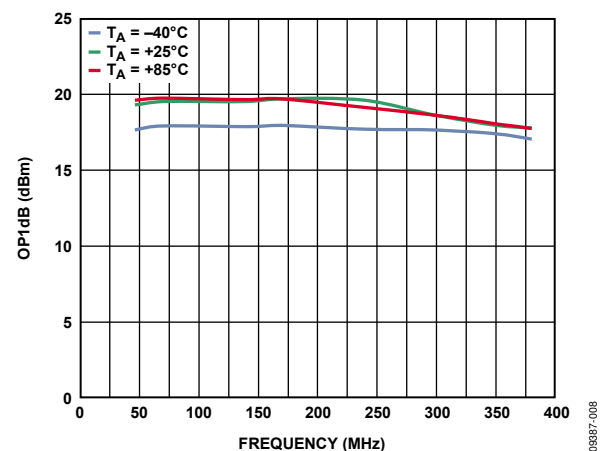


Figure 11. OP1dB vs. Frequency at Maximum Gain, Three Temperatures

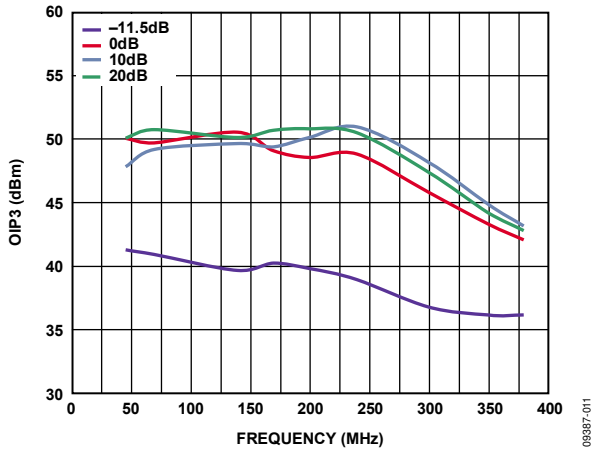


Figure 12. Output Third-Order Intercept vs. Frequency at Four Gain Codes

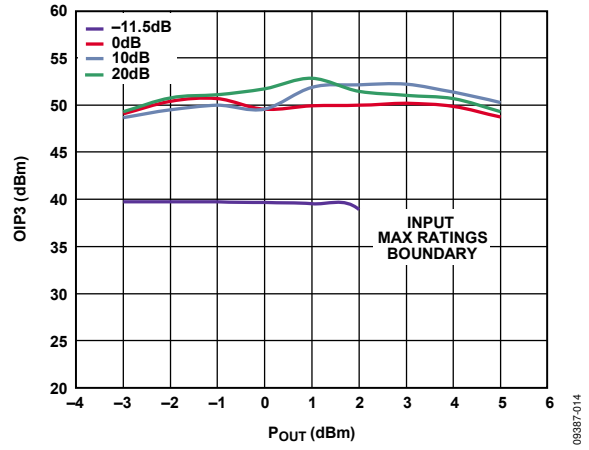


Figure 15. Output Third-Order Intercept vs. Power at Four Gain Codes, Frequency = 140 MHz at 2 Vp-p Composite

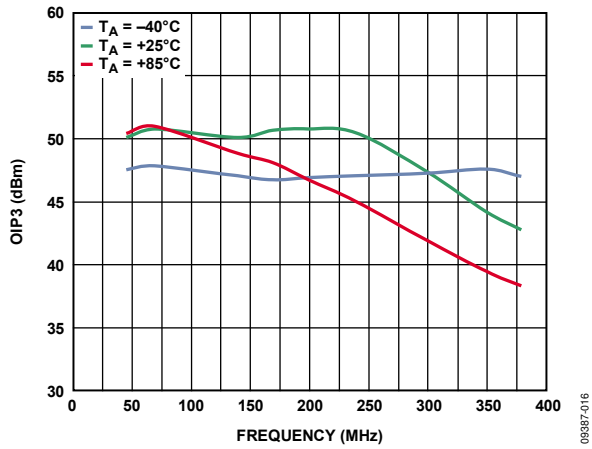


Figure 13. Output Third-Order Intercept vs. Frequency, Three Temperatures at 2 Vp-p Composite

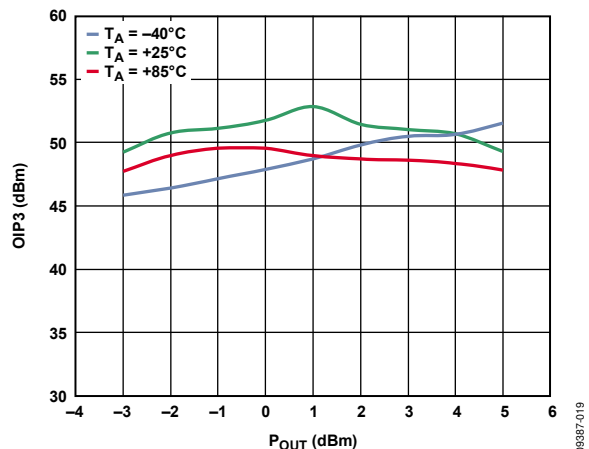


Figure 16. Output Third-Order Intercept vs. Power, Frequency = 140 MHz, Three Temperatures

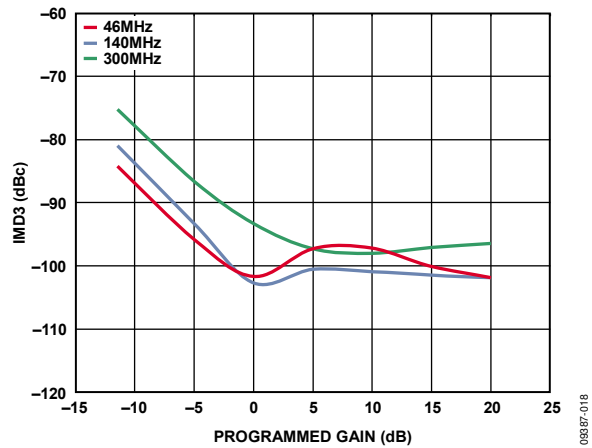


Figure 14. Two-Tone Output IMD3 vs. Programmed Gain, at 46 MHz, 140 MHz, 300 MHz

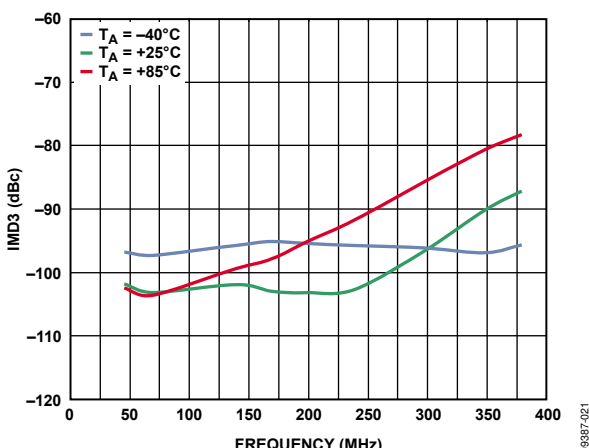


Figure 17. Two-Tone Output IMD3 vs. Frequency, Three Temperatures

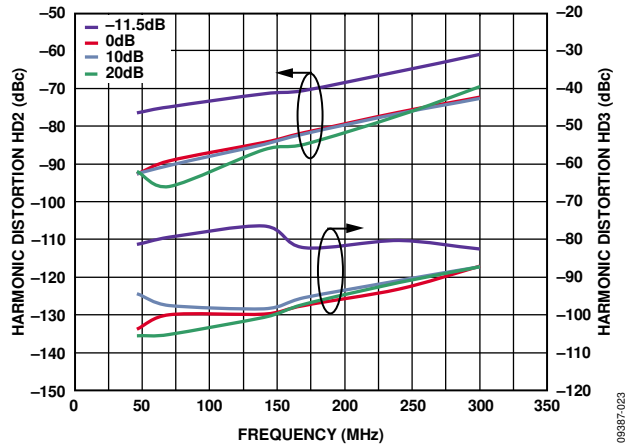


Figure 18. Harmonic Distortion vs. Frequency at Four Gain Codes

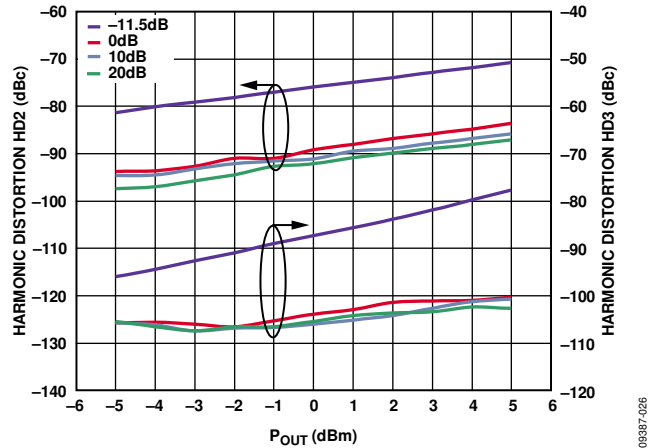


Figure 21. Harmonic Distortion vs. Power at Four Gains, Frequency = 140 MHz

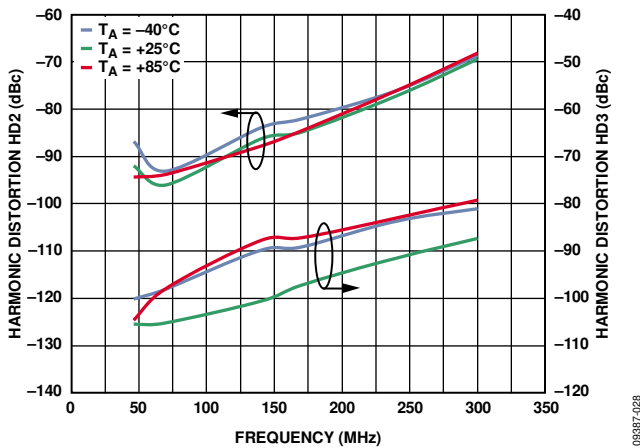


Figure 19. Harmonic Distortion vs. Frequency, Three Temperatures

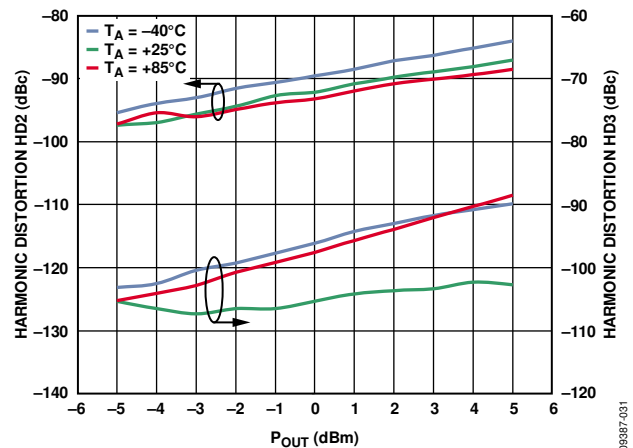


Figure 22. Harmonic Distortion vs. Power, Frequency = 140 MHz, Three Temperatures

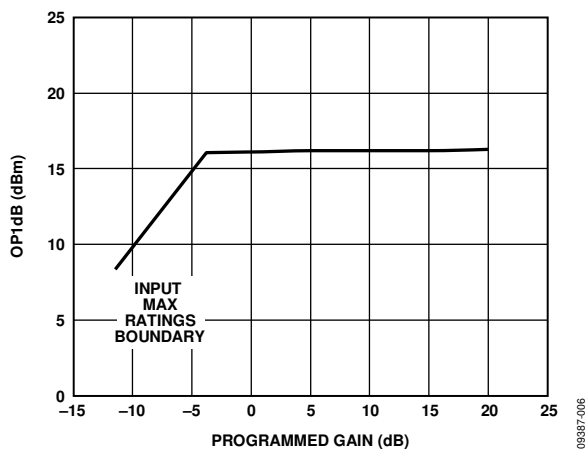


Figure 20. OP1dB vs. Programmed Gain at 140 MHz, Low Power Mode

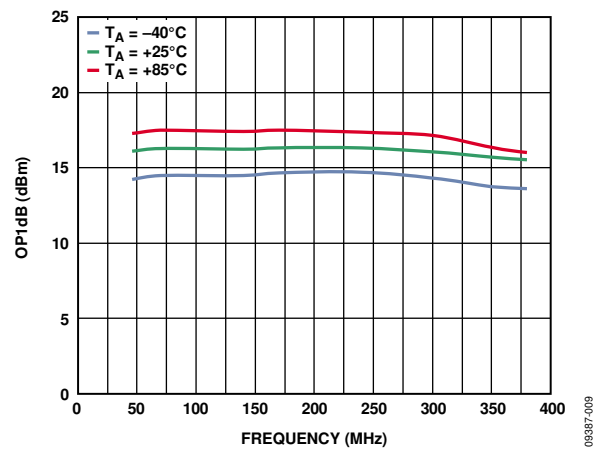


Figure 23. OP1dB vs. Frequency at Maximum Gain, Three Temperatures, Low Power Mode

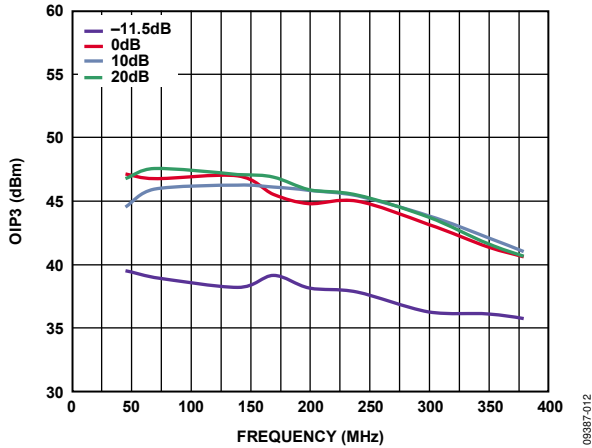


Figure 24. Output Third-Order Intercept vs. Frequency at Four Gain Codes, Low Power Mode at 2 V p-p Composite

09387-012

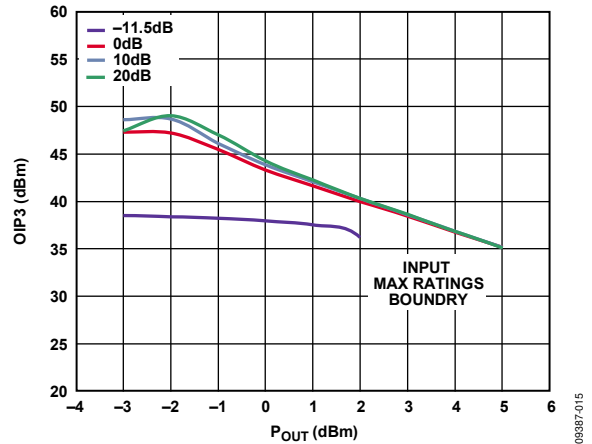


Figure 27. Output Third-Order Intercept vs. Power at Four Gain Codes, Frequency = 140 MHz, Low Power Mode

09387-015

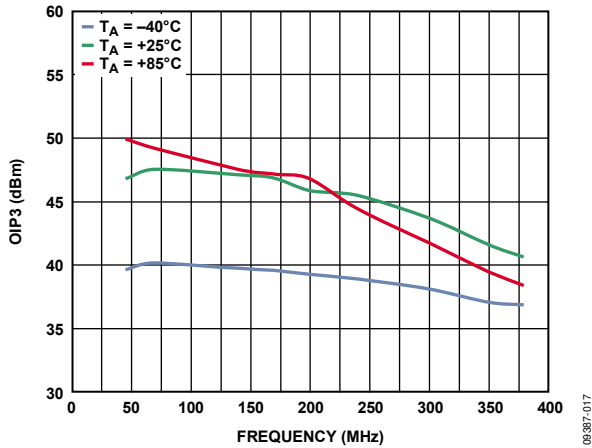


Figure 25. Output Third-Order Intercept vs. Frequency, Three Temperatures, Low Power Mode

09387-017

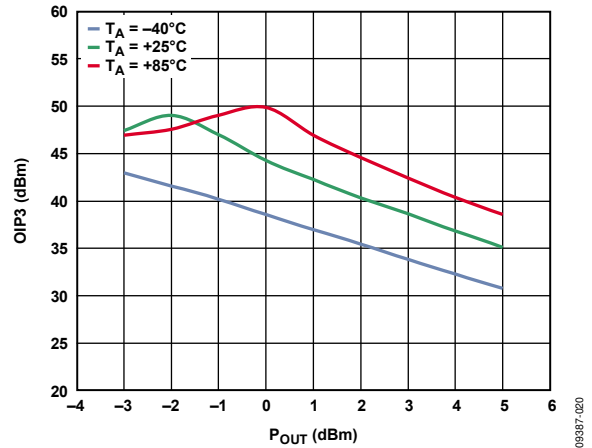


Figure 28. Output Third-Order Intercept vs. Power, Three Temperatures, Low Power Mode at 2 V p-p Composite

09387-020

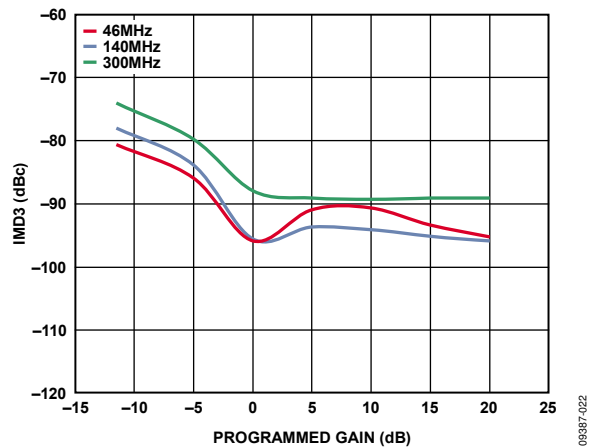


Figure 26. Two-Tone Output IMD3 vs. Programmed Gain at 46 MHz, 140 MHz, 300 MHz; Low Power Mode

09387-022

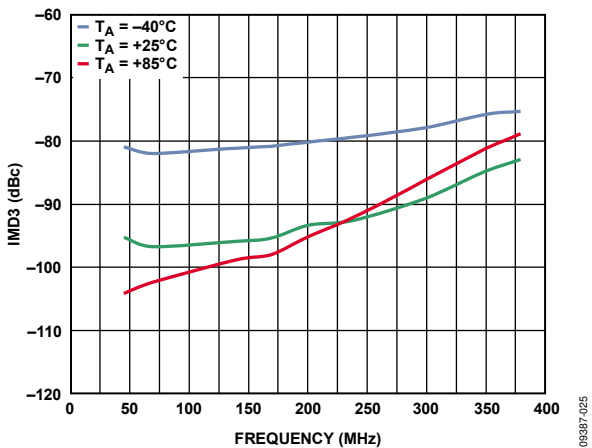


Figure 29. Two-Tone Output IMD3 vs. Frequency, Three Temperatures, Low Power Mode

09387-025

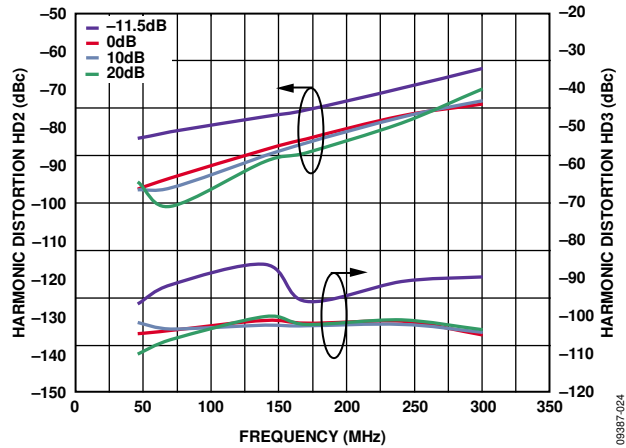


Figure 30. Harmonic Distortion vs. Frequency at Four Gain Codes, Low Power Mode

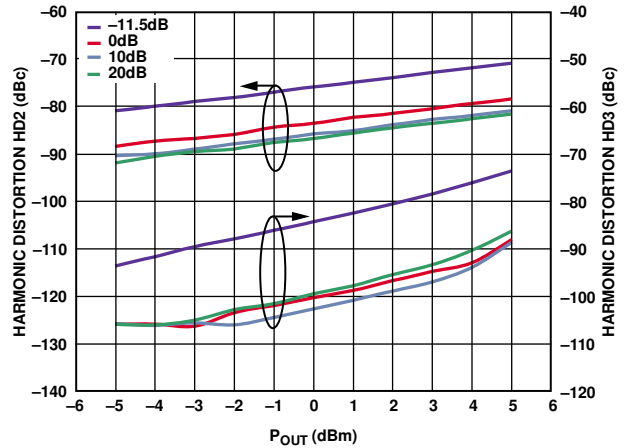


Figure 33. Harmonic Distortion vs. Power at Four Gain Codes, Frequency = 140 MHz, Low Power Mode

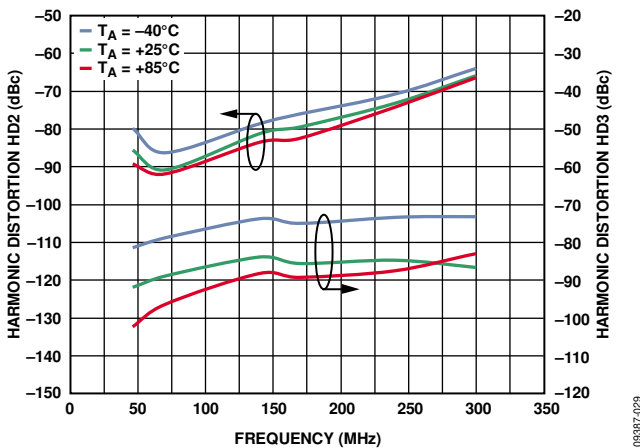


Figure 31. Harmonic Distortion vs. Frequency, Three Temperatures, Low Power Mode

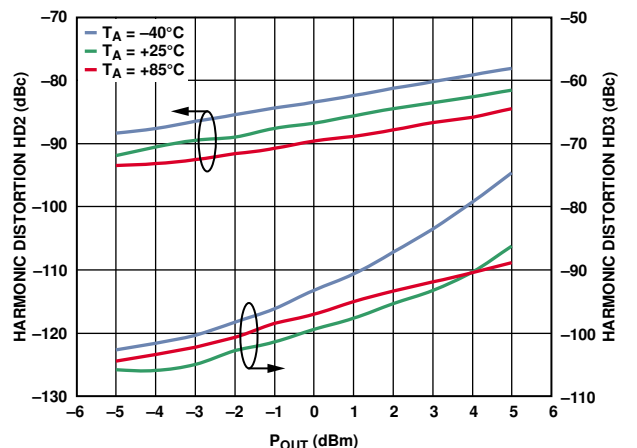


Figure 34. Harmonic Distortion vs. Power, Frequency = 140 MHz, Three Temperatures, Low Power Mode

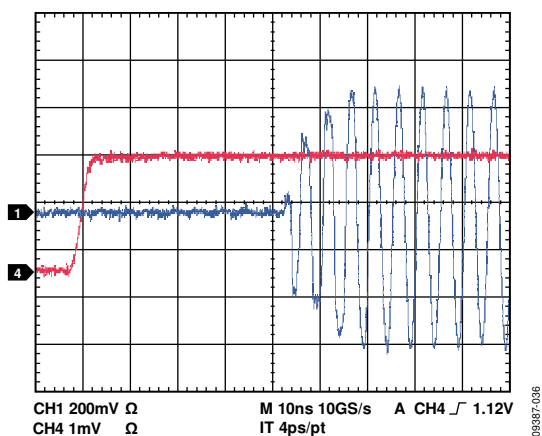


Figure 32. Enable Time Domain Response

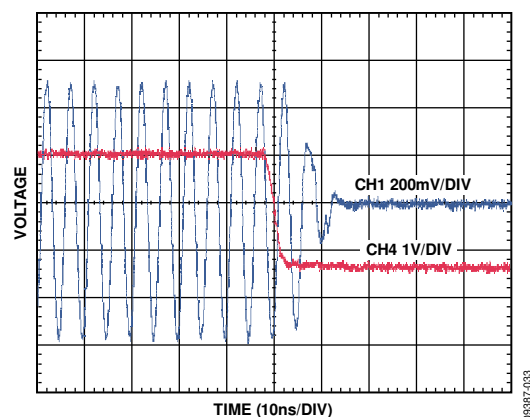


Figure 35. Disable Time Domain Response

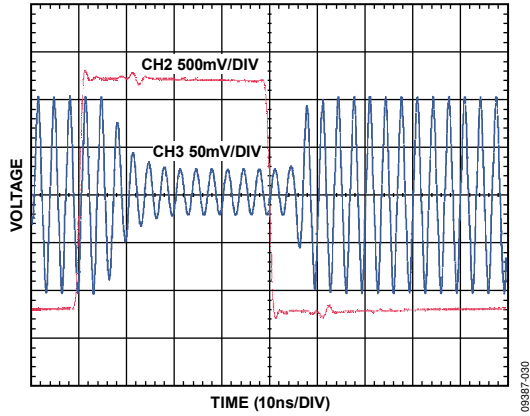


Figure 36. Gain Step Time Domain Response

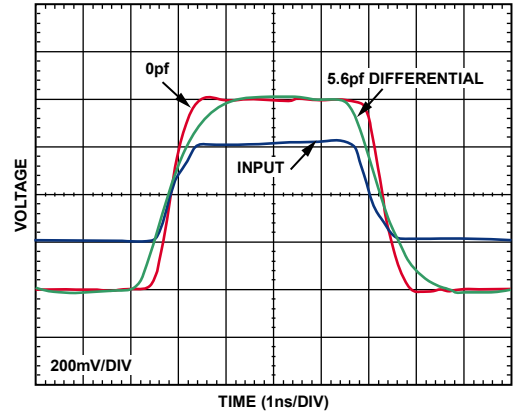


Figure 39. Large Signal Pulse Response, 0 pF and 5.6 pF, 2 V p-p Composite

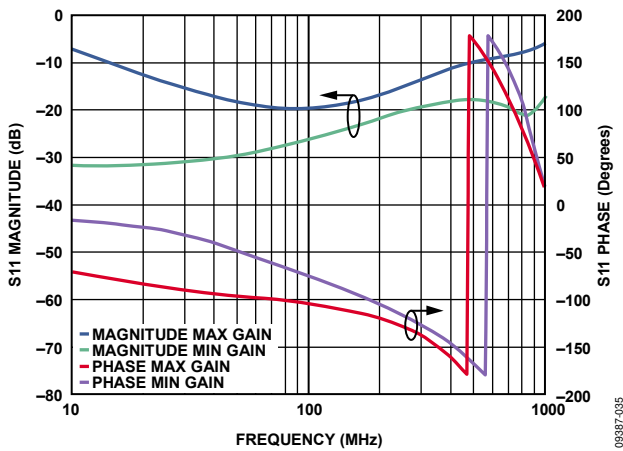


Figure 37. S11 Magnitude and Phase vs. Frequency

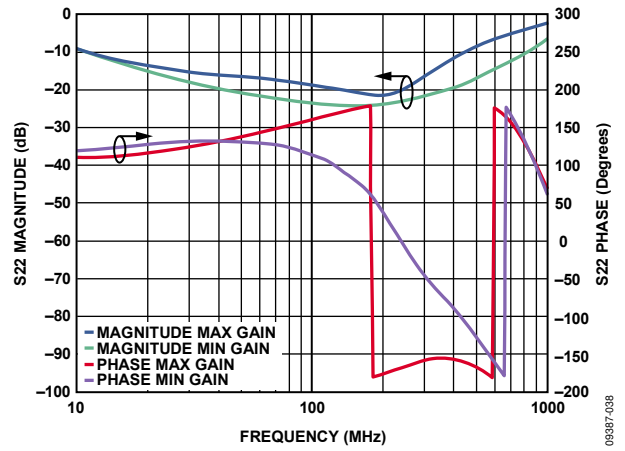


Figure 40. S22 Magnitude and Phase vs. Frequency

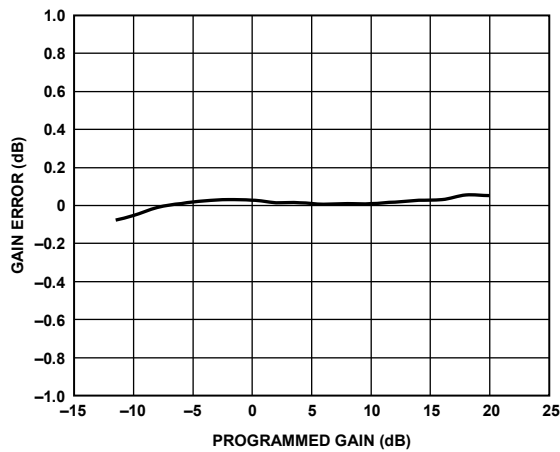


Figure 38. Gain Step Error, Frequency = 140 MHz

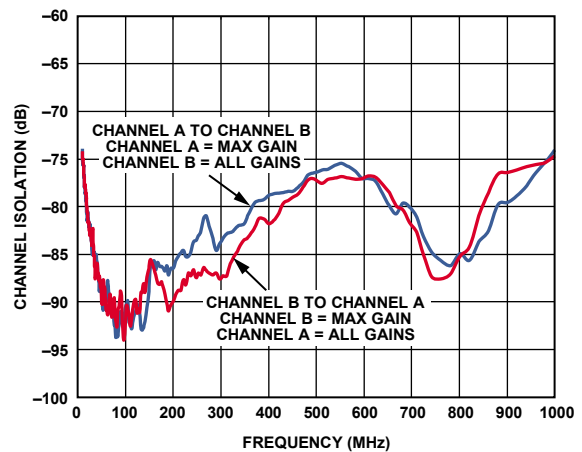


Figure 41. Channel Isolation vs. Frequency

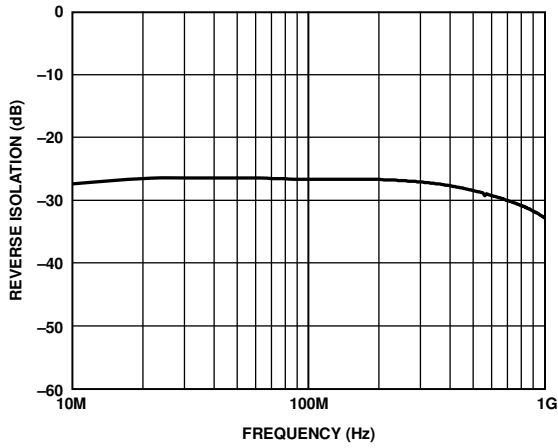


Figure 42. Reverse Isolation vs. Frequency

09387-039

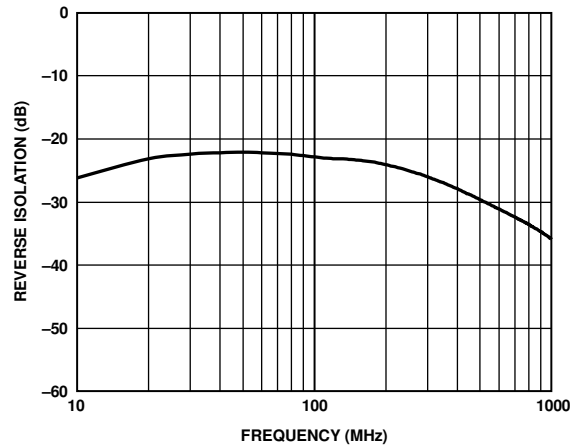


Figure 45. Disable-State Reverse Isolation vs. Frequency

09387-042

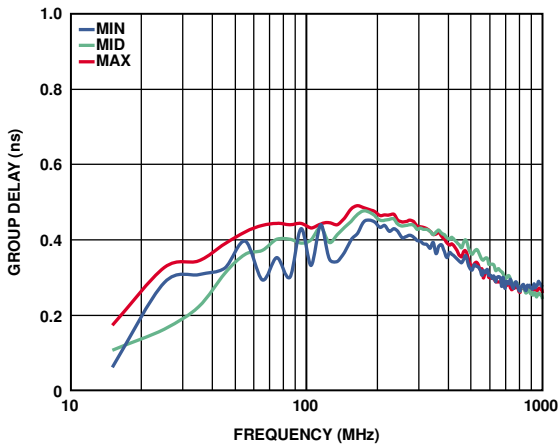


Figure 43. Group Delay vs. Frequency at Max, Mid, and Min Gain Outputs

09387-040

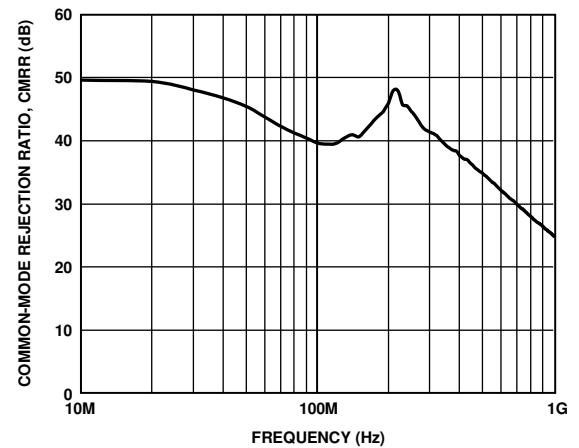


Figure 46. Common-Mode Rejection Ratio vs. Frequency

09387-044

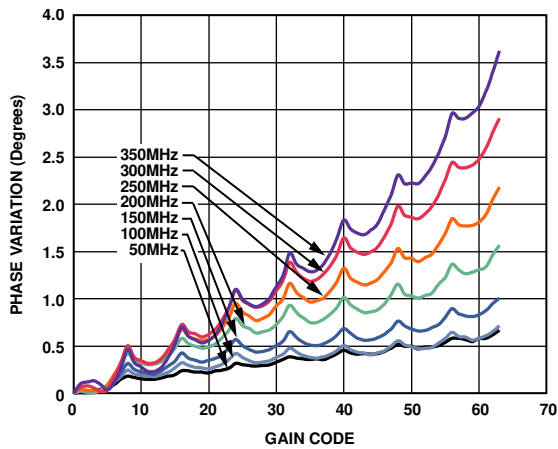


Figure 44. Phase Variation vs. Gain Code

09387-041



# CHARACTERIZATION AND TEST CIRCUITS

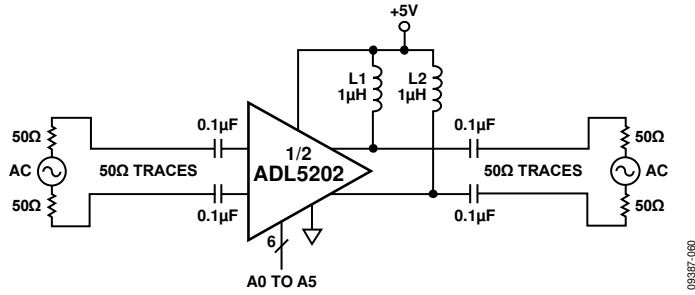


Figure 47. Test Circuit for S-Parameters on Dedicated 50 Ω Differential-to-Differential Board

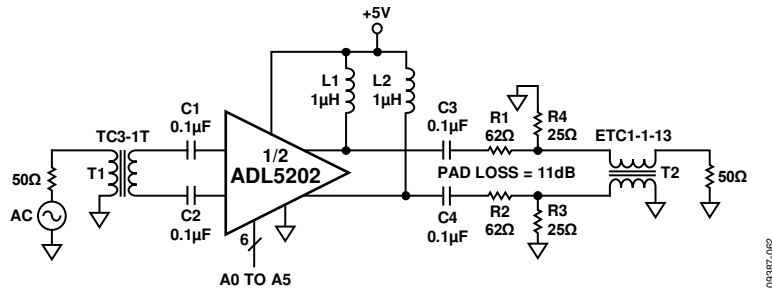


Figure 48. Test Circuit for Distortion, Gain, and Noise

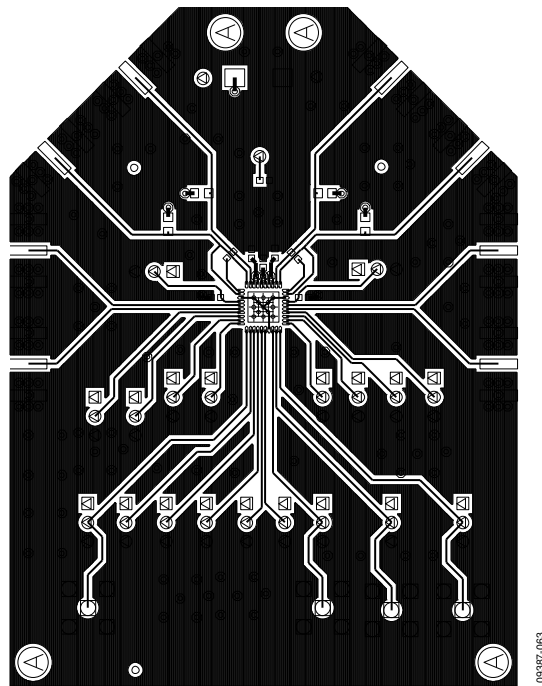


Figure 49. Differential-to-Differential Characterization Board, Circuit Side Layout

# THEORY OF OPERATION

## DIGITAL INTERFACE OVERVIEW

The ADL5202 VGA has three digital gain control options: the parallel control interface, serial peripheral interface, and gain up/down interface. The desired gain control option is selected via two control pins, MODE0 and MODE1 (see Table 4 for the truth table for the mode control pins). The gain code is in a 6-bit binary format. A voltage of between 1.4 V and 3.3 V is required for a logic high.

Three pins are common to all gain control options: PM, PWUPA, and PWUPB. PM allows the user to choose operation in nominal mode or high performance mode. PWUPA and PWUPB are power-up pins for Channel A and Channel B, respectively. Physical pins are shared among the three interfaces, resulting in as many as three different functions per digital pin (see Table 3).

Table 4. Digital Control Interface Selection Truth Table

| MODE1 | MODE0 | Interface               |
|-------|-------|-------------------------|
| 0     | 0     | Parallel control        |
| 0     | 1     | Serial peripheral (SPI) |
| 1     | 0     | Up/down                 |
| 1     | 1     | Up/down                 |

## PARALLEL DIGITAL INTERFACE

The parallel digital interface uses six binary bits (Bits[A5:A0] or Bits[B5:B0]) and a latch pin (LATCHA or LATCHB) per amplifier. The latch pin controls whether the input data latch is transparent or latched. In transparent mode, gain changes as input gain control bits change. In latched mode, gain is determined by the latched gain setting and does not change with changing input gain control bits.

## SERIAL PERIPHERAL INTERFACE (SPI)

The SPI uses three pins (SDIO, SCLK, and  $\overline{CSA}$  or  $\overline{CSB}$ ). The SPI data register consists of two bytes: six gain control bits, two attenuation step size address bits, one read/write bit, and seven don't care bits. SDIO is the serial data input and output pin. The SCLK pin is the serial clock, and  $\overline{CSA}$  or  $\overline{CSB}$  is the channel select pin.

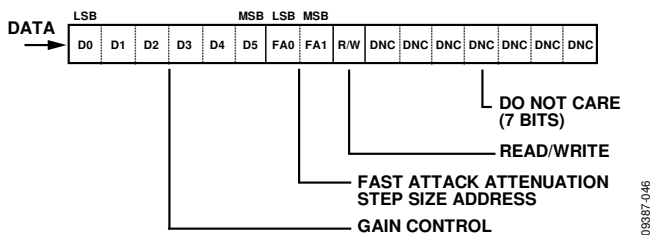


Figure 50. 16-Bit SPI Register

To write to the SPI register,  $\overline{CSA}$  or  $\overline{CSB}$  must be pulled low and 16 clock pulses must be applied to SCLK. Individual channel SPI registers can be selected by pulling  $\overline{CSA}$  or  $\overline{CSB}$  low. By pulling the  $\overline{CSA}$  and  $\overline{CSB}$  pins low simultaneously, the same data can be written to both SPI registers.

To read the SPI register value, the R/W bit must be set high,  $\overline{CSA}$  or  $\overline{CSB}$  must be pulled low, and the part must be clocked. After the register has been read out during the next 16 clock cycles, the SPI is automatically put into write mode. Note that there is only one SDIO pin. Readback from the registers should be performed individually.

## Fast Attack

The fast attack feature, accessible via the SPI, allows the gain to be reduced from its present gain setting by a predetermined step size. Four different attenuation step sizes are available. The truth table for fast attack is shown in Table 5.

Table 5. SPI 2-Bit Attenuation Step Size Truth Table

| FA1 | FA0 | Step Size (dB) |
|-----|-----|----------------|
| 0   | 0   | 2              |
| 0   | 1   | 4              |
| 1   | 0   | 8              |
| 1   | 1   | 16             |

SPI fast attack mode is controlled by the FA\_A or FA\_B pin. A logic high on the FA\_A or FA\_B pin results in an attenuation that is selected by Bits[FA1:FA0] in the SPI register.

## GAIN UP/DOWN INTERFACE

The GS1 and GS0 pins control the up/down gain step function. Gain is increased by a clock pulse on the UPDN\_CLK\_A pin or the UPDN\_CLK\_B pin (rising and falling edges) when the UPDN\_DAT\_A or UPDN\_DAT\_B pin is high. Gain is decreased by a clock pulse on the UPDN\_CLK\_A or UPDN\_CLK\_B pin when the UPDN\_DAT\_A or UPDN\_CLKB pin is low. The truth table for the gain step function is shown in Table 6. Reset is detected by a rising edge latching data having one polarity, with the falling edge latching the opposite polarity. Reset results in a minimum binary gain code of 111111.

Table 6. Step Size Control Truth Table

| GS1 | GS0 | Step Size (dB) |
|-----|-----|----------------|
| 0   | 0   | 0.5            |
| 0   | 1   | 1              |
| 1   | 0   | 2              |
| 1   | 1   | 4              |

The step size is selectable using the GS1 and GS0 pins. The gain is limited by the top and bottom of the control range.

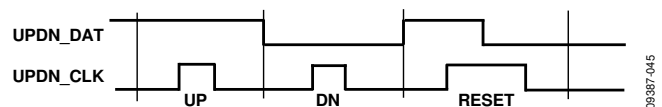


Figure 51. Up/Down Timing

**TRUTH TABLE**

Table 7. Gain Code vs. Voltage Gain Lookup Table

| 6-Bit Binary Gain Code | Voltage Gain (dB) | 6-Bit Binary Gain Code | Voltage Gain (dB) |
|------------------------|-------------------|------------------------|-------------------|
| 000000                 | 20                | 100000                 | 4                 |
| 000001                 | 19.5              | 100001                 | 3.5               |
| 000010                 | 19                | 100010                 | 3                 |
| 000011                 | 18.5              | 100011                 | 2.5               |
| 000100                 | 18                | 100100                 | 2                 |
| 000101                 | 17.5              | 100101                 | 1.5               |
| 000110                 | 17                | 100110                 | 1                 |
| 000111                 | 16.5              | 100111                 | 0.5               |
| 001000                 | 16                | 101000                 | 0                 |
| 001001                 | 15.5              | 101001                 | -0.5              |
| 001010                 | 15                | 101010                 | -1                |
| 001011                 | 14.5              | 101011                 | -1.5              |
| 001100                 | 14                | 101100                 | -2                |
| 001101                 | 13.5              | 101101                 | -2.5              |
| 001110                 | 13                | 101110                 | -3                |
| 001111                 | 12.5              | 101111                 | -3.5              |
| 010000                 | 12                | 110000                 | -4                |
| 010001                 | 11.5              | 110001                 | -4.5              |
| 010010                 | 11                | 110010                 | -5                |
| 010011                 | 10.5              | 110011                 | -5.5              |
| 010100                 | 10                | 110100                 | -6                |
| 010101                 | 9.5               | 110101                 | -6.5              |
| 010110                 | 9                 | 110110                 | -7                |
| 010111                 | 8.5               | 110111                 | -7.5              |
| 011000                 | 8                 | 111000                 | -8                |
| 011001                 | 7.5               | 111001                 | -8.5              |
| 011010                 | 7                 | 111010                 | -9                |
| 011011                 | 6.5               | 111011                 | -9.5              |
| 011100                 | 6                 | 111100                 | -10               |
| 011101                 | 5.5               | 111101                 | -10.5             |
| 011110                 | 5                 | 111110                 | -11               |
| 011111                 | 4.5               | 111111                 | -11.5             |

**LOGIC TIMING**

To write to the ADL5202, refer to the timing shown in Figure 2 (reproduced in this section as Figure 52). The write mode uses a 16-bit serial word on the SDIO pin. The R/W of the word must be low to write Bits[D0:D5], which are the binary weighted codes for the attenuation level (0 = minimum attenuation, 63 = maximum attenuation). The FA0 and FA1 bits control the fast attack step size. The DNC bits are nonfunctional, do not care bits. Reading the ADL5202 SPI register requires the following two steps:

1. Set the R/W bit high using a 16-bit word and the timing described in this section and Figure 52. All other bits are ignored when the R/W bit is high.
2. The SDIO is used as an output during the next sequence. The written pattern is serially clocked out on SDIO using 16 clocks and the timing described in this section and Figure 52. The R/W bit automatically returns low to the write state following the read sequence.

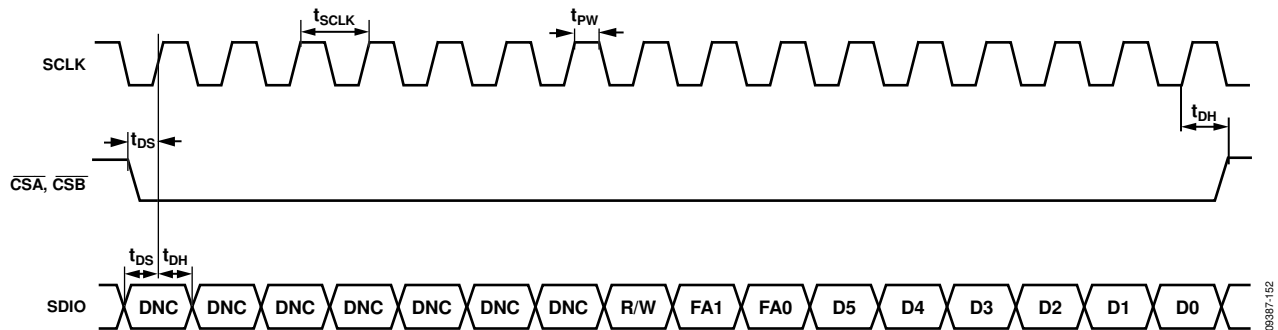


Figure 52. SPI Interface Read/Write Mode Timing Diagram

## CIRCUIT DESCRIPTION

### BASIC STRUCTURE

The ADL5202 is a dual, differential, variable gain amplifier, with each amplifier consisting of a 150 Ω digitally controlled, passive attenuator that is followed by a highly linear transconductance amplifier with feedback.

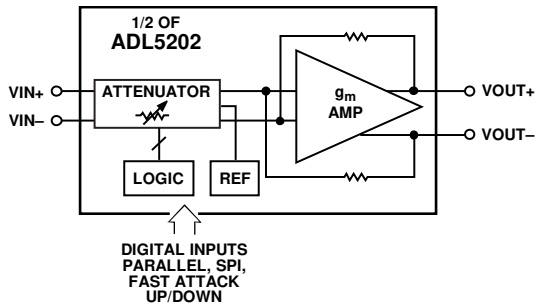


Figure 53. Simplified Schematic

### Input System

The dc voltage level at the inputs of each amplifier is set by two independent internal voltage reference circuits to approximately 1.6 V. The references are not accessible and cannot be adjusted.

Each amplifier can be powered down by pulling the corresponding power-up pin down to ground (logic low). When powered down, the total current of each amplifier reduces to 7 mA (typical). The dc level at the inputs remains at approximately 1.6 V, regardless of the state of the PWUPA or PWUPB pin.

### Output Amplifier

The gain of the output amplifier is set to 22 dB when driving a 150 Ω load. The input and output resistance of this amplifier is set to 150 Ω in matched condition. If the load or the source resistance is different from 150 Ω, the following equations can be used to determine the resulting gain and input/output resistances.

$$\text{Voltage Gain} = A_V = 0.09 \times (2000) // R_L$$

$$R_{IN} = (2000 + R_L) / (1 + 0.09 \times R_L)$$

$$S_{21} (\text{Gain}) = 2 \times R_{IN} / (R_{IN} + R_S) \times A_V$$

$$R_{OUT} = (2000 + R_S) / (1 + 0.09 \times R_S)$$

Note that at the maximum attenuation setting,  $R_S$ , as seen by the output amplifier, is the output resistance of the attenuator, which is 150 Ω. However, at minimum attenuation,  $R_S$  is the source resistance that is connected to the input of the part.

The dc current to the outputs of each amplifier is supplied through two external chokes. The inductance of the chokes and the resistance of the load, in parallel with the output resistance of the device, add a low frequency pole to the response. The parasitic capacitance of the chokes adds to the output capacitance of the part. This total capacitance, in parallel with the load and output resistance, sets the high frequency pole of the device. Generally, the larger the inductance of the choke, the higher its parasitic capacitance. Therefore, this trade-off must be considered when the value and type of the choke are selected. For an operation frequency of 15 MHz to 700 MHz driving a 150 Ω load, 1 μH chokes with a self resonant frequency (SRF) of 160 MHz or higher are recommended (such as the 0805LS-102XJBB from Coilcraft). If higher value chokes are used, a 4 MHz zero, due to the internal ac-coupled feedback, causes an increase in  $S_{21}$  of up to 6 dB at frequencies below 4 MHz. The supply current of each amplifier consists of about 35 mA through the VPOS pin and 50 mA through the two chokes combined. The latter increases with temperature at approximately 2.5 mA per 10°C. The total choke current increases to 75 mA for high performance mode. Each amplifier has two output pins for each polarity, and they are oriented in an alternating fashion. When designing the board, care should be taken to minimize the parasitic capacitance due to the routing that connects the corresponding outputs together. To minimize the parasitic capacitance, a good practice is to avoid any ground or power plane under this routing region and under the chokes.

### Gain Control

The gain of each amplifier can be adjusted using the parallel control interface, the serial peripheral interface, or the gain up/down interface. In general, the gain step size is 0.5 dB, but larger sizes can be programmed using the various interfaces, as described in the Digital Interface Overview section. Each amplifier has a maximum gain of +20 dB (Code 0) to -11.5 dB (Code 63).

The noise figure of each amplifier is approximately 7.5 dB at maximum gain setting, and it increases as the gain is reduced. The increase in noise figure is equal to the reduction in gain. The linearity of the part measured at the output is first-order independent of the gain setting. From -4 dB to +20 dB gain, OIP3 is approximately 50 dBm into 150 Ω load at 200 MHz (0 dBm per tone). At gain settings below -4 dB, OIP3 drops to approximately 40 dBm.

# APPLICATIONS INFORMATION

## BASIC CONNECTIONS

Figure 54 shows the basic connections for operating the ADL5202. A voltage between 4.5 V and 5.5 V should be applied to the VPOS pins. Each supply pin should be decoupled with at least one low inductance, surface-mount ceramic capacitor of 0.1  $\mu\text{F}$ , placed as close as possible to the device.

The outputs of the ADL5202 must be pulled up to the positive supply with 1  $\mu\text{H}$  RF chokes. The differential outputs are biased to the positive supply and require ac coupling capacitors, preferably 0.1  $\mu\text{F}$ . Similarly, the input pins are at bias voltages of about 1.6 V above ground and should be ac-coupled as well. The ac coupling capacitors and the RF chokes are the principle limitations for operation at low frequencies.

The digital pins (mode control pins, associated SPI and parallel gain control pins, PM, PWUPA, and PWUPB) operate on a voltage of 3.3 V.

To enable each channel of the ADL5202, the PWUPA or PWUPB pin must be pulled high ( $1.4 \text{ V} \leq \text{PWUPA/PWUPB} \leq 3.3 \text{ V}$ ). Taking PWUPA or PWUPB low puts the channels of the ADL5202 in sleep mode, reducing current consumption to approximately 7 mA per channel at ambient.

## ADC DRIVING

The ADL5202 is a highly linear, variable gain amplifier that is optimized for ADC interfacing. The output IMDs and noise floor remain constant throughout the 31.5 dB gain range. This is a valuable feature in a variable gain receiver where it is desirable to maintain a constant instantaneous dynamic range as the receiver range is modified. The output noise is 18 nV/ $\sqrt{\text{Hz}}$ , which is compatible with 14- or 16-bit ADCs. The two-tone IMDs are usually greater than -100 dB for -1 dBm into 150  $\Omega$  or 2 V p-p output. The 150  $\Omega$  output impedance makes the task of designing a filter for the high input impedance ADCs more straightforward.

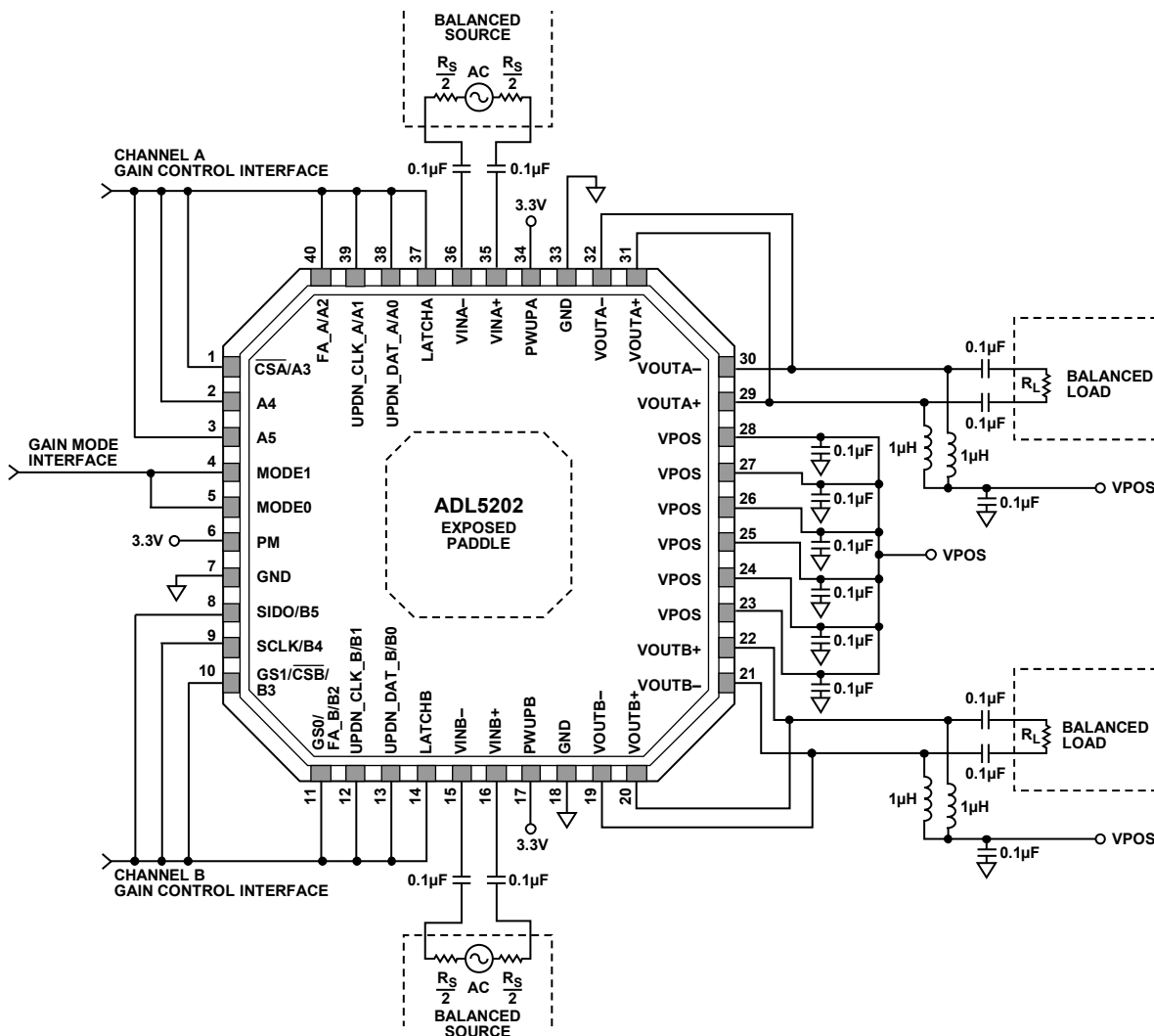


Figure 54. Basic Connections

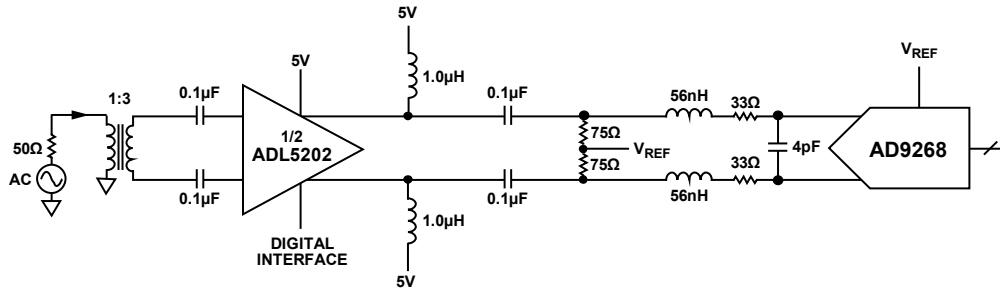


Figure 55. Wideband ADC Interfacing Example Featuring One-Half of the ADL5202 and the AD9268

Figure 55 shows one-half of the ADL5202 driving a two-pole, 100 MHz low-pass filter into the AD9268. The AD9268 is a 16-bit, 125 MSPS analog-to-digital converter with a buffered wideband input, which presents a 6 kΩ differential input impedance and requires between a 1 V or 2 V input swing to reach full scale. This example uses the 2 V p-p input. For optimum performance, the ADL5202 should be driven differentially, using an impedance transformer or input balun.

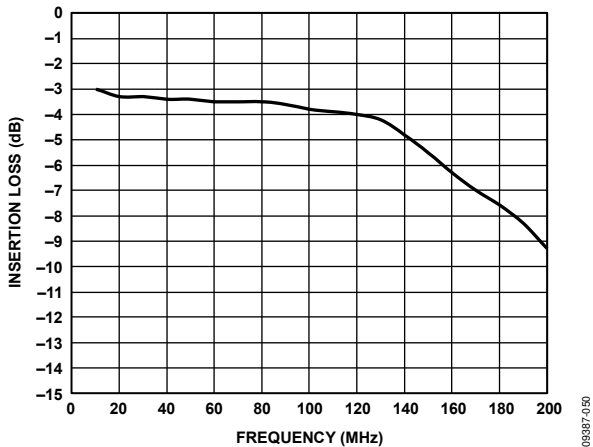


Figure 56. Measured Frequency Response of Wideband ADC Interface, as Depicted in Figure 55

Figure 55 uses a 1:3 impedance transformer to provide the 150 Ω input impedance of the ADL5202 with a matched input. The outputs of the ADL5202 are biased through the two 1 µH inductors, and the two 0.1 µF capacitors on the outputs decouple the 5 V inductor voltage from the input common-mode voltage of the AD9268. The two 75 Ω resistors provide the 150 Ω load to the ADL5202 whose gain is load dependent. The 56 nH inductors and 4 pF capacitor constitute the (100 MHz – 1 dB) low-pass filter. The two 33 Ω isolation resistors suppress any switching currents from the ADC input sample-and-hold circuitry. The circuit depicted in Figure 55 provides variable gain, isolation, filtering, and source matching for the AD9268. Using this circuit with the ADL5202 in a gain of 20 dB (maximum gain), an SNR of 69 dB, and an SFDR performance of >86 dBc is achieved at 100 MHz, as shown in Figure 57.

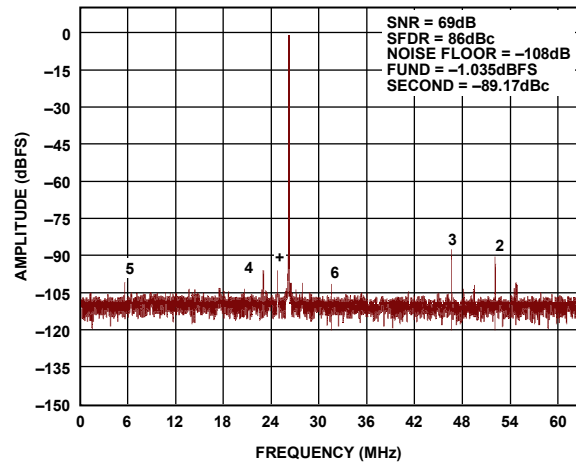


Figure 57. Measured Single-Tone Performance of the Circuit in Figure 55 for a 100 MHz Input Signal

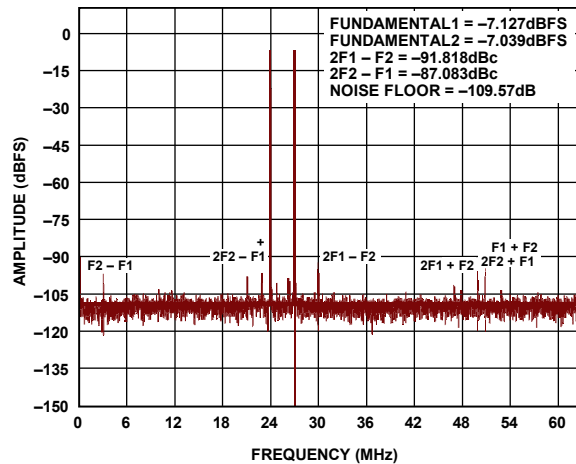


Figure 58. Measured Two-Tone Performance of the Circuit in Figure 55 for a 100 MHz Input Signal

An alternative narrow-band approach is presented in Figure 59. By designing a narrow band-pass antialiasing filter between the ADL5202 and the target ADC, the output noise of the ADL5202 outside of the intended Nyquist zone can be attenuated, helping to preserve the available SNR of the ADC. In general, the SNR improves by several decibels (dB) when including a reasonable order antialiasing filter. In this example, a low loss 1:3 input transformer is used to match the 150 Ω balanced input of the ADL5202 to a 50 Ω unbalanced source, resulting in minimum insertion loss at the input.

Figure 59 is optimized for driving some of the Analog Devices popular unbuffered ADCs, such as the AD9246, AD9640, and AD6655. Table 8 includes antialiasing filter component recommendations for popular IF sampling center frequencies. Inductor L5 works in parallel with the on-chip ADC input capacitance and a portion of the capacitance presented by C4 to form a resonant tank circuit. The resonant tank helps to ensure that the ADC input acts like a real resistance at the target center frequency.

In addition, the L6 inductor shorts the ADC inputs at dc, which introduces a zero into the transfer function. The ac coupling capacitors and the bias chokes introduce additional zeros into the

transfer function. The final overall frequency response takes on a band-pass characteristic, helping to reject noise outside of the intended Nyquist zone. Table 8 provides initial suggestions for prototyping purposes. Some empirical optimization may be needed to help compensate for actual PCB parasitics.

**LAYOUT CONSIDERATIONS**

The ADL5202 has two output pins for each polarity, and they are oriented in an alternating fashion. When designing the board, care should be taken to minimize the parasitic capacitance due to the routing that connects the corresponding outputs together. A good practice is to avoid any ground or power plane under this routing region and under the chokes to minimize the parasitic capacitance.

If the common-mode load capacitance including the capacitance of the trace is > 2 pF, use parasitic suppressing resistors at the device output pins. The resistors should be placed in the output traces just after the crossover connections. Use 5 Ω series resistors (Size 0402) to adequately de-Q the output system without a significant decrease in gain.

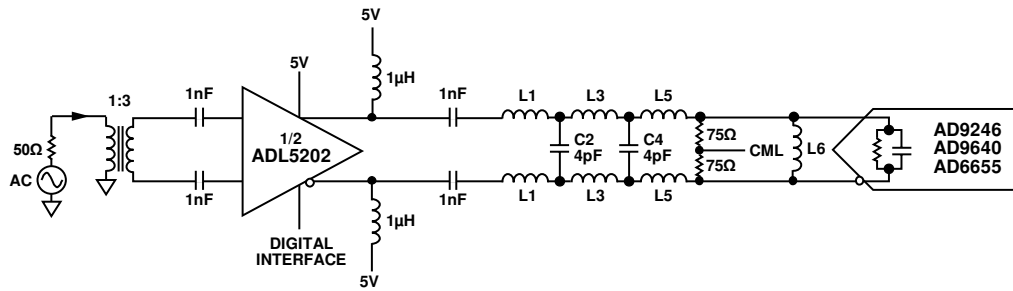


Figure 59. Narrow-Band IF Sampling Solution for Unbuffered ADC Applications

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**Table 8. Interface Filter Recommendations for Various IF Sampling Frequencies**

| Center Frequency | 1 dB Bandwidth | L1    | C2    | L3     | C4     | L5    | L6     |
|------------------|----------------|-------|-------|--------|--------|-------|--------|
| 96 MHz           | 27 MHz         | 68 nH | 15 pF | 220 nH | 15 pF  | 68 nH | 150 nH |
| 140 MHz          | 31 MHz         | 47 nH | 11 pF | 150 nH | 11 pF  | 47 nH | 82 nH  |
| 170 MHz          | 25 MHz         | 39 nH | 10 pF | 120 nH | 10 pF  | 47 nH | 51 nH  |
| 211 MHz          | 40 MHz         | 30 nH | 7 pF  | 100 nH | 7.5 pF | 30 nH | 43 nH  |

## EVALUATION BOARD

The ADL5202 evaluation board is available with software to program the variable gain control. It is a 4-layer board with a split ground plane for analog and digital sections. Special care is taken to place the power decoupling capacitors close to the device pins. The board is designed for easy single-ended (through a Mini-Circuits TC3-1T+ RF transformer) or differential configuration for each channel.

## EVALUATION BOARD CONTROL SOFTWARE

The ADL5202 evaluation board is configured with a USB-friendly interface to program the gain of the ADL5202. The software graphic user interface (see Figure 60) lets users select a particular gain mode and gain level to write to the device and also to read back data from the SDIO pin, showing the currently programmed gain setting. The software setup files can be downloaded from the ADL5202 product page at [www.analog.com](http://www.analog.com).

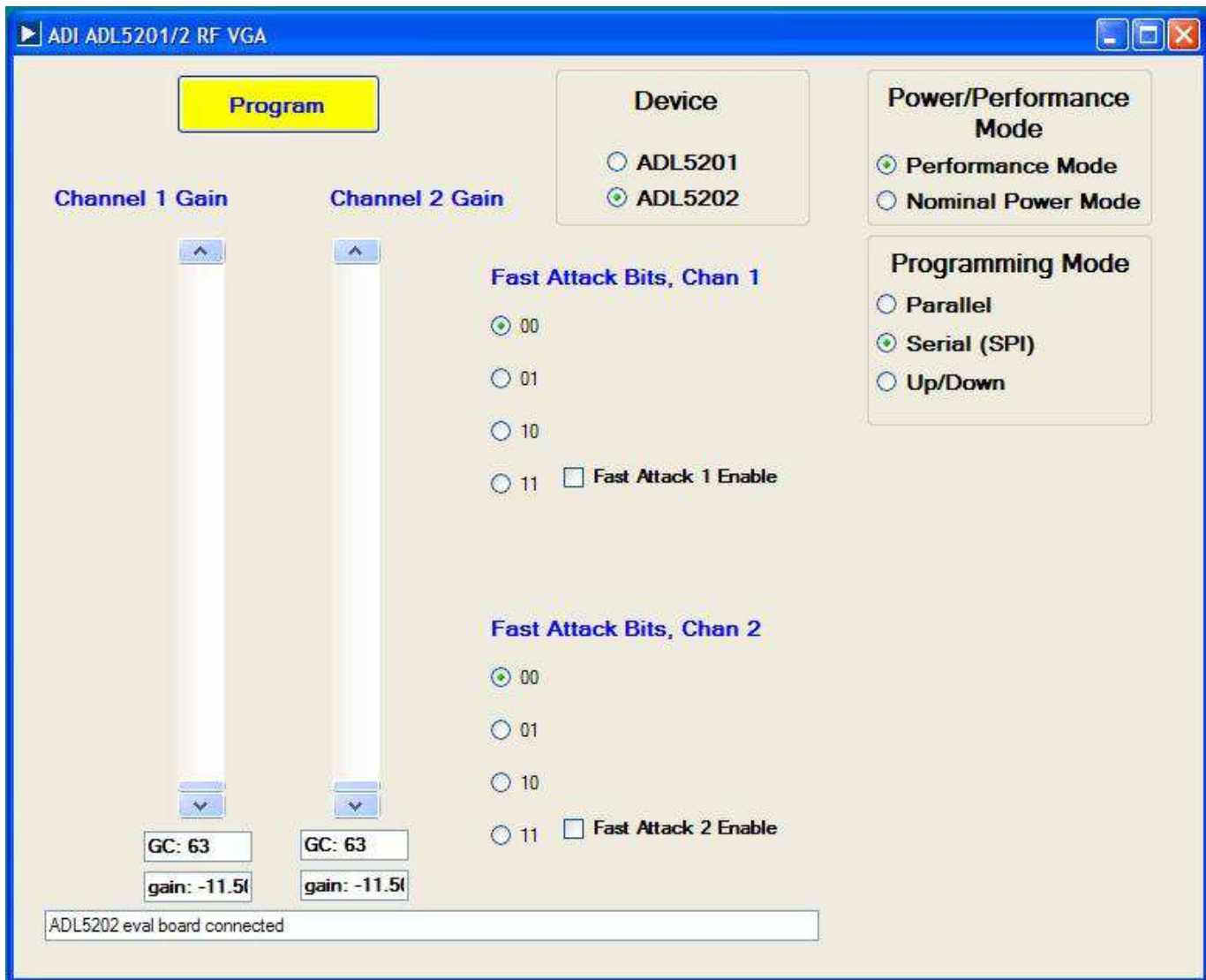


Figure 60. Evaluation Control Software



EVALUATION BOARD SCHEMATICS AND ARTWORK

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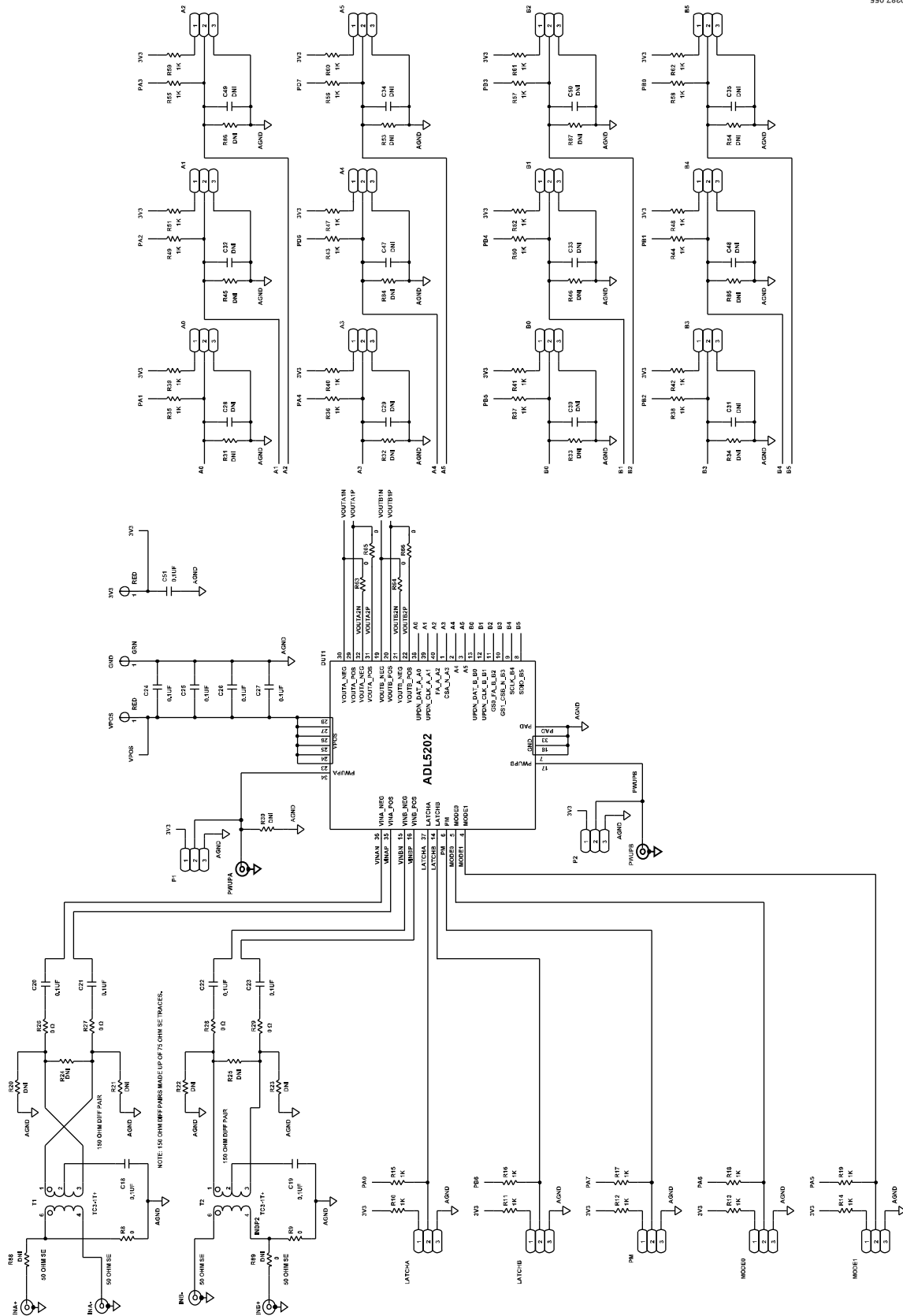


Figure 61. Evaluation Board Schematic

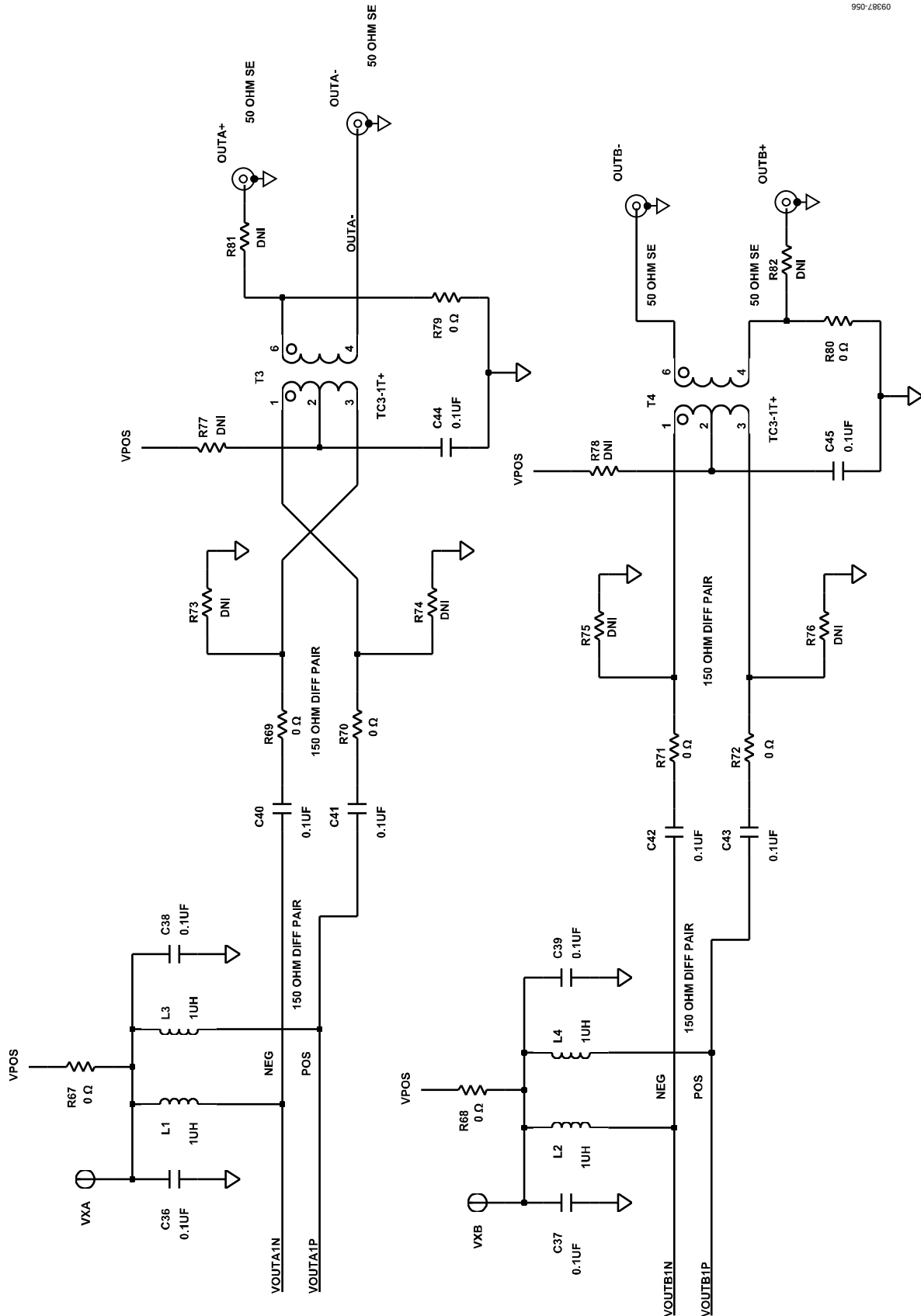


Figure 62. RF Output Detail