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ANALOG DEVICES

400 MHz to 6 GHz Quadrature Demodulator

Data Sheet **ADL5380**

FEATURES

Operating RF and LO frequency: 400 MHz to 6 GHz
Input IP3
- **30 dBm at 900 MHz**
- **28 dBm at 1900 MHz**

Input IP2: >65 dBm at 900 MHz
Input P1dB (IP1dB): 11.6 dBm at 900 MHz
Noise figure (NF)
- **10.9 dB at 900 MHz**
- **11.7 dB at 1900 MHz**

Voltage conversion gain: ~7 dB
Quadrature demodulation accuracy at 900 MHz
- **Phase accuracy: ~0.2°**
- **Amplitude balance: ~0.07 dB**

Demodulation bandwidth: ~390 MHz
Baseband I/Q drive: 2 V p-p into 200 Ω
Single 5 V supply

APPLICATIONS

Cellular W-CDMA/GSM/LTE
Microwave point-to-(multi)point radios
Broadband wireless and WiMAX

FUNCTIONAL BLOCK DIAGRAM

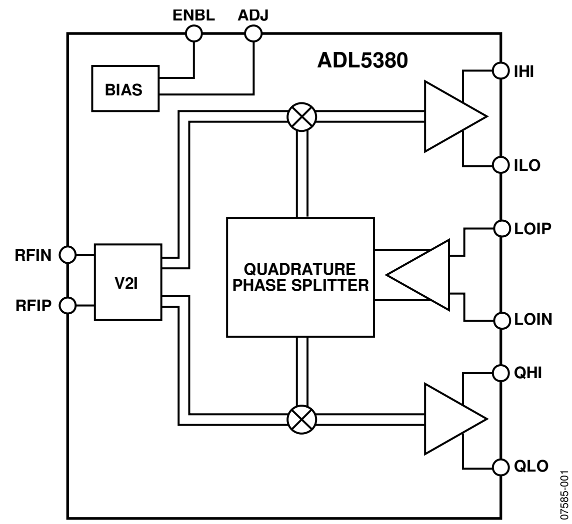

Figure 1.

GENERAL DESCRIPTION

The ADL5380 is a broadband quadrature I-Q demodulator that covers an RF/IF input frequency range from 400 MHz to 6 GHz. With a NF = 10.9 dB, IP1dB = 11.6 dBm, and IIP3 = 29.7 dBm at 900 MHz, the ADL5380 demodulator offers outstanding dynamic range suitable for the demanding infrastructure direct-conversion requirements. The differential RF inputs provide a well-behaved broadband input impedance of 50 Ω and are best driven from a 1:1 balun for optimum performance.

Excellent demodulation accuracy is achieved with amplitude and phase balances of ~0.07 dB and ~0.2°, respectively. The demodulated in-phase (I) and quadrature (Q) differential outputs are fully buffered and provide a voltage conversion gain of ~7 dB. The buffered baseband outputs are capable of driving a 2 V p-p differential signal into 200 Ω.

The fully balanced design minimizes effects from second-order distortion. The leakage from the LO port to the RF port is <−50 dBm. Differential dc offsets at the I and Q outputs are typically <20 mV. Both of these factors contribute to the excellent IIP2 specification, which is >65 dBm.

The ADL5380 operates off a single 4.75 V to 5.25 V supply. The supply current is adjustable by placing an external resistor from the ADJ pin to either the positive supply, V_S, (to increase supply current and improve IIP3) or to ground (which decreases supply current at the expense of IIP3).

The ADL5380 is fabricated using the Analog Devices, Inc., advanced silicon-germanium bipolar process and is available in a 24-lead exposed paddle LFCSP.

Rev. B Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
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ADL5380* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD-FMCOMMS6-EBZ Evaluation Board
- ADL5380 Evaluation Boards
- FPGA Mezzanine Card for Wireless Communications

DOCUMENTATION

Data Sheet

- ADL5380: 400 MHz to 6 GHz Quadrature Demodulator Data Sheet

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

REFERENCE DESIGNS

- CN0245
- CN0374

REFERENCE MATERIALS

Press

- New PLLs Deliver Widest Frequency Range Coverage and Lowest VCO Phase Noise in a Single Device

Product Selection Guide

- RF Source Booklet

Technical Articles

- Assess Quadrature-Demodulator Noise Figure Using Vector Signal Analysis
- Direct Conversion Receiver Designs Enable Multi-standard/Multi-band Operation
- Semiconductors Simplify Direct-Conversion Design

DESIGN RESOURCES

- adl5380 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

12/14—Rev. A to Rev. B

7/13—Rev. 0 to Rev. A

7/09—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, T_A = 25°C, f_{LO} = 900 MHz, f_{IF} = 4.5 MHz, P_{LO} = 0 dBm, Z_O = 50 Ω, unless otherwise noted. Baseband outputs differentially loaded with 450 Ω. Loss of the balun used to drive the RF port was de-embedded from these measurements.

Table 1.

Parameter	Condition	Min	Typ	Max	Unit
OPERATING CONDITIONS					
LO and RF Frequency Range		0.4		6	GHz
LO INPUT	LOIP, LOIN				
Input Return Loss	LO driven differentially through a balun at 900 MHz		−10		dB
LO Input Level		−6	0	+6	dBm
I/Q BASEBAND OUTPUTS	QHI, QLO, IHI, ILO				
Voltage Conversion Gain	450 Ω differential load on I and Q outputs at 900 MHz		6.9		dB
	200 Ω differential load on I and Q outputs at 900 MHz		5.9		dB
Demodulation Bandwidth	1 V p-p signal, 3 dB bandwidth		390		MHz
Quadrature Phase Error	At 900 MHz		0.2		Degrees
I/Q Amplitude Imbalance			0.07		dB
Output DC Offset (Differential)	0 dBm LO input at 900 MHz		±10		mV
Output Common Mode	Dependent on ADJ pin setting				
	V_{ADJ} ~ 4 V (set by 1.5 kΩ from ADJ pin to V_S)		V_S − 2.5		V
	V_{ADJ} ~ 4.8 V (set by 200 Ω from ADJ pin to V_S)		V_S − 2.8		V
	V_{ADJ} ~ 2.4 V (ADJ pin open)		V_S − 1.2		V
0.1 dB Gain Flatness			37		MHz
Output Swing	Differential 200 Ω load		2		V p-p
Peak Output Current	Each pin		12		mA
POWER SUPPLIES	V_S = VCC1, VCC2, VCC3				
Voltage		4.75		5.25	V
Current	1.5 kΩ from ADJ pin to V_S; ENBL pin low		245		mA
	1.5 kΩ from ADJ pin to V_S; ENBL pin high		145		mA
ENABLE FUNCTION	Pin ENBL				
Off Isolation			−70		dB
Turn-On Settling Time	ENBL high to low		45		ns
Turn-Off Settling Time	ENBL low to high		950		ns
ENBL High Level (Logic 1)		2.5			V
ENBL Low Level (Logic 0)				1.7	V
DYNAMIC PERFORMANCE at RF = 900 MHz	V_{ADJ} ~ 4 V (set by 1.5 kΩ from ADJ pin to V_S)				
Conversion Gain			6.9		dB
Input P1dB			11.6		dBm
RF Input Return Loss	RFIP, RFIN driven differentially through a balun		−19		dB
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		68		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		29.7		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−52		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−67		dBc
IQ Magnitude Imbalance			0.07		dB
IQ Phase Imbalance			0.2		Degrees
Noise Figure			10.9		dB
Noise Figure Under Blocking Conditions	With a −5 dBm input interferer 5 MHz away		13.1		dB

Parameter	Condition	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE at RF = 1900 MHz	V_{ADJ} ~ 4 V (set by 1.5 kΩ from ADJ pin to V_S)				
Conversion Gain			6.8		dB
Input P1dB			11.6		dBm
RF Input Return Loss	RFIP, RFIN driven differentially through a balun		−13		dB
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		61		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		27.8		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−49		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−77		dBc
IQ Magnitude Imbalance			0.07		dB
IQ Phase Imbalance			0.25		Degrees
Noise Figure			11.7		dB
Noise Figure Under Blocking Conditions	With a −5 dBm input interferer 5 MHz away		14		dB
DYNAMIC PERFORMANCE at RF = 2700 MHz	V_{ADJ} ~ 4 V (set by 1.5 kΩ from ADJ pin to V_S)				
Conversion Gain			7.4		dB
Input P1dB			11		dBm
RF Input Return Loss	RFIP, RFIN driven differentially through a balun		−10		dB
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		54		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		28		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−49		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−73		dBc
IQ Magnitude Imbalance			0.07		dB
IQ Phase Imbalance			0.5		Degrees
Noise Figure			12.3		dB
DYNAMIC PERFORMANCE at RF = 3600 MHz	V_{ADJ} ~ 4.8 V (set by200 Ω from ADJ pin to V_S)				
Conversion Gain			6.3		dB
Input P1dB			9.6		dBm
RF Input Return Loss	RFIP, RFIN driven differentially through a balun		−11		dB
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		48		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		21		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−46		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−72		dBc
IQ Magnitude Imbalance			0.14		dB
IQ Phase Imbalance			1.1		Degrees
Noise Figure			14.2		dB
Noise Figure Under Blocking Conditions	With a −5 dBm input interferer 5 MHz away		16.2		dB
DYNAMIC PERFORMANCE at RF = 5800 MHz	V_{ADJ} ~ 2.4 V (ADJ pin left open)				
Conversion Gain			5.8		dB
Input P1dB			8.2		dBm
RF Input Return Loss	RFIP, RFIN driven differentially through a balun		−7.5		dB
Second-Order Input Intercept (IIP2)	−5 dBm each input tone		44		dBm
Third-Order Input Intercept (IIP3)	−5 dBm each input tone		20.6		dBm
LO to RF	RFIN, RFIP terminated in 50 Ω		−47		dBm
RF to LO	LOIN, LOIP terminated in 50 Ω		−62		dBc
IQ Magnitude Imbalance			0.07		dB
IQ Phase Imbalance			−1.25		Degrees
Noise Figure			15.5		dB
Noise Figure Under Blocking Conditions	With a −5 dBm input interferer 5 MHz away		18.9		dB

ABSOLUTE MAXIMUM RATINGS

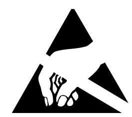
Table 2.

Parameter	Rating
Supply Voltage: VCC1, VCC2, VCC3	5.5 V
LO Input Power	13 dBm (re: 50 Ω)
RF Input Power	15 dBm (re: 50 Ω)
Internal Maximum Power Dissipation	1370 mW
θ_{JA}[1]	53°C/W
θ_{JC}	2.5°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +125°C

[1] Per JDEC standard JESD 51-2. For information on optimizing thermal impedance, see the Thermal Grounding and Evaluation Board Layout section.

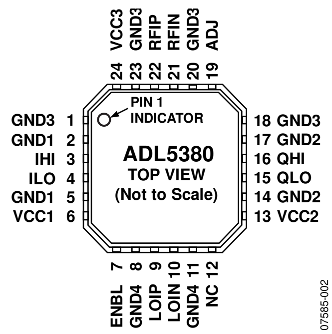
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.
2. THE EXPOSED PAD SHOULD BE CONNECTED TO A LOW IMPEDANCE THERMAL AND ELECTRICAL GROUND PLANE.

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 5, 8, 11, 14, 17, 18, 20, 23	GND1, GND2, GND3, GND4	Ground Connect.
3, 4, 15, 16	IHI, ILO, QLO, QHI	I Channel and Q Channel Mixer Baseband Outputs. These outputs have a 50 Ω differential output impedance (25 Ω per pin). Each output pair can swing 2 V p-p (differential) into a load of 200 Ω. The output 3 dB bandwidth is ~400 MHz.
6, 13, 24	VCC1, VCC2, VCC3	Supply. Positive supply for LO, IF, biasing, and baseband sections. Decouple these pins to the board ground using the appropriate-sized capacitors.
7	ENBL	Enable Control. When pulled low, the part is fully enabled; when pulled high, the part is partially powered down and the output is disabled.
9, 10	LOIP, LOIN	Local Oscillator Input. Pins must be ac-coupled. A differential drive through a balun is necessary to achieve optimal performance. Recommended balun is the Mini-Circuits® TC1-1-13 for lower frequencies, the Johanson Technology 3600 balun for midband frequencies, and the Johanson Technology 5400 balun for high band frequencies. Balun choice depends on the desired frequency range of operation.
12	NC	No Connect. Do not connect to this pin.
19	ADJ	A resistor to V_S that optimizes third-order intercept. For operation <3 GHz, R_{ADJ} = 1.5 kΩ. For operation from 3 GHz to 4 GHz, R_{ADJ} = 200 Ω. For operation >5 GHz, R_{ADJ} = open. See the Circuit Description section for more details.
21, 22	RFIN, RFIP	RF Input. A single-ended 50 Ω signal can be applied differentially to the RF inputs through a 1:1 balun. Recommended balun is the Mini-Circuits TC1-1-13 for lower frequencies, the Johanson Technology 3600 balun for midband frequencies, and the Johanson Technology 5400 balun for high band frequencies. Balun choice depends on the desired frequency range of operation.
	EP	Exposed Pad. The exposed pad should be connected to a low impedance thermal and electrical ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, T_A = 25°C, LO drive level = 0 dBm, RF input balun loss is de-embedded, unless otherwise noted.

LOW BAND OPERATION

RF = 400 MHz to 3 GHz; Mini-Circuits TC1-1-13 balun on LO and RF inputs, 1.5 kΩ from the ADJ pin to V_S.

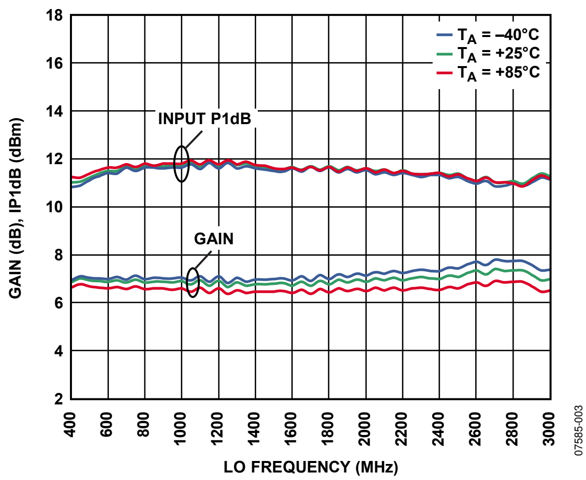


Figure 3. Conversion Gain and Input 1 dB Compression Point (IP1dB) vs. LO Frequency

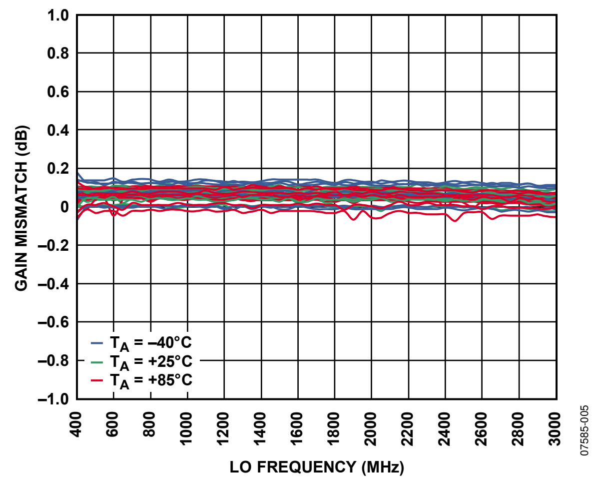


Figure 5. IQ Gain Mismatch vs. LO Frequency

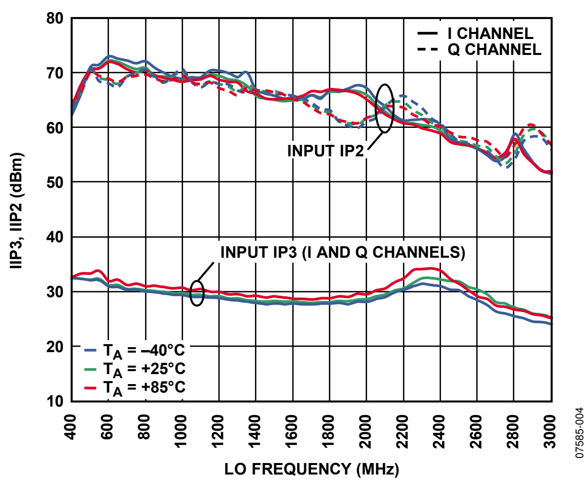


Figure 4. Input Third-Order Intercept (IIP3) and Input Second-Order Intercept Point (IIP2) vs. LO Frequency

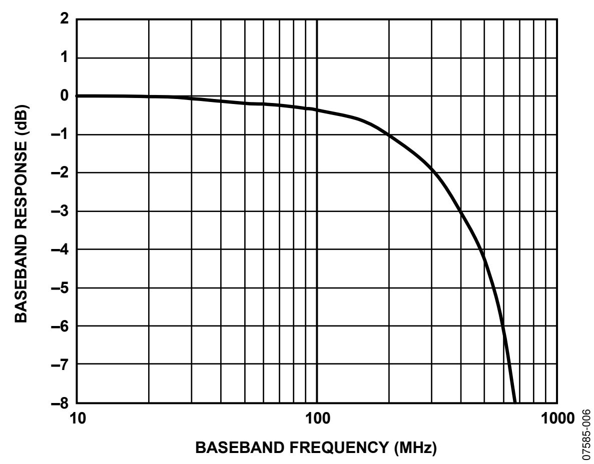


Figure 6. Normalized IQ Baseband Frequency Response

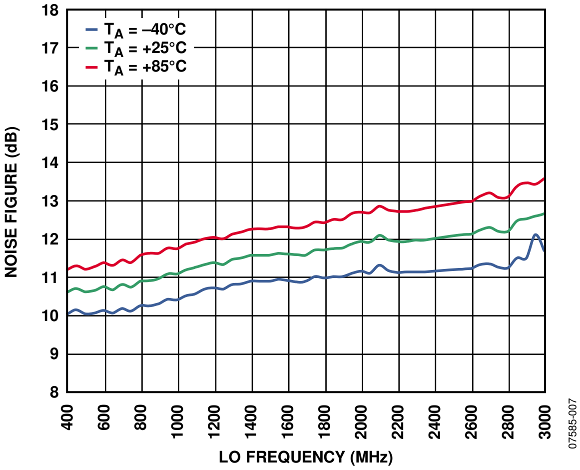


Figure 7. Noise Figure vs. LO Frequency

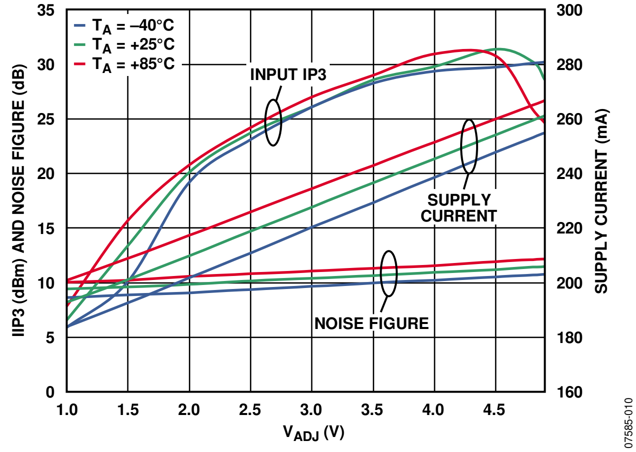


Figure 10. IIP3, Noise Figure, and Supply Current vs. V_{ADJ}, f_{LO} = 900 MHz

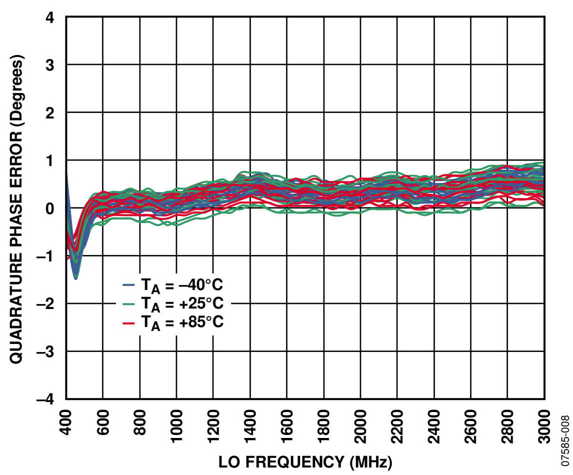


Figure 8. IQ Quadrature Phase Error vs. LO Frequency

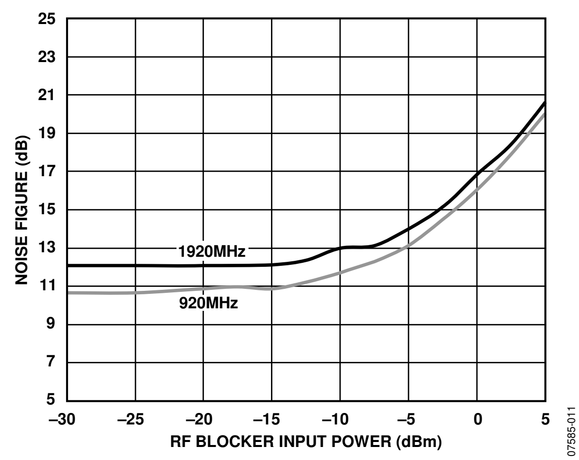


Figure 11. Noise Figure vs. Input Blocker Level, f_{LO} = 900 MHz, f_{LO} = 1900 MHz (RF Blocker 5 MHz Offset)

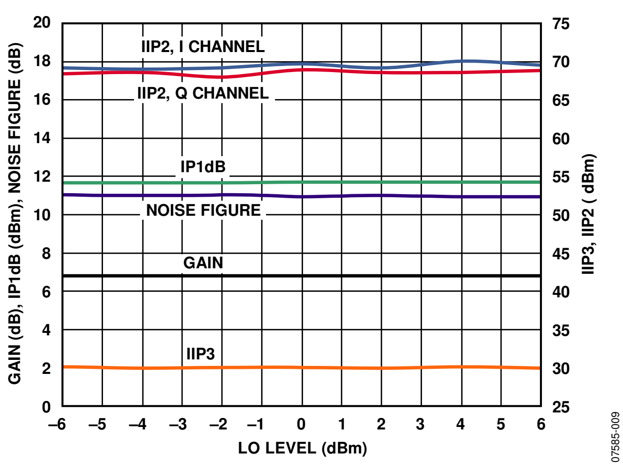


Figure 9. Conversion Gain, IP1dB, Noise Figure, IIP3, and IIP2 vs. LO Level, f_{LO} = 900 MHz

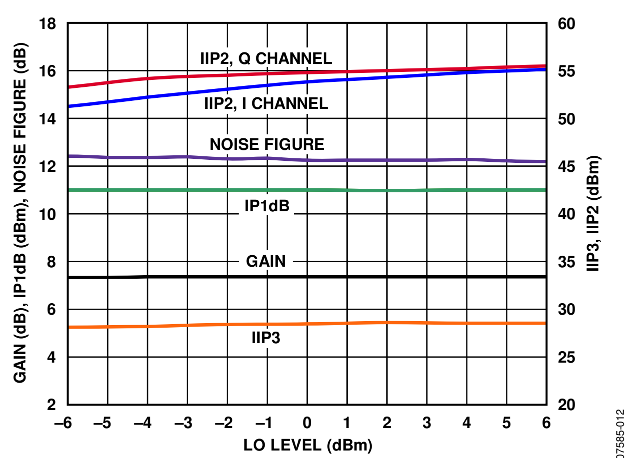


Figure 12. Conversion Gain, IP1dB, Noise Figure, IIP3, and IIP2 vs. LO Level, f_{LO} = 2700 MHz

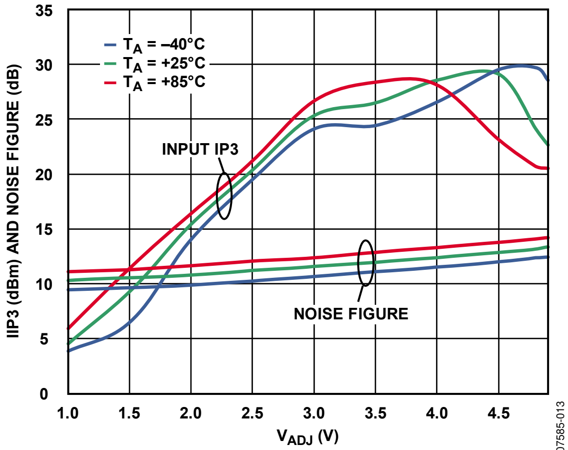


Figure 13. IIP3 and Noise Figure vs. V_{ADJ}, f_{LO} = 2700 MHz

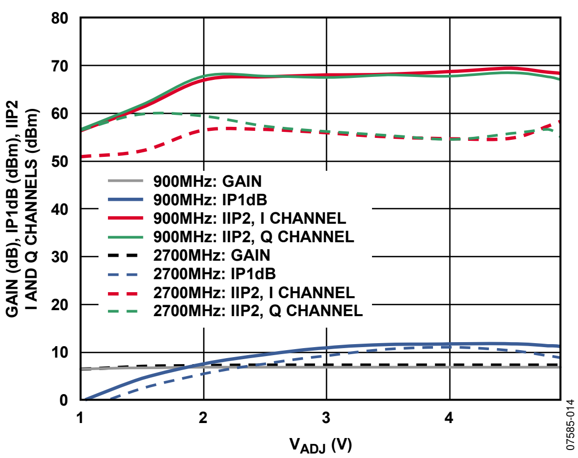


Figure 14. Conversion Gain, IP1dB, and IIP2 vs. V_{ADJ}, f_{LO} = 900 MHz, f_{LO} = 2700 MHz

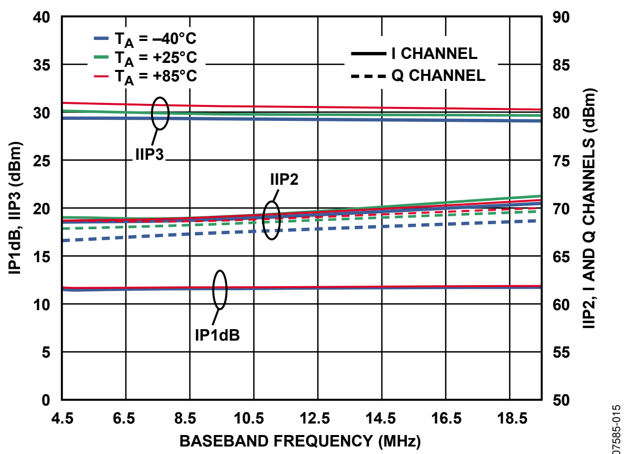


Figure 15. IP1dB, IIP3, and IIP2 vs. Baseband Frequency

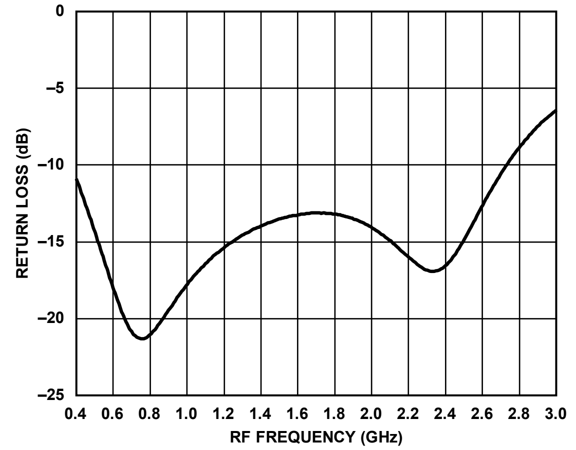


Figure 16. RF Port Return Loss vs. RF Frequency Measured on Characterization Board Through TC1-1-13 Balun

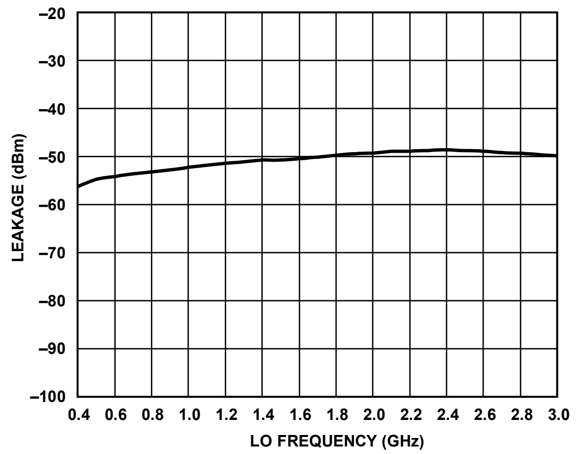


Figure 17. LO-to-RF Leakage vs. LO Frequency

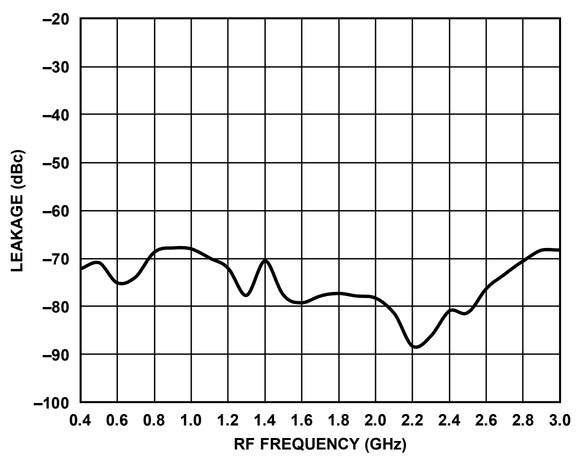


Figure 18. RF-to-LO Leakage vs. RF Frequency

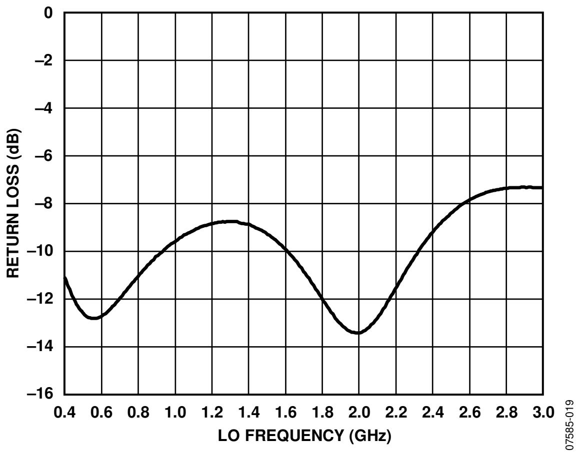


Figure 19. LO Port Return Loss vs. LO Frequency Measured on Characterization Board Through TC1-1-13 Balun

MIDBAND OPERATION

RF = 3 GHz to 4 GHz; Johanson Technology 3600BL14M050T balun on LO and RF inputs, 200 Ω from V_{ADJ} to V_S.

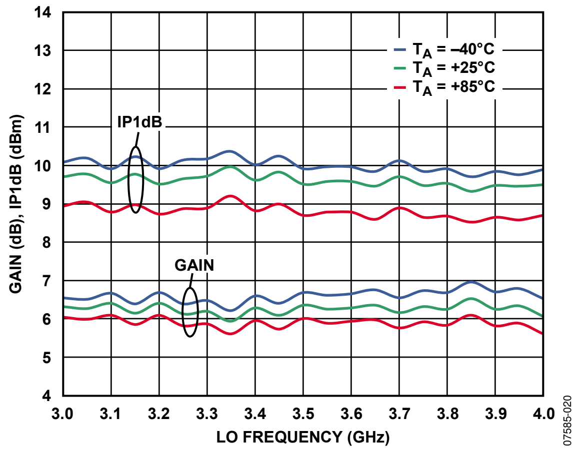


Figure 20. Conversion Gain and Input 1 dB Compression Point (IP1dB) vs. LO Frequency

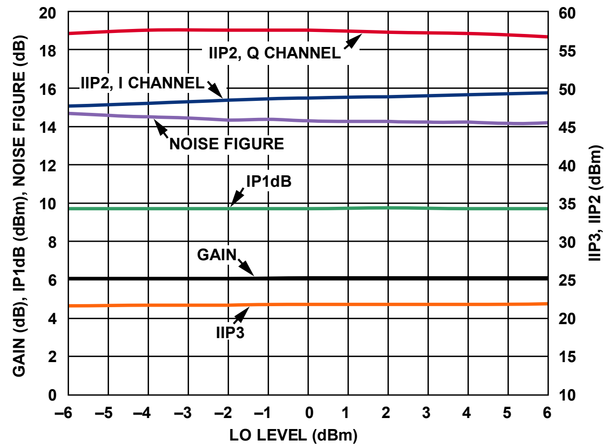


Figure 23. Conversion Gain, IP1dB, Noise Figure, IIP3, and IIP2 vs. LO Level, f_{LO} = 3600 MHz

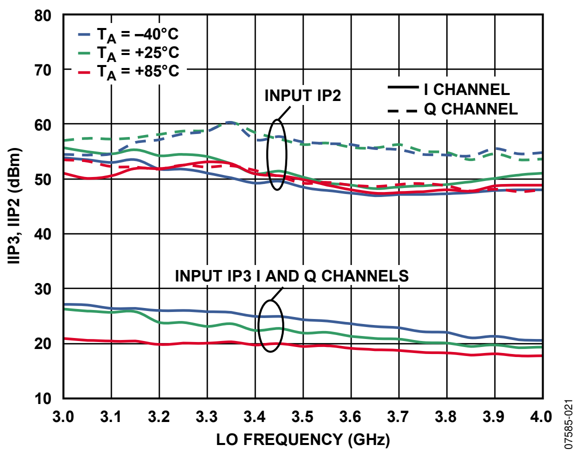


Figure 21. Input Third-Order Intercept (IIP3) and Input Second-Order Intercept Point (IIP2) vs. LO Frequency

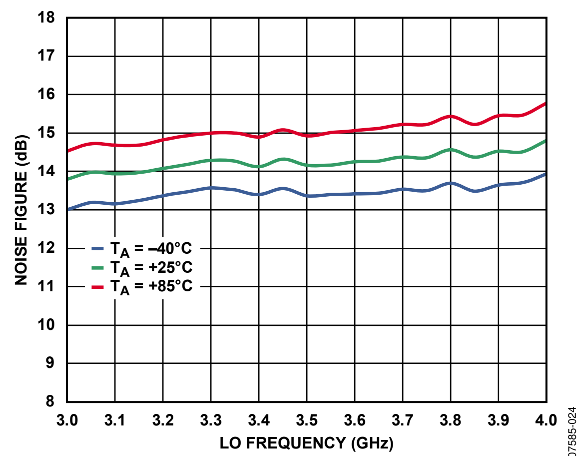


Figure 24. Noise Figure vs. LO Frequency

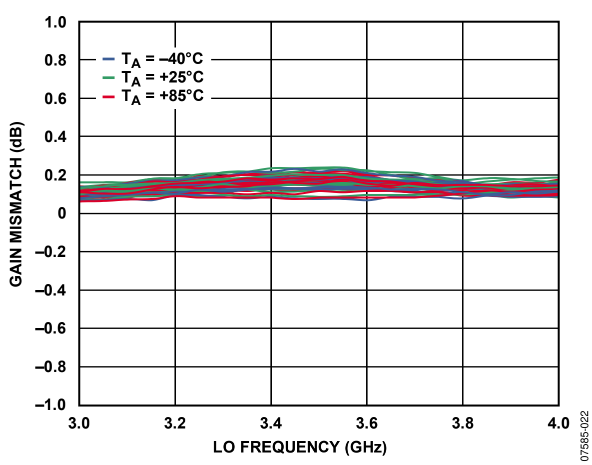


Figure 22. IQ Gain Mismatch vs. LO Frequency

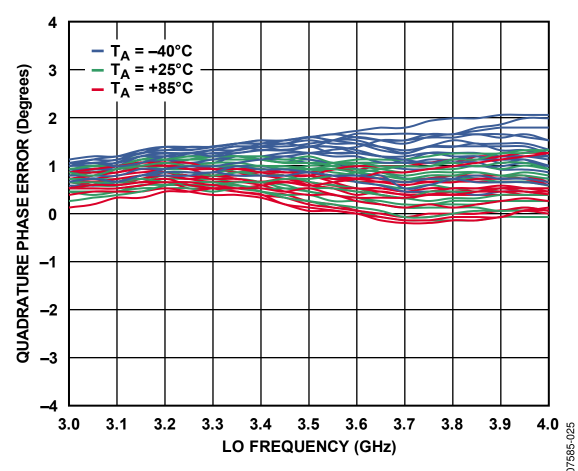


Figure 25. IQ Quadrature Phase Error vs. LO Frequency

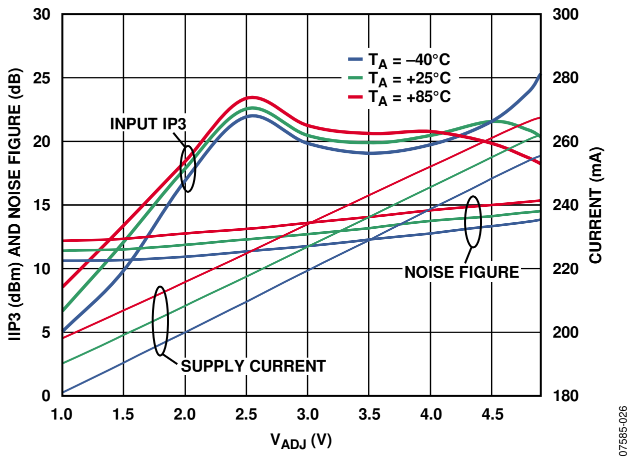


Figure 26. IIP3, Noise Figure, and Supply Current vs. V_{ADJ}, f_{LO} = 3600 MHz

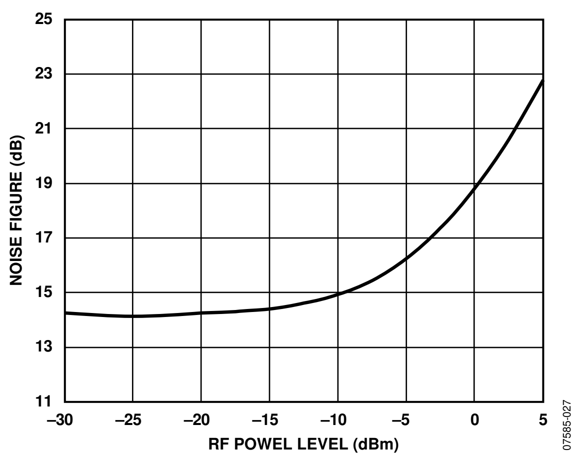


Figure 27. Noise Figure vs. Input Blocker Level, f_{LO} = 3600 MHz (RF Blocker 5 MHz Offset)

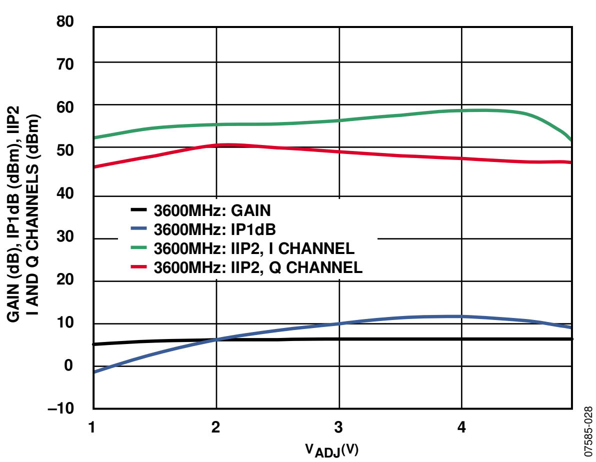


Figure 28. Conversion Gain, IP1dB, and IIP2 vs. V_{ADJ}, f_{LO} = 3600 MHz

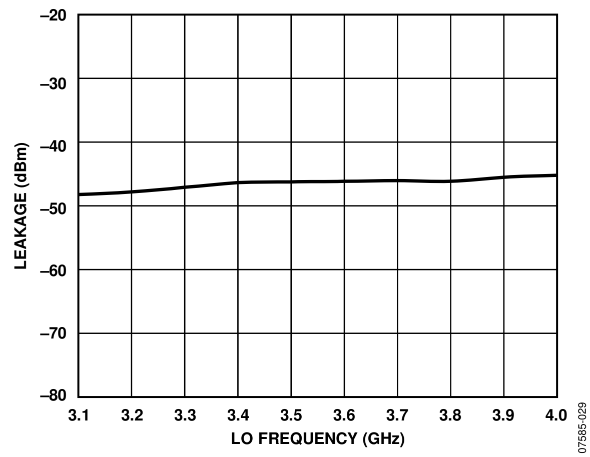


Figure 29. LO-to-RF Leakage vs. LO Frequency

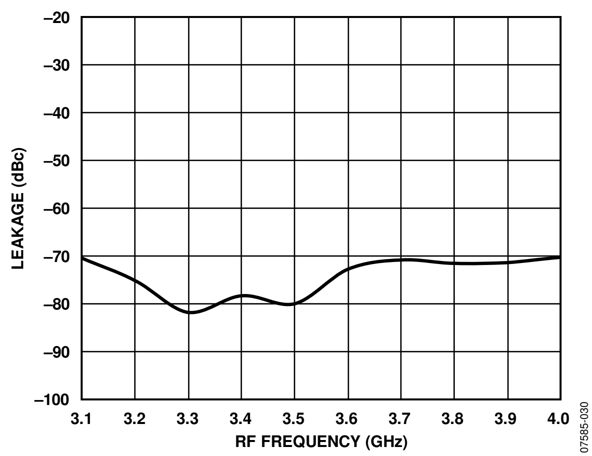


Figure 30. RF-to-LO Leakage vs. RF Frequency

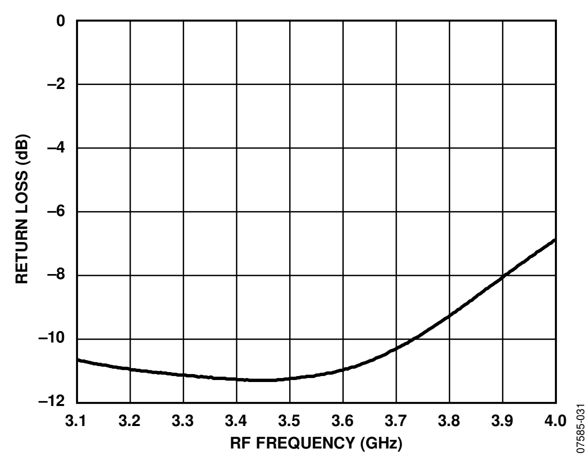


Figure 31. RF Port Return Loss vs. RF Frequency Measured on Characterization Board Through Johanson Technology 3600 Balun

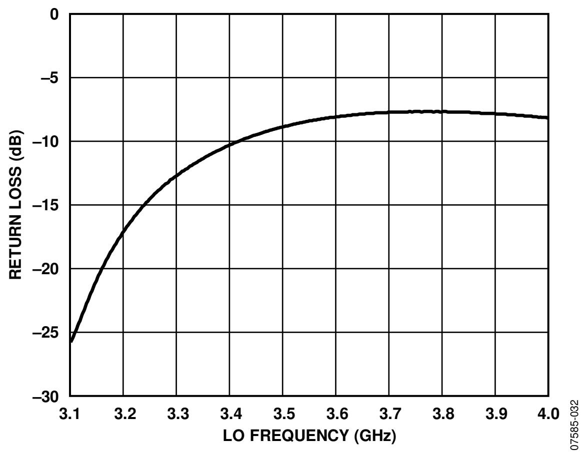


Figure 32. LO Port Return Loss vs. LO Frequency Measured on Characterization Board Through Johanson Technology 3600 Balun

HIGH BAND OPERATION

RF = 5 GHz to 6 GHz; Johanson Technology 5400BL15B050E balun on LO and RF inputs, the ADJ pin is open.

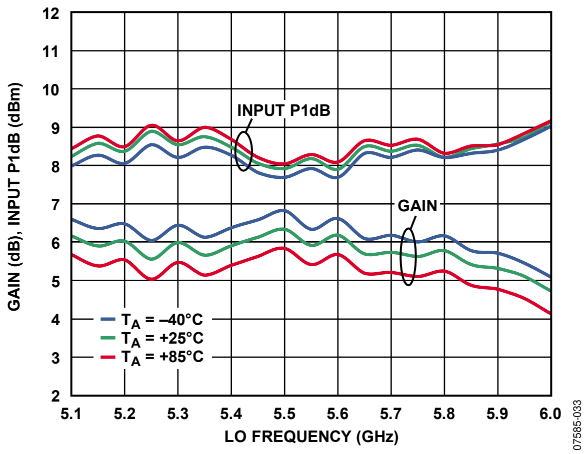


Figure 33. Conversion Gain and Input 1 dB Compression Point (IP1dB) vs. LO Frequency

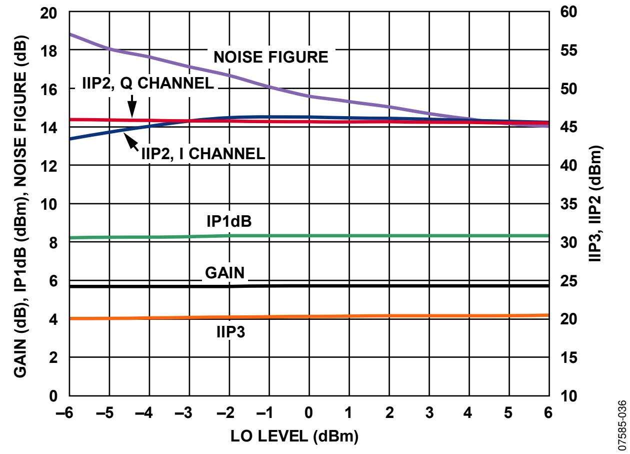


Figure 36. Conversion Gain, IP1dB, Noise Figure, IIP3, and IIP2 vs. LO Level, f_{LO} = 5800 MHz

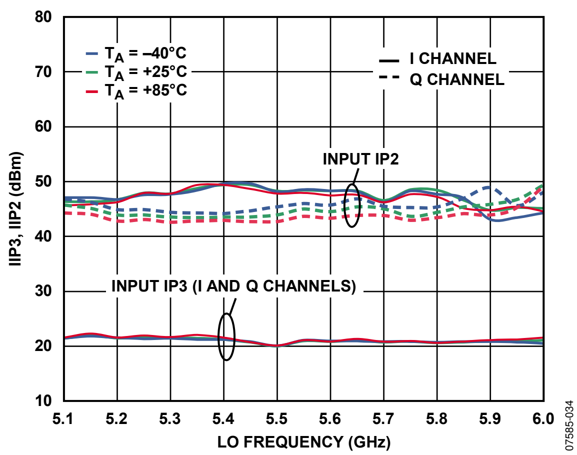


Figure 34. Input Third-Order Intercept (IIP3) and Input Second-Order Intercept Point (IIP2) vs. LO Frequency

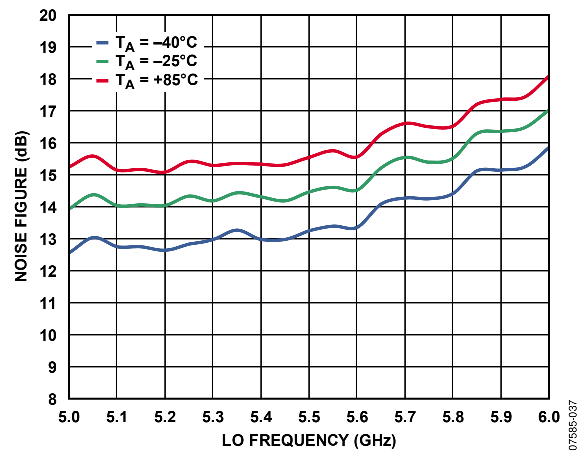


Figure 37. Noise Figure vs. LO Frequency

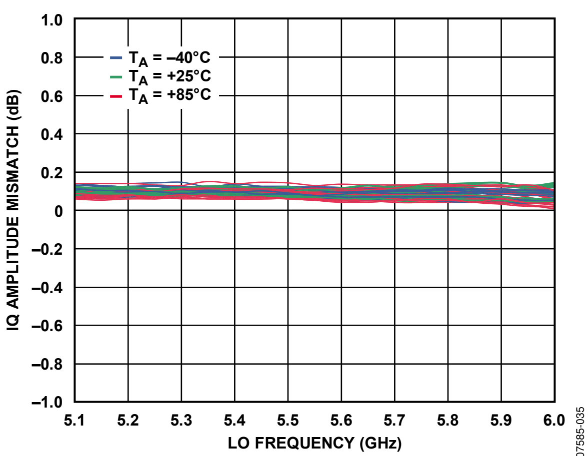


Figure 35. IQ Gain Mismatch vs. LO Frequency

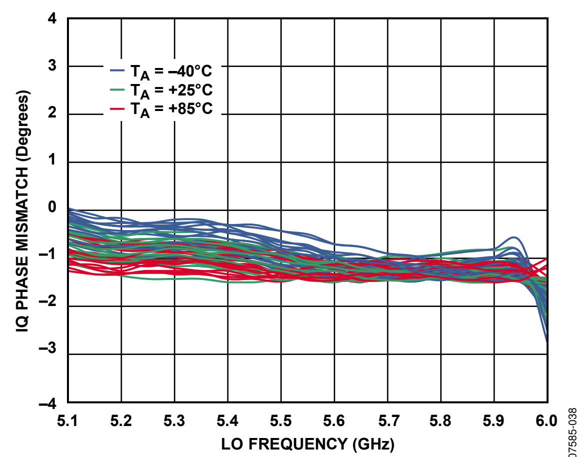


Figure 38. IQ Quadrature Phase Error vs. LO Frequency

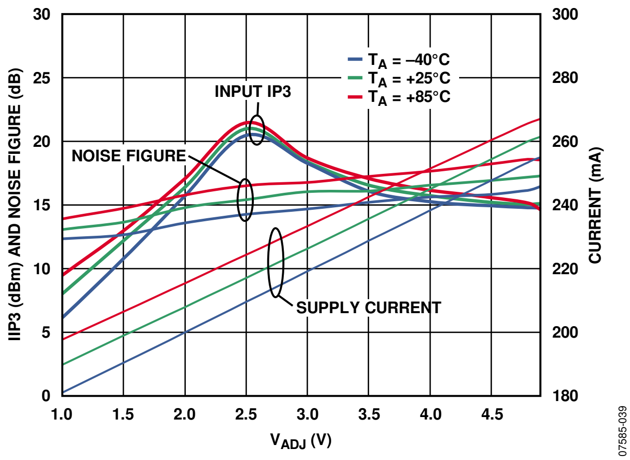


Figure 39. IIP3, Noise Figure, and Supply Current vs. V_{ADJ}, f_{LO} = 5800 MHz

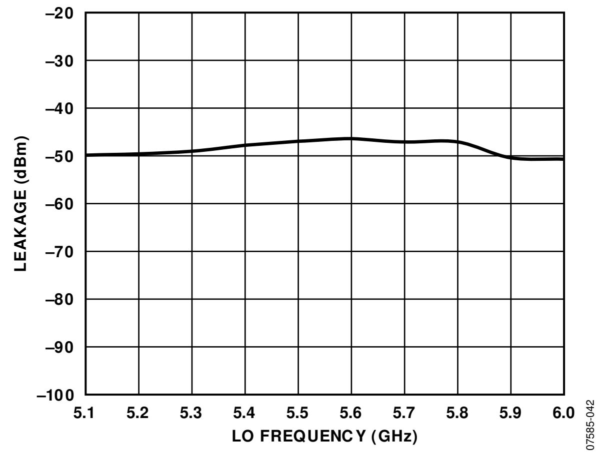


Figure 42. LO-to-RF Leakage vs. LO Frequency

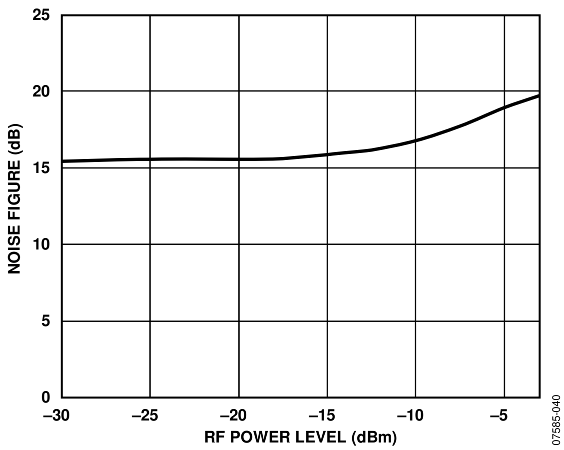


Figure 40. Noise Figure vs. Input Blocker Level, f_{LO} = 5800 MHz (RF Blocker 5 MHz Offset)

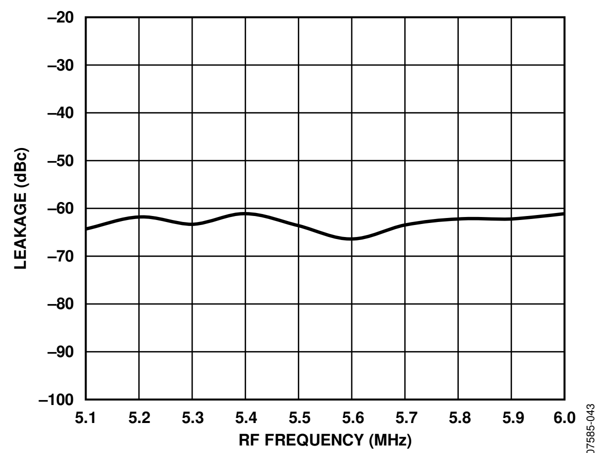


Figure 43. RF-to-LO Leakage vs. RF Frequency

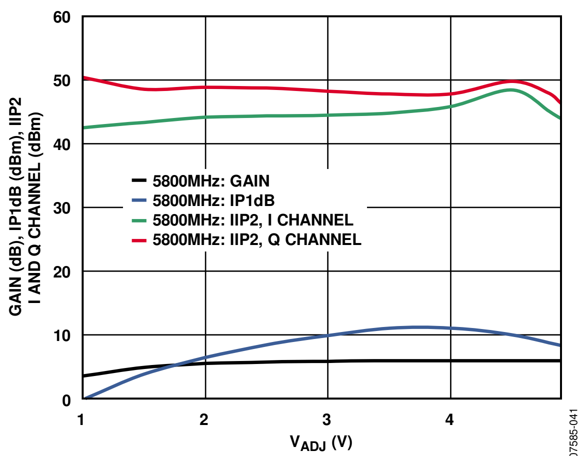


Figure 41. Conversion Gain, IP1dB, and IIP2 vs. R_{BIAS}, f_{LO} = 5800 MHz

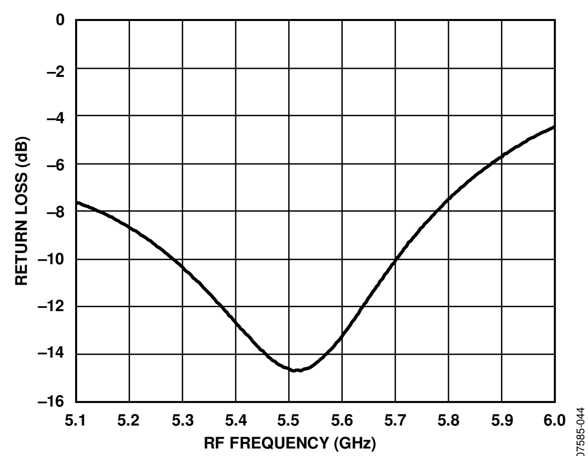


Figure 44. RF Port Return Loss vs. RF Frequency Measured on Characterization Board Through Johanson Technology 5400 Balun

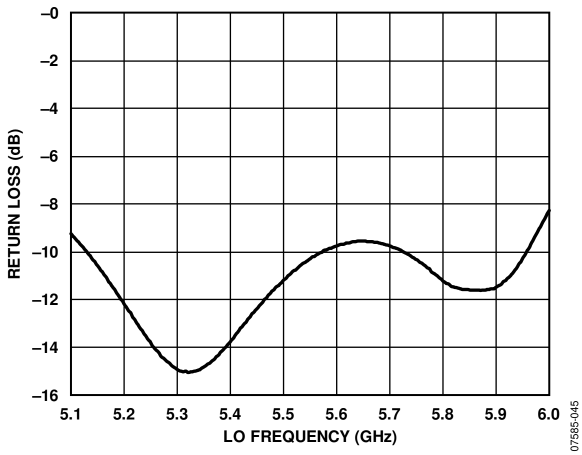


Figure 45. LO Port Return Loss vs. LO Frequency Measured on Characterization Board Through Johanson Technology 5400 Balun

DISTRIBUTIONS FOR f_{LO} = 900 MHz

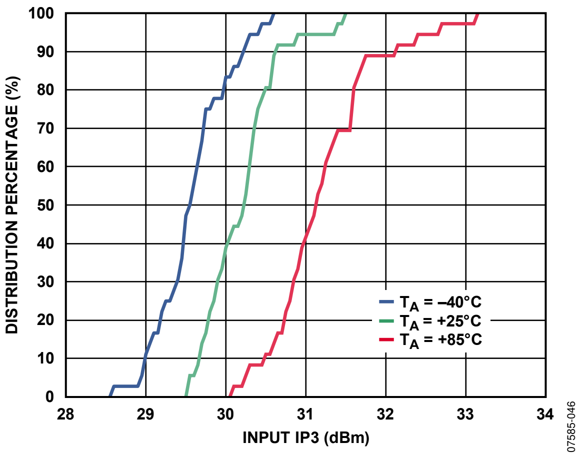


Figure 46. IIP3 Distributions

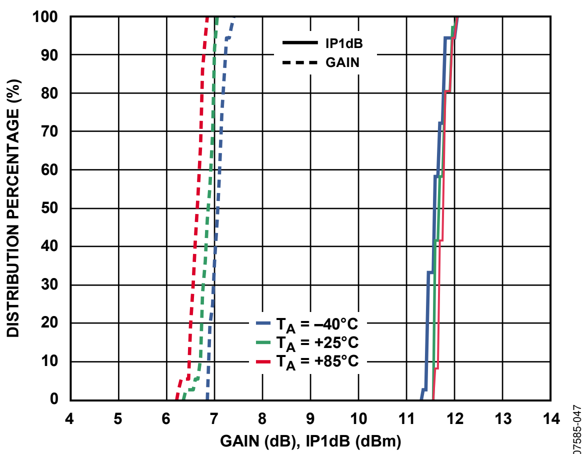


Figure 47. Gain and IP1dB Distributions

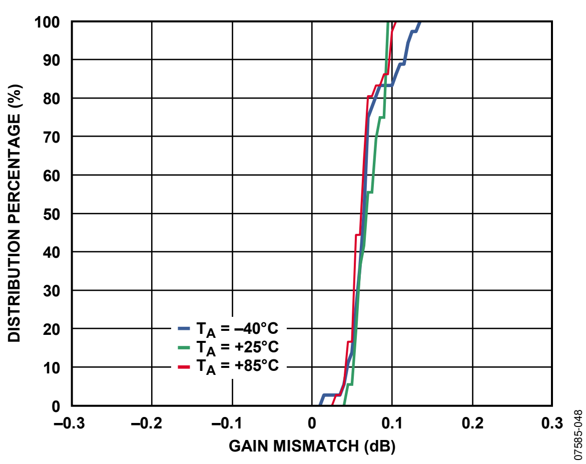


Figure 48. IQ Gain Mismatch Distributions

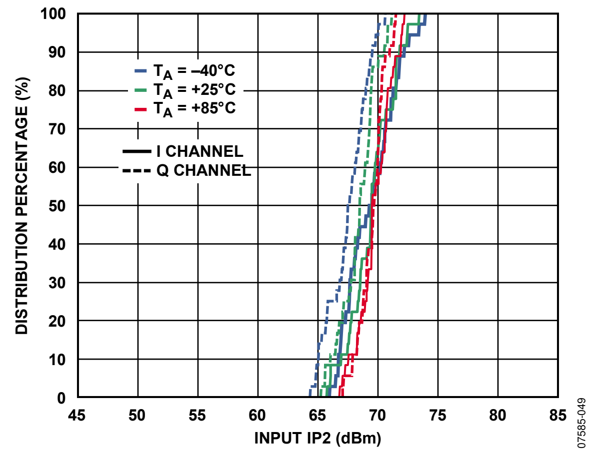


Figure 49. IIP2 Distributions for I Channel and Q Channel

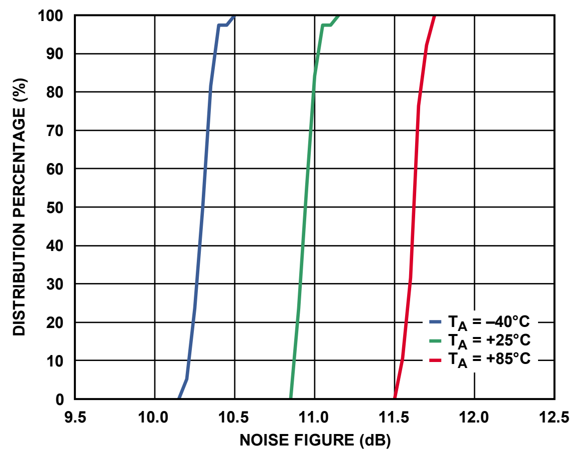


Figure 50. Noise Figure Distributions

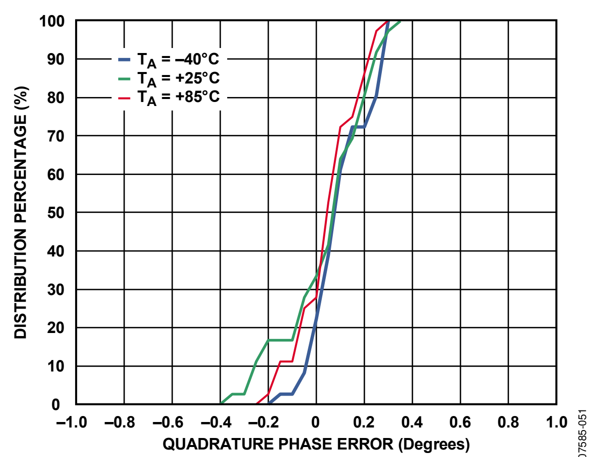


Figure 51. IQ Quadrature Phase Error Distributions

DISTRIBUTIONS FOR f_{LO} = 1900 MHz

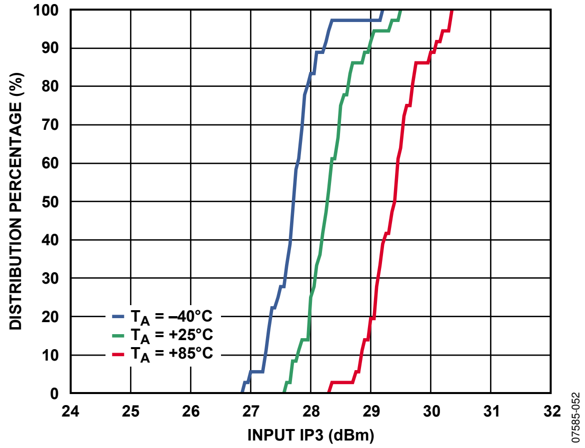


Figure 52. IIP3 Distributions

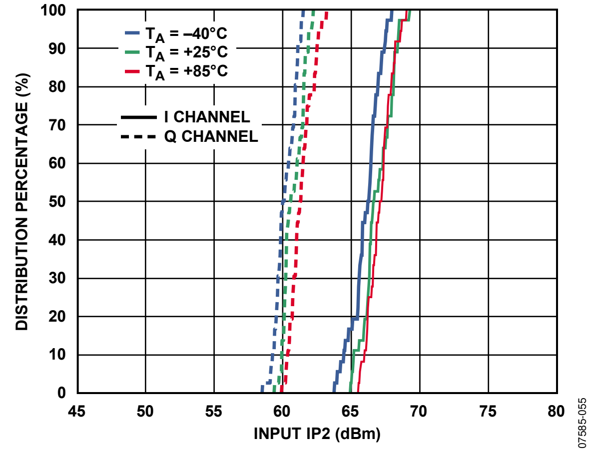


Figure 55. IIP2 Distributions for I Channel and Q Channel

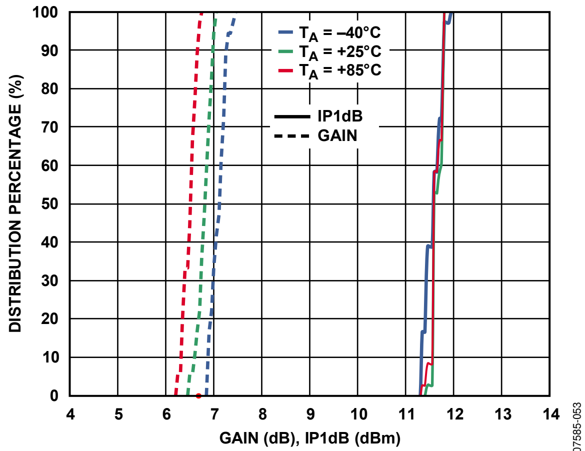


Figure 53. Gain and IP1dB Distributions

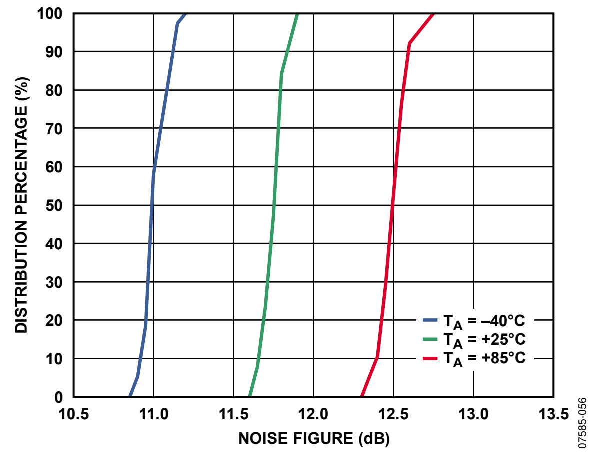


Figure 56. Noise Figure Distributions

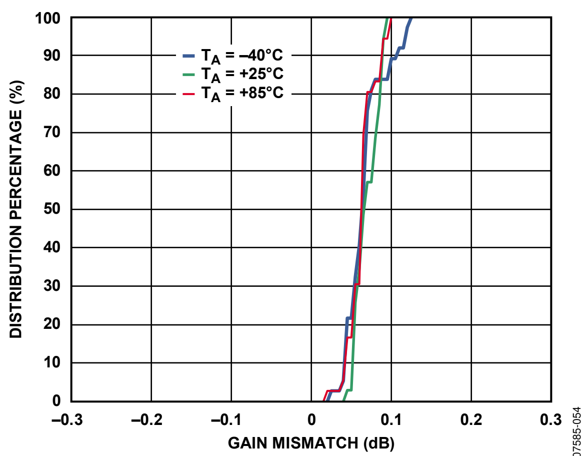


Figure 54. IQ Gain Mismatch Distributions

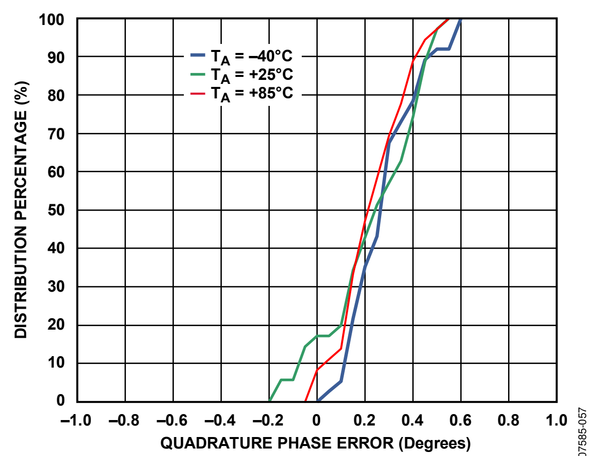


Figure 57. IQ Quadrature Phase Error Distributions

DISTRIBUTIONS FOR f_{LO} = 2700 MHz

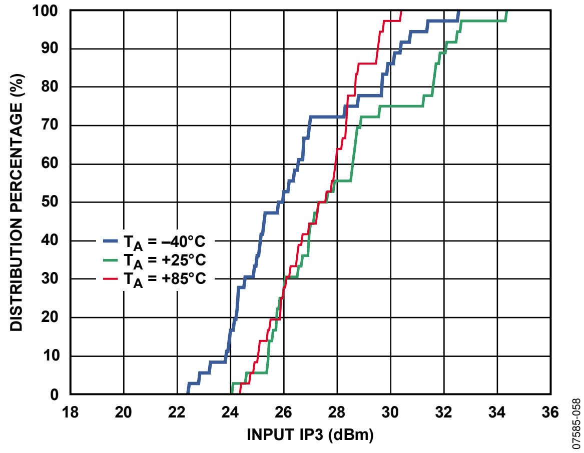


Figure 58. IIP3 Distributions

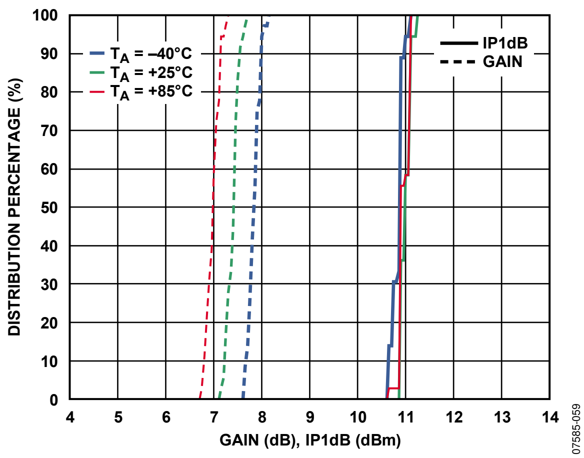


Figure 59. Gain and IP1dB Distributions

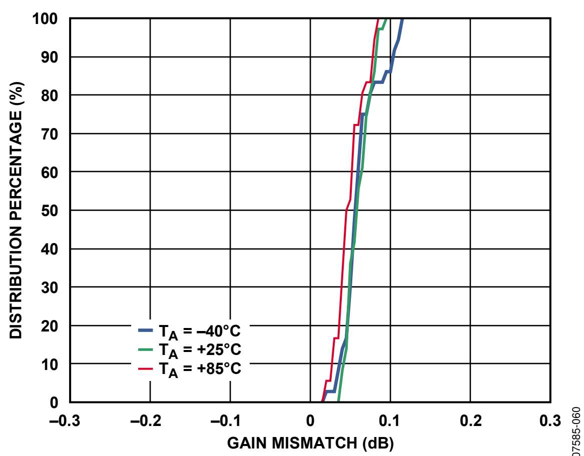


Figure 60. IQ Gain Mismatch Distributions

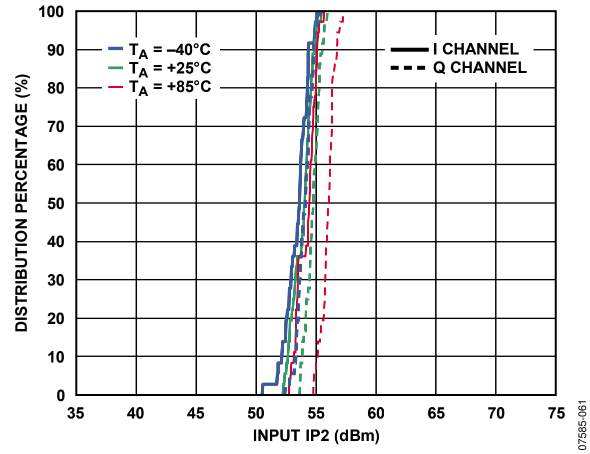


Figure 61. IIP2 Distributions for I Channel and Q Channel

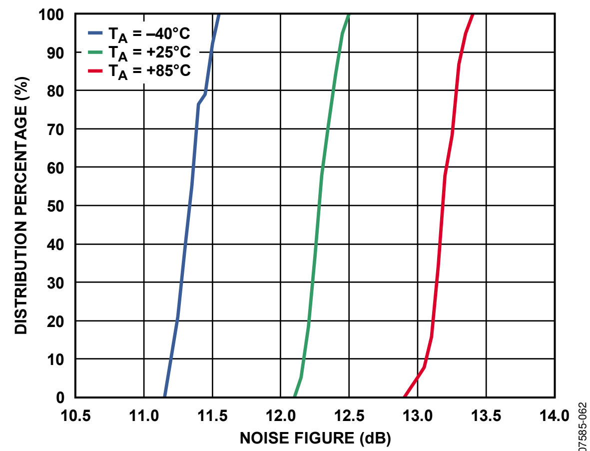


Figure 62. Noise Figure Distributions

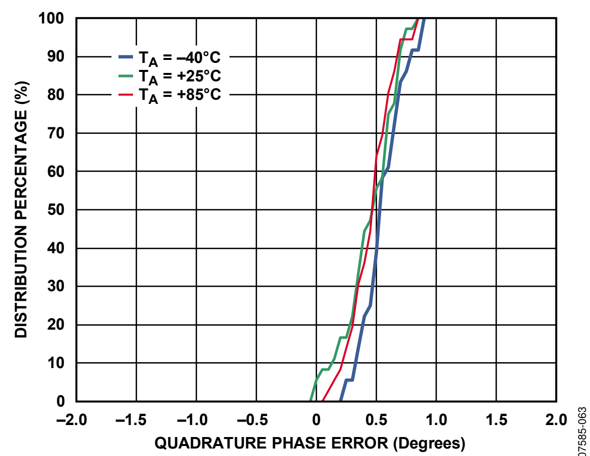


Figure 63. IQ Quadrature Phase Error Distributions

DISTRIBUTIONS FOR f_{LO} = 3600 MHz

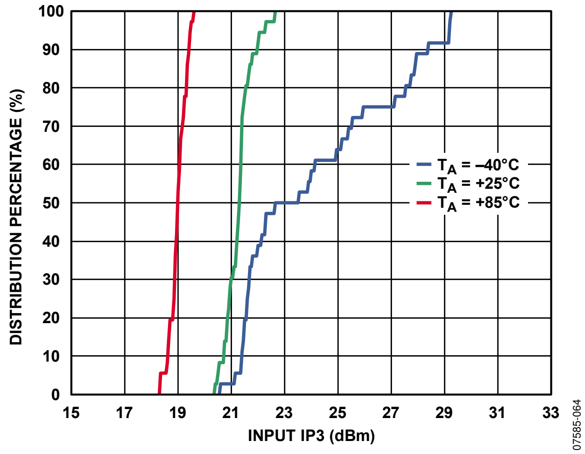


Figure 64. IIP3 Distributions

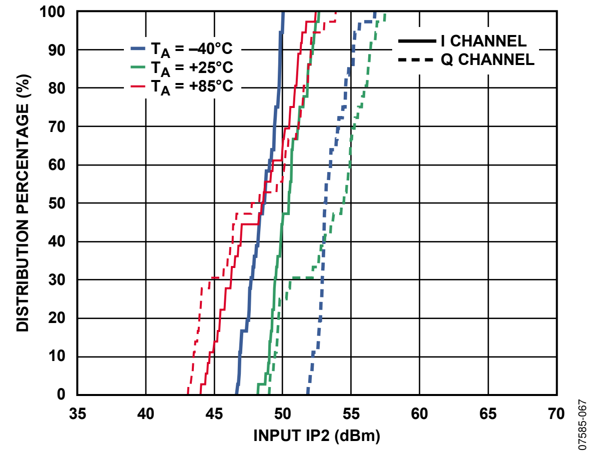


Figure 67. IIP2 Distributions for I Channel and Q Channel

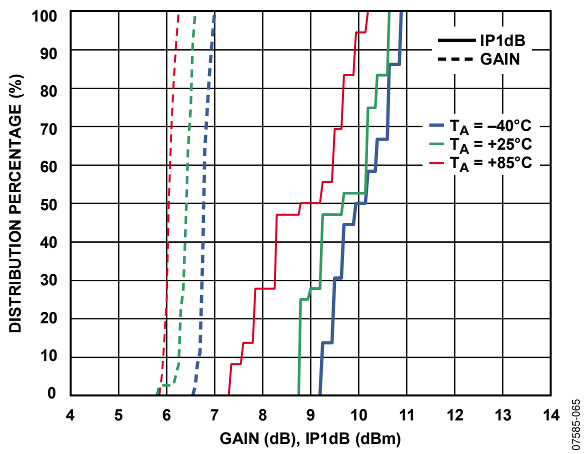


Figure 65. Gain and IP1dB Distributions

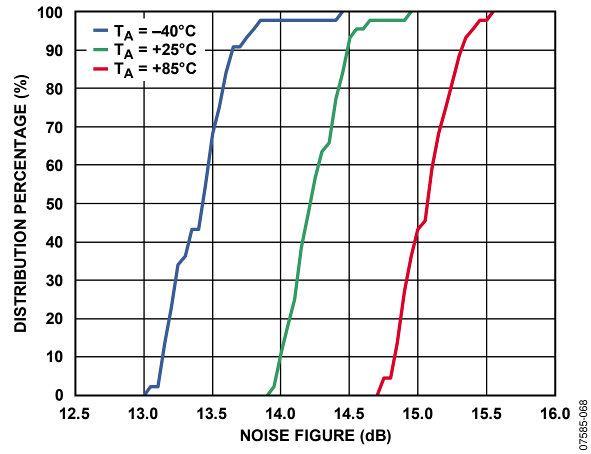


Figure 68. Noise Figure Distributions

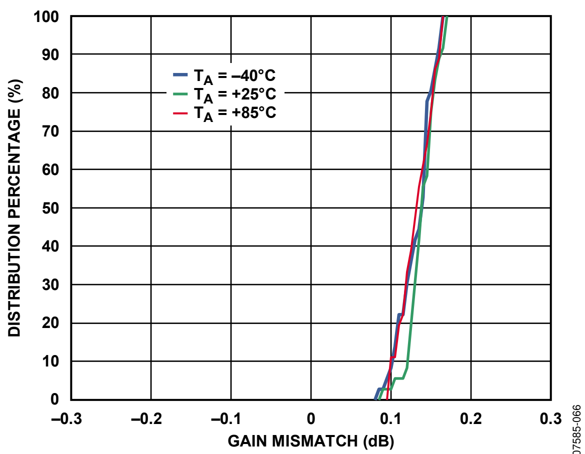


Figure 66. IQ Gain Mismatch Distributions

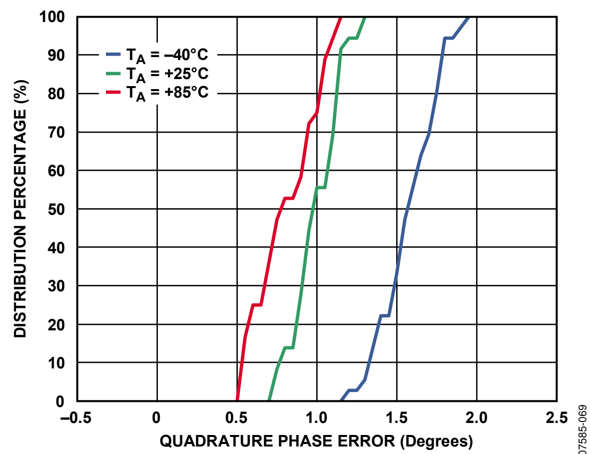


Figure 69. IQ Quadrature Phase Error Distributions

DISTRIBUTIONS FOR f_{LO} = 5800 MHz

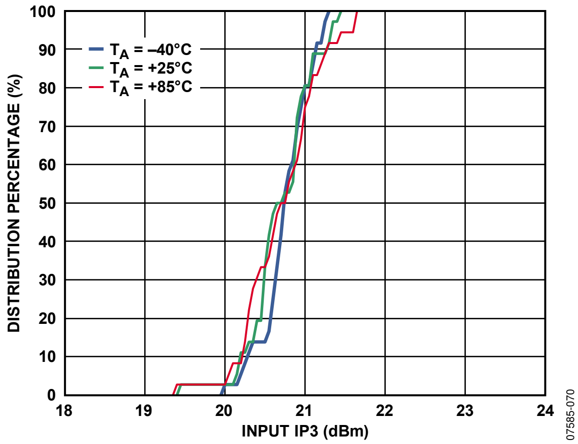


Figure 70. IIP3 Distributions

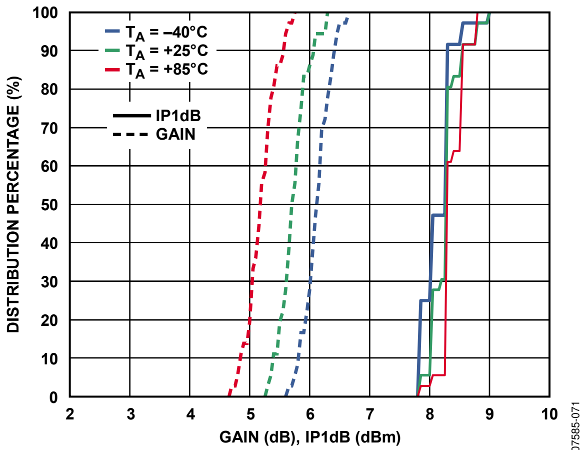


Figure 71. Gain and IP1dB Distributions

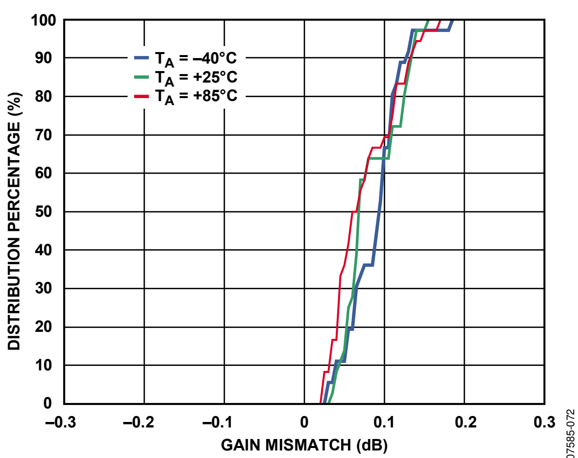


Figure 72. IQ Gain Mismatch Distributions

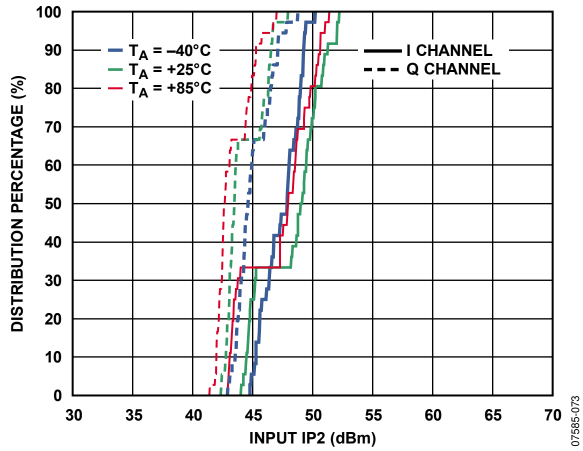


Figure 73. IIP2 Distributions for I Channel and Q Channel

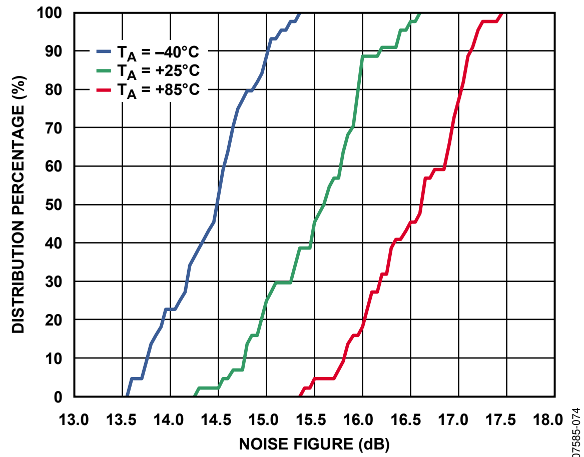


Figure 74. Noise Figure Distributions

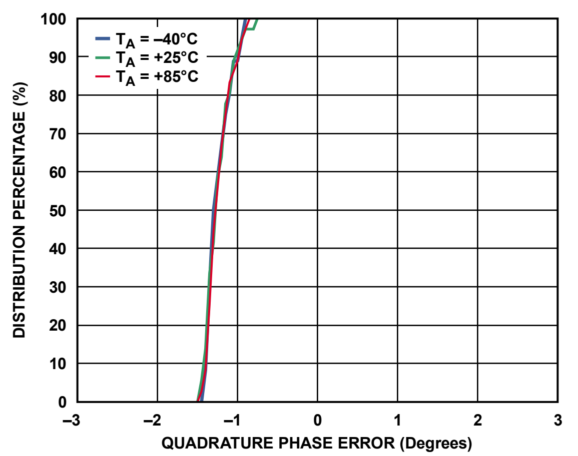


Figure 75. IQ Quadrature Phase Error Distributions

CIRCUIT DESCRIPTION

The ADL5380 can be divided into five sections: the local oscillator (LO) interface, the RF voltage-to-current (V-to-I) converter, the mixers, the differential emitter follower outputs, and the bias circuit. A detailed block diagram of the device is shown in Figure 76.

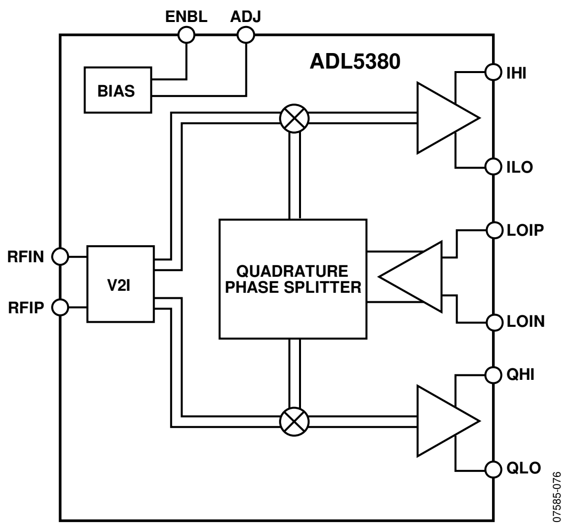


Figure 76. Block Diagram

The LO interface generates two LO signals at 90° of phase difference to drive two mixers in quadrature. RF signals are converted into currents by the V-to-I converters that feed into the two mixers. The differential I and Q outputs of the mixers are buffered via emitter followers. Reference currents to each section are generated by the bias circuit. A detailed description of each section follows.

LO INTERFACE

The LO interface consists of a polyphase quadrature splitter followed by a limiting amplifier. The LO input impedance is set by the polyphase, which splits the LO signal into two differential signals in quadrature. The LO input impedance is nominally 50 Ω. Each quadrature LO signal then passes through a limiting amplifier that provides the mixer with a limited drive signal. For optimal performance, the LO inputs must be driven differentially.

V-TO-I CONVERTER

The differential RF input signal is applied to a V-to-I converter that converts the differential input voltage to output currents. The V-to-I converter provides a differential 50 Ω input impedance. The V-to-I bias current can be adjusted up or down using the ADJ pin (Pin 19). Adjusting the current up improves IIP3 and IP1dB but degrades SSB NF. Adjusting the current down improves SSB NF but degrades IIP3 and IP1dB. The current adjustment can be made by connecting a resistor from the ADJ pin (Pin 19) to V_S to increase the bias current or to ground to decrease the bias current. Table 4 approximately dictates the relationship between the resistor used (R_{ADJ}), the resulting ADJ pin voltage, and the resulting baseband common-mode output voltage.

Table 4. ADJ Pin Resistor Values and Approximate ADJ Pin Voltages

R_{ADJ}	~V_{ADJ} (V)	~ Baseband Common-Mode Output (V)
200 Ω to V_S	4.8	2.2
600 Ω to V_S	4.5	2.3
1.54 kΩ to V_S	4	2.5
3.8 kΩ to V_S	3.5	2.7
10 kΩ to V_S	3	3
Open	2.5	3.2
9 kΩ to GND	2	3.4
3.5 kΩ to GND	1.5	3.6
1.5 kΩ to GND	1	3.8

MIXERS

The ADL5380 has two double-balanced mixers: one for the in-phase channel (I channel) and one for the quadrature channel (Q channel). These mixers are based on the Gilbert cell design of four cross-connected transistors. The output currents from the two mixers are summed together in the resistive loads that then feed into the subsequent emitter follower buffers.

EMITTER FOLLOWER BUFFERS

The output emitter followers drive the differential I and Q signals off chip. The output impedance is set by on-chip 25 Ω series resistors that yield a 50 Ω differential output impedance for each baseband port. The fixed output impedance forms a voltage divider with the load impedance that reduces the effective gain. For example, a 500 Ω differential load has 1 dB lower effective gain than a high (10 kΩ) differential load impedance.

BIAS CIRCUIT

A band gap reference circuit generates the reference currents used by different sections. The bias circuit can be enabled and partially disabled using ENBL (Pin 7). If ENBL is grounded or left open, the part is fully enabled. Pulling ENBL high shuts off certain sections of the bias circuitry, reducing the standing power to about half of its fully enabled consumption and disabling the outputs.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 77 shows the basic connections schematic for the ADL5380.

POWER SUPPLY

The nominal voltage supply for the ADL5380 is 5 V and is applied to the VCC1, VCC2, and VCC3 pins. Connect ground to the GND1, GND2, GND3, and GND4 pins. Solder the exposed paddle on the underside of the package to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, these layers should be stitched together with nine vias under the exposed paddle. The AN-772 Application Note discusses the thermal and electrical grounding of the LFCSP in detail. Decouple each of the supply pins using two capacitors; recommended capacitor values are 100 pF and 0.1 µF.

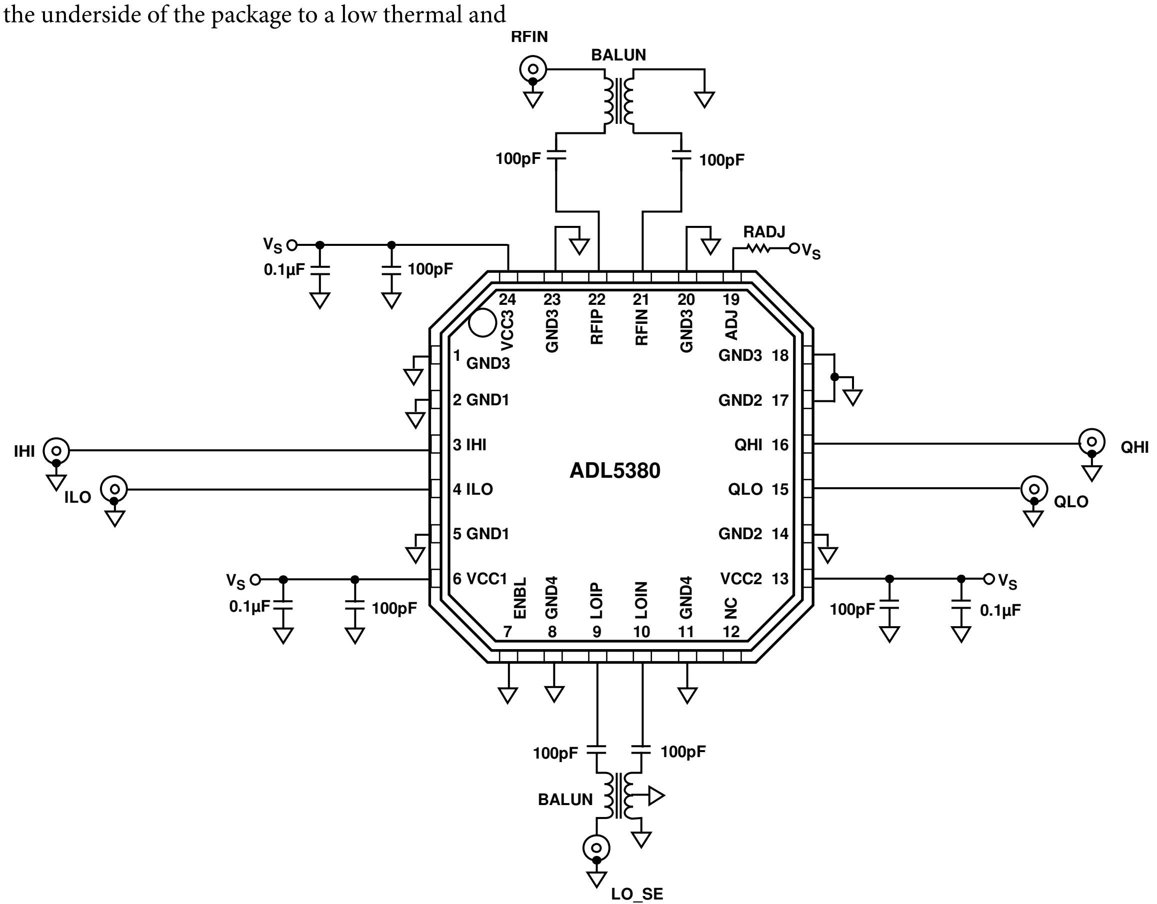


Figure 77. Basic Connections Schematic

LOCAL OSCILLATOR AND RF INPUTS

The RF and LO inputs have a differential input impedance of approximately 50 Ω as shown in Figure 78. Figure 79 shows the return loss. For optimum performance, both the LO and RF ports should be ac-coupled and driven differentially through a balun as shown in Figure 80 and Figure 81. The user has many different types of balun to choose from and from a variety of manufacturers. For the data presented in this data sheet all measurements were gathered with the baluns listed below. For applications that are band specific, the recommended baluns are:

- Up to 3 GHz is the Mini-Circuits TC1-1-13.
- From 3 GHz to 4 GHz is the Johanson Technology 3600BL14M050.
- From 4.9 GHz to 6 GHz is the Johanson Technology 5400BL15B050.

For wideband applications covering the entire 400 MHz to 6 GHz range of the ADL5380, the recommended balun is the TCM1-63AX+ from Mini-Circuits. This wide and maximally flat balun allows coverage of the entire frequency range with one component.

The recommended drive level for the LO port is between −6 dBm and +6 dBm.

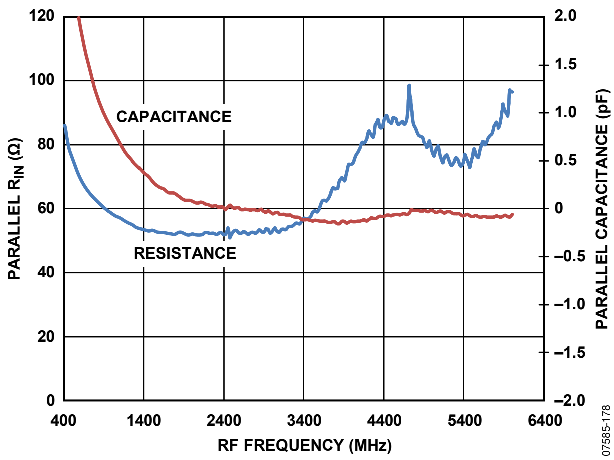


Figure 78. Differential Input Impedance of the RF Port

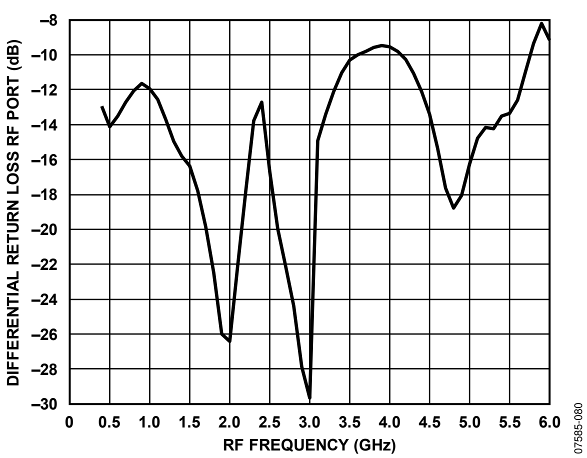


Figure 79. Differential RF Port Return Loss

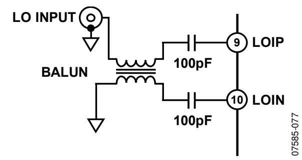


Figure 80. Differential LO Drive

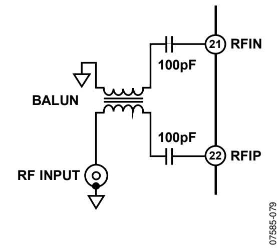


Figure 81. RF Input

Alternatively, if the single-ended drive of both the LO and RF ports is the desired mode of operation, degradations in IIP2 will be observed because of the lack of common mode rejection. The degradation in IIP2 is more prevalent at high frequencies, specifically frequencies greater than 1600 MHz. At low frequencies, the ADL5380 has inherent common mode rejection offering superior IIP2 performance in the 70 dBm range. As shown in Figure 82 and Figure 83, in single-ended mode, the largest performance impact is seen in IIP2 while minimal performance degradation is observed in IIP3.

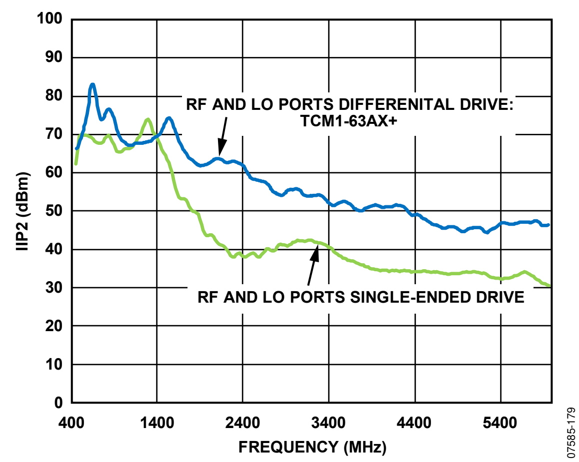


Figure 82. IIP2 vs. Frequency Comparison for Single-Ended and Differential Drive of the RF and LO Ports