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FEATURES

- Output frequency range: 50 MHz to 2200 MHz
- 1 dB output compression: 11 dBm @ 350 MHz
- Noise floor: -160 dBm/Hz @ 350 MHz
- Sideband suppression: -46 dBc @ 350 MHz
- Carrier feedthrough: -38 dBm @ 350 MHz
- 30 dB of linear AGC dynamic range @ 350 MHz
- Single supply: 4.75 V to 5.5 V
- 40-lead, Pb-free LFCSP_VQ with exposed paddle

APPLICATIONS

- Radio-link infrastructures
- Cable modem termination systems
- Wireless/cellular infrastructure systems
- Wireless local loops
- WiMAX/broadband wireless access systems

GENERAL DESCRIPTION

The ADL5386 is a quadrature modulator with unmatched integration levels for low intermediate frequency (IF) and radio frequency (RF) transmitters within broadband wireless access systems, microwave radio links, cable modem termination systems, and cellular infrastructure equipment. The ADL5386 operates over a frequency range of 50 MHz to 2200 MHz. Its excellent phase accuracy and amplitude balance supports high data rate, complex modulation for next-generation communication infrastructure equipment.

In addition, the ADL5386 incorporates a standalone logarithmic power detector, as well as a voltage variable attenuator (VVA). The attenuator has its own separate input and output pins for easy cascading with filters and buffer amplifiers. The wide dynamic range of the power detector and VVA provides flexibility in the choice of the signal monitoring point in the transmitter system.

The wide baseband input bandwidth of 700 MHz allows for either baseband drive or a drive from a complex IF signal. Typical applications are in IF or direct-to-RF radio-link transmitters, cable modem termination systems, broadband wireless access systems, and cellular infrastructure equipment.

The ADL5386 takes signals from two differential baseband inputs and modulates them onto two carriers in quadrature with each other. The two internal carriers are derived from a single-ended, external local oscillator (LO) input signal at twice the frequency as the desired output. The output amplifier is designed to drive a 50 Ω load.

The ADL5386 consists of two die, one fabricated using the Analog Devices, Inc., advanced SiGe bipolar process, and the other using an external GaAs process. The ADL5386 is packaged in a 40-lead, Pb-free LFCSP_VQ with an exposed paddle. Performance is specified over the -40°C to +85°C range. A Pb-free evaluation board is also available.

FUNCTIONAL BLOCK DIAGRAM

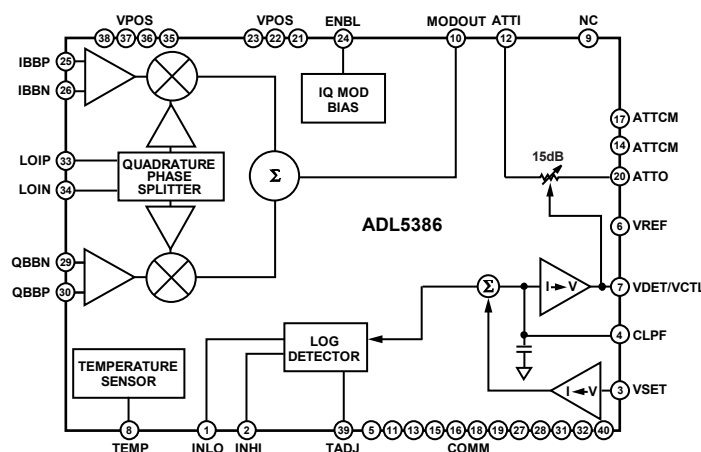


Figure 1.

Rev. 0

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ADL5386* PRODUCT PAGE QUICK LINKS

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADL5386 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1237: Precise Control of I/Q Modulator Output Power Using the ADL5386 Quadrature Modulator and the AD5621 12-Bit DAC

Data Sheet

- ADL5386: 50-2200 MHz Quadrature Modulator w/ Integrated Detector & VVA Data Sheet

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- ADL5386 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADL5386 EngineerZone Discussions.

SAMPLE AND BUY

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REVISION HISTORY**1/09—Revision 0: Initial Version**

SPECIFICATIONS

Unless otherwise noted, $V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $LO = -7\text{ dBm}$, I/Q inputs = 1.4 V p-p differential sine waves in quadrature on a 500 mV dc bias, baseband frequency = 1 MHz, LO source and RF output load impedances are 50 Ω .

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
MODULATOR DYNAMIC CHARACTERISTICS					
Operating Frequency Range		50		2200	MHz
External LO Frequency Range	External LO frequency is twice output frequency	100		4400	MHz
Output Frequency = 50 MHz					
Output Power	Single (lower) sideband output		5.6		dBm
Modulator Voltage Gain			-1.3		dB
Output P1dB			10.8		dBm
Output Return Loss			-21		dB
Carrier Leakage	Unadjusted (nominal drive level)		-43		dBm
	At 85°C after optimization at 25°C		-63		dBm
	At -40°C after optimization at +25°C		-63		dBm
Sideband Suppression	Unadjusted (nominal drive level)		-48		dBc
	At 85°C after optimization at 25°C		-60		dBc
	At -40°C after optimization at +25°C		-60		dBc
Quadrature Error			-0.2		Degrees
I/Q Amplitude Balance			0.05		dB
Second Harmonic	$(f_{LO} - (2 \times f_{BB}))$, $P_{OUT} = 5\text{ dBm}$		-80		dBc
Third Harmonic	$(f_{LO} + (3 \times f_{BB}))$, $P_{OUT} = 5\text{ dBm}$		-58		dBc
Output IP2	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3\text{ dBm}$ per tone		76		dBm
Output IP3	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3\text{ dBm}$ per tone		26		dBm
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		-159		dBm/Hz
Output Frequency = 140 MHz					
Output Power	Single (lower) sideband output		5.7		dBm
Modulator Voltage Gain			-1.2		dB
Output P1dB			11.1		dBm
Output Return Loss			-21		dB
Carrier Leakage	Unadjusted (nominal drive level)		-42		dBm
	At 85°C after optimization at 25°C		-62		dBm
	At -40°C after optimization at +25°C		-62		dBm
Sideband Suppression	Unadjusted (nominal drive level)		-57		dBc
	At 85°C after optimization at 25°C		-60		dBc
	At -40°C after optimization at +25°C		-60		dBc
Quadrature Error			-0.2		Degrees
I/Q Amplitude Balance			0.05		dB
Second Harmonic	$(f_{LO} - (2 \times f_{BB}))$, $P_{OUT} = 5\text{ dBm}$		-79		dBc
Third Harmonic	$(f_{LO} + (3 \times f_{BB}))$, $P_{OUT} = 5\text{ dBm}$		-56		dBc
Output IP2	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3\text{ dBm}$ per tone		75		dBm
Output IP3	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3\text{ dBm}$ per tone		25		dBm
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		-160		dBm/Hz
Output Frequency = 350 MHz					
Output Power	Single (lower) sideband output	4	5.5	7	dBm
Modulator Voltage Gain			-1.4		dB
Output P1dB			11.1		dBm
Output Return Loss			-19		dB
Carrier Leakage	Unadjusted (nominal drive level)		-38		dBm
	At 85°C after optimization at 25°C		-58		dBm
	At -40°C after optimization at +25°C		-58		dBm

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Parameter	Conditions	Min	Typ	Max	Unit
Sideband Suppression	Unadjusted (nominal drive level)		-46		dBc
	At 85°C after optimization at 25°C		-57		dBc
	At -40°C after optimization at +25°C		-57		dBc
Quadrature Error			-0.5		Degrees
I/Q Amplitude Balance			0.05		dB
Second Harmonic	$(f_{LO} - (2 \times f_{BB}))$, $P_{OUT} = 5$ dBm		-76		dBc
Third Harmonic	$(f_{LO} + (3 \times f_{BB}))$, $P_{OUT} = 5$ dBm		-53		dBc
Output IP2	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3$ dBm per tone		74		dBm
Output IP3	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3$ dBm per tone		25		dBm
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		-160		dBm/Hz
	20 MHz offset from LO, output power = -5 dBm		-156		dBm/Hz
Output Frequency = 860 MHz					
Output Power	Single (lower) sideband output	3.8	5.3	6.8	dBm
Modulator Voltage Gain			-1.6		dB
Output P1dB			11.4		dBm
Output Return Loss			-15		dB
Carrier Leakage			-37		dBm
Sideband Suppression	Unadjusted (nominal drive level)		-37		dBm
	At 85°C after optimization at 25°C		-56		dBm
	At -40°C after optimization at +25°C		-56		dBm
Sideband Suppression	Unadjusted (nominal drive level)		-39		dBc
	At 85°C after optimization at 25°C		-55		dBc
	At -40°C after optimization at +25°C		-55		dBc
Quadrature Error			-0.9		Degrees
I/Q Amplitude Balance			0.05		dB
Second Harmonic	$(f_{LO} - (2 \times f_{BB}))$, $P_{OUT} = 5$ dBm		-72		dBc
Third Harmonic	$(f_{LO} + (3 \times f_{BB}))$, $P_{OUT} = 5$ dBm		-49		dBc
Output IP2	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3$ dBm per tone		73		dBm
Output IP3	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3$ dBm per tone		25		dBm
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		-160		dBm/Hz
	20 MHz offset from LO, output power = -5 dBm		-157		dBm/Hz
Output Frequency = 1450 MHz					
Output Power	Single (lower) sideband output		4.3		dBm
Modulator Voltage Gain			-2.6		dB
Output P1dB			10.6		dBm
Output Return Loss			-15		dB
Carrier Leakage			-35		dBm
Sideband Suppression	Unadjusted (nominal drive level)		-35		dBm
	At 85°C after optimization at 25°C		-50		dBm
	At -40°C after optimization at +25°C		-50		dBm
Sideband Suppression	Unadjusted (nominal drive level)		-43		dBc
	At 85°C after optimization at 25°C		-45		dBc
	At -40°C after optimization at +25°C		-45		dBc
Quadrature Error			-0.2		Degrees
I/Q Amplitude Balance			0.03		dB
Second Harmonic	$(f_{LO} - (2 \times f_{BB}))$, $P_{OUT} = 5$ dBm		-67		dBc
Third Harmonic	$(f_{LO} + (3 \times f_{BB}))$, $P_{OUT} = 5$ dBm		-45		dBc
Output IP2	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3$ dBm per tone		63		dBm
Output IP3	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3$ dBm per tone		25		dBm
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		-160		dBm/Hz

Parameter	Conditions	Min	Typ	Max	Unit
Output Frequency = 1900 MHz					
Output Power	Single (lower) sideband output		3.2		dBm
Modulator Voltage Gain			-3.7		dB
Output P1dB			9.2		dBm
Output Return Loss			-13		dBm
Carrier Leakage	Unadjusted (nominal drive level)		-35		dBm
	At 85°C after optimization at 25°C		-53		dBm
	At -40°C after optimization at +25°C		-53		dBm
Sideband Suppression	Unadjusted (nominal drive level)		-30		dBc
	At 85°C after optimization at 25°C		-45		dBc
	At -40°C after optimization at +25°C		-45		dBc
Quadrature Error			-3		Degrees
I/Q Amplitude Balance			0.02		dB
Second Harmonic	$(f_{LO} - (2 \times f_{BB}))$, $P_{OUT} = 5$ dBm		-59		dBc
Third Harmonic	$(f_{LO} + (3 \times f_{BB}))$, $P_{OUT} = 5$ dBm		-45		dBc
Output IP2	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3$ dBm per tone		55		dBm
Output IP3	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3$ dBm per tone		23		dBm
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		-160		dBm/Hz
	20 MHz offset from LO, output power = -5 dBm		-156		dBm/Hz
Output Frequency = 2150 MHz					
Output Power	Single (lower) sideband output		2.5		dBm
Modulator Voltage Gain			-4.4		dB
Output P1dB			8.4		dBm
Output Return Loss			-11		dB
Carrier Leakage	Unadjusted (nominal drive level)		-35		dBm
	At 85°C after optimization at 25°C		-48		dBm
	At -40°C after optimization at +25°C		-46		dBm
Sideband Suppression	Unadjusted (nominal drive level)		-34		dBc
	At 85°C after optimization at 25°C		-45		dBc
	At -40°C after optimization at +25°C		-45		dBc
Quadrature Error			-1.2		Degrees
I/Q Amplitude Balance			0.03		dB
Second Harmonic	$(f_{LO} - (2 \times f_{BB}))$, $P_{OUT} = 5$ dBm		-56		dBc
Third Harmonic	$(f_{LO} + (3 \times f_{BB}))$, $P_{OUT} = 5$ dBm		-48		dBc
Output IP2	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3$ dBm per tone		53		dBm
Output IP3	F1 = 3.5 MHz, F2 = 4.5 MHz, $P_{OUT} = -3$ dBm per tone		21		dBm
Noise Floor	20 MHz offset from LO, all BB inputs at a bias of 500 mV		-160		dBm/Hz
	20 MHz offset from LO, output power = -5 dBm		-155		dBm/Hz
LO Inputs	Pin LOIP and Pin LOIN				
LO Drive Level	Characterization performed at typical level	-13	-7	+2	dBm
	Characterization performed at typical level (<140 MHz)	-7	-7	+2	dBm
Input Impedance			50		Ω
Input Return Loss	350 MHz, LOIN ac-coupled to ground		-7		dB
Baseband Inputs	Pin IBBP, Pin IBBN, Pin QBBP, Pin QBBN				
I and Q Input Bias Level			500		mV
Input Bias Current			-60		μ A
Bandwidth (0.1 dB)	$f_{LO} = 2 \times 900$ MHz, $P_{OUT} \approx -4$ dBm		50		MHz
Bandwidth (3 dB)	$f_{LO} = 2 \times 900$ MHz, $P_{OUT} \approx -4$ dBm		700		MHz

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Parameter	Conditions	Min	Typ	Max	Unit
VOLTAGE VARIABLE ATTENUATOR					
Pin VCTL, Pin ATTI, and Pin ATTO, open-loop mode, attenuation control applied to VCTL					
Output Frequency = 50 MHz					
Insertion Loss	Minimum attenuation, $V_{VCTL} = 2\text{ V}$		1.7		dB
Attenuation Range	Attenuation at $V_{VCTL} = 2\text{ V}$ – Attenuation at $V_{VCTL} = 0\text{ V}$		37.8		dB
Return Loss			17		dB
Input IP3	Minimum attenuation, $V_{VCTL} = 2\text{ V}$, $\Delta f = 1\text{ MHz}$, input power = -3 dBm per tone		36		dBm
Output Frequency = 140 MHz					
Insertion Loss	Minimum attenuation, $V_{VCTL} = 2\text{ V}$		1.9		dB
Attenuation Range	Attenuation at $V_{VCTL} = 2\text{ V}$ – Attenuation at $V_{VCTL} = 0\text{ V}$		37		dB
Return Loss			17		dB
Input IP3	Minimum attenuation, $V_{VCTL} = 2\text{ V}$, $\Delta f = 1\text{ MHz}$, input power = -3 dBm per tone		36		dBm
Output Frequency = 350 MHz					
Insertion Loss	Minimum attenuation, $V_{VCTL} = 2\text{ V}$		2.2		dB
Attenuation Range	Attenuation at $V_{VCTL} = 2\text{ V}$ – Attenuation at $V_{VCTL} = 0\text{ V}$		26.2		dB
Return Loss			17		dB
Input IP3	Minimum attenuation, $V_{VCTL} = 2\text{ V}$, $\Delta f = 1\text{ MHz}$, input power = -3 dBm per tone		35		dBm
Output Frequency = 860 MHz					
Insertion Loss	Minimum attenuation, $V_{VCTL} = 2\text{ V}$		2.5		dB
Attenuation Range	Attenuation at $V_{VCTL} = 2\text{ V}$ – Attenuation at $V_{VCTL} = 0\text{ V}$		21		dB
Return Loss			14		dB
Input IP3	Minimum attenuation, $V_{VCTL} = 2\text{ V}$, $\Delta f = 1\text{ MHz}$, input power = -3 dBm per tone		35		dBm
Output Frequency = 1900 MHz					
Insertion Loss	Minimum attenuation, $V_{VCTL} = 2\text{ V}$		3		dB
Attenuation Range	Attenuation at $V_{VCTL} = 2\text{ V}$ – Attenuation at $V_{VCTL} = 0\text{ V}$		19		dB
Return Loss			13		dB
Input IP3	Minimum attenuation, $V_{VCTL} = 2\text{ V}$, $\Delta f = 1\text{ MHz}$, input power = -3 dBm per tone		36		dBm
Output Frequency = 2150 MHz					
Insertion Loss	Minimum attenuation, $V_{VCTL} = 2\text{ V}$		3.3		dB
Attenuation Range	Attenuation at $V_{VCTL} = 2\text{ V}$ – Attenuation at $V_{VCTL} = 0\text{ V}$		17		dB
Return Loss			13		dB
Input IP3	Minimum attenuation, $V_{VCTL} = 2\text{ V}$, $\Delta f = 1\text{ MHz}$, input power = -3 dBm per tone		35		dBm
SWITCHING CHARACTERISTICS					
VCTL Response Time	ATTCM (Pin 14 and Pin 17) = 1000 pF				
	Frequency = 350 MHz, $V_{VCTL} = 2\text{ V}$ to 0 V; measured from 50 % of V_{VCTL} to 10% of RF envelope		125		ns
	Frequency = 350 MHz, $V_{VCTL} = 0\text{ V}$ to 2 V; measured from 50 % of V_{VCTL} to 90% of RF envelope		15		ns
LOG DETECTOR					
In measurement mode, VDET/VCTL is shorted to VSET; in controller mode, the setpoint voltage is applied to VSET; the CW input signal is applied at INHI					
f = 50 MHz	$R_{TADJ} = 22.1\text{ k}\Omega$				
$\pm 1\text{ dB}$ Dynamic Range	$T_A = 25^\circ\text{C}$		28		dB
Slope ¹			-21		mV/dB
Intercept ¹			18.2		dBm
VDET or VSET Voltage	$P_{IN} = -10\text{ dBm}$		0.59		V
	$P_{IN} = -30\text{ dBm}$		1.01		V

Parameter	Conditions	Min	Typ	Max	Unit
f = 140 GHz	R _{TADJ} = 22.1 kΩ				
±1 dB Dynamic Range	T _A = 25°C		28		dB
Slope ¹			-21.1		mV/dB
Intercept ¹			17.8		dBm
VDET or VSET Voltage	P _{IN} = -10 dBm		0.59		V
	P _{IN} = -30 dBm		1.01		V
f = 350 MHz	R _{TADJ} = 22.1 kΩ				
±1 dB Dynamic Range	T _A = 25°C		26		dB
Slope ¹			-21.3		mV/dB
Intercept ¹			17.1		dBm
VDET or VSET Voltage	P _{IN} = -10 dBm		0.58		V
	P _{IN} = -30 dBm		1.0		V
f = 860 MHz	R _{TADJ} = 22.1 kΩ				
±1 dB Dynamic Range	T _A = 25°C		25		dB
Slope ¹			-21.6		mV/dB
Intercept ¹			16.2		dBm
VDET or VSET Voltage	P _{IN} = -10 dBm		0.57		V
	P _{IN} = -30 dBm		1.00		V
f = 1900 MHz	R _{TADJ} = 22.1 kΩ				
±1 dB Dynamic Range	T _A = 25°C		26		dB
Slope ¹			-22.7		mV/dB
Intercept ¹			13.5		dBm
VDET or VSET Voltage	P _{IN} = -10 dBm		0.54		V
	P _{IN} = -30 dBm		0.99		V
f = 2150 MHz	R _{TADJ} = 22.1 kΩ				
±1 dB Dynamic Range	T _A = 25°C		24		dB
Slope ¹			-23.2		mV/dB
Intercept ¹			12.6		dBm
VDET or VSET Voltage	P _{IN} = -10 dBm		0.53		V
	P _{IN} = -30 dBm		0.99		V
LOG DETECTOR OUTPUT INTERFACE					
VDET Voltage Swing	VDET				
	V _{VSET} = 0 V, INHI = open, controller mode		2		V
	V _{VSET} = 2 V, INHI = open, controller mode		10		mV
Small Signal Bandwidth	Simulated, INHI = -10 dBm, from CLPF to VOUT		>100		MHz
Output Noise	INHI = 2.2 GHz, -10 dBm, f _{NOISE} = 100 kHz, C _{CLPF} = open		73		nV/√Hz
Fall Time	Input level = no signal to -10 dBm, 90% to 10%, C _{CLPF} = 8 pF		42		ns
	Input level = no signal to -10 dBm, 90% to 10%, C _{CLPF} = 0.1 μF		178		μs
Rise Time	Input level = -10 dBm to no signal, 10% to 90%, C _{CLPF} = 8 pF		29		ns
	Input level = -10 dBm to no signal, 10% to 90%, C _{CLPF} = 0.1 μF		174		μs
Video Bandwidth			15		MHz
VSET Incremental Input Resistance	P _{OUT} = 0 dBm, AGC mode, V _{VSET} = 0.9 V to 1 V		33,000		dV/dI
VSET Input Bias Current	P _{OUT} = 0 dBm, AGC mode, V _{VSET} = 1 V		25		μA
TADJ INTERFACE					
Input Resistance	TADJ				
	TADJ = 0.9 V, sourcing 50 μA		13		kΩ
Disable Threshold Voltage	TADJ = open		V _{VPOS} - 0.4		V
TEMPERATURE SENSOR OUTPUT					
Output Voltage	TEMP				
	T _A = 27.15°C, 300K, R _L = 1 MΩ (after full warmup)		1.45		V
Temperature Slope	-40°C ≤ T _A ≤ +85°C, R _L = 1 MΩ		4.6		mV/°C
Output Impedance			1		kΩ

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Parameter	Conditions	Min	Typ	Max	Unit
ENABLE INPUT	ENBL				
Input Bias Current	ENBL = 5 V		0.5		μA
	ENBL = 0 V		-0.7		μA
ENBL High Level (Logic 1)		1.5			V
ENBL Low Level (Logic 0)				0.4	V
POWER SUPPLIES	Pin VPOS				
Voltage		4.75		5.5	V
Supply Current	ENBL = high		230	245	mA
	In sleep mode, ENBL = low and TADJ = high		2.2		mA
	In detector disabled mode, ENBL = high and TADJ = high		215		mA

¹ Slope and intercept are determined by calculating the best-fit line between the power levels of -33 dBm and -10 dBm at the specified input frequency.

TYPICAL INPUT AND OUTPUT IMPEDANCES

Unless otherwise noted, $V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$. All impedances are normalized to $50\ \Omega$. The effects of the test fixture are de-embedded up to the pins of the device.

Table 2.

Frequency (MHz)	LO Input Impedance at 2× Frequency	Modulator Output Impedance	Detector Input Impedance
50	1.393 - j0.027	0.847 - j0.016	28.463 - j11.386
140	1.406 + j0.013	0.839 + j0.019	15.159 - j15.234
350	1.441 + j0.039	0.82 + j0.065	4.661 - j10.6
860	1.66 + j0.077	0.764 + j0.166	1.158 - j4.58
1450	2.261 - j0.304	0.799 + j0.231	0.567 - j2.545
1900	1.436 - j1.898	0.856 + j0.371	0.375 - j1.866
2150	0.517 - j1.446	0.862 + j0.51	0.308 - j1.652

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
IBBP, IBBN, QBBP, QBBN Range	0 V to 2.0 V
LOIP and LOIN	13 dBm
Internal Power Dissipation	1.4 W
θ_{JA} (Exposed Paddle Soldered Down)	38°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

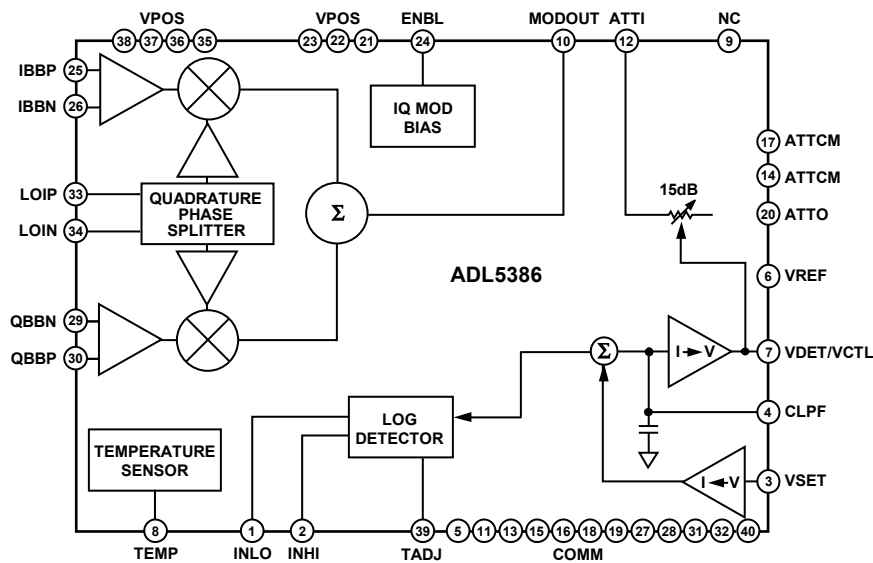
ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES**
 1. NC = NO CONNECT.
 2. CONNECT THE EXPOSED PAD TO GROUND VIA A LOW IMPEDANCE PATH.

Figure 2. Pin Configuration

07864-002

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INLO	Detector Common. This pin should be ac-coupled to ground.
2	INHI	Detector Input. When operating in AGC mode, a portion of the signal at the output of the VVA (or at the output of a subsequent stage) is coupled back to this input. The signal should be ac-coupled into INHI. To provide a 50 Ω match at INHI, a 50 Ω resistor should be connected between INHI and ground (with the ac-coupling capacitor placed between the resistor and the INHI pin).
3	VSET	Setpoint Input. Setpoint input for controller mode or feedback input for measurement mode.
4	CLPF	AGC Loop Filter Capacitor. The ground-referenced capacitor that is connected to this pin sets the loop bandwidth of the AGC circuit.
5, 11, 13, 15, 16, 18, 19, 27, 28, 31, 32, 40	COMM	Device Common. Connect these pins to the same low impedance ground plane.
6	VREF	Attenuator Control Voltage Reference. In AGC mode, this pin should be left open. In open-loop mode, when the VVA is being controlled externally, a 2 V reference voltage should be applied to this pin.
7	VDET/VCTL	Detector Output/VVA Control Voltage Input. When the VVA is being controlled externally (open-loop mode), the attenuation is controlled by the external voltage applied to this pin. The VVA control range is from 0 V (maximum attenuation) to 2 V (minimum attenuation). In this mode, VREF (Pin 6) should be tied to approximately 2 V. When the VVA is being operated in AGC mode, this pin is left open with the voltage on the pin representing the AGC drive voltage to the VVA. If the VVA is not being used, the AGC log amp can be used as a standalone detector by connecting this pin to VSET. In this mode, the log amp output voltage is available at this pin.
8	TEMP	Temperature Sensor Output. This pin provides a standalone temperature sensor output voltage. At room temperature, the nominal output voltage is equal to 1.45 V. The slope of the output voltage is equal to 4.6 mV/°C.
9	NC	No Connect. Do not connect this pin.
10	MODOUT	RF Output of IQ Modulator. Single-ended, 50 Ω internally biased RF output. MODOUT is generally ac-coupled to the input of the VVA (either ATTI or ATTO).
12, 20	ATTI, ATTO	VVA RF Input/Output. ATTI is normally ac-coupled to MODOUT. However, because the VVA is completely reversible, MODOUT can also drive ATTO with ATTI operating as the VVA output.
14, 17	ATTCM	VVA Input/Output Common. These pins should be ac-coupled to ground.
21 to 23, 35 to 38	VPOS	Power Supply. Positive supply voltage pins. All pins should be connected to the same supply (VS). To ensure adequate external bypassing, connect a 0.1 μF capacitor between each pin and ground.

Pin No.	Mnemonic	Description
24	ENBL	IQ Modulator Enable. The IQ modulator is enabled by connecting this pin to VPOS and is disabled by connecting ENBL to ground.
25, 26, 29, 30	IBBP, IBBN, QBPN, QBPN	Differential In-Phase and Quadrature Baseband Inputs. These high impedance inputs should be dc-biased to 0.5 V. Nominal characterized ac signal swing is 700 mV p-p on each pin, resulting in a differential drive of 1.4 V p-p on each input pair. These inputs are not self-biased and have to be externally biased.
33	LOIP	Local Oscillator Input. The local oscillator signal, at two times the output frequency, should be ac-coupled into this pin.
34	LOIN	Local Oscillator Common. This pin should be ac-coupled to ground.
39	TADJ	Temperature Compensation Adjustment Pin and Detector Enable/Disable. This pin is primarily used to provide temperature compensation to the on-chip log amp based AGC circuit. The correct compensation current is set by connecting a ground-referenced resistor to this pin. A value of 22.1 k Ω is recommended for the frequencies over which the ADL5386 is specified. The TADJ pin can also be used to power down the detector section of the ADL5386 by connecting it to VPOS. The detector must be disabled when the modulator/VVA is operating in open loop mode.
41 (EPAD)	Exposed Pad (EPAD)	Connect the exposed pad to ground via a low impedance path.

TYPICAL PERFORMANCE CHARACTERISTICS MODULATOR

Unless otherwise noted, $V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $LO = -7\text{ dBm}$, I/Q inputs = 1.4 V p-p differential sine waves in quadrature on a 500 mV dc bias, baseband frequency = 1 MHz, LO source and RF output load impedances are 50 Ω .

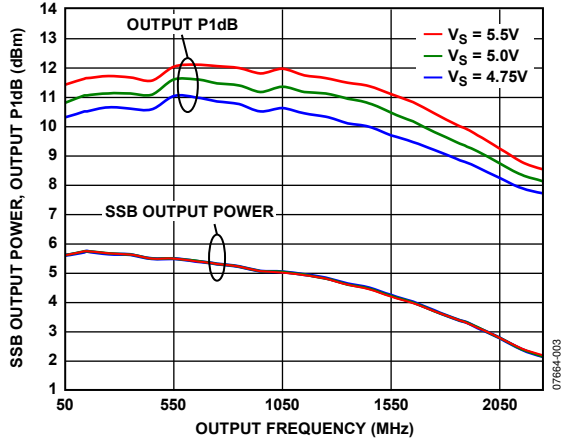


Figure 3. Single Sideband (SSB) Output Power (P_{OUT}), Output P 1 dB vs. Output Frequency and Power Supply

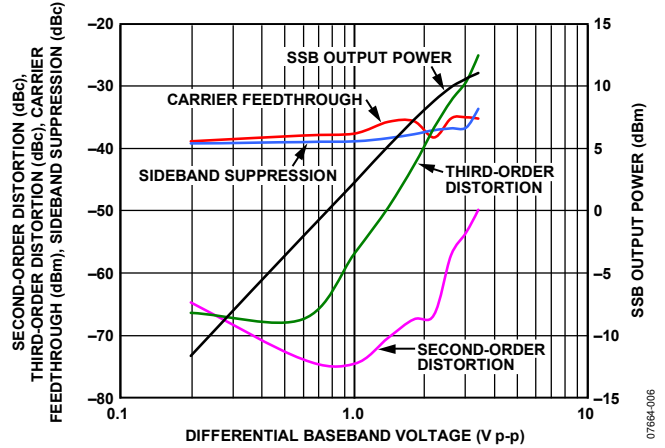


Figure 6. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB Output Power vs. Differential Baseband Voltage, Output Frequency = 860 MHz

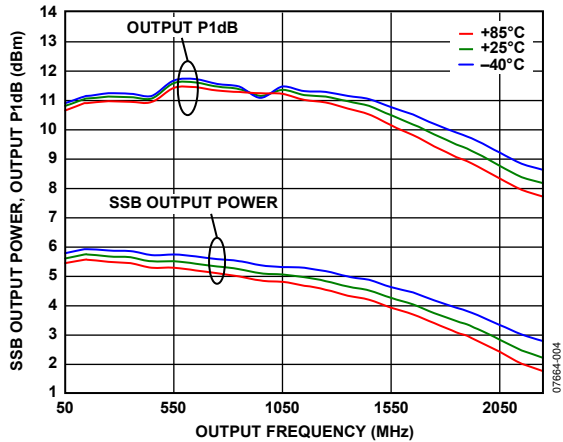


Figure 4. Single Sideband (SSB) Output Power (P_{OUT}), Output P 1 dB vs. Output Frequency and Temperature

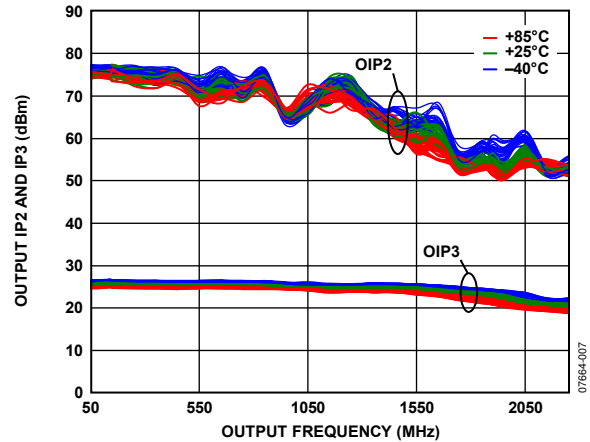


Figure 7. Output IP2 and IP3 vs. Output Frequency and Temperature

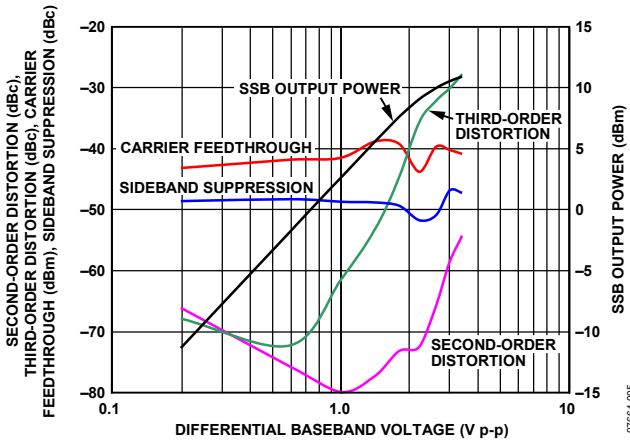


Figure 5. Second- and Third-Order Distortion, Carrier Feedthrough, Sideband Suppression, and SSB Output Power vs. Differential Baseband Voltage, Output Frequency = 350 MHz

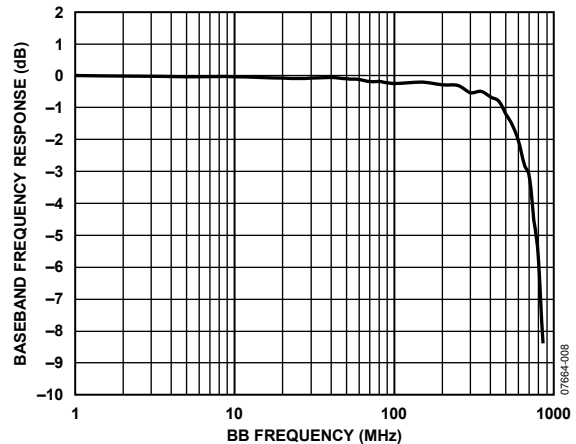


Figure 8. Baseband Frequency Response Normalized to Response for 1 MHz BB Signal, Carrier Frequency = 500 MHz

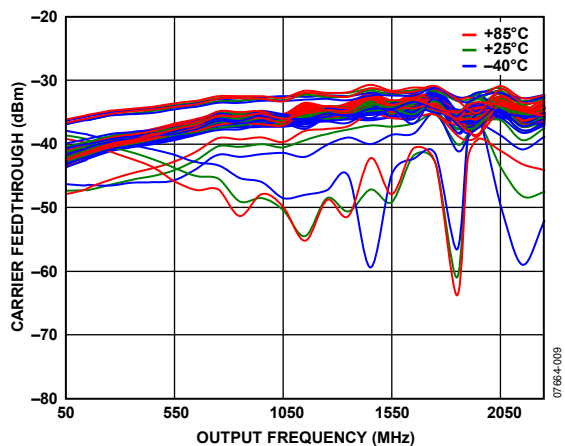


Figure 9. Carrier Feedthrough Distribution vs. Output Frequency and Temperature

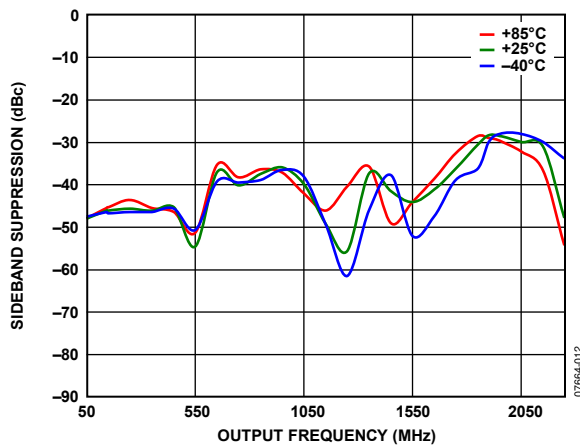


Figure 12. Sideband Suppression vs. Output Frequency and Temperature

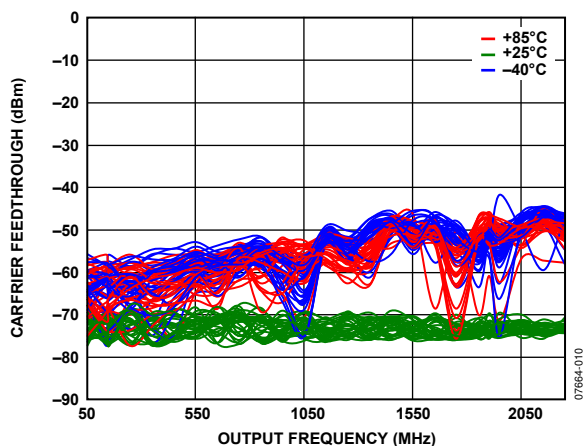


Figure 10. Carrier Feedthrough Distribution at Temperature Extremes, After Nulling to < -65 dBm at $T_A = 25^\circ\text{C}$ vs. Output Frequency

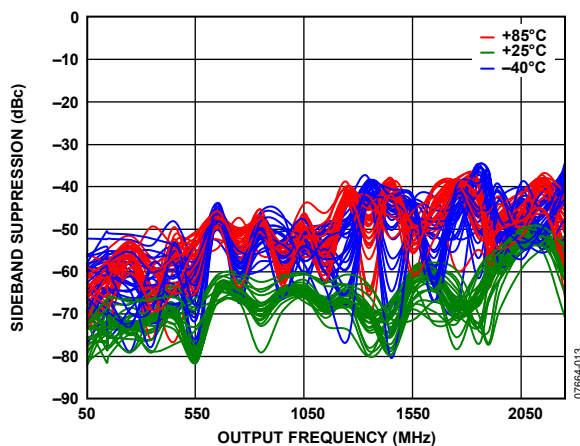


Figure 13. Sideband Suppression Distribution at Temperature Extremes, After Sideband Suppression Nulled to < -50 dBc at $T_A = 25^\circ\text{C}$ vs. Output Frequency

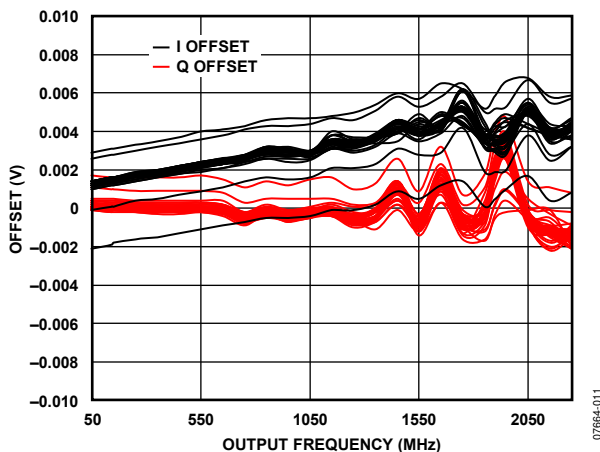


Figure 11. Distribution of I Offset and Q Offset Required to Null Carrier Feedthrough vs. Output Frequency

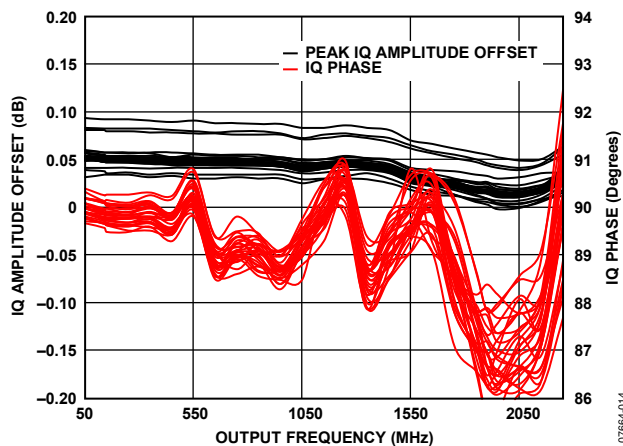


Figure 14. Distribution of Peak Q Amplitude to Null Undesired Sideband (Peak I Amplitude Held Constant at 0.7 V) and Distribution of IQ Phase to Null Undesired Sideband vs. Output Frequency

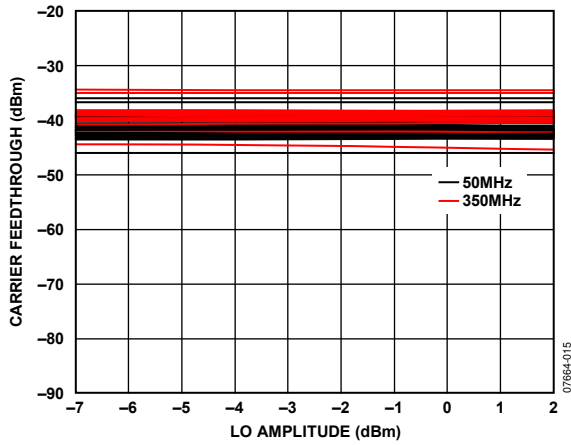


Figure 15. Carrier Feedthrough Distribution vs. LO Amplitude at 50 MHz and 350 MHz

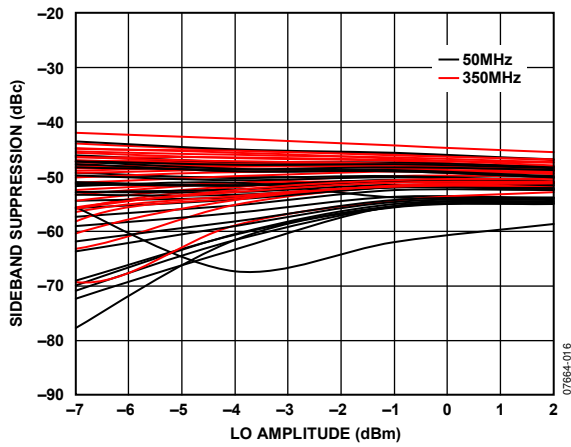


Figure 16. Sideband Suppression Distribution vs. LO Amplitude at 50 MHz and 350 MHz

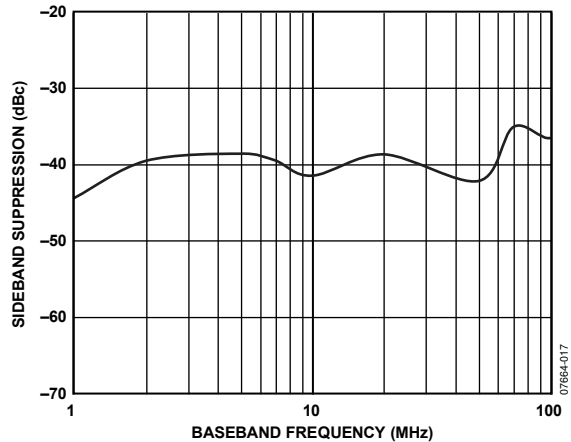


Figure 17. Sideband Suppression vs. Baseband Frequency, Output Frequency = 350 MHz

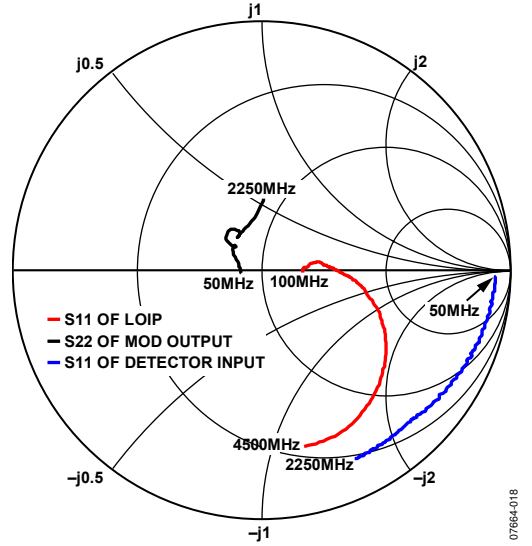


Figure 18. Modulator Output Impedance, LO Input Impedance and Detector Input Impedance (Unterminated) vs. Frequency

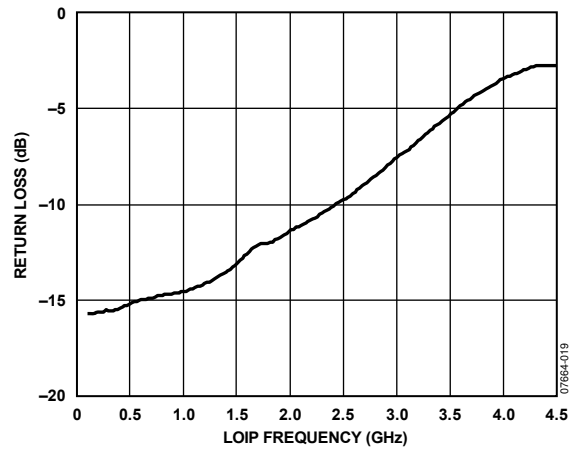


Figure 19. LO Port Input Return Loss vs. LOIP Frequency

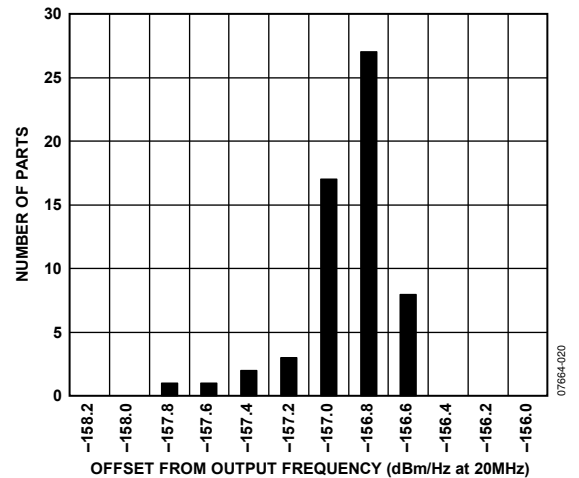


Figure 20. 20 MHz Offset Noise Floor Distribution, Output Frequency = 360 MHz, $P_{out} = -5$ dBm, QPSK Carrier, Symbol Rate = 3.84 MS/PS

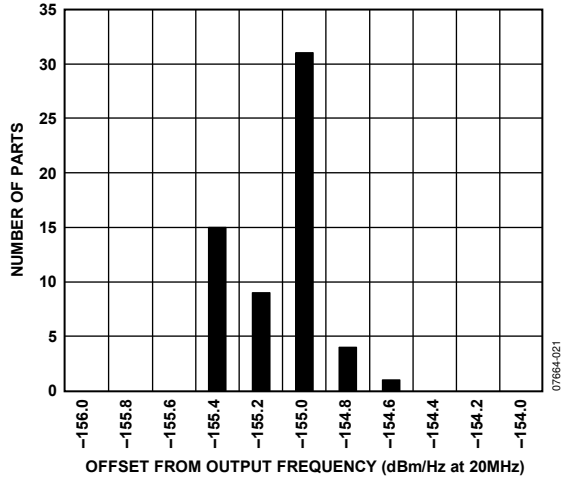


Figure 21. 20 MHz Offset Noise Floor Distribution, Output Frequency = 860 MHz, $P_{OUT} = -5$ dBm, 64 QAM Carrier, Symbol Rate = 5 MSPS

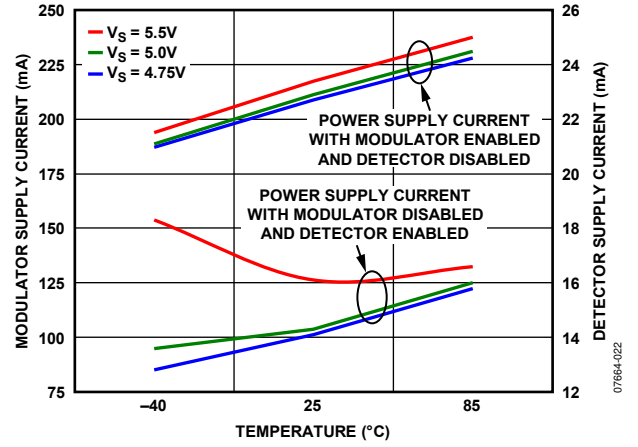


Figure 22. Power Supply Current vs. Temperature and Supply Voltage

VOLTAGE VARIABLE ATTENUATOR

Unless otherwise noted, $V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

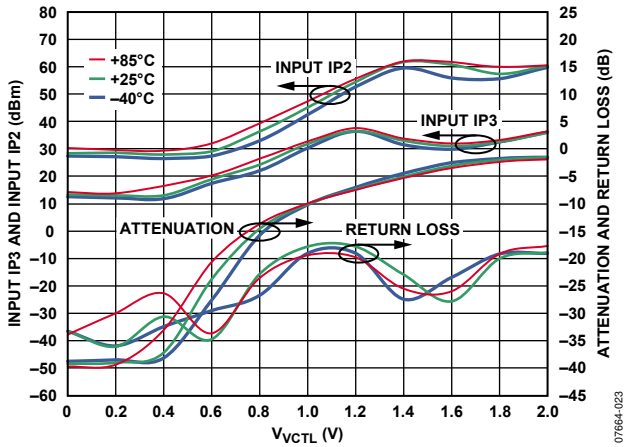


Figure 23. IIP3, IIP2, Attenuation, and Return Loss vs. V_{VCTL} Voltage and Temperature at 140 MHz

07864-023

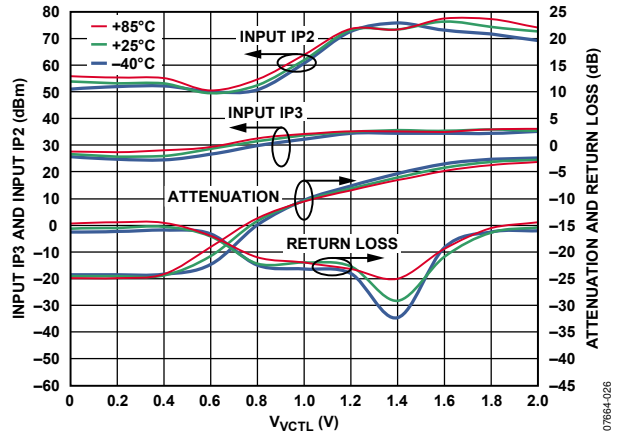


Figure 26. IIP3, IIP2, Attenuation, and Return Loss vs. V_{VCTL} Voltage and Temperature at 1450 MHz

07864-026

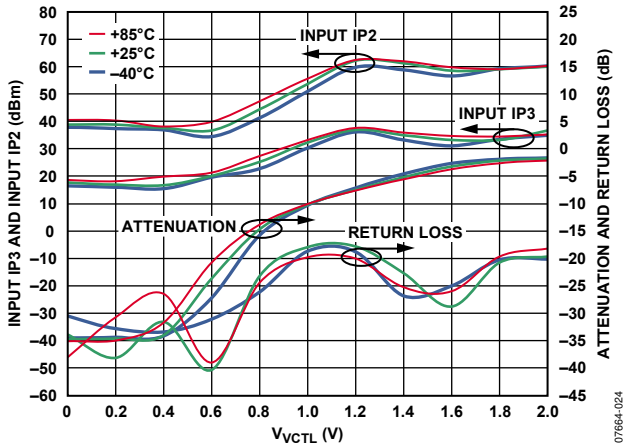


Figure 24. IIP3, IIP2, Attenuation, and Return Loss vs. V_{VCTL} Voltage and Temperature at 350 MHz

07864-024

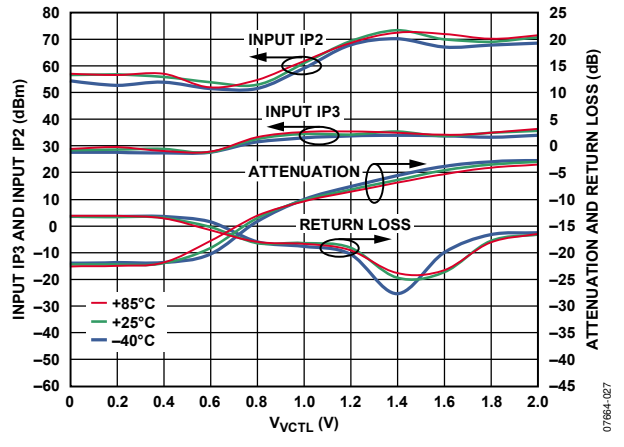


Figure 27. IIP3, IIP2, Attenuation, and Return Loss vs. V_{VCTL} Voltage and Temperature at 1900 MHz

07864-027

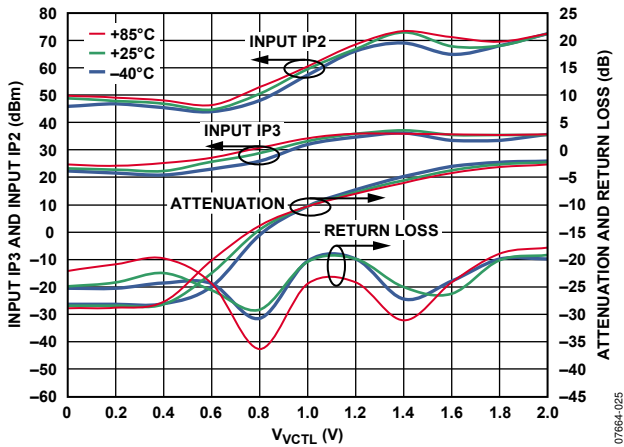


Figure 25. IIP3, IIP2, Attenuation, and Return Loss vs. V_{VCTL} Voltage and Temperature at 860 MHz

07864-025

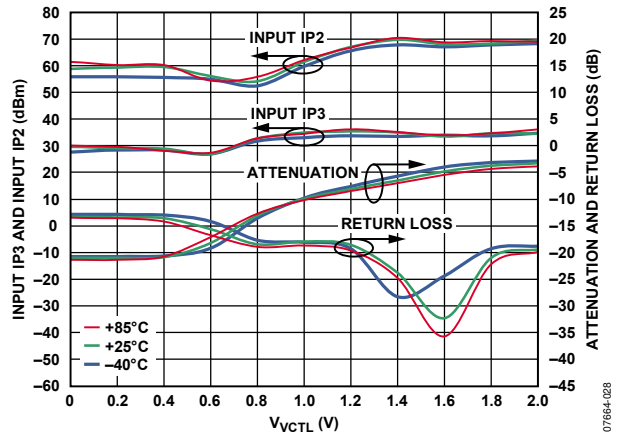


Figure 28. IIP3, IIP2, Attenuation, and Return Loss vs. V_{VCTL} Voltage and Temperature at 2150 MHz

07864-028

DETECTOR

Unless otherwise noted, $V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

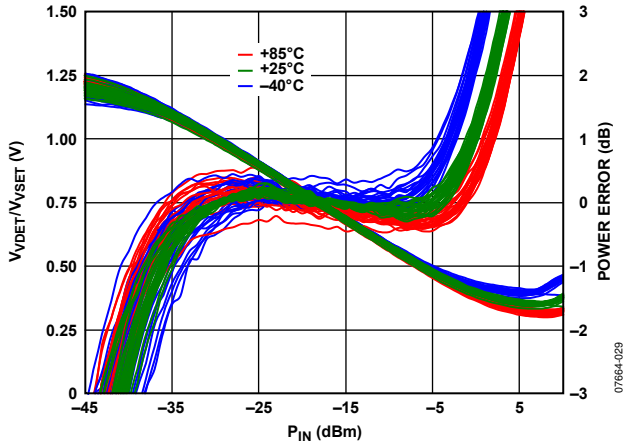


Figure 29. V_{VDET}/V_{VSET} Voltage and Log Conformance vs. Input Amplitude at 350 MHz, $R_{TADJ} = 22.1\text{ k}\Omega$

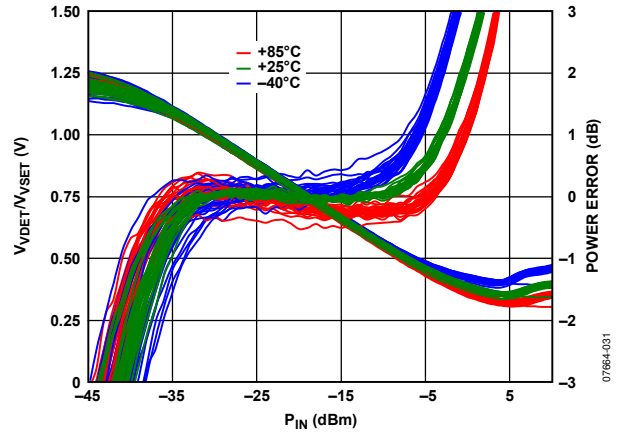


Figure 31. V_{VDET}/V_{VSET} Voltage and Log Conformance vs. Input Amplitude at 1450 MHz, $R_{TADJ} = 22.1\text{ k}\Omega$

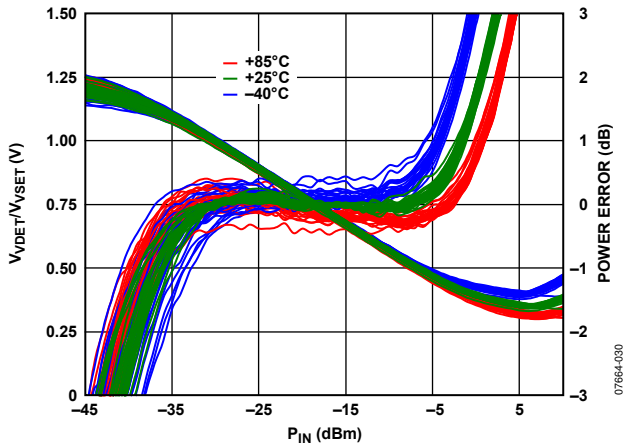


Figure 30. V_{VDET}/V_{VSET} Voltage and Log Conformance vs. Input Amplitude at 860 MHz, $R_{TADJ} = 22.1\text{ k}\Omega$

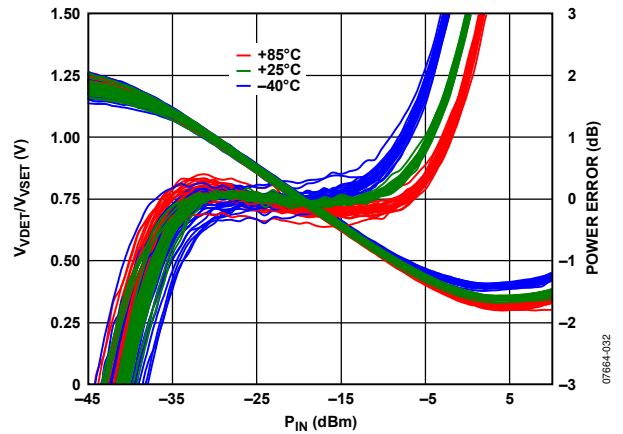


Figure 32. V_{VDET}/V_{VSET} Voltage and Log Conformance vs. Input Amplitude at 2150 MHz, $R_{TADJ} = 22.1\text{ k}\Omega$

CLOSED-LOOP AGC MODE

Unless otherwise noted, $V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $LO = -7\text{ dBm}$, I/Q inputs = 1.4 V p-p differential sine waves in quadrature on a 500 mV dc bias, baseband frequency = 1 MHz, LO source and RF output load impedances are 50 Ω . For AGC mode characterization setup, refer to Figure 42.

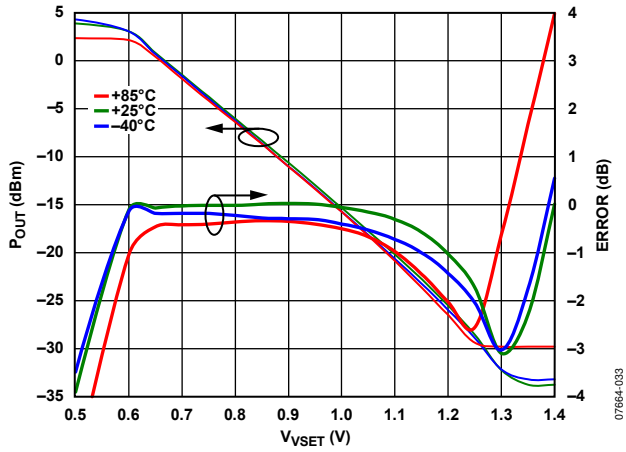


Figure 33. P_{OUT} and Error vs. V_{VSET} at 140 MHz

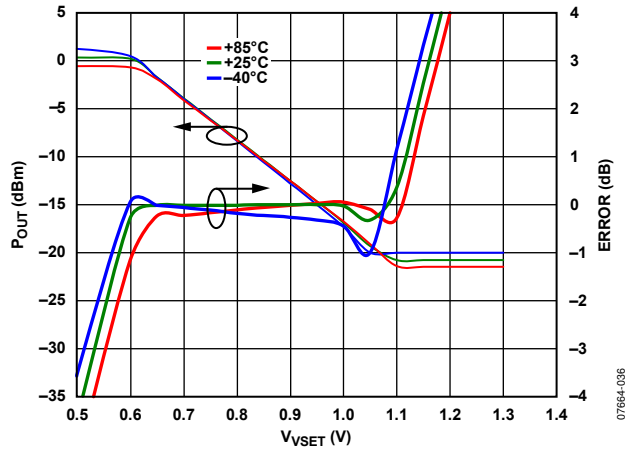


Figure 36. P_{OUT} and Error vs. V_{VSET} at 1450 MHz

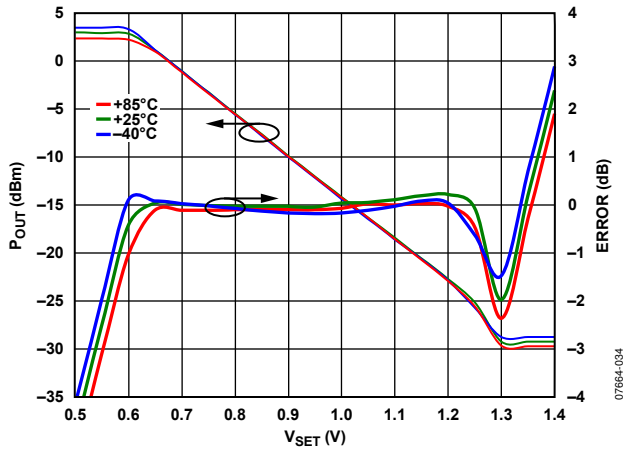


Figure 34. P_{OUT} and Error vs. V_{VSET} at 350 MHz

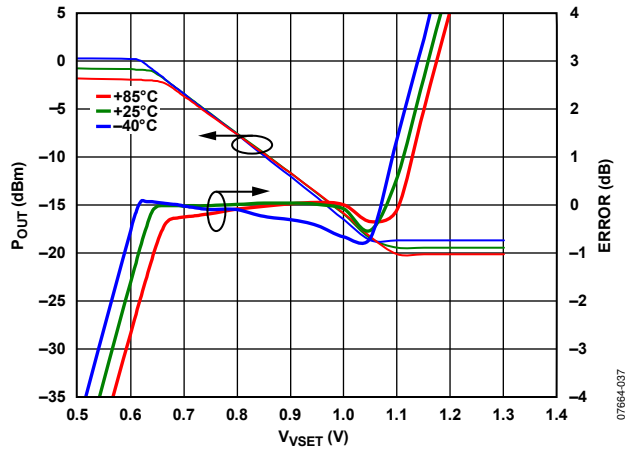


Figure 37. P_{OUT} and Error vs. V_{VSET} at 1900 MHz

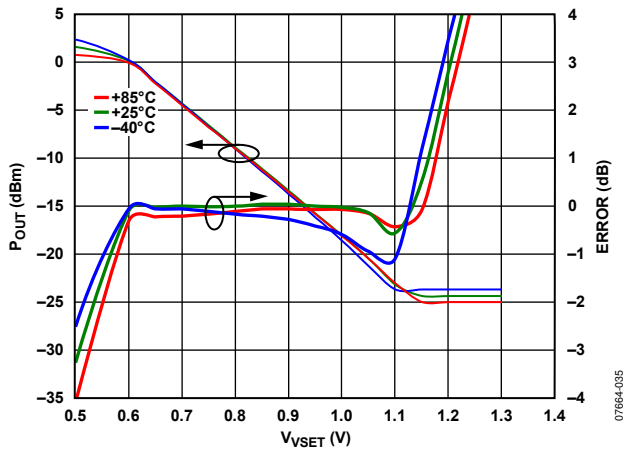


Figure 35. P_{OUT} and Error vs. V_{VSET} at 860 MHz

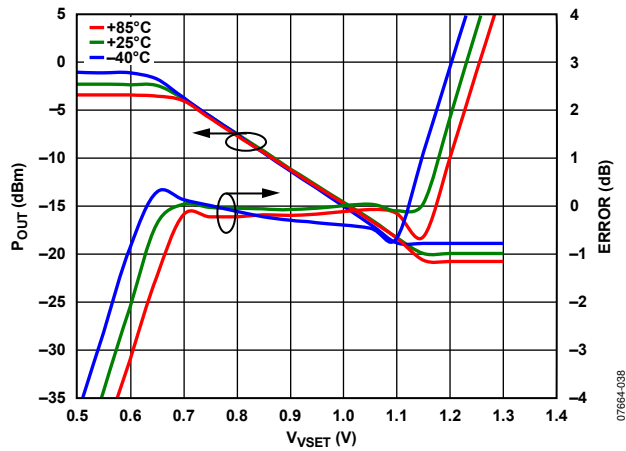


Figure 38. P_{OUT} and Error vs. V_{VSET} at 2150 MHz

CIRCUIT DESCRIPTION

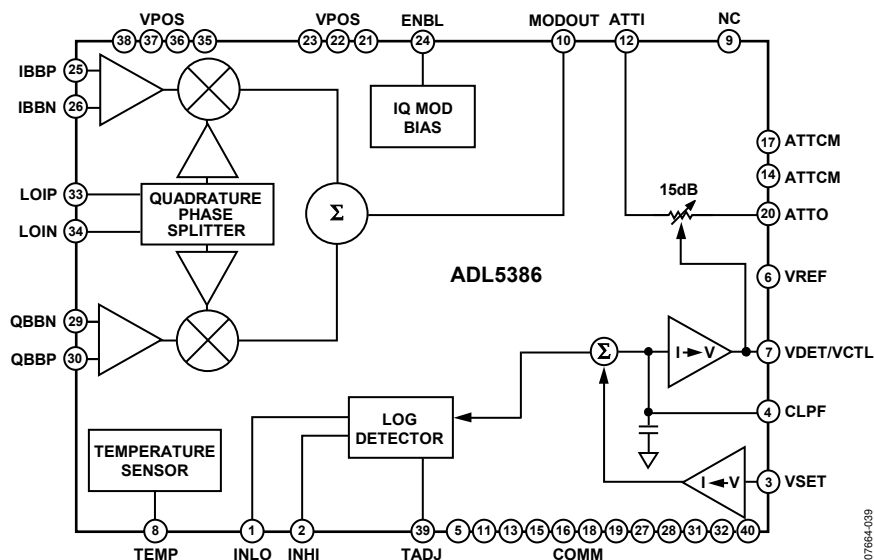


Figure 39. Block Diagram

OVERVIEW

The ADL5386 consists of three sections: a quadrature modulator, a logarithmic detector, and a voltage variable attenuator (VVA). The modulator section contains the circuitry for the following functions:

- Local oscillator (LO) interface
- Baseband voltage-to-current (V-to-I) converter
- Mixers
- Differential-to-single-ended (D-to-S) amplifier
- Temperature sensor and bias circuit

The detector section contains the logarithmic detector and amplifiers interfacing to the VSET input and VDET output. The variable attenuator section consists of a PI network of PHEMTs and resistors implemented on a GaAs die separate from the silicon die where the rest of the circuits reside. A detailed block diagram of the device is shown in Figure 39.

QUADRATURE MODULATOR SECTION

The LO interface generates two LO signals at 90° of phase difference to drive two mixers in quadrature. Baseband signals are converted into currents by the V-to-I converters that feed into the two mixers. The outputs of the mixers are combined in the differential-to-single-ended amplifier, which provides a $50\ \Omega$ output interface. Reference currents to each section are generated by the bias circuit. A detailed description of each section follows.

LO Interface

The LO interface consists of a buffer amplifier followed by a pair of frequency dividers that generate two carriers at half the input frequency and in quadrature with each other. Each carrier is then amplified and amplitude-limited to drive the double-balanced mixers.

V-to-I Converter

The differential baseband input voltages that are applied to the baseband input pins are fed to a pair of common-emitter, voltage-to-current converters. The output currents then modulate the two half-frequency LO carriers in the mixer stage.

Mixers

The ADL5386 has two double-balanced mixers: one for the in-phase channel (I channel) and one for the quadrature channel (Q channel). These mixers are based on the Gilbert cell design of four cross-connected transistors. The output currents from the two mixers are summed together in the resistor-inductor loads in the D-to-S amplifier.

D-to-S Amplifier

The output D-to-S amplifier consists of two emitter followers driving a totem-pole output stage. Output impedance is established by the emitter resistors in the output transistors. The output of this stage connects to the output (VOUT) pin.

Bias Circuits

A band gap based bias circuit provides proportional-to-absolute temperature as well as temperature stable reference currents for the different circuits in the modulator section. The ENBL input controls the operation of this bias circuit. When ENBL is pulled to a low level, the bias references are turned off, and the whole modulator section is turned off as a result. A voltage that is proportional to the absolute temperature of the circuit is also available at the TEMP pin.

A separator bias circuit provides the reference currents as well as the reference voltages for the detector and voltage variable attenuator sections. This bias circuit can also be disabled by pulling the TADJ pin high, which in turn shuts down the detector section.

LOGARITHMIC DETECTOR

The design of the log detector is similar to that of the [AD8317](#) standalone log detector device, where the log function is generated by a series of limiting amplifiers and detectors. The output current from this log detector is compared with that from a voltage-to-current converter connected to the VSET input. Any net difference between these two currents is pumped into an on-chip integrating capacitor that is generally augmented by additional off-chip capacitance. The voltage on the integrating capacitor is amplified and produces an output error voltage that is generally used to adjust the attenuation of the voltage variable attenuator until the VSET current and the current from the log detector are balanced.

VOLTAGE VARIABLE ATTENUATOR (VVA)

The VVA is implemented on a GaAs die separate from the silicon die where the modulator and detector reside. The VVA is formed by PHEMTs and resistors connected in a PI network to provide the attenuator function. The gate source bias on the PHEMTs are controlled by the voltages on the VREF and VDET/VCTL pins, resulting in different attenuation between ATTI and ATTO as the voltage at VDET/VCTL is varied. The resistance in the shunt paths between ATTI and ATTO to ATTCM vary in the opposite manner as the paths between ATTI and ATTO to maintain good return loss through different attenuation levels.

BASIC CONNECTIONS

OPEN-LOOP POWER CONTROL MODE

Figure 41 shows the basic connections for operating the ADL5386 when the voltage variable attenuator (VVA) is driven from an external voltage source and not from the built-in AGC circuit. In this mode, the inputs to the RF detector should be both ac-coupled to ground. The TADJ pin is tied to the supply, disabling the unused detector and reducing the current consumption by approximately 15 mA. The IQ modulator is enabled by pulling the ENBL pin high. The IQ modulator is enabled by pulling the ENBL pin high.

The output of the modulator is ac-coupled to the input of the VVA (Pin ATTI). The VVA is bidirectional; therefore, the modulator can also be configured to drive ATTO and to take the final output at ATTIL.

The attenuation of the VVA is controlled by the voltages on Pin VREF and Pin VDET/VCTL. VREF should be tied to a low impedance external voltage of 2 V. This voltage can be conveniently derived from the supply voltage using a pair of resistors, but this voltage must then be buffered with an op amp to prevent bias current related voltage drops.

With VREF set to 2 V, a variable voltage between 0 V and 2 V on VDET/VCTL sets the attenuation. Maximum attenuation is achieved when $V_{DET}/V_{CTL} = 0$ V, and minimum attenuation is achieved when $V_{DET}/V_{CTL} = 2$ V.

Figure 40 shows a plot of P_{OUT} vs. the control voltage (applied to the VDET/VCTL pin) at 350 MHz when the modulator is driven by 1 V p-p sine and cosine signals on its baseband inputs and a $2 \times$ LO of 700 MHz.

In this mode, the detector cannot be used in any kind of standalone mode because its output pin (VDET/VCTL) is used as an input.

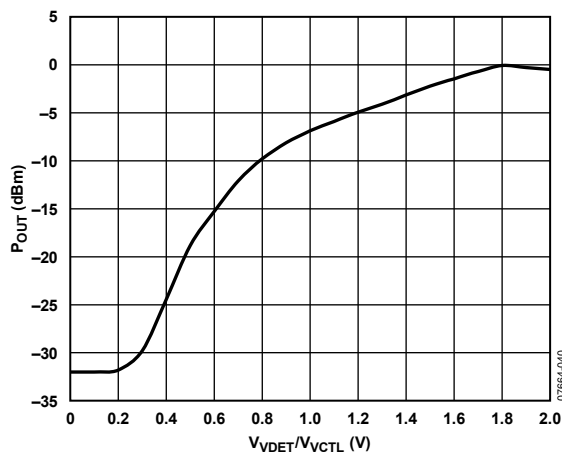


Figure 40. P_{OUT} vs. V_{DET}/V_{CTL} at 350 MHz for Open-Loop Power Control Mode

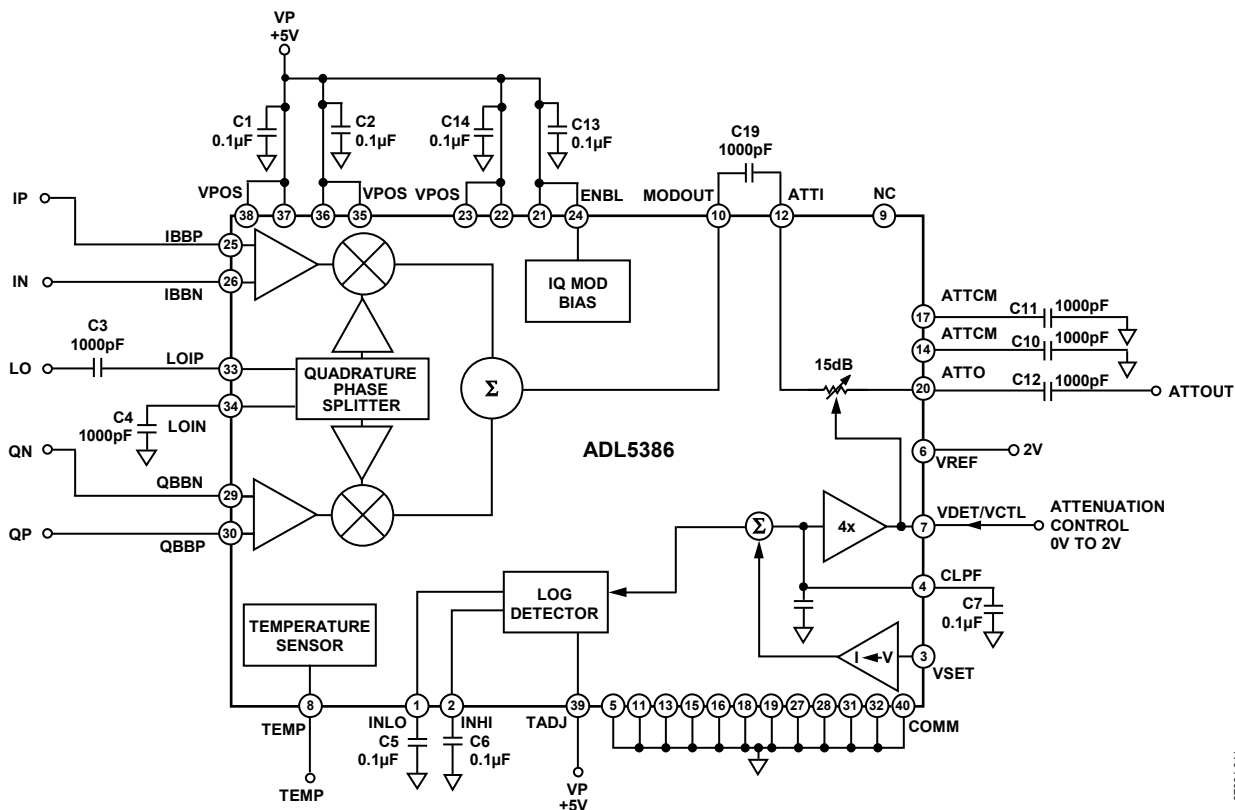


Figure 41. Basic Connections for Open-Loop Power Control Mode

POWER SUPPLY AND GROUNDING

The VPOS supply pins should be connected to a common 5 V supply. This supply can vary from 4.75 to 5.5 V. The power supply pins should be adequately decoupled using 0.1 μF capacitors located close to each pin. Adjacent pins can share decoupling capacitors, as shown in Figure 41.

The COMM ground pins should be connected to a common low impedance ground plane. The exposed paddle on the underside of the package is also soldered to a low thermal and electrical impedance ground plane. If the ground plane spans multiple layers on the circuit board, the layers should be stitched together with nine vias under the exposed paddle. The Analog Devices, AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*, discusses the thermal and electrical grounding of the LFCSP in detail.

DEVICE ENABLE AND DISABLE

The IQ modulator section can be enabled or disabled by pulling the ENBL pin high or low, respectively. The detector section of the circuit can be disabled by pulling the TADJ pin high.

BASEBAND INPUTS

The baseband inputs, QBBP, QBBN, IBBP, and IBBN, must be driven from a differential source. The nominal drive level of 1.4 V p-p differential (700 mV p-p on each pin) is biased to a common-mode level of 500 mV dc. This drive level generates an output power level (at MODOUT) of between 2 dBm and 6 dBm based on output frequency.

The dc common-mode bias level for the baseband inputs can range from 400 mV to 600 mV. This results in a reduction in the usable input ac swing range. The nominal dc bias of 500 mV allows for the largest ac swing, limited on the bottom end by the ADL5386 input range and on the top end by the output compliance range on most Analog Devices DACs.

LO INPUT

A single-ended LO signal is applied to the LOIP pin through an ac coupling capacitor. A square wave or a sine wave can be used to drive the LO port. The recommended LO drive power is -7 dBm. An LO power level of -7 dBm is the minimum level that should be used for output frequencies below 140 MHz ($f_{LO} \leq 280$ MHz). At output frequencies above 140 MHz, the LO power can be reduced to -13 dBm. The LO return pin, LOIN, should be ac-coupled to ground through a low impedance path.

The nominal LO drive of -7 dBm can be increased to up to $+2$ dBm. The effect of LO power on sideband suppression and carrier feedthrough is shown in Figure 15 and Figure 16.

AGC MODE

The on-board log amp power detector of the ADL5386 can be used to implement an automatic output power control (commonly referred to as AGC) loop that effectively linearizes the transfer function of the VVA. To implement this mode, a number of circuit modifications are necessary.

A portion of the output signal of the VVA is coupled back to the input of the log amp detector. This can be done with a power splitter or with a directional coupler as shown in Figure 42. The coupling factor or power split ratio should be set so that the detector never sees a power level that is greater than about -10 dBm (the transfer function of the detector loses some linearity above this level). In the example shown in Figure 42, a maximum output power from the VVA/modulator of $+3$ dBm is desired. A directional coupler with a coupling factor of approximately $+15$ dB drops this level down to -12 dBm at the input of the detector.

The input signal to the detector produces a current that is drawn from the summing node (Pin CLPF) into the detector block. A setpoint voltage that is applied to the VSET pin is converted into a current that is pumped into the summing node. If these two currents are not equal, the net current flows into or out of the CLPF capacitor on Pin 4. This changes the voltage on the CLPF node that in turn changes the voltage on the VDET/VCTL pin. This pin is internally connected to the attenuation control pin of the VVA. Therefore, the attenuation control voltage on Pin 7 (VDET/VCTL) increases or decreases until the I_{SET} and I_{DET} currents match. When this equilibrium is reached, the voltage on CLPF (and thereby on the control voltage node of the VVA) is held steady.

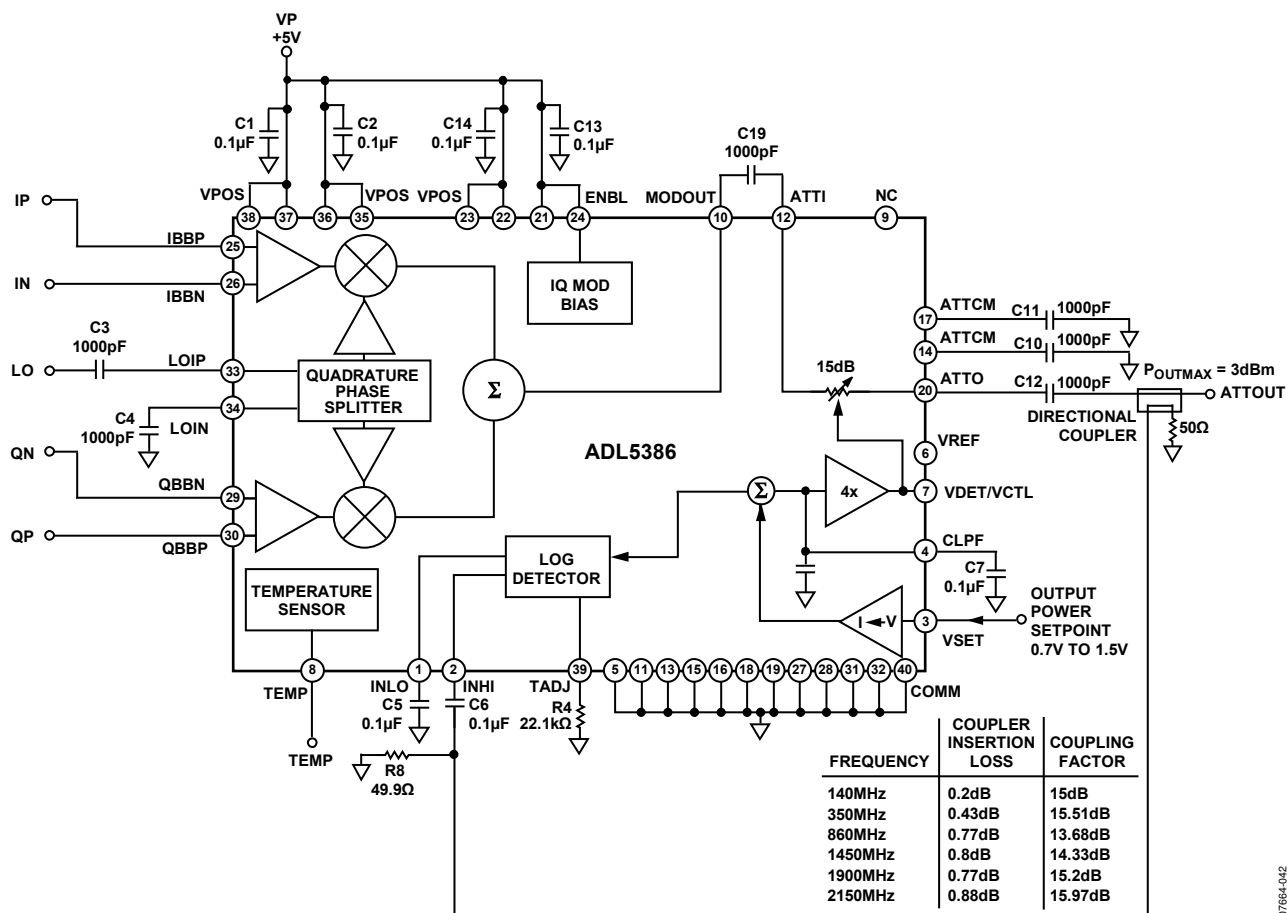


Figure 42. Basic Connections for AGC Mode

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Figure 43 shows the resulting transfer function of the AGC loop, that is, output power (on ATTO) vs. setpoint voltage (on VSET) at 350 MHz. Figure 43 shows a linear-in-dB relationship between P_{OUT} and V_{VSET} over at least 25 dB. It also includes a plot of the linearity of the transfer function in dB. The linearity is calculated by measuring the slope and intercept of the transfer function using the V_{VSET} and P_{OUT} data between V_{VSET} levels of 0.7 and 1 V. This yields an idealized transfer function of

$$P_{OUT_IDEAL} = SLOPE \times (V_{VSET} - INTERCEPT)$$

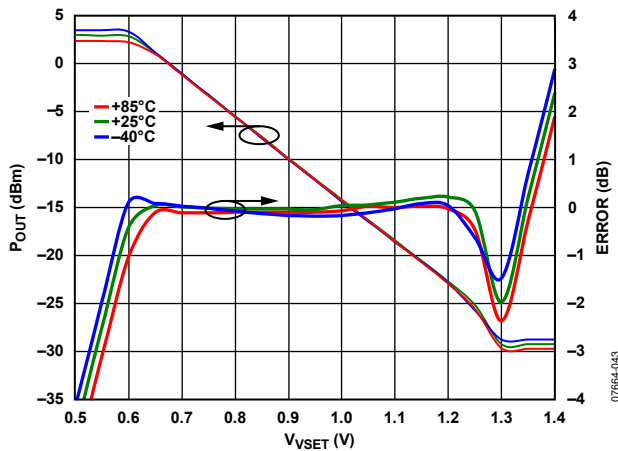


Figure 43. P_{OUT} vs. V_{VSET} Transfer Function in AGC Mode (1 V p-p Differential Baseband Input Voltage on I and Q)

The error in decibels is given by

$$ERROR (dB) = (P_{OUT} - P_{OUT_IDEAL})/SLOPE$$

The relationship between the input level of the detector and the voltage on V_{VSET} follows from the nominal transfer function of the detector when operating in measurement mode (V_{VSET} is connected directly to V_{DET}). Figure 44 shows the measurement mode relationship between the detector input level and the output voltage at 350 MHz. Figure 44 shows that an input level of -12 dBm produces an output of 0.6 V. In AGC mode, a setpoint voltage of 0.6 V causes the loop to adjust until the detector input level is -12 dBm. Remembering the coupling factor of the directional coupler, the -12 dBm level at the detector corresponds to a power level of approximately $+3$ dBm at the output of the VVA. Therefore, with a 15 dB coupling factor, a setpoint voltage of 0.6 produces an output power from the VVA of 3 dBm, as shown in Figure 43.

In general, the loop should be designed with a level of attenuation between ATTO and INHI (detector input) that results in the detector always seeing a power level that is within its linear operating range. Because the power detector has a linear input range that is larger than the attenuation range of the VVA this is generally achievable. In addition, it is desirable to map the desired VVA output power range into the detector's region of maximum linearity. In the example shown, where a maximum output power of $+3$ dBm is desired, the input range to the detector is -12 dBm to -44 dBm. Notice how the degraded linearity of the detector below -40 dBm (see Figure 44) can also be observed in the closed-loop transfer function at output power levels below -25 dBm (Figure 43).

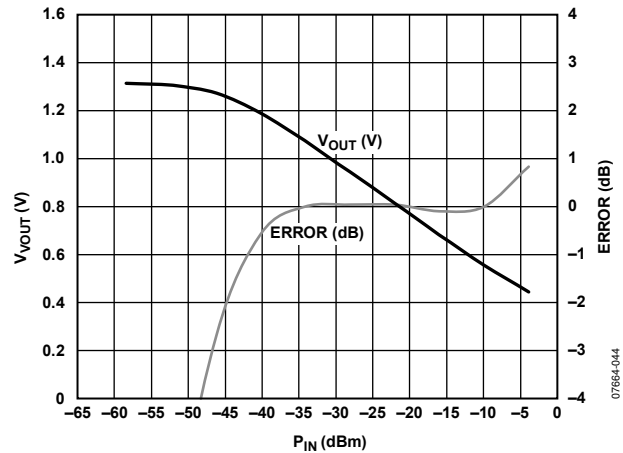


Figure 44. Measurement Mode Relationship Between V_{VOUT}/V_{VSET} and Detector Input Power at 350 MHz

SETTING THE TADJ RESISTOR

The primary component of the temperature variation of the V_{VOUT}/V_{VSET} voltage and the detector RF input is the drift of the intercept. This temperature drift can be compensated by connecting a resistor between TADJ (Pin 39) and ground. The optimum resistance value for the frequencies at which the ADL5386 is characterized has been experimentally determined to be 22.1 kΩ. Note that the accuracy specifications of the detector and performance plots assume that this resistance is in place.