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1 MHz to 10 GHz, 62 dB Dual Log Detector/Controller

ADL5519

FEATURES

- Wide bandwidth: 1 MHz to 10 GHz
- Dual-channel and channel difference output ports
- Integrated accurate scaled temperature sensor
- 62 dB dynamic range (±3 dB)
- >50 dB with ±1 dB up to 8 GHz
- Stability over temperature: ±0.5 dB (−40°C to +85°C)
- Low noise detector/controller outputs
- Pulse response time: 6 ns/8 ns (fall time/rise time)
- Supply operation: 3.3 V to 5.5 V @ 60 mA
- Fabricated using high speed SiGe process
- Small footprint, 5 mm × 5 mm, 32-lead LFCSP
- Operating temperature range: −40°C to +125°C

APPLICATIONS

- RF transmitter power amplifier linearization and gain/power control
- Power monitoring in radio link transmitters
- Dual-channel wireless infrastructure radios
- Antenna VSWR monitor
- RSSI measurement in base stations, WLAN, WiMAX, radar

FUNCTIONAL BLOCK DIAGRAM

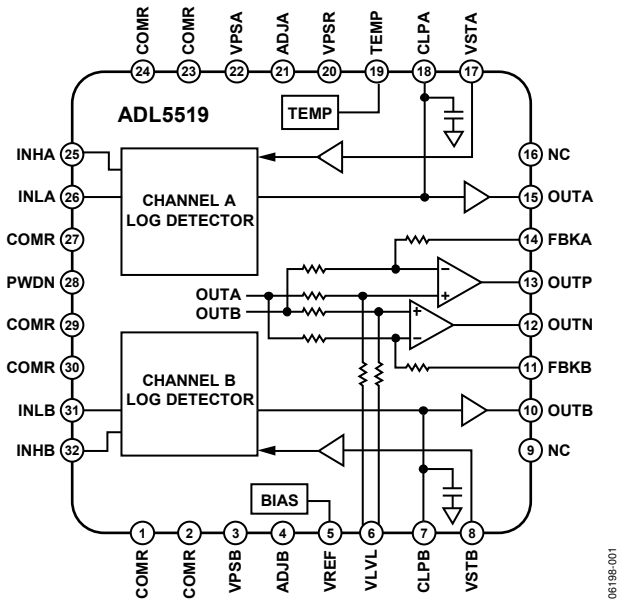

Figure 1.

GENERAL DESCRIPTION

The ADL5519 is a dual-demodulating logarithmic amplifier that incorporates two AD8317s. It can accurately convert an RF input signal into a corresponding decibel-scaled output. The ADL5519 provides accurately scaled, independent, logarithmic output voltages for both RF measurement channels. The device has two additional output ports, OUTP and OUTN, that provide the measured differences between the OUTA and OUTB channels. The on-chip channel matching makes the log amp outputs insensitive to temperature and process variations.

The temperature sensor pin provides a scaled voltage that is proportional to the temperature over the operating temperature range of the device.

The ADL5519 maintains accurate log conformance for signals from 1 MHz to 8 GHz and provides useful operation to 10 GHz. The ±3 dB dynamic range is typically 62 dB and has a ±1 dB dynamic range of >50 dB (re: 50 Ω). The ADL5519 has a response time of 6 ns/8 ns (fall time/rise time) that enables RF burst detection to a pulse rate of greater than 50 MHz. The device provides unprecedented logarithmic intercept stability vs. ambient temperature conditions. A supply of 3.3 V to 5.5 V is required to power the device. Current consumption is typically 60 mA, and it decreases to less than 1 mA when the device is disabled.

The device is capable of supplying four log amp measurements simultaneously. Linear-in-dB measurements are provided at OUTA and OUTB with conveniently scaled slopes of −22 mV/dB. The log amp difference between OUTA and OUTB is available as differential or single-ended signals at OUTP and OUTN. An optional voltage applied to VLVL provides a common-mode reference level to offset OUTP and OUTN above ground. The broadband output pins can support many system solutions.

Any of the ADL5519 output pins can be configured to provide a control voltage to a variable gain amplifier (VGA). Special attention has been paid to minimize the broadband noise of the output pins so that they can be used for controller applications.

The ADL5519 is fabricated on a SiGe bipolar IC process and is available in a 5 mm × 5 mm, 32-lead LFCSP with an operating temperature range of −40°C to +125°C.

Rev. A

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ADL5519* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADL5519 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1040: RF Power Calibration Improves Performance of Wireless Transmitters

Data Sheet

- ADL5519: 1 kHz to 10 GHz, 64 dB Dynamic Range Dual Log Detector/Controller Data Sheet

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

REFERENCE MATERIALS

Product Selection Guide

- RF Source Booklet

Technical Articles

- Design a Logamp RF Pulse Detector
- Detecting Fast RF Bursts using Log Amps
- Log Amps and Directional Couplers Enable VSWR Detection
- Make Precise Base-Station Power Measurements
- Measurement and Control of RF Power, Part I
- Measurement and Control of RF Power, Part II
- Measurement and Control of RF Power, Part III
- Measuring the RF Power in CDMA2000 and W-CDMA High Power Amplifiers (HPAs)
- Measuring VSWR and Gain in Wireless Systems

DESIGN RESOURCES

- ADL5519 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADL5519 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

4/09—Rev. 0 to Rev. A

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1/08—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage, V_P = VPSR = VPSA = VPSB = 5 V, C_{LPF} = 1000 pF, T_A = 25°C, 50 Ω termination resistor at INHA, INHB, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
SIGNAL INPUT INTERFACE	INHA, INHB (Pin 25, Pin 32)				
Specified Frequency Range		0.001		10	GHz
DC Common-Mode Voltage			V_P – 0.7		V
MEASUREMENT MODE, 100 MHz OPERATION	ADJA (Pin 21) = 0.65 V, ADJB (Pin 4) = 0.7 V; OUTA, OUTB (Pin 15, Pin 10) shorted to VSTA, VSTB (Pin 17, Pin 8); OUTP, OUTN (Pin 13, Pin 12) shorted to FBKA, FBKB (Pin 14, Pin 11), respectively; sinusoidal input signal; error referred to best-fit line using linear regression between P_{INHA}, P_{INHB} = −40 dBm and −10 dBm				
Input Impedance			1670‖0.47		Ω‖pF
OUTA, OUTB ± 1 dB Dynamic Range			51		dB
	−40°C < T_A < +85°C		42		dB
OUTA, OUTB Maximum Input Level	±1 dB error		−1		dBm
OUTA, OUTB Minimum Input Level	±1 dB error		−52		dBm
OUTA, OUTB, OUTP, OUTN Slope[1]			−22		mV/dB
OUTA, OUTB Intercept[1]			22		dBm
Output Voltage (High Power In)	OUTA, OUTB @ P_{INHA}, P_{INHB} = −16 dBm		0.7		V
Output Voltage (Low Power In)	OUTA, OUTB @ P_{INHA}, P_{INHB} = −40 dBm		1.37		V
OUTP, OUTN Dynamic Gain Range	±1 dB error		50		dB
	−40°C < T_A < +85°C		44		dB
Temperature Sensitivity	Deviation from OUTA, OUTB @ 25°C				
	−40°C < T_A < +85°C, P_{INHA}, P_{INHB} = −16 dBm		±0.25		dB
	25°C < T_A < 85°C, P_{INHA}, P_{INHB} = −40 dBm		+0.16		dB
	−40°C < T_A < +25°C, P_{INHA}, P_{INHB} = −40 dBm		−0.6		dB
	Distribution of OUTP, OUTN from 25°C				
	25°C < T_A < 85°C, P_{INHA} = −16 dBm, P_{INHB} = −30 dBm, typical error = −0.09 dB		±0.25		dB
	−40°C < T_A < +25°C, P_{INHA} = −16 dBm, P_{INHB} = −30 dBm, typical error = 0.25 dB		±0.4		dB
	25°C < T_A < 85°C, P_{INHA} = −40 dBm, P_{INHB} = −30 dBm, typical error = 0.05 dB		±0.25		dB
	−40°C < T_A < +25°C, P_{INHA} = −40 dBm, P_{INHB} = −30 dBm, typical error = −0.23 dB		±0.45		dB
Input A-to-Input B Isolation			80		dB
Input A-to-OUTB Isolation	Frequency separation = 1 kHz, P_{INHA} = −50 dBm, P_{INHA} − P_{INHB} when OUTB/Slope = 1 dB		60		dB
Input B-to-OUTA Isolation	Frequency separation = 1 kHz, P_{INHB} = −50 dBm, P_{INHB} − P_{INHA} when OUTA/Slope = 1 dB		60		dB
MEASUREMENT MODE, 900 MHz OPERATION	ADJA = 0.6 V, ADJB = 0.65 V; OUTA, OUTB shorted to VSTA, VSTB; OUTP, OUTN shorted to FBKA, FBKB, respectively; sinusoidal input signal; error referred to best fit line using linear regression between P_{INHA}, P_{INHB} = −40 dBm and −10 dBm				
Input Impedance			925‖0.54		Ω‖pF
OUTA, OUTB ± 1 dB Dynamic Range			54		dB
	−40°C < T_A < +85°C		49		dB
OUTA, OUTB Maximum Input Level	±1 dB error		−2		dBm
OUTA, OUTB Minimum Input Level	±1 dB error		−56		dBm
OUTA, OUTB, OUTP, OUTN Slope[1]			−22		mV/dB
OUTA, OUTB Intercept[1]			20.3		dBm
Output Voltage (High Power In)	OUTA, OUTB @ P_{INHA}, P_{INHB} = −10 dBm		0.67		V
Output Voltage (Low Power In)	OUTA, OUTB @ P_{INHA}, P_{INHB} = −40 dBm		1.34		V

Parameter	Conditions	Min	Typ	Max	Unit
OUTP, OUTN Dynamic Gain Range	±1 dB error		55		dB
	−40°C < T_A < +85°C		48		dB
Temperature Sensitivity	Deviation from OUTA, OUTB @ 25°C				
	−40°C < T_A < +85°C, P_{INHA}, P_{INHB} = −16 dBm		±0.25		dB
	25°C < T_A < 85°C, P_{INHA}, P_{INHB} = −40 dBm		+0.25		dB
	−40°C < T_A < +25°C, P_{INHA}, P_{INHB} = −40 dBm		−0.5		dB
	Distribution OUTP, OUTN from 25°C				
	25°C < T_A < 85°C, P_{INHA} = −16 dBm, P_{INHB} = −30 dBm, typical error = −0.08 dB		±0.25		dB
	−40°C < T_A < +25°C, P_{INHA} = −16 dBm, P_{INHB} = −30 dBm typical error = 0.3 dB		±0.4		dB
	25°C < T_A < 85°C, P_{INHA} = −40 dBm, P_{INHB} = −30 dBm, typical error = 0.17 dB		±0.25		dB
	−40°C < T_A < +25°C, P_{INHA} = −40 dBm, P_{INHB} = −30 dBm, typical error = −0.19 dB		±0.4		dB
Input A-to-Input B Isolation			75		dB
Input A-to-OUTB Isolation	Frequency separation = 1 kHz, P_{INHA} = −50 dBm, P_{INHA} − P_{INHB} when OUTB/Slope = 1 dB		50		dB
Input B-to-OUTA Isolation	Frequency separation = 1 kHz, P_{INHB} = −50 dBm, P_{INHB} − P_{INHA} when OUTA/Slope = 1 dB		50		dB
MEASUREMENT MODE, 1.9 GHz OPERATION	ADJA = 0.5 V, ADJB = 0.55 V; OUTA, OUTB shorted to VSTA, VSTB; OUTP, OUTN shorted to FBKA, FBKB, respectively; sinusoidal input signal; error referred to best fit line using linear regression between P_{INHA}, P_{INHB} = −40 dBm and −10 dBm				
Input Impedance			525‖0.36		Ω‖pF
OUTA, OUTB ± 1 dB Dynamic Range			55		dB
	−40°C < T_A < +85°C		49		dB
OUTA, OUTB Maximum Input Level	±1 dB error		−4		dBm
OUTA, OUTB Minimum Input Level	±1 dB error		−59		dBm
OUTA, OUTB, OUTP, OUTN Slope[1]			−22		mV/dB
OUTA, OUTB Intercept[1]			18		dBm
Output Voltage (High Power In)	OUTA, OUTB @ P_{INHA}, P_{INHB} = −10 dBm		0.62		V
Output Voltage (Low Power In)	OUTA, OUTB @ P_{INHA}, P_{INHB} = −40 dBm		1.28		V
OUTP, OUTN Dynamic Gain Range	±1 dB error		55		dB
	−40°C < T_A < +85°C		48		dB
Temperature Sensitivity	Deviation from OUTA, OUTB @ 25°C				
	−40°C < T_A < +85°C, P_{INHA}, P_{INHB} = −16 dBm		±0.2		dB
	25°C < T_A < 85°C, P_{INHA}, P_{INHB} = −40 dBm		+0.25		dB
	−40°C < T_A < +25°C, P_{INHA}, P_{INHB} = −40 dBm		−0.5		dB
	Distribution of OUTP, OUTN from 25°C				
	25°C < T_A < 85°C, P_{INHA} = −16 dBm, P_{INHB} = −30 dBm, typical error = −0.07 dB		±0.3		dB
	−40°C < T_A < +25°C, P_{INHA} = −16 dBm, P_{INHB} = −30 dBm, typical error = 0.23 dB		±0.4		dB
	25°C < T_A < 85°C, P_{INHA} = −40 dBm, P_{INHB} = −30 dBm, typical error = 0.16 dB		±0.3		dB
	−40°C < T_A < +25°C, P_{INHA} = −40 dBm, P_{INHB} = −30 dBm, typical error = −0.22 dB		±0.4		dB
Input A-to-Input B Isolation			65		dB
Input A-to-OUTB Isolation	Frequency separation = 1 kHz, P_{INHA} = −50 dBm, P_{INHA} − P_{INHB} when OUTB/Slope = 1 dB		46		dB
Input B-to-OUTA Isolation	Frequency separation = 1 kHz, P_{INHB} = −50 dBm, P_{INHB} − P_{INHA} when OUTA/Slope = 1 dB		46		dB

Parameter	Conditions	Min	Typ	Max	Unit
MEASUREMENT MODE, 2.2 GHz OPERATION	ADJA = 0.48 V, ADJB = 0.6 V; OUTA, OUTB shorted to VSTA, VSTB; OUTP, OUTN shorted to FBKA, FBKB, respectively; sinusoidal input signal; error referred to best fit line using linear regression between P_{INHA}, P_{INHB} = −40 dBm and −10 dBm				
Input Impedance			408||0.34		Ω||pF
OUTA, OUTB ± 1 dB Dynamic Range			55		dB
	−40°C < T_A < +85°C		50		dB
OUTA, OUTB Maximum Input Level	±1 dB error		−5		dBm
OUTA, OUTB Minimum Input Level	±1 dB error		−60		dBm
OUTA, OUTB, OUTP, OUTN Slope[1]			−22		mV/dB
OUTA, OUTB Intercept[1]			16.9		dBm
Output Voltage (High Power In)	OUTA, OUTB @ P_{INHA}, P_{INHB} = −10 dBm		0.6		V
Output Voltage (Low Power In)	OUTA, OUTB @ P_{INHA}, P_{INHB} = −40 dBm		1.26		V
OUTP, OUTN Dynamic Gain Range	±1 dB error		56		dB
	−40°C < T_A < +85°C		40		dB
Temperature Sensitivity	Deviation from OUTA, OUTB @ 25°C				
	−40°C < T_A < +85°C, P_{INHA}, P_{INHB} = −16 dBm		±0.28		dB
	25°C < T_A < 85°C, P_{INHA}, P_{INHB} = −40 dBm		+0.3		dB
	−40°C < T_A < +25°C, P_{INHA}, P_{INHB} = −40 dBm		−0.5		dB
	Distribution of OUTP, OUTN from 25°C				
	25°C < T_A < 85°C, P_{INHA} = −16 dBm, P_{INHB} = −30 dBm, typical error = −0.07 dB		±0.25		dB
	−40°C < T_A < +25°C, P_{INHA} = −16 dBm, P_{INHB} = −30 dBm, typical error = 0.25 dB		±0.4		dB
	25°C < T_A < 85°C, P_{INHA} = −40 dBm, P_{INHB} = −30 dBm, typical error = 0.17 dB		±0.25		dB
	−40°C < T_A < +25°C, P_{INHA} = −40 dBm, P_{INHB} = −30 dBm typical error = −0.22dB		±0.4		dB
Input A-to-Input B Isolation			60		dB
Input A-to-OUTB Isolation	Frequency separation = 1 kHz, P_{INHA} = −50 dBm, P_{INHA} − P_{INHB} when OUTB/Slope = 1 dB		46		dB
Input B-to-OUTA Isolation	Frequency separation = 1 kHz, P_{INHB} = −50 dBm, P_{INHB} − P_{INHA} when OUTA/Slope = 1 dB		46		dB
MEASUREMENT MODE, 3.6 GHz OPERATION	ADJA = 0.35 V ADJB = 0.42; OUTA, OUTB shorted to VSTA, VSTB; OUTP, OUTN shorted to FBKA, FBKB, respectively; sinusoidal input signal; error referred to best fit line using linear regression between P_{INHA}, P_{INHB} = −40 dBm and −10 dBm				
Input Impedance			187||0.66		Ω||pF
OUTA, OUTB ± 1 dB Dynamic Range			54		dB
	−40°C < T_A < +85°C		44		dB
OUTA, OUTB Maximum Input Level	±1 dB error		−4		dBm
OUTA, OUTB Minimum Input Level	±1 dB error		−58		dBm
OUTA, OUTB, OUTP, OUTN Slope[1]			−22.5		mV/dB
OUTA, OUTB Intercept[1]			17		dBm
Output Voltage (High Power In)	OUTA, OUTB @ P_{INHA}, P_{INHB} = −10 dBm		0.62		V
Output Voltage (Low Power In)	OUTA, OUTB @ P_{INHA}, P_{INHB} = −40 dBm		1.31		V
OUTP, OUTN Dynamic Gain Range	±1 dB error		52		dB
	−40°C < T_A < +85°C		42		dB

Parameter	Conditions	Min	Typ	Max	Unit
Temperature Sensitivity	Deviation from OUTA, OUTB @ 25°C				
	$-40°C < T_A < +85°C$, P_{INHA}, $P_{INHB} = -16$ dBm		±0.4		dB
	$25°C < T_A < 85°C$, P_{INHA}, $P_{INHB} = -40$ dBm		+0.6		dB
	$-40°C < T_A < +25°C$, P_{INHA}, $P_{INHB} = -40$ dBm		−0.45		dB
	Distribution of OUTP, OUTN from 25°C				
	$25°C < T_A < 85°C$, $P_{INHA} = -16$ dBm, $P_{INHB} = -30$ dBm, typical error = −0.07 dB		±0.25		dB
	$-40°C < T_A < +25°C$, $P_{INHA} = -16$ dBm, $P_{INHB} = -30$ dBm, typical error = 0.27 dB		±0.45		dB
	$25°C < T_A < 85°C$, $P_{INHA} = -40$ dBm, $P_{INHB} = -30$ dBm, typical error = 0.31 dB		±0.3		dB
	$-40°C < T_A < +25°C$, $P_{INHA} = -40$ dBm, $P_{INHB} = -30$ dBm, typical error = −0.14 dB		±0.5		dB
Input A-to-Input B Isolation			40		dB
Input A-to-OUTB Isolation	Frequency separation = 1 kHz, $P_{INHA} = -50$ dBm, $P_{INHA} - P_{INHB}$ when OUTB/Slope = 1 dB		20		dB
Input B-to-OUTA Isolation	Frequency separation = 1 kHz, $P_{INHB} = -50$ dBm, $P_{INHB} - P_{INHA}$ when OUTA/Slope = 1 dB		20		dB
MEASUREMENT MODE, 5.8 GHz OPERATION	ADJA = 0.58 V, ADJB = 0.7 V; OUTA, OUTB shorted to VSTA, VSTB; OUTP, OUTN shorted to FBKA, FBKB respectively; sinusoidal input signal; error referred to best fit line using linear regression between P_{INHA}, $P_{INHB} = -40$ dBm and −20 dBm				
Input Impedance			28||1.19		Ω||pF
OUTA, OUTB ± 1 dB Dynamic Range			53		dB
	$-40°C < T_A < +85°C$		45		dB
OUTA, OUTB Maximum Input Level	±1 dB error		−2		dBm
OUTA, OUTB Minimum Input Level	±1 dB error		−55		dBm
OUTA, OUTB, OUTP, OUTN Slope[1]			−22.5		mV/dB
OUTA, OUTB Intercept[1]			20		dBm
Output Voltage (High Power In)	OUTA, OUTB @ P_{INHA}, $P_{INHB} = -10$ dBm		0.68		V
Output Voltage (Low Power In)	OUTA, OUTB @ P_{INHA}, $P_{INHB} = -40$ dBm		1.37		V
OUTP, OUTN Dynamic Gain Range	±1 dB error		53		dB
	$-40°C < T_A < +85°C$		46		dB
Temperature Sensitivity	Deviation from OUTA, OUTB @ 25°C				
	$-40°C < T_A < +85°C$, P_{INHA}, $P_{INHB} = -16$dBm		±0.25		dB
	$25°C < T_A < 85°C$, P_{INHA}, $P_{INHB} = -40$ dBm		+0.25		dB
	$-40°C < T_A < +25°C$, P_{INHA}, $P_{INHB} = -40$ dBm		−0.4		dB
	Distribution of OUTP, OUTN from 25°C				
	$25°C < T_A < 85°C$, $P_{INHA} = -16$ dBm, $P_{INHB} = -30$ dBm, typical error = 0.02 dB		±0.3		dB
	$-40°C < T_A < +25°C$, $P_{INHA} = -16$ dBm, $P_{INHB} = -30$ dBm, typical error = 0.25 dB		±0.4		dB
	$25°C < T_A < 85°C$, $P_{INHA} = -40$ dBm, $P_{INHB} = -30$ dBm, typical error = 0.13 dB		±0.3		dB
	$-40°C < T_A < +25°C$, $P_{INHA} = -40$ dBm, $P_{INHB} = -30$ dBm, typical error = 0.06 dB		±0.5		dB
Input A-to-Input B Isolation			45		dB
Input A-to-OUTB Isolation	Frequency separation = 1 kHz, $P_{INHA} = -50$ dBm, $P_{INHA} - P_{INHB}$ when OUTB/Slope = 1 dB		48		dB
Input B-to-OUTA Isolation	Frequency separation = 1 kHz, $P_{INHB} = -50$ dBm, $P_{INHB} - P_{INHA}$ when OUTA/Slope = 1 dB		48		dB

Parameter	Conditions	Min	Typ	Max	Unit
MEASUREMENT MODE, 8 GHz OPERATION	ADJA = 0.72 V, ADJB = 0.82 V to GND; OUTA, OUTB shorted to VSTA, VSTB; OUTP, OUTN shorted to FBKA, FBKB, respectively; sinusoidal input signal; error referred to best fit line using linear regression between P_{INHA}, P_{INHB} = −40 dBm and −20 dBm				
Input Impedance			+10‖−1.92		Ω‖pF
OUTA, OUTB ± 1 dB Dynamic Range			48		dB
	−40°C < T_A < +85°C		38		dB
OUTA, OUTB Maximum Input Level	±1 dB error		0		dBm
OUTA, OUTB Minimum Input Level	±1 dB error		−48		dBm
OUTA, OUTB, OUTP, OUTN Slope[1]			−22		mV/dB
OUTA, OUTB Intercept[1]			26		dBm
Output Voltage (High Power In)	OUTA, OUTB @ P_{INHA}, P_{INHB} = −10 dBm		0.81		V
Output Voltage (Low Power In)	OUTA, OUTB @ P_{INHA}, P_{INHB} = −40 dBm		1.48		V
OUTP, OUTN Dynamic Gain Range	±1 dB error		50		dB
	−40°C < T_A < +85°C		42		dB
Temperature Sensitivity	Deviation from OUTA, OUTB @ 25°C				
	−40°C < T_A < +85°C, P_{INHA}, P_{INHB} = −16 dBm		±0.4		dB
	25°C < T_A < 85°C, P_{INHA}, P_{INHB} = −40 dBm		−0.1		dB
	−40°C < T_A < +25°C, P_{INHA}, P_{INHB} = −40 dBm		+0.5		dB
	Distribution of OUTP, OUTN from 25°C				
	25°C < T_A < 85°C, P_{INHA} = −16 dBm, P_{INHB} = −30 dBm, typical error = 0.2dB		±0.3		dB
	−40°C < T_A < +25°C, P_{INHA} = −16 dBm, P_{INHB} = −30 dBm, typical error = 0.09dB		±0.5		dB
	25°C < T_A < 85°C, P_{INHA} = −40 dBm, P_{INHB} = −30 dBm, typical error = −0.07dB		±0.3		dB
	−40°C < T_A < +25°C, P_{INHA} = −40 dBm, P_{INHB} = −30 dBm, typical error = 0.17 dB		±0.5		dB
Input A-to-Input B Isolation			45		dB
Input A-to-OUTB Isolation	Frequency separation = 1 kHz, P_{INHA} = −50 dBm, P_{INHA} − P_{INHB} when OUTB/Slope = 1 dB		30		dB
Input B-to-OUTA Isolation	Frequency separation = 1 kHz, P_{INHB} = −50 dBm, P_{INHB} − P_{INHA} when OUTA/Slope = 1 dB		30		dB
OUTPUT INTERFACE	OUTA, OUTB; OUTP, OUTN				
OUTA, OUTB Voltage Range	VSTA, VSTB = 1.7 V, RF in = open		0.3		V
	VSTA, VSTB = 0 V, RF in = open		V_P − 0.4		V
OUTP, OUTN Voltage Range	FBKA, FBKB = open and OUTA < OUTB, R_L ≥ 240 Ω to ground		0.09		V
	FBKA, FBKB = open and OUTA > OUTB, R_L ≥ 240 Ω to ground		V_P − 0.15		V
Source/Sink Current	Output held at 1 V to 1% change		10		mA
Capacitance Drive			1		nF
Output Noise	INHA, INHB = 2.2 GHz, −10 dBm, f_{NOISE} = 100 kHz, CLPA, CLPB = open		10		nV/√Hz
Fall Time	Input level = no signal to −10 dBm, 80% to 20%, CLPA, CLPB = 10 pF		12		ns
	Input level = no signal to −10 dBm, 80% to 20%, CLPA, CLPB = open		6		ns
Rise Time	Input level = −10 dBm to no signal, 20% to 80%, CLPA, CLPB = 10 pF		16		ns
	Input level = −10 dBm to no signal, 20% to 80%, CLPA, CLPB = open		8		ns
Video Bandwidth (or Envelope Bandwidth)			10		MHz
SETPOINT INTERFACE	VSTA, VSTB				
Nominal Input Range	Input level = 0 dBm, measurement mode		0.38		V
	Input level = −50 dBm, measurement mode		1.6		V
Input Resistance	Controller mode, sourcing 50 µA		40		kΩ

Parameter	Conditions	Min	Typ	Max	Unit
DIFFERENCE LEVEL ADJUST	VLVL (Pin 6)				
Input Voltage	OUTP, OUTN = FBKA, FBKB			$V_P - 1$	V
Input Resistance	OUTP, OUTN = FBKA, FBKB		100		kΩ
TEMPERATURE COMPENSATION	ADJA, ADJB				
Input Resistance	ADJA, ADJB = 0.9 V, sourcing 50 µA		13		kΩ
Disable Threshold Voltage	ADJA, ADJB = open		$V_P - 0.4$		V
VOLTAGE REFERENCE	VREF (Pin 5)				
Output Voltage			1.15		V
Temperature Sensitivity	$-40°C < T_A < +25°C$; relative $T_A = 25°C$		+26		µV/°C
	$25°C < T_A < 85°C$; relative $T_A = 25°C$		−26		µV/°C
Current Limit Source/Sink			3/3		mA
TEMPERATURE REFERENCE	TEMP (Pin 19)				
Output Voltage			1.36		V
Temperature Sensitivity	$-40°C < T_A < +125°C$		4.5		mV/°C
Current Limit Source/Sink			4/50		mA/µA
POWER-DOWN INTERFACE	PWDN (Pin 28)				
Logic Level to Enable	Logic low enables		0		V
Logic Level to Disable	Logic high disables		$V_P - 0.2$		V
Input Current	Logic high PWDN = 5 V		2		µA
	Logic low PWDN = 0 V		20		µA
Enable Time	PWDN low to OUTA, OUTB at 100% final value, CLPA, CLPB = open, RF in = −10 dBm		0.4		µs
Disable Time	PWDN high to OUTA, OUTB at 10% final value, CLPA, CLPB = open, RF in = 0 dBm		0.25		µs
POWER INTERFACE	VPSA, VPSB, VPSR				
Supply Voltage		3.3		5.5	V
Quiescent Current			60		mA
vs. Temperature	$-40°C \le T_A \le +85°C$		147		µA/°C
Disable Current	ADJA, ADJB = PWDN = V_P		<1		mA

[1] Slope and intercept are determined by calculating the best-fit line between the power levels of −40 dBm and −10 dBm at the specified input frequency.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage: VPSA, VPSB, VPSR	5.7 V
V_{SET} Voltage: VSTA, VSTB	0 to V_P
Input Power (Single-Ended, Re: 50 Ω) INHA, INLA, INHB, INLB	12 dBm
Internal Power Dissipation	420 mW
θ_{JA}	42°C/W
Maximum Junction Temperature	142°C
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

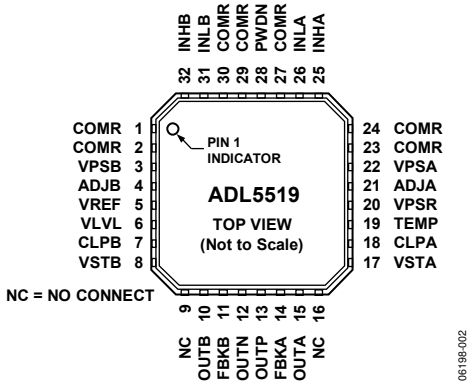

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	COMR	Connect via low impedance to common.
2	COMR	Connect via low impedance to common.
3	VPSB	Positive Supply for Channel B. Apply 3.3 V to 5.5 V supply voltage.
4	ADJB	Dual-Function Pin: Temperature Adjust Pin for Channel B and Power-Down Interface for OUTB.
5	VREF	Voltage Reference (1.15 V).
6	VLVL	DC Common-Mode Adjust for Difference Output.
7	CLPB	Loop Filter Pin for Channel B.
8	VSTB	Setpoint Control Input for Channel B.
9	NC	No Connect.
10	OUTB	Output Voltage for Channel B.
11	FBKB	Difference Op Amp Feedback Pin for OUTN Op Amp.
12	OUTN	Difference Output (OUTB − OUTA + VLVL).
13	OUTP	Difference Output (OUTA − OUTB + VLVL).
14	FBKA	Difference Op Amp Feedback Pin for OUTP Op Amp.
15	OUTA	Output Voltage for Channel A.
16	NC	No Connect.
17	VSTA	Setpoint Control Input for Channel A.
18	CLPA	Loop Filter Pin for Channel A.
19	TEMP	Temperature Sensor Output (1.3 V with 4.5 mV/°C Slope).
20	VPSR	Positive Supply for Difference Outputs and Temperature Sensor. Apply 3.3 V to 5.5 V supply voltage.
21	ADJA	Dual-Function Pin: Temperature Adjust Pin for Channel A and Power-Down Interface for OUTA.
22	VPSA	Positive Supply for Channel A. Apply 3.3 V to 5.5 V supply voltage.
23	COMR	Connect via low impedance to common.
24	COMR	Connect via low impedance to common.
25	INHA	AC-Coupled RF Input for Channel A.
26	INLA	AC-Coupled RF Common for Channel A.
27	COMR	Connect via low impedance to common.
28	PWDN	Power-Down for Difference Output and Temperature Sensor.
29	COMR	Connect via low impedance to common.
30	COMR	Connect via low impedance to common.
31	INLB	AC-Coupled RF Common for Channel B.
32	INHB	AC-Coupled RF Input for Channel B.
	Paddle	Internally connected to COMR.

TYPICAL PERFORMANCE CHARACTERISTICS

V_P = 5 V; T_A = +25°C, −40°C, +85°C; CLPA, CLPB = 1 µF. Colors: +25°C black, −40°C blue, +85°C red.

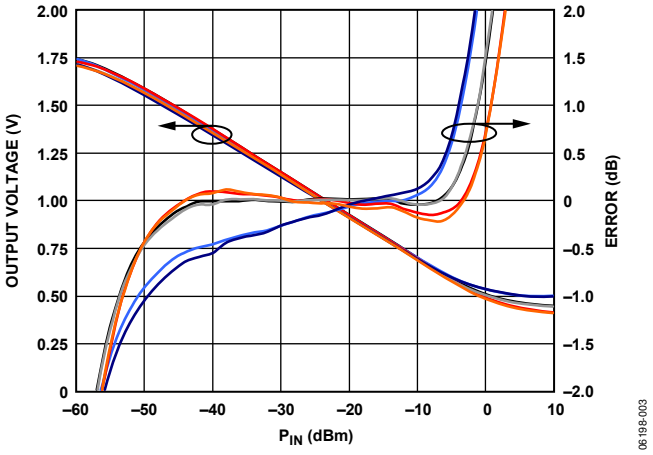

Figure 3. OUTA, OUTB Voltage and Log Conformance vs. Input Amplitude at 100 MHz, Typical Device, ADJA, ADJB = 0.65 V, 0.7 V, Sine Wave, Single-Ended Drive

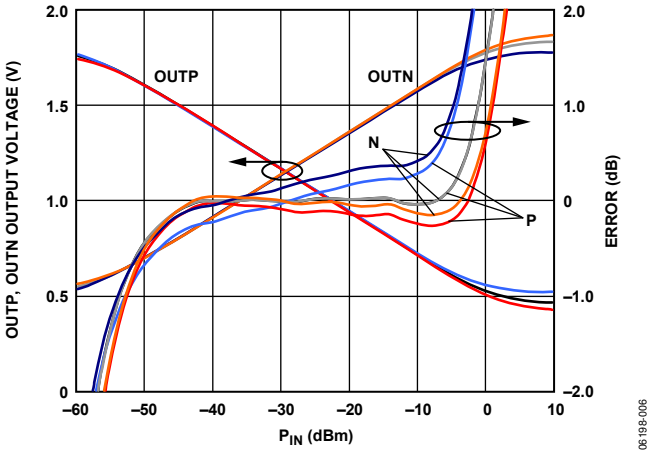

Figure 6. OUTP, OUTN Gain Error and Voltage vs. Input Amplitude at 100 MHz, Typical Device, ADJA, ADJB = 0.65 V, 0.7, Sine Wave, Single-Ended Drive, P_{INHB} = −30 dBm, Channel A Swept

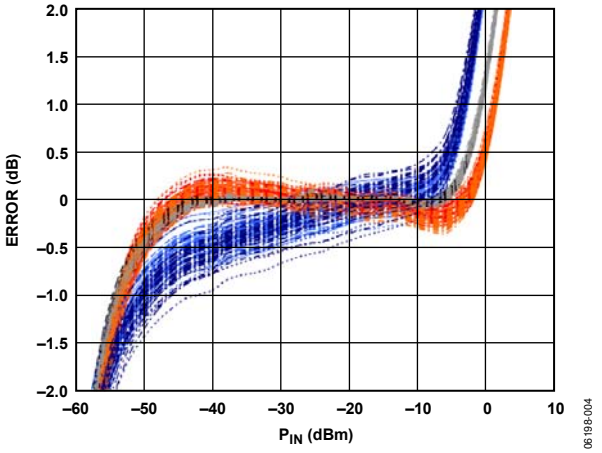

Figure 4. Distribution of OUTA, OUTB Error over Temperature After Ambient Normalization vs. Input Amplitude for 45 Devices, Frequency = 100 MHz, ADJA, ADJB = 0.65 V, 0.7 V, Sine Wave, Single-Ended Drive

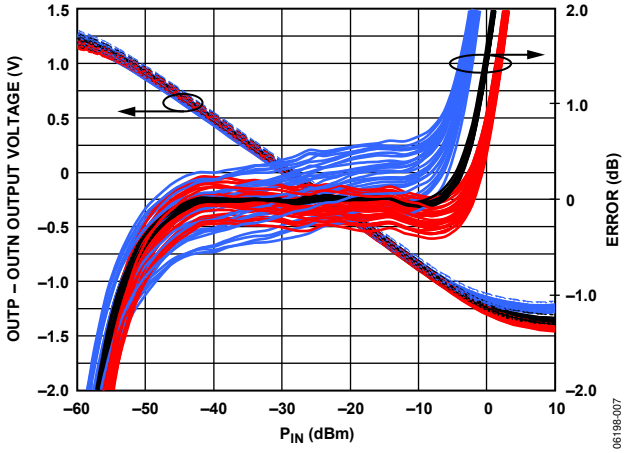

Figure 7. Distribution of [OUTP – OUTN] Gain Error and Voltage vs. Input Amplitude over Temperature, After Ambient Normalization for 45 Devices from a Nominal Lot, Frequency = 100 MHz, ADJA, ADJB = 0.65 V, 0.7 V, Sine Wave, Single-Ended Drive, P_{INHB} = −30 dBm, Channel A Swept

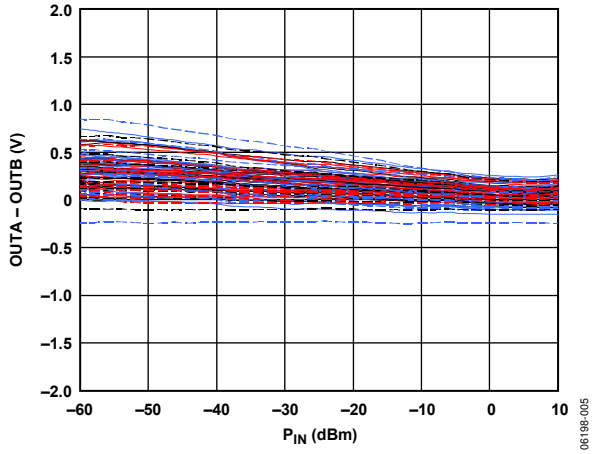

Figure 5. Distribution of [OUTA – OUTB] Voltage Difference over Temperature for 45 Devices from a Nominal Lot, Frequency = 100 MHz, ADJA, ADJB = 0.65 V, 0.7 V, Sine Wave, Single-Ended Drive

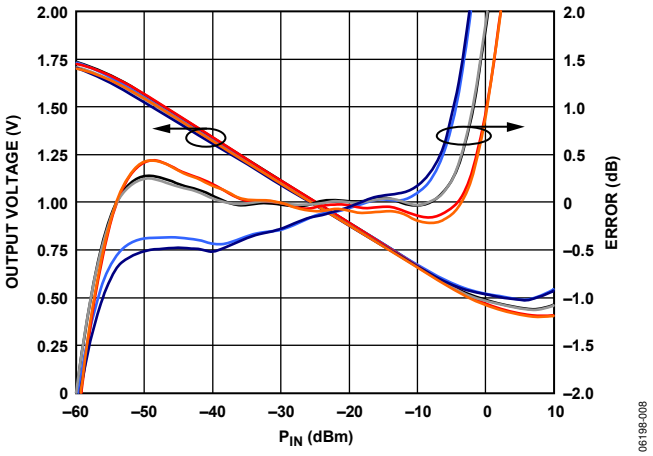

Figure 8. OUTA, OUTB Voltage and Log Conformance vs. Input Amplitude at 900 MHz, Typical Device, ADJA, ADJB = 0.6 V, 0.65 V, Sine Wave, Single-Ended Drive

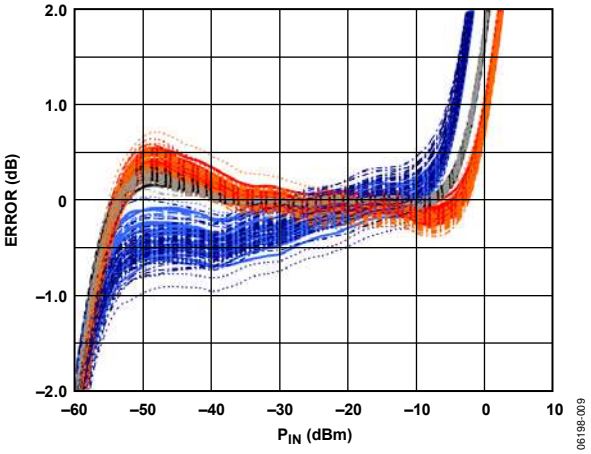

Figure 9. Distribution of OUTA, OUTB Error over Temperature After Ambient Normalization vs. Input Amplitude for 45 Devices, Frequency = 900 MHz, ADJA, ADJB = 0.6 V, 0.65 V, Sine Wave, Single-Ended Drive

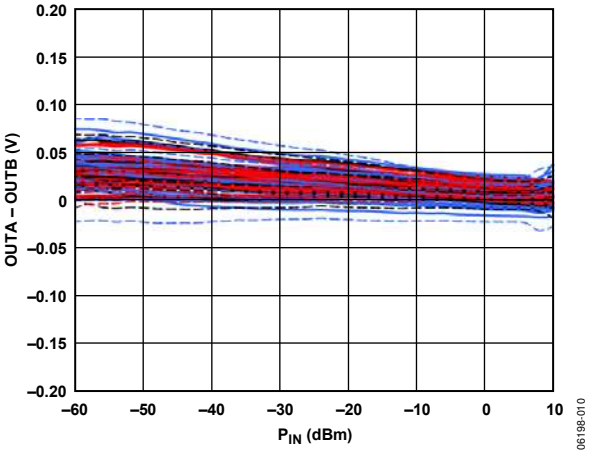

Figure 10. Distribution of [OUTA – OUTB] Voltage Difference over Temperature for 45 Devices from a Nominal Lot, Frequency = 900 MHz, ADJA, ADJB = 0.6 V, 0.65 V, Sine Wave, Single-Ended Drive

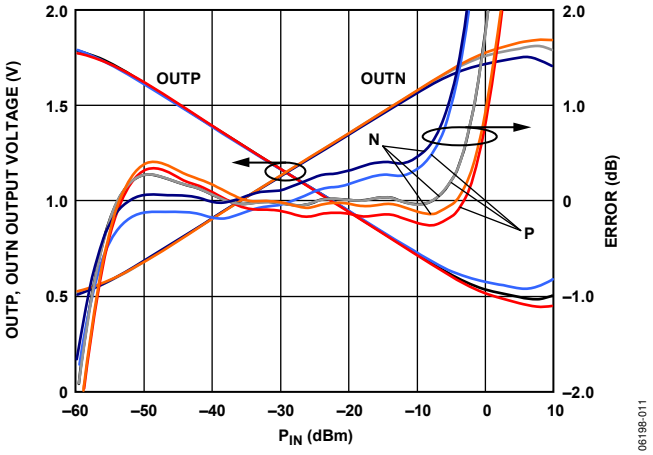

Figure 11. OUTP, OUTN Gain Error and Voltage vs. Input Amplitude at 900 MHz, Typical Device, ADJA, ADJB = 0.6 V, 0.65 V, Sine Wave, Single-Ended Drive; P_{INHB} = –30 dBm, Channel A Swept

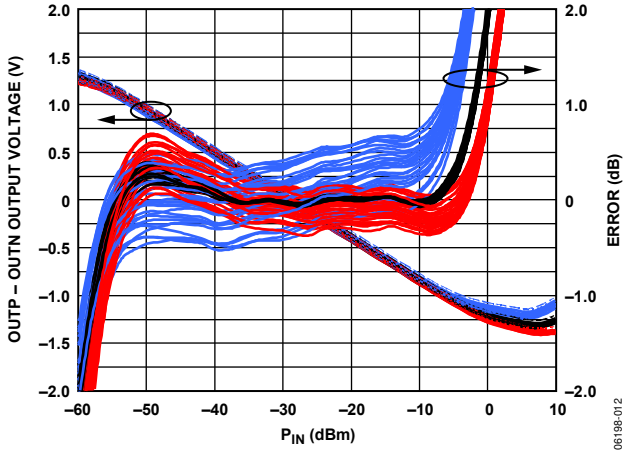

Figure 12. Distribution of [OUTP – OUTN] Gain Error and Voltage vs. Input Amplitude over Temperature, After Ambient Normalization for 45 Devices from a Nominal Lot, Frequency = 900 MHz, ADJA, ADJB = 0.6 V, 0.65 V, Sine Wave, Single-Ended Drive, P_{INHB} = –30 dBm, Channel A Swept

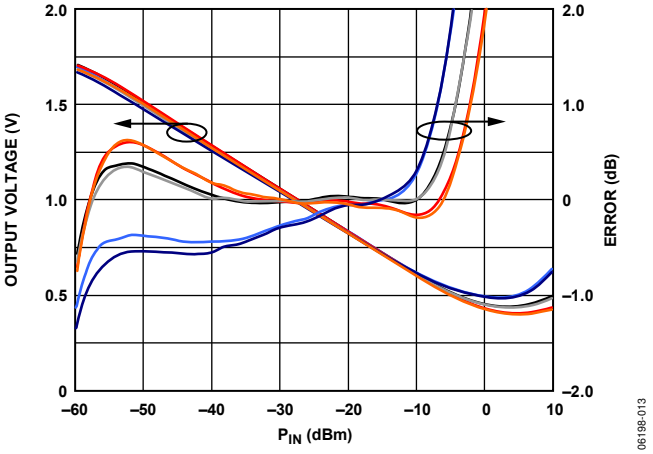

Figure 13. OUTA, OUTB Voltage and Log Conformance vs. Input Amplitude at 1.9 GHz, Typical Device, ADJA, ADJB = 0.5 V, 0.55 V, Sine Wave, Single-Ended Drive

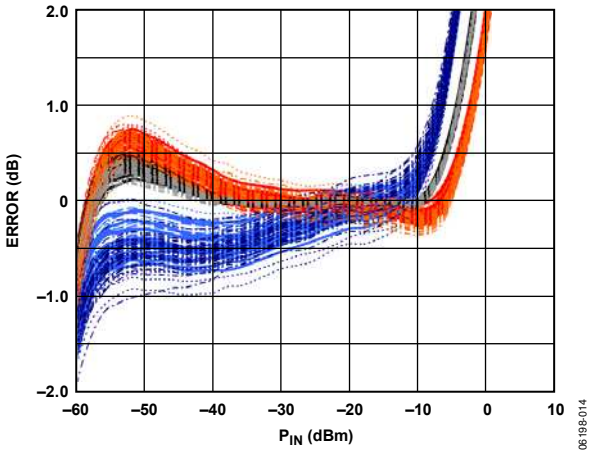

Figure 14. Distribution of OUTA, OUTB Error over Temperature After Ambient Normalization vs. Input Amplitude for 45 Devices, Frequency = 1.9 GHz, ADJA, ADJB = 0.5 V, 0.55 V, Sine Wave, Single-Ended Drive

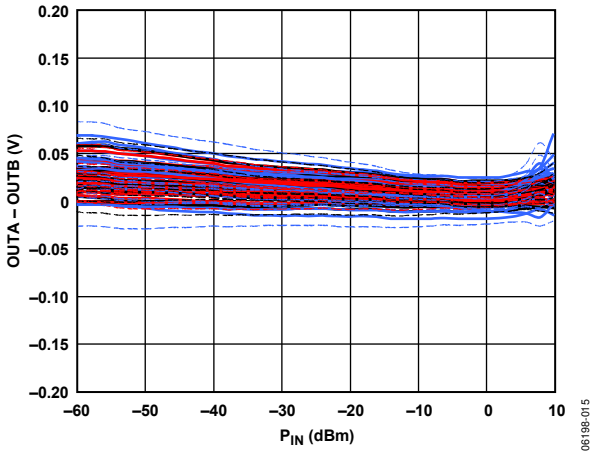

Figure 15. Distribution of [OUTA – OUTB] Voltage Difference over Temperature for 45 Devices from a Nominal Lot, Frequency = 1.9 GHz, ADJA, ADJB = 0.5 V, 0.55 V, Sine Wave, Single-Ended Drive

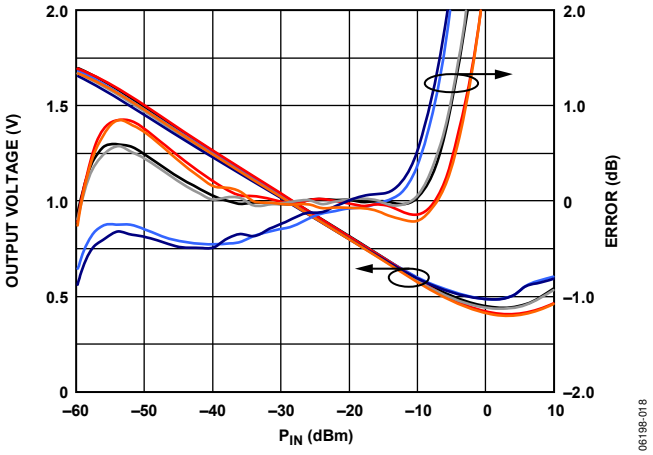

Figure 18. OUTA, OUTB Voltage and Log Conformance vs. Input Amplitude at 2.2 GHz, Typical Device, ADJA, ADJB = 0.48 V, 0.6 V, Sine Wave, Single-Ended Drive

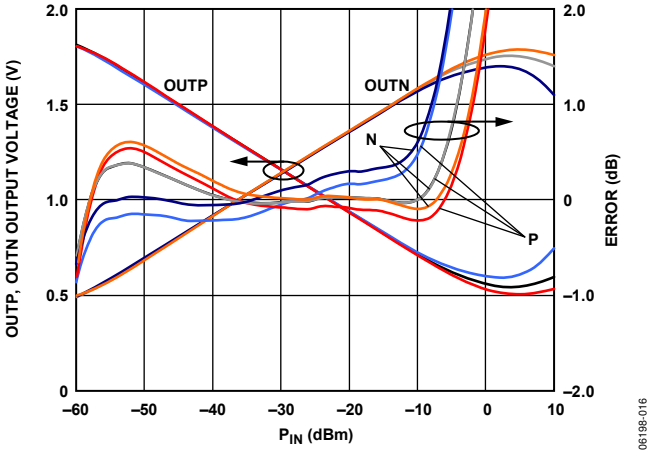

Figure 16. OUTP, OUTN Gain Error and Voltage vs. Input Amplitude at 1.9 GHz, with B Input Held at −30 dBm and A Input Swept, Typical Device, ADJA, ADJB = 0.5 V, 0.55 V, Sine Wave, Single-Ended Drive, P_{INHB} = −30 dBm, Channel A Swept

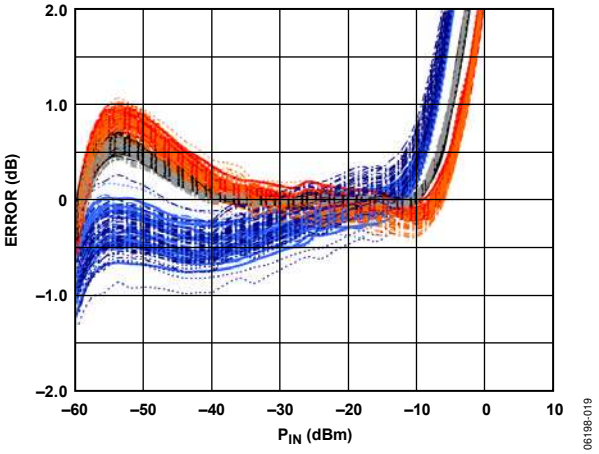

Figure 19. Distribution of OUTA, OUTB Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 45 Devices from a Nominal Lot, Frequency = 2.2 GHz, ADJA, ADJB = 0.48 V, 0.6 V, Sine Wave, Single-Ended Drive

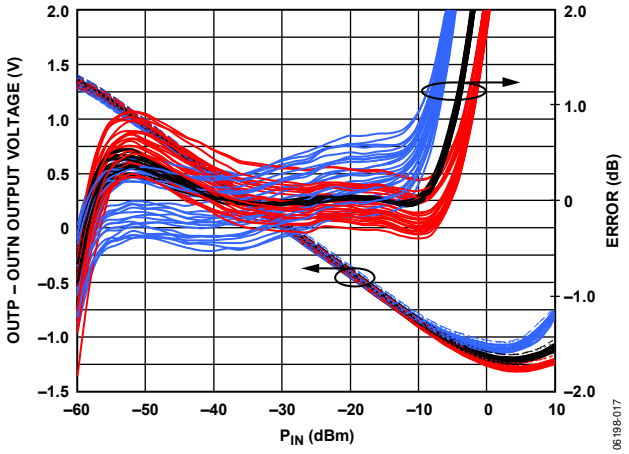

Figure 17. Distribution of [OUTP – OUTN] Gain Error and Voltage vs. Input Amplitude over Temperature, After Ambient Normalization for 45 Devices from a Nominal Lot, Frequency = 1.9 GHz, ADJA, ADJB = 0.5 V, 0.55 V, Sine Wave, Single-Ended Drive, P_{INHB} = −30 dBm, Channel A Swept

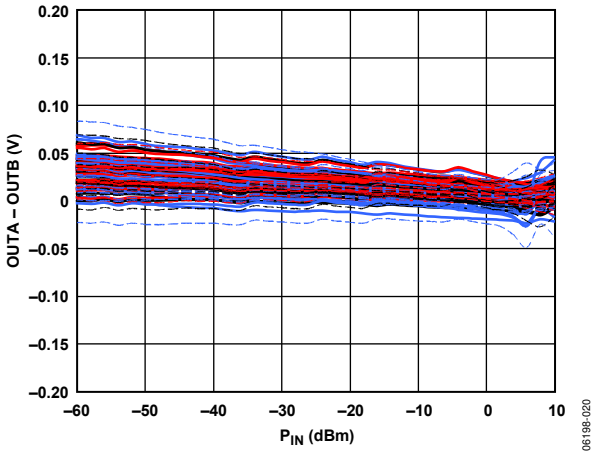

Figure 20. Distribution of [OUTA – OUTB] Voltage Difference over Temperature for 45 Devices from a Nominal Lot, Frequency = 2.2 GHz, ADJA, ADJB = 0.48 V, 0.6 V, Sine Wave, Single-Ended Drive

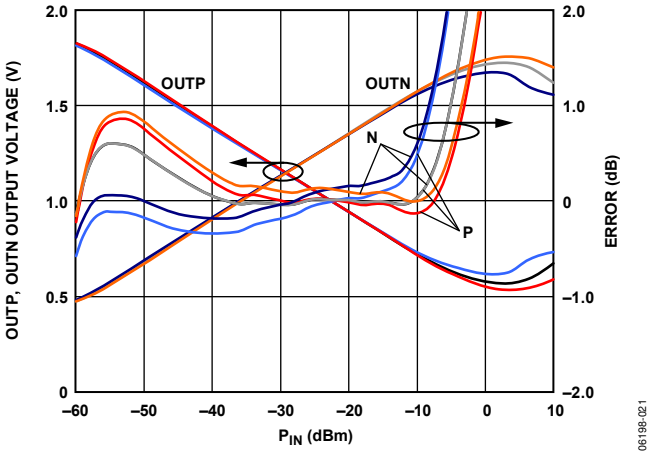

Figure 21. OUTP, OUTN Gain Error and Voltage vs. Input Amplitude at 2.2 GHz, Typical Device, ADJA, ADJB = 0.48 V, 0.6 V, Sine Wave, Single-Ended Drive, P_{INHB} = −30 dBm, Channel A Swept

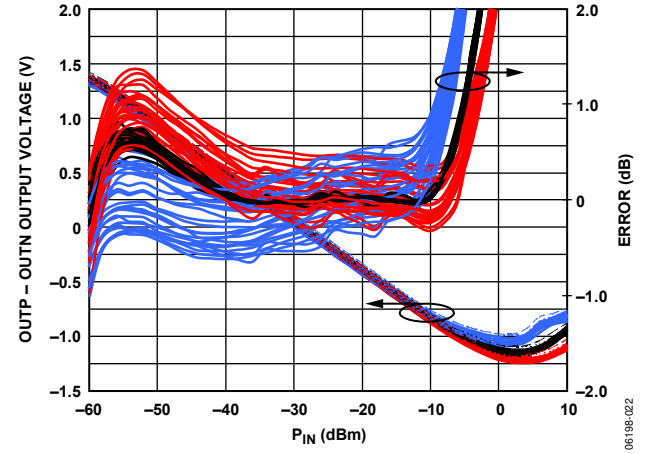

Figure 22. Distribution of [OUTP – OUTN] Gain Error and Voltage vs. Input Amplitude over Temperature, After Ambient Normalization for 45 Devices from a Nominal Lot, Frequency = 2.2 GHz, ADJA, ADJB = 0.48 V, 0.6 V, Sine Wave, Single-Ended Drive, P_{INHB} = −30 dBm, Channel A Swept

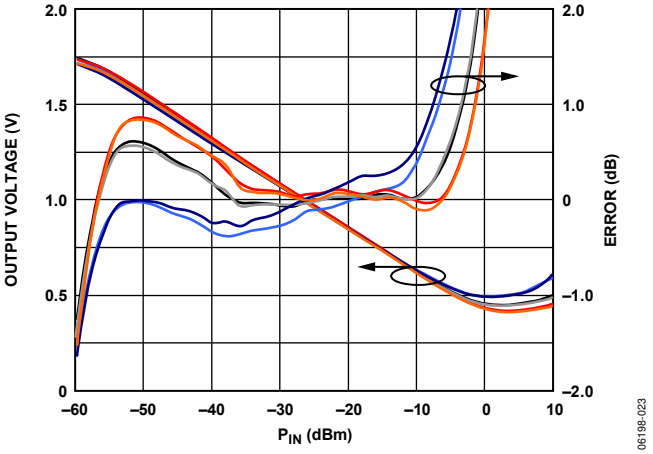

Figure 23. OUTA, OUTB Voltage and Log Conformance vs. Input Amplitude at 3.6 GHz, Typical Device, ADJA, ADJB = 0.35 V, 0.42 V, Sine Wave, Single-Ended Drive

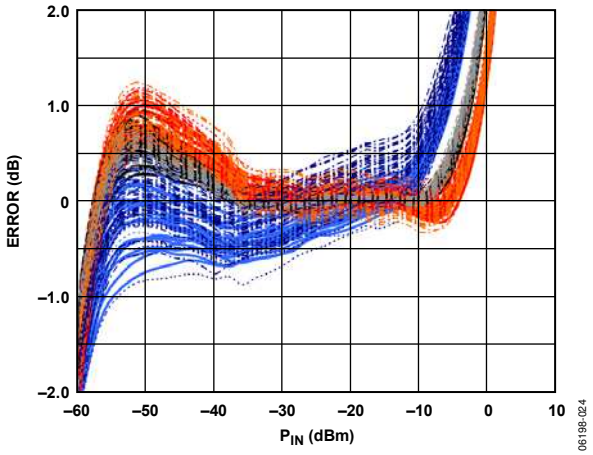

Figure 24. Distribution of OUTA, OUTB Error over Temperature After Ambient Normalization vs. Input Amplitude for 45 Devices from a Nominal Lot, Frequency = 3.6 GHz, ADJA, ADJB = 0.35 V, 0.42 V, Sine Wave, Single-Ended Drive

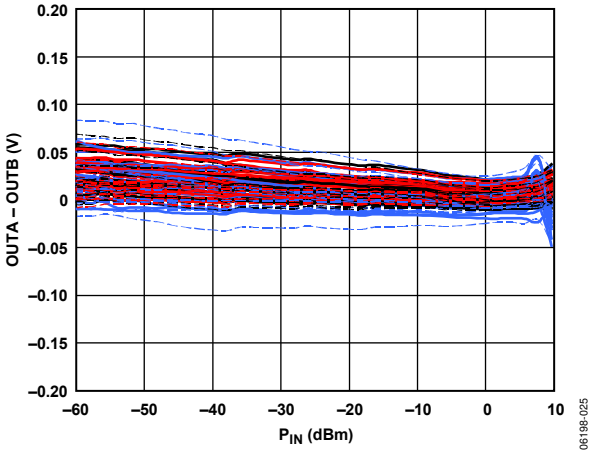

Figure 25. Distribution of [OUTA – OUTB] Voltage Difference over Temperature for 45 Devices from a Nominal Lot, Frequency = 3.6 GHz, ADJA, ADJB = 0.35 V, 0.42 V, Sine Wave, Single-Ended Drive

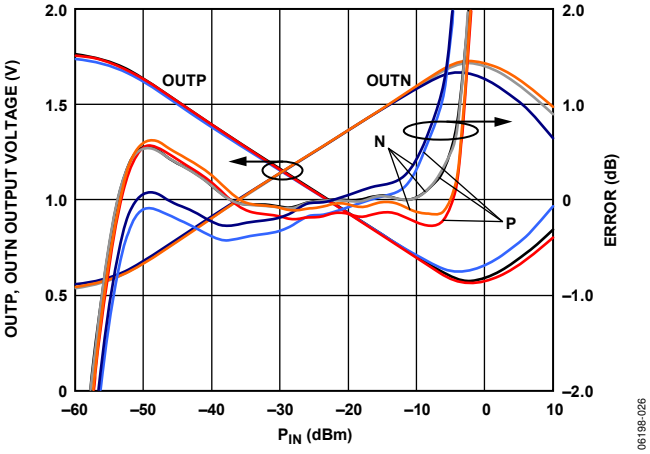

Figure 26. OUTP, OUTN Gain Error and Voltage vs. Input Amplitude at 3.6 GHz, Typical Device, ADJA, ADJB = 0.35 V, 0.42 V, Sine Wave, Single-Ended Drive; P_{INHB} = −30 dBm, Channel A Swept

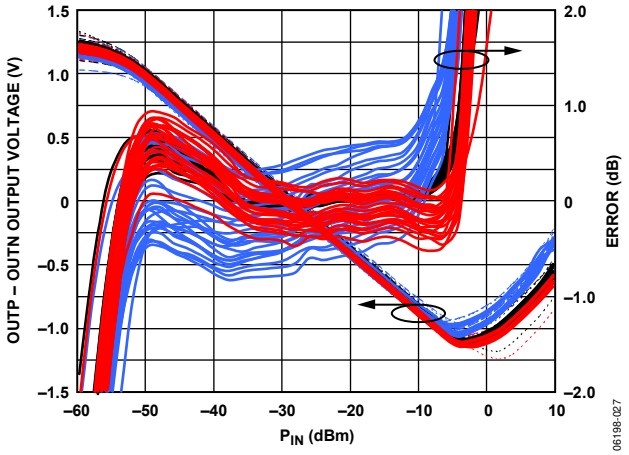

Figure 27. Distribution of [OUTP – OUTN] Gain Error and Voltage vs. Input Amplitude over Temperature, After Ambient Normalization for 45 Devices from a Nominal Lot, Frequency = 3.6 GHz, ADJA, ADJB = 0.35 V, 0.42 V, Sine Wave, Single-Ended Drive, P_{INHB} = −30 dBm, Channel A Swept

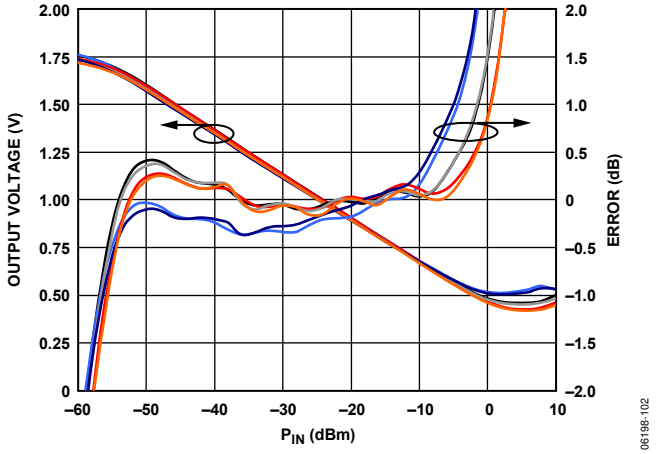

Figure 28. OUTA, OUTB Voltage and Log Conformance vs. Input Amplitude at 5.8 GHz, Typical Device, ADJA, ADJB = 0.58 V, 0.7 V, Sine Wave, Single-Ended Drive

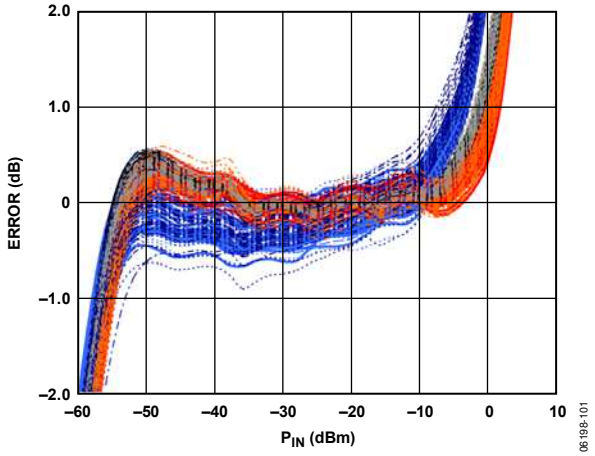

Figure 29. Distribution of OUTA, OUTB Error over Temperature After Ambient Normalization vs. Input Amplitude for at Least 15 Devices from Multiple Lots, Frequency = 5.8 GHz, ADJA, ADJB = 0.58 V, 0.7 V, Sine Wave, Single-Ended Drive

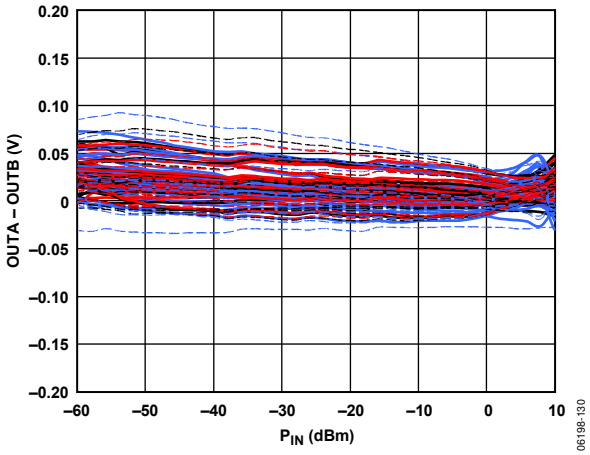

Figure 30. Distribution of [OUTA – OUTB] Voltage Difference over Temperature for 45 Devices from a Nominal Lot, Frequency = 5.8 GHz, ADJA, ADJB = 0.58 V, 0.7 V, Sine Wave, Single-Ended Drive

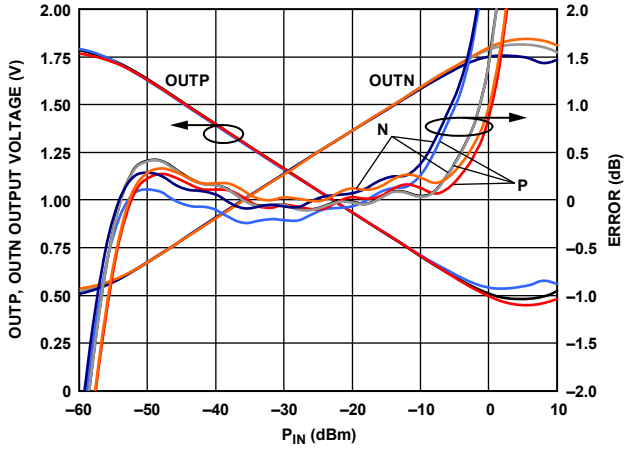

Figure 31. OUTP, OUTN Gain Error and Voltage vs. Input Amplitude at 5.8 GHz, Typical Device, ADJA, ADJB = 0.58 V, 0.7 V, Sine Wave, Single-Ended Drive, P_{INHB} = −30 dBm, Channel A Swept

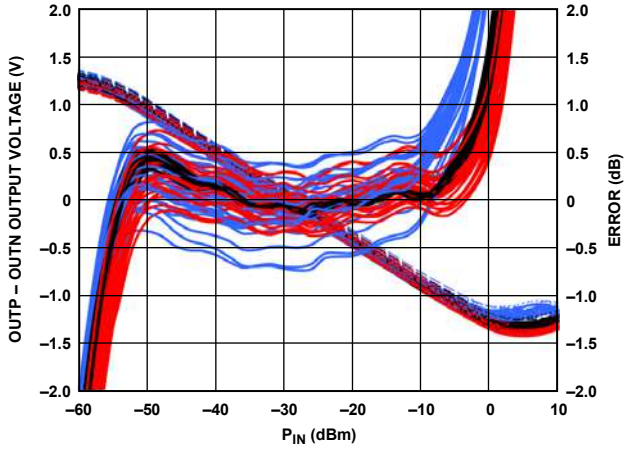

Figure 32. Distribution of [OUTP – OUTN] Gain Error and Voltage vs. Input Amplitude over Temperature, After Ambient Normalization for 45 Devices from a Nominal Lot, Frequency = 5.8 GHz, ADJA, ADJB = 0.58 V, 0.7 V, Sine Wave, Single-Ended Drive, P_{INHB} = −30 dBm, Channel A Swept

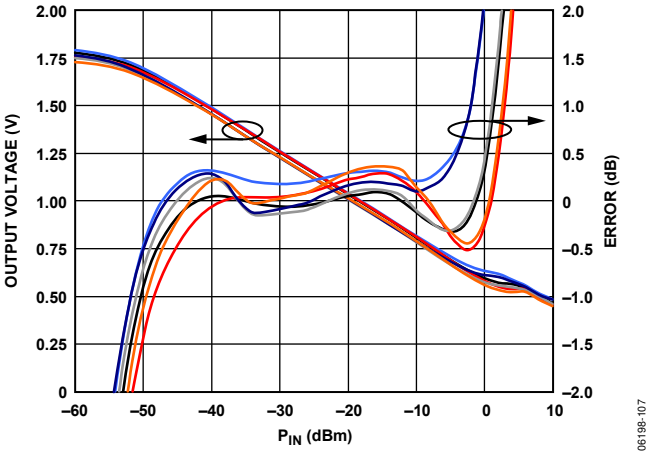

Figure 33. OUTA, OUTB Voltage and Log Conformance vs. Input Amplitude at 8 GHz, Typical Device, ADJA, ADJB = 0.72 V, 0.82 V, Sine Wave, Single-Ended Drive

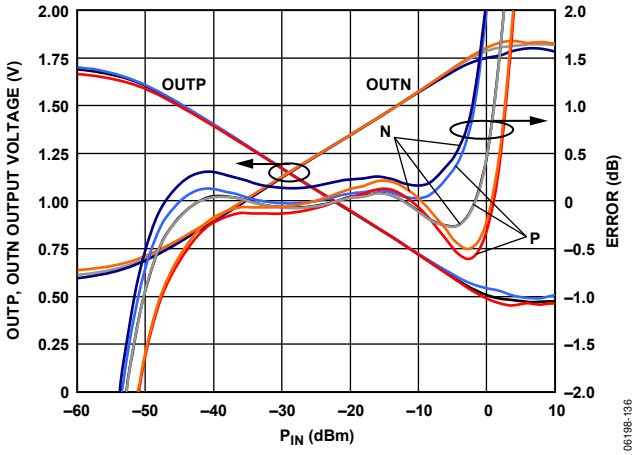

Figure 36. OUTP, OUTN Gain Error and Voltage vs. Input Amplitude at 8 GHz, Typical Device, ADJA, ADJB = 0.72 V, 0.82 V, Sine Wave, Single-Ended Drive, P_{INHB} = −30 dBm, Channel A Swept

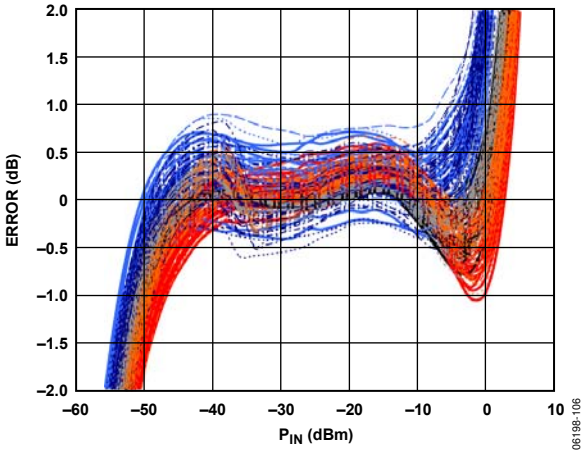

Figure 34. Distribution of OUTA, OUTB Error over Temperature After Ambient Normalization vs. Input Amplitude for 45 Devices from a Nominal Lot, Frequency = 8 GHz, ADJA, ADJB = 0.72 V, 0.82 V, Sine Wave, Single-Ended Drive

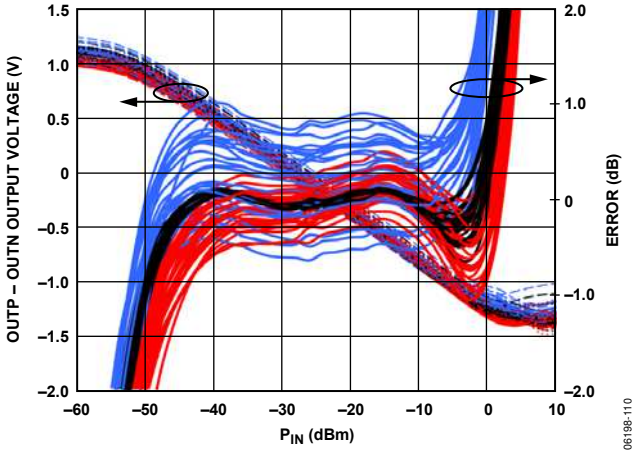

Figure 37. Distribution of [OUTP – OUTN] Gain Error and Voltage vs. Input Amplitude over Temperature, After Ambient Normalization for 45 Devices from a Nominal Lot, Frequency = 8 GHz, ADJA, ADJB = 0.72 V, 0.82 V, Sine Wave, Single-Ended Drive, P_{INHB} = −30 dBm, Channel A Swept

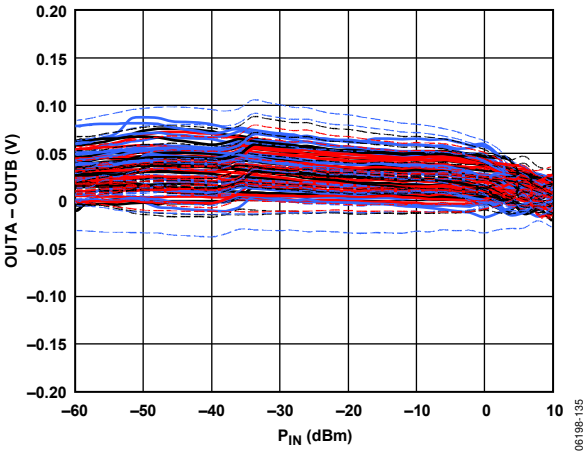

Figure 35. Distribution of [OUTA – OUTB] Voltage Difference over Temperature for 45 Devices from a Nominal Lot, Frequency = 8 GHz, ADJA, ADJB = 0.72 V, 0.82 V, Sine Wave, Single-Ended Drive

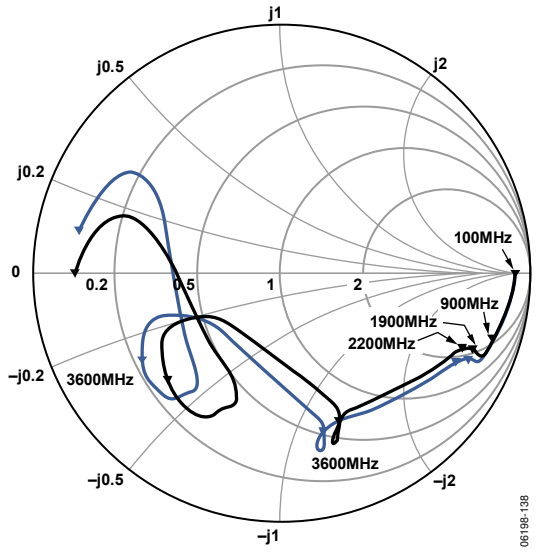

Figure 38. Single-Ended Input Impedance (S11) vs. Frequency; Z_O = 50 Ω

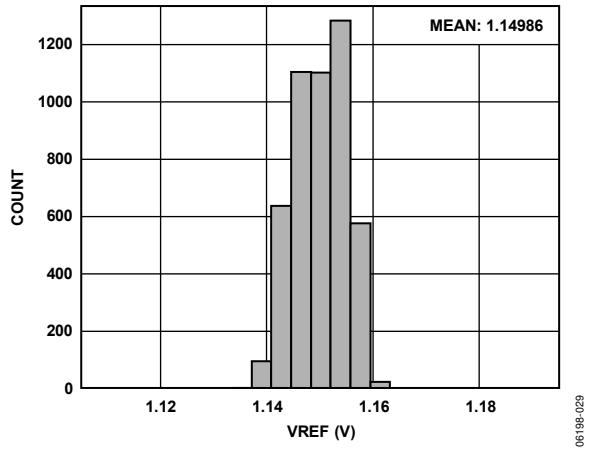

Figure 39. Distribution of VREF Pin Voltage for 4000 Devices

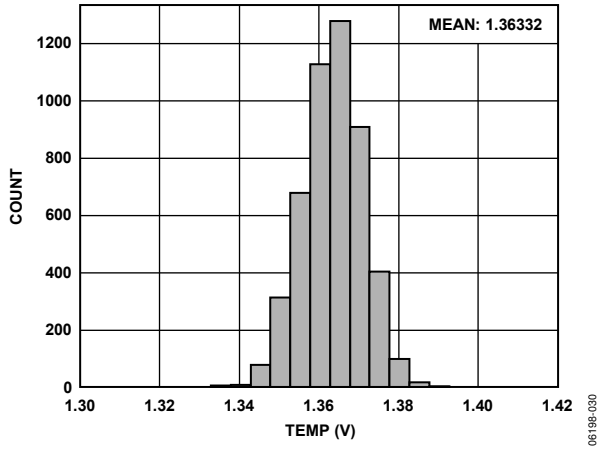

Figure 40. Distribution of TEMP Pin Voltage for 4000 Devices

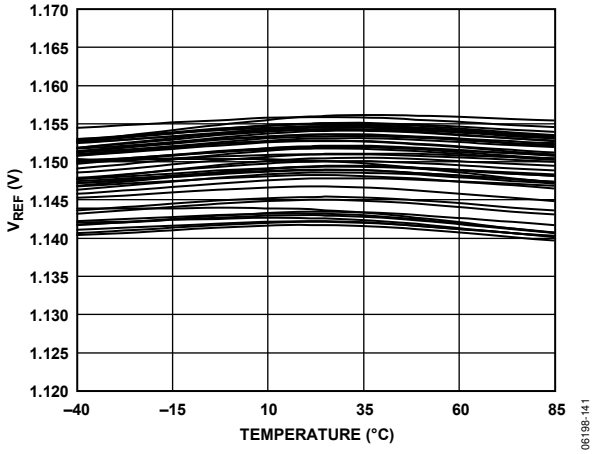

Figure 41. Change in VREF Pin Voltage vs. Temperature for 45 Devices

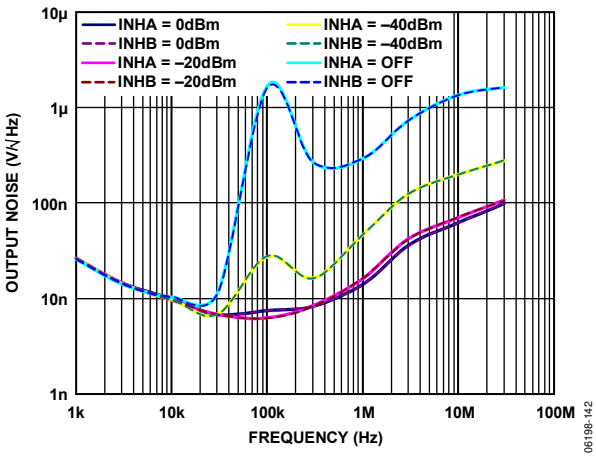

Figure 42. Noise Spectral Density of OUTA, OUTB; CLPA, CLPB = Open

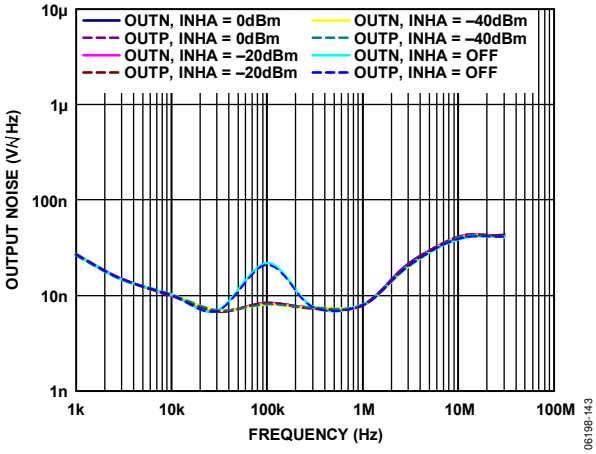

Figure 43. Noise Spectral Density of OUTP, OUTN; CLPA, CLPB = 0.1 µF, Frequency = 2140 MHz

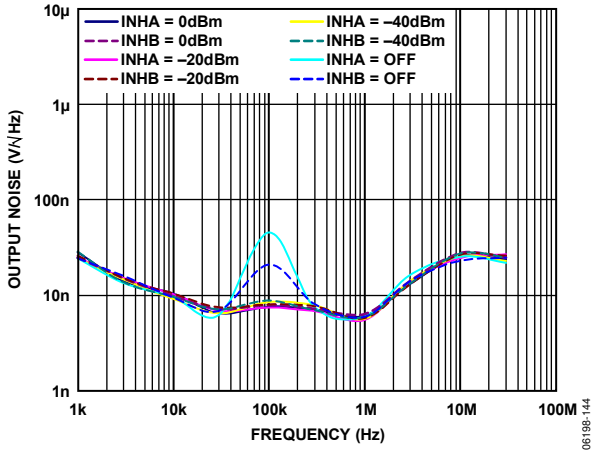

Figure 44. Noise Spectral Density of OUTA, OUTB; CLPA, CLPB = 0.1 µF, Frequency = 2140 MHz

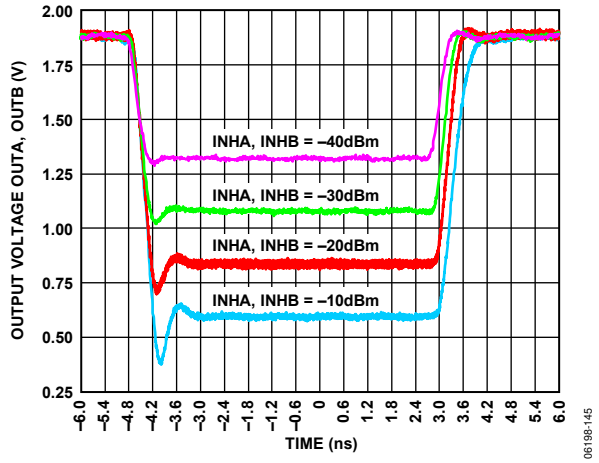

Figure 45. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency = 900 MHz, CLPA = Open

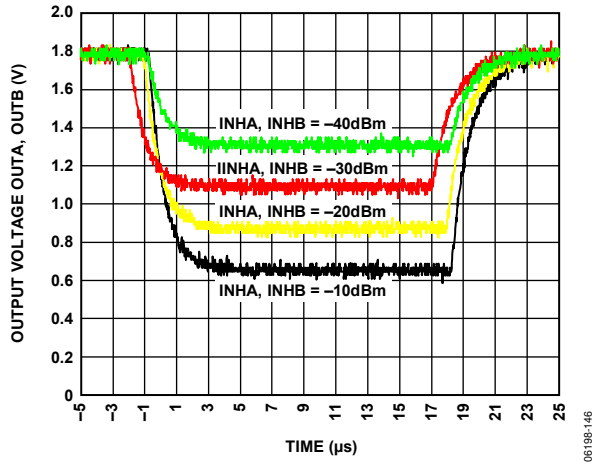

Figure 46. Output Response to RF Burst Input for Various RF Input Levels, Carrier Frequency = 900 MHz, CLPA = 0.1 µF

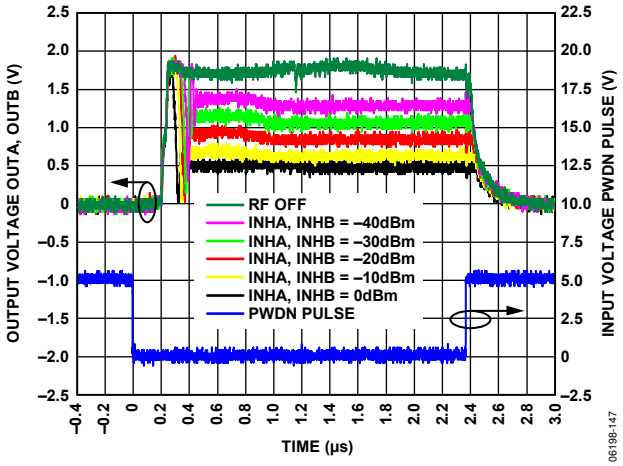

Figure 47. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency = 900 MHz, CLPA = Open

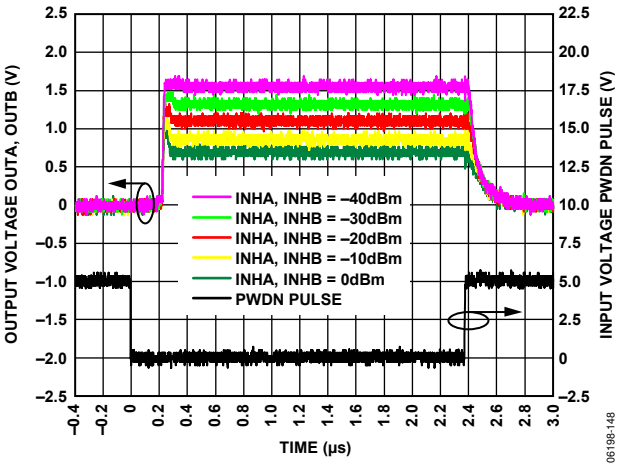

Figure 48. Output Response Using Power-Down Mode for Various RF Input Levels, Carrier Frequency = 900 MHz, CLPA = 0.1 µF

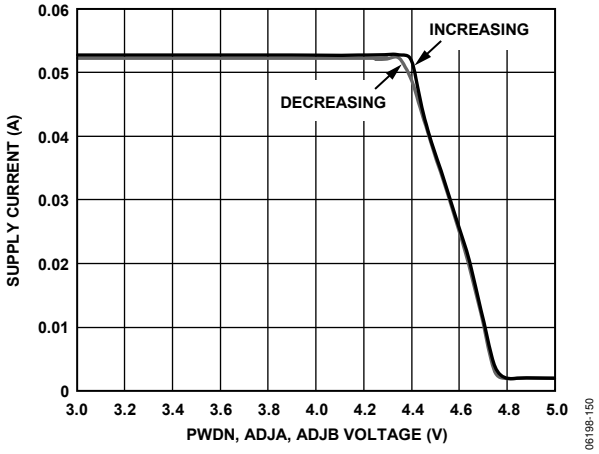

Figure 49. Supply Current vs. V_{PWDN}, V_{ADJA}, V_{ADJB}

THEORY OF OPERATION

The ADL5519 is a dual-channel, six-stage demodulating logarithmic amplifier that is specifically designed for use in RF measurement and power control applications at frequencies up to 10 GHz. The ADL5519 is a derivative of the AD8317 logarithmic detector/controller core. The ADL5519 maintains tight intercept variability vs. temperature over a 50 dB range. Each measurement channel offers performance equivalent to that of the AD8317. The complete circuit block diagram is shown in Figure 50.

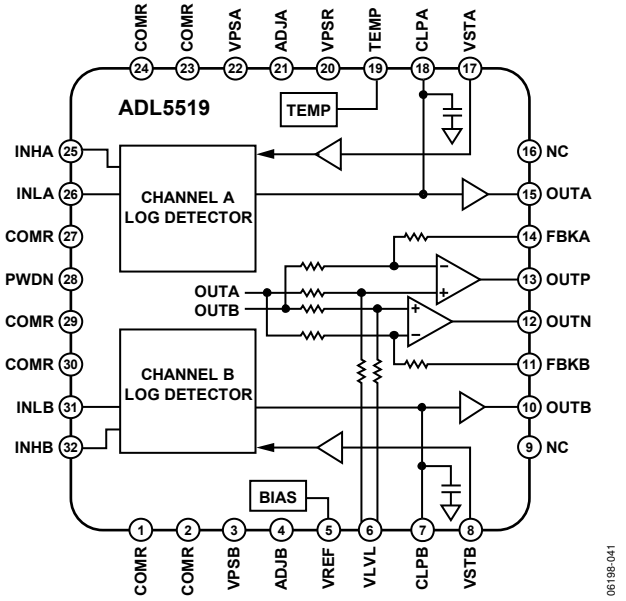

Figure 50. Block Diagram

Each measurement channel is a full differential design using a proprietary, high speed SiGe process that extends high frequency performance. Figure 51 shows the basic diagram of the Channel A signal path; its functionality is identical to that of the Channel B signal path.

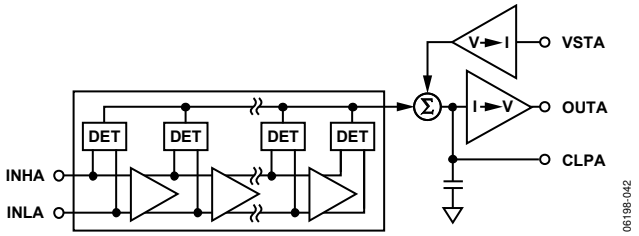

Figure 51. Single Channel Block Diagram

The maximum input with ±1 dB log conformance error is typically −5 dBm (re: 50 Ω). The noise spectral density referred to the input is 1.15 nV/√Hz, which is equivalent to a voltage of 118 μV rms in a 10.5 GHz bandwidth or a noise power of −66 dBm (re: 50 Ω). This noise spectral density sets the lower limit of the dynamic range. However, the low end accuracy of the ADL5519 is enhanced by specially shaping the demodulating transfer characteristic to partially compensate for errors due to internal noise. The common pins provide a quality, low impedance connection to the printed circuit board (PCB) ground. The package paddle, which is internally connected to the COMR pins, should also be grounded to the PCB to reduce thermal impedance from the die to the PCB.

The logarithmic function is approximated in a piecewise fashion by six cascaded gain stages. For a more comprehensive explanation of the logarithm approximation, refer to the AD8307 data sheet. The cells have a nominal voltage gain of 9 dB each, with a 3 dB bandwidth of 10.5 GHz. Using precision biasing, the gain is stabilized over temperature and supply variations. The overall dc gain is high because of the cascaded nature of the gain stages. An offset compensation loop is included to correct for offsets within the cascaded cells. At the output of each gain stage, a square-law detector cell is used to rectify the signal.

The RF signal voltages are converted to a fluctuating differential current, having an average value that increases with signal level. Along with the six gain stages and detector cells, an additional detector is included at the input of each measurement channel, providing a 54 dB dynamic range in total. After the detector currents are summed and filtered, the following function is formed at the summing node:

$$I_D \times \log_{10}(V_{IN}/V_{INTERCEPT}) \quad (1)$$

where:

I_D is the internally set detector current.

V_{IN} is the input signal voltage.

$V_{INTERCEPT}$ is the intercept voltage (that is, when $V_{IN} = V_{INTERCEPT}$, the output voltage would be 0 V, if it were capable of going to 0 V).

USING THE ADL5519

BASIC CONNECTIONS

The ADL5519 is specified for operation up to 10 GHz. As a result, low impedance supply pins with adequate isolation between functions are essential. A power supply voltage between 3.3 V and 5.5 V should be applied to VPSA, VPSB, and VPSR. Power supply decoupling capacitors of 100 pF and 0.1 µF should be connected close to these power supply pins (see Figure 53).

The paddle of the LFCSP package is internally connected to COMR. For optimum thermal and electrical performance, the paddle should be soldered to a low impedance ground plane.

INPUT SIGNAL COUPLING

The ADL5519 inputs are differential but were characterized and are generally used single ended. When using the ADL5519 in single-ended mode, the INHA, INHB pins must be ac-coupled, and INLA, INLB must be ac-coupled to ground. Suggested coupling capacitors are 47 nF, ceramic 0402-style capacitors for input frequencies of 1 MHz to 10 GHz. The coupling capacitors should be mounted close to the INHA, INHB and INLA, INLB pins. The coupling capacitor values can be increased to lower the input stage high-pass cutoff frequency.

The high-pass corner is set by the input coupling capacitors and the internal 10 pF high-pass capacitor. The dc voltage on INHA, INHB and INLA, INLB is approximately one diode voltage drop below the supply voltage.

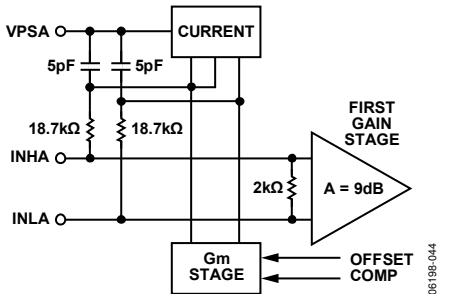

Figure 52. Single-Channel Input Interface

Although the input can be reactively matched, in general this reactive matching is not necessary. An external 52.3 Ω shunt resistor (connected on the signal side of the input coupling capacitors, as shown in Figure 53) combines with the relatively high input impedance to give an adequate broadband match of 50 Ω.

The coupling time constant, $50 \times C_C/2$, forms a high-pass corner with a 3 dB attenuation at $f_{HP} = 1/(2\pi \times 50 \times C_C)$, where C1 = C2 = C3 = C4 = C_C. Using the typical value of 47 nF, this high-pass corner is ~68 kHz. In high frequency applications, f_{HP} should be as large as possible to minimize the coupling of unwanted low frequency signals. In low frequency applications, a simple RC network forming a low-pass filter should be added at the input for similar reasons. This low-pass filter should generally be placed at the generator side of the coupling capacitors, thereby lowering the required capacitance value for a given high-pass corner frequency.

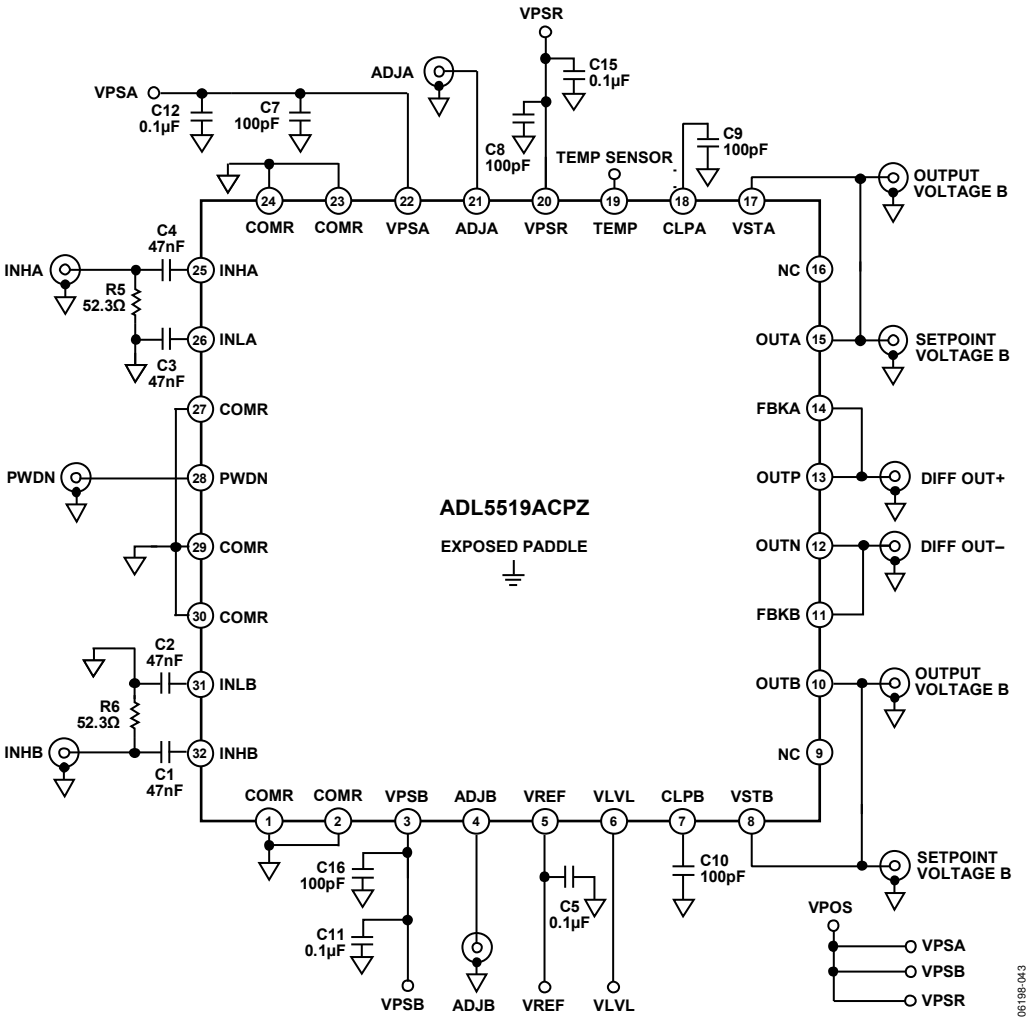

Figure 53. Basic Connections for Operation in Measurement Mode

TEMPERATURE SENSOR INTERFACE

The ADL5519 provides a temperature sensor output capable of driving 4 mA. The temperature scaling factor of the output voltage is ~4.48 mV/°C. The typical absolute voltage at 27°C is approximately 1.36 V.

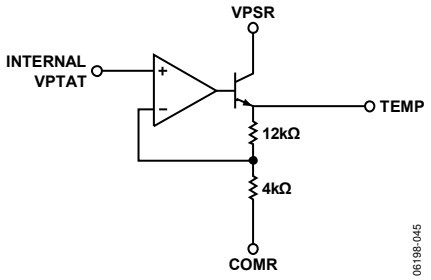

Figure 54. TEMP Interface Simplified Schematic

VREF INTERFACE

The VREF pin provides a highly stable voltage reference. The voltage on the VREF pin is 1.15 V, which is capable of driving 3 mA. An equivalent internal resistance is connected from VREF to COMR for 3 mA sink capability.

POWER-DOWN INTERFACE

The operating and stand-by currents for the ADL5519 at 27°C are approximately 60 mA and less than 1 mA, respectively. To completely power down the ADL5519, the PWDN and ADJA, ADJB pins must be pulled within 200 mV of the supply voltage. When powered on, the output reaches to within 0.1 dB of its steady-state value in about 0.5 µs; the reference voltage is available to full accuracy in a much shorter time.

This wake-up response time varies, depending on the input coupling network and the capacitance at the CLPA, CLPB pins. PWDN disables the OUTP, OUTN, VREF, and TEMP pins. The power-down pin, PWDN, is a high impedance pin.

The ADJA and ADJB pins, when pulled within 200 mV of the supply voltage, disable OUTA and OUTB, respectively.

SETPOINT INTERFACE—VSTA, VSTB

The VSTA, VSTB inputs are high impedance (40 kΩ) pins that drive inputs of internal op amps. The V_{SET} voltage appears across the internal 1.5 kΩ resistor to generate a current, I_{SET}. When a portion of V_{OUT} is applied to VSTA, VSTB, the feedback loop forces

$$-I_D \times \log_{10}(V_{IN}/V_{INTERCEPT}) = I_{SET} \quad (2)$$

If $V_{SET} = V_{OUT}/2x$, then $I_{SET} = V_{OUT}/(2x \times 1.5\ k\Omega)$.

The result is

$$V_{OUT} = (-I_D \times 1.5\ k\Omega \times 2x) \times \log_{10}(V_{IN}/V_{INTERCEPT})$$

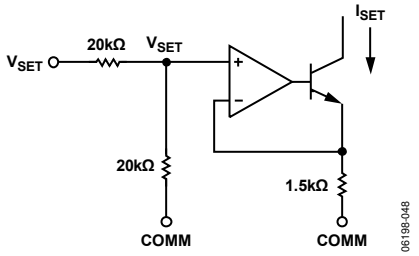

Figure 55. VSTA, VSTB Interface Simplified Schematic

The slope is given by $-I_D \times 2x \times 1.5\ k\Omega = -22\ mV/dB \times x$. For example, if a resistor divider to ground is used to generate a V_{SET} voltage of $V_{OUT}/2$, then x = 2. The slope is set to −880 V/decade or −44 mV/dB. See the Altering the Slope section for additional information.

OUTPUT INTERFACE—OUTA, OUTB

The OUTA, OUTB pins are driven by a push-pull output stage. The rise time of the output is limited mainly by the slew on CLPA, CLPB. The fall time is an RC-limited slew given by the load capacitance and the pull-down resistance at OUTA, OUTB. There is an internal pull-down resistor of 1.6 kΩ The resistive load at OUTA, OUTB can be placed in parallel with the internal pull-down resistor to reduce the discharge time. OUTA, OUTB can source greater than 10 mA.

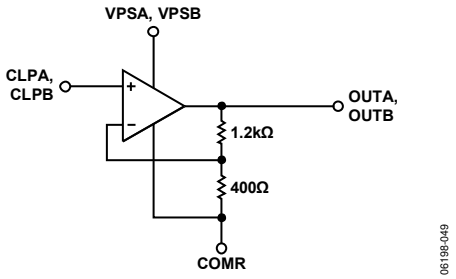

Figure 56. OUTA, OUTB Interface Simplified Schematic

DIFFERENCE OUTPUT—OUTP, OUTN

The ADL5519 incorporates two operational amplifiers with rail-to-rail output capability to provide a channel difference output.

As in the case of the output drivers for OUTA, OUTB, the output stages have the capability of driving greater than 10 mA. OUTA and OUTB are internally connected through 1 kΩ resistors to the inputs of each op amp. The VLVL pin is connected to the positive terminal of both op amps through 1 kΩ resistors to provide level shifting. The negative feedback terminal is also made available through a 1 kΩ resistor. The input impedance of VLVL is 1 kΩ, and the input impedance of FBKA, FBKB is 1 kΩ. See Figure 57 for the connections of these pins.

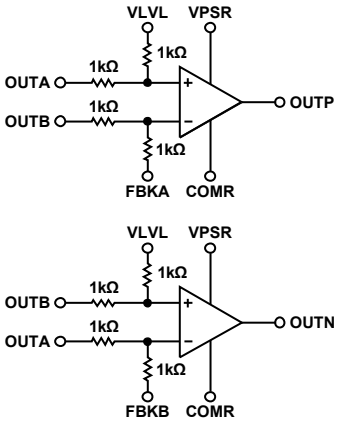

Figure 57. OUTP, OUTN Interface Simplified Schematic

If OUTP is connected to FBKA, OUTP is given as

$$OUTP = OUTA - OUTB + VLVL \quad (3)$$

If OUTN is connected to FBKB, OUTN is given as

$$OUTN = OUTB - OUTA + VLVL \quad (4)$$

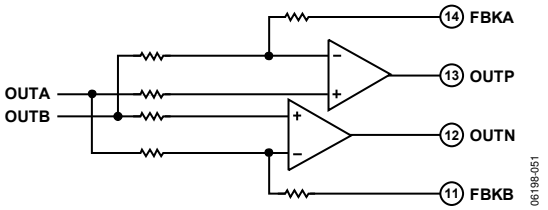

Figure 58. Op Amp Connections (All Resistors Are 1 kΩ ± 20%)

In this configuration, all four measurements, OUTA, OUTB, OUTP, and OUTN, are available simultaneously. A differential output can be taken from OUTP − OUTN, and VLVL can be used to adjust the common-mode level for an ADC connection. This is convenient not only for driving a differential ADC but also for removing any temperature variation on VLVL.

DESCRIPTION OF CHARACTERIZATION

The general hardware configuration used for most of the ADL5519 characterization is shown in Figure 59. The signal sources used in this example are the E8251A from Agilent Technologies. The INHA, INHB input pins are driven by Agilent signal sources, and the output voltages are measured using a voltmeter.

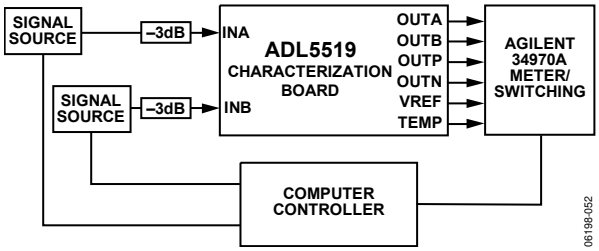

Figure 59. General Characterization Configuration

BASIS FOR ERROR CALCULATIONS

The input power and output voltage are used to calculate the slope and intercept values. The slope and intercept are calculated using linear regression over the input range from −40 dBm to −10 dBm. The slope and intercept terms are used to generate an ideal line. The error is the difference in measured output voltage compared to the ideal output line. This is a measure of the linearity of the device. Refer to the Device Calibration section for more information on calculating slope, intercept, and error.

Error from the linear response to the CW waveform is not a measure of absolute accuracy because it is calculated using the slope and intercept of each device. However, error verifies the linearity and the effects of modulation on device response. Similarly, at temperature extremes, error represents the output voltage variations from the 25°C ideal line performance. Data presented in the graphs is the typical error distribution observed during characterization of the ADL5519.

Pulse response of the ADL5519 is 6 ns/8 ns rise/fall times. For the fastest response time, the capacitance on OUTA, OUTB should be kept to a minimum. Any capacitance on the output pins should be counterbalanced with an equal capacitance on the CLPA, CLPB pins to prevent ringing on the output.

DEVICE CALIBRATION

The measured transfer function of the ADL5519 at 2.2 GHz is shown in Figure 60. The figure shows plots of both output voltage vs. input power and calculated error vs. input power. As the input power varies from −60 dBm to −5 dBm, the output voltage varies from 1.7 V to about 0.5 V.

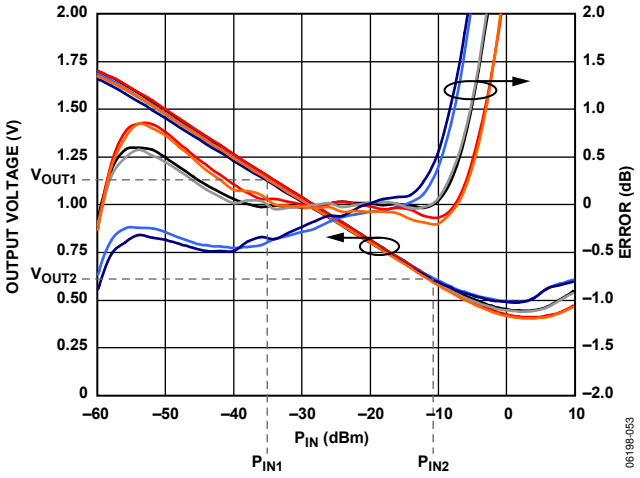

Figure 60. Transfer Function at 2.2 GHz with Calibration Points

Because slope and intercept vary from device to device, board-level calibration must be performed to achieve the highest accuracy. The equation for output voltage can be written as

$$V_{OUT} = Slope \times (P_{IN} - Intercept) \quad (6)$$

where:
Slope is the change in output voltage divided by the change in input power, P_{IN}, expressed in decibels (dB).
Intercept is the calculated power at which the output voltage would be 0 V. Note that an output voltage of 0 V can never be achieved.

In general, calibration is performed by applying two known signal levels to the ADL5519 input and measuring the corresponding output voltages. The calibration points are generally chosen to be within the linear-in-dB operating range of the device (see the Specifications section for more details).

Calculation of the slope and intercept is accomplished using the following equations:

$$Slope = (V_{OUT1} - V_{OUT2})/(P_{IN1} - P_{IN2}) \quad (7)$$

$$Intercept = P_{IN1} - (V_{OUT1}/Slope) \quad (8)$$

Once slope and intercept are calculated, an equation can be written that calculates the input power based on the output voltage of the detector.

$$P_{IN}\,(Unknown) = (V_{OUT1(MEASURED)}/Slope) + Intercept \quad (9)$$

The log conformance error of the calculated power is given by

$$Error\ (\text{dB}) = (V_{OUT(MEASURED)} - V_{OUT(IDEAL)})/Slope \quad (10)$$

Figure 60 includes a plot of the error at 25°C, the temperature at which the log amp is calibrated. Note that the error is not 0 dB over the full dynamic range. This is because the log amp does not perfectly follow the ideal V_{OUT} vs. P_{IN} equation, even within its operating region. The error at the calibration points of −35 dBm and −11 dBm is equal to 0 dB, by definition.

Figure 60 also shows error plots for the output voltage at −40°C and +85°C. These error plots are calculated using the slope and intercept at 25°C. This is consistent with calibration in a mass-production environment, where calibration over temperature is not practical.

ADJUSTING ACCURACY THROUGH CHOICE OF CALIBRATION POINTS

In some applications, very high accuracy is required at one power level or over a reduced input range. For example, in a wireless transmitter, the accuracy of the high power amplifier (HPA) is most critical at or close to full power.

In applications like AGC control loops, good linearity and temperature performance are necessary over a large input power range. The temperature crossover point (the power level at which there is no drift in performance from −40°C to −80°C) can be shifted from high power levels to midpower levels using the method shown in the Temperature Compensation Adjustment section. This shift equalizes the temperature performance over the complete power range. The linearity of the transfer function can be equalized by changing the calibration points.

Figure 61 demonstrates this equalization by changing the calibration points used in Figure 60 to −46 dBm and −22 dBm. This adjustment of the calibration points changes the linearity to greater than ±0.25 dB over a 50 dB dynamic range at the expense of a slight decrease in linearity at power levels between −40 dBm and −25 dBm.

Calibration points should be chosen to suit the application at hand. In general, however, do not choose calibration points in the nonlinear portion of the log amp transfer function (greater than −10 dBm or less than −40 dBm, in this example).

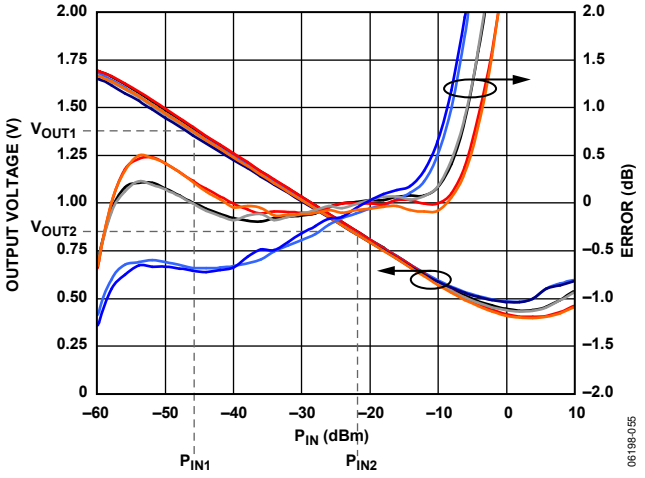

Figure 61. Dynamic Range Extension by Choosing Calibration Points That Are Close to the End of the Linear Range, 2.14 GHz