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FEATURES

- Power conversion gain of 1.6 dB
- Wideband RF, LO, and IF ports
- SSB noise figure of 11 dB
- Input IP3 of 28 dBm
- Input P1dB of 12 dBm
- Typical LO drive of 0 dBm
- Low LO leakage
- Single supply operation: 5 V @ 240 mA
- Exposed paddle, 4 mm × 4 mm, 24-lead LFCSP package

APPLICATIONS

- Cellular base station receivers
- Main and diversity receiver designs
- Radio link downconverters

GENERAL DESCRIPTION

The ADL5802 uses high linearity, double-balanced, active mixer cores with integrated LO buffer amplifiers to provide high dynamic range frequency conversion from 100 MHz to 6 GHz. The mixers benefit from a proprietary linearization architecture that provides enhanced input IP3 performance when subject to high input levels. A bias adjust feature allows the input linearity, SSB noise figure, and dc current to be optimized using a single control pin. The high input linearity allows the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in degradation in dynamic performance. The balanced active mixer arrangement provides superb LO to RF and LO to IF leakage, typically better than -30 dBm.

FUNCTIONAL BLOCK DIAGRAM

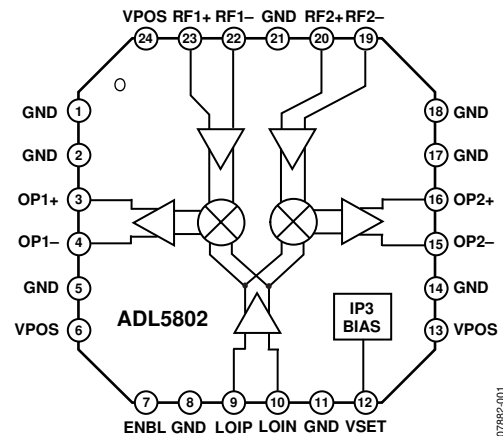


Figure 1.

The IF outputs are designed for a 200 Ω source impedance and provide a typical voltage conversion gain of 7.6 dB when loaded into a 200 Ω load.

The ADL5802 is fabricated using a SiGe high performance IC process. The device is available in a compact 4 mm × 4 mm, 24-lead LFCSP package and operates over a -40°C to +85°C temperature range. An evaluation board is also available.

ADL5802* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADL5802 Evaluation Board

DOCUMENTATION

Data Sheet

- ADL5802: Dual Channel, High IP3, 100MHz to 6GHz Active Mixer Sheet

TOOLS AND SIMULATIONS

- ADIsimPLL™
- ADIsimRF

REFERENCE MATERIALS

Press

- Analog Devices' 4-GHz PLL Synthesizer Offers Leading Phase Noise Performance
- New Analog Devices' PLL Synthesizers Deliver Utmost Flexibility and Phase Noise Performance

Product Selection Guide

- RF Source Booklet

DESIGN RESOURCES

- ADL5802 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADL5802 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

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REVISION HISTORY

2/15—Rev. A to Rev. B

Updated Outline Dimensions	29
Changes to Ordering Guide	29

6/12—Rev. 0 to Rev. A

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11/09—Revision 0: Initial Version

SPECIFICATIONS

$V_S = 5\text{ V}$, $V_{SET} = 4\text{ V}$, $T_A = 25^\circ\text{C}$, $f_{LO} = (f_{RF} - 153)\text{ MHz}$, LO power = 0 dBm, $Z_0^1 = 50\ \Omega$, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20 dB over a limited bandwidth		18		dB
Input Impedance			50		Ω
RF Frequency Range		100		6000	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, $f = 200\text{ MHz}$		240		Ω
IF Frequency Range	Can be matched externally to 3000 MHz	LF		600	MHz
DC Bias Voltage ²	Externally generated	4.75	V_S	5.25	V
LO INTERFACE					
LO Power		-10	0	+10	dBm
Return Loss			18		dB
Input Impedance			50		Ω
LO Frequency Range		100		6000	MHz
POWER INTERFACE					
Supply Voltage		4.75	5	5.25	V
Quiescent Current	Resistor programmable		220	300	mA
Disable Current	ENBL pin low		170		mA
Enable Time	Time from ENBL pin low to power-up		182		ns
Disable Time	Time from ENBL pin high to power-down		28		ns
DYNAMIC PERFORMANCE at $f_{RF} = 900\text{ MHz}/1900\text{ MHz}$					
Power Conversion Gain ³	$f_{RF} = 900\text{ MHz}$		1.5		dB
	$f_{RF} = 1900\text{ MHz}$		1.6		dB
Voltage Conversion Gain ⁴	$f_{RF} = 900\text{ MHz}$		7.5		dB
	$f_{RF} = 1900\text{ MHz}$		7.6		dB
SSB Noise Figure	$f_{CENT} = 900\text{ MHz}$		10		dB
	$f_{CENT} = 1900\text{ MHz}$		11		dB
SSB Noise Figure Under Blocking ⁵	$f_{CENT} = 900\text{ MHz}$		18		dB
	$f_{CENT} = 1900\text{ MHz}$		22		dB
Input Third Order Intercept ⁶	$f_{CENT} = 890\text{ MHz}$		26		dBm
	$f_{CENT} = 1890\text{ MHz}$		28		dBm
Input Second Order Intercept ⁷	$f_{CENT} = 890\text{ MHz}$		60		dBm
	$f_{CENT} = 1890\text{ MHz}$		45		dBm
Input 1 dB Compression Point	$f_{RF} = 900\text{ MHz}$		12		dBm
	$f_{RF} = 1900\text{ MHz}$		12		dBm
LO to IF Output Leakage	Unfiltered IF output		-35		dBm
LO to RF Input Leakage			-30		dBm
RF to IF Output Isolation			25		dBc
RFI1 to RFI2 Channel Isolation			45		dBc
IF/2 Spurious ⁸	0 dBm input power, $f_{RF} = 900\text{ MHz}$		-68		dBc
IF/3 Spurious ⁸	0 dBm input power, $f_{RF} = 900\text{ MHz}$		-67		dBc
IF/2 Spurious ⁸	0 dBm input power, $f_{RF} = 1900\text{ MHz}$		-53		dBc
IF/3 Spurious ⁸	0 dBm input power, $f_{RF} = 1900\text{ MHz}$		-59		dBc
DYNAMIC PERFORMANCE at $f_{RF} = 2500\text{ MHz}$ ⁹					
Power Conversion Gain ¹⁰			-0.5		dB
Voltage Conversion Gain ⁴			5.67		dB
SSB Noise Figure			11.5		dB
SSB Noise Figure Under Blocking ¹¹	$f_{CENT} = 2145\text{ MHz}$		18		dB
Input Third Order Intercept ⁶	$f_{CENT} = 2500\text{ MHz}$		30		dBm

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Input Second Order Intercept ⁷	$f_{CENT} = 2500$ MHz		47		dBm
Input 1 dB Compression Point			13		dBm
LO to IF Output Leakage	Unfiltered IF output		36		dBm
LO to RF Input Leakage			31		dBm
RF to IF Output Isolation			26		dBc
RF11 to RF12 Channel Isolation			42		dBc
IF/2 Spurious ⁸	0 dBm input power		-52		dBc
IF/3 Spurious ⁸	0 dBm input power		-56		dBc
DYNAMIC PERFORMANCE at $f_{RF} = 3500$ MHz ¹²					
Power Conversion Gain ¹³			-0.5		dB
Voltage Conversion Gain ⁴			5.5		dB
SSB Noise Figure			12.5		dB
SSB Noise Figure Under Blocking ¹⁴	$f_{CENT} = 3500$ MHz		18		dB
Input Third Order Intercept ⁵	$f_{CENT} = 3500$ MHz		25		dBm
Input Second Order Intercept ⁷	$f_{CENT} = 3500$ MHz		39		dBm
Input 1 dB Compression Point			13		dBm
LO to IF Output Leakage	Unfiltered IF output		33		dBm
LO to RF Input Leakage			28		dBm
RF to IF Output Isolation			31		dBc
RF11 to RF12 Channel Isolation			39		dBc
IF/2 Spurious ⁸	0 dBm input power		-46		dBc
IF/3 Spurious ⁸	0 dBm input power		-63		dBc
DYNAMIC PERFORMANCE at $f_{RF} = 5500$ MHz ¹⁵					
Power Conversion Gain ¹⁶			-3		dB
Voltage Conversion Gain ⁴			5.67		dB
SSB Noise Figure			14		dB
SSB Noise Figure Under Blocking ¹⁷	$f_{CENT} = 5800$ MHz		17		dB
Input Third Order Intercept ⁵	$f_{CENT} = 5500$ MHz		23		dBm
Input Second Order Intercept ⁷	$f_{CENT} = 5500$ MHz		35		dBm
Input 1 dB Compression Point			13		dBm
LO to IF Output Leakage	Unfiltered IF output		42		dBm
LO to RF Input Leakage			27		dBm
RF to IF Output Isolation			50		dBc
RF11 to RF12 Channel Isolation			33		dBc
IF/2 Spurious ⁸	0 dBm input power		-49		dBc
IF/3 Spurious ⁸	0 dBm input power		-64		dBc

¹ Z_0 is the characteristic impedance assumed for all measurements and the PCB.

² Supply voltage must be applied from an external circuit through choke inductors.

³ Excluding 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (TC1-1-13M+), and PCB loss.

⁴ $Z_{SOURCE} = 50 \Omega$, differential; $Z_{LOAD} = 200 \Omega$, differential 5 dBm; Z_{SOURCE} is the impedance of the source instrument; Z_{LOAD} is the load impedance at the output.

⁵ $f_{RF1} = f_{CENT}$, $f_{BLOCKER} = (f_{CENT} - 5)$ MHz, $f_{LO} = (f_{CENT} - 153)$ MHz, blocker level = 0 dBm.

⁶ $f_{RF1} = (f_{CENT} - 1)$ MHz, $f_{RF2} = f_{CENT}$, $f_{LO} = (f_{CENT} - 153)$ MHz, each RF tone at -10 dBm.

⁷ $f_{RF1} = f_{CENT}$, $f_{RF2} = (f_{CENT} + 100)$ MHz, $f_{LO} = (f_{CENT} - 153)$ MHz, each RF tone at -10 dBm.

⁸ For details, see the Spur Performance section.

⁹ $V_S = 5$ V, $V_{SET} = 4.5$ V, $T_A = 25^\circ\text{C}$, $f_{LO} = (f_{RF} - 211)$ MHz, LO power = 0 dBm, $Z_0 = 50 \Omega$.

¹⁰ Excluding 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (2500BL14M050), and PCB loss.

¹¹ $f_{RF1} = f_{CENT}$, $f_{BLOCKER} = (f_{CENT} - 5)$ MHz, $f_{LO} = (f_{CENT} - 235)$ MHz, blocker level = 0 dBm.

¹² $V_S = 5$ V, $V_{SET} = 5$ V, $T_A = 25^\circ\text{C}$, $f_{LO} = (f_{RF} - 153)$ MHz, LO power = 0 dBm, $Z_0 = 50 \Omega$.

¹³ Including 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (3600BL14M050), and PCB loss.

¹⁴ $f_{RF1} = f_{CENT}$, $f_{BLOCKER} = (f_{CENT} - 5)$ MHz, $f_{LO} = (f_{CENT} - 153)$ MHz, blocker level = -20 dBm.

¹⁵ $V_S = 5$ V, $V_{SET} = 4.8$ V, $T_A = 25^\circ\text{C}$, $f_{LO} = (f_{RF} - 380)$ MHz, LO power = 0 dBm, $Z_0 = 50 \Omega$.

¹⁶ Including 4:1 IF port transformer (TC4-1W+), RF and LO port transformers (5400BL15B050), and PCB loss.

¹⁷ $f_{RF1} = f_{CENT}$, $f_{BLOCKER} = (f_{CENT} - 5)$ MHz, $f_{LO} = (f_{CENT} - 300)$ MHz, blocker level = -20 dBm.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, VPOS	5.5 V
VSET, ENBL	5.5 V
OP1+, OP1–, OP2+, OP2–	5.5 V
RF Input Power	20 dBm
Internal Power Dissipation	1.6 W
θ_{JA} (Exposed Paddle Soldered Down) ¹	26.5°C/W
θ_{JC} (at Exposed Paddle)	8.7°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C

¹ As measured on the evaluation board. For details, see the Evaluation Board section.

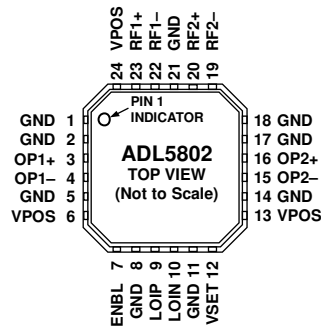
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



07862-002

- NOTES
 1. THERE IS AN EXPOSED PADDLE THAT MUST BE SOLDERED TO GROUND.

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1, 2, 5, 8, 11, 14, 17, 18, 21	GND	Device Common (DC Ground).
3, 4	OP1+, OP1-	Channel 1 Mixer Differential Output Terminals. Bias must be applied through pull-up choke inductors or the center tap of the IF transformer.
6, 13, 24	VPOS	Positive Supply Voltage. 5.0 V nominal.
7	ENBL	Device Enable. Pull low or leave disconnected to enable the device; pull high to disable the device.
9, 10	LOIP, LOIN	Differential LO Input Terminals. Internally matched to 50 Ω; must be ac-coupled.
12	VSET	High Input IP3 Bias Control. For high input IP3 performance, apply ~4 V to 5 V. Improved noise figure (NF) performance and lower supply current can be set by applying ~2 V to 3 V to the VSET pin. A resistor can be connected to the supply to raise the voltage, whereas a resistor to GND lowers the voltage.
15, 16	OP2-, OP2+	Channel 2 Mixer Differential Output Terminals. Bias must be applied through pull-up choke inductors or the center tap of the IF transformer.
19, 20	RF2-, RF2+	Differential RF Input Terminals for Channel 2. Internally matched to 50 Ω; must be ac-coupled.
22, 23	RF1-, RF1+	Differential RF Input Terminals for Channel 1. Internally matched to 50 Ω; must be ac-coupled.
	EPAD	Exposed Paddle. Must be soldered to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

DOWNCONVERTER MODE USING A BROADBAND BALUN

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 4\text{ V}$, $IF = 153\text{ MHz}$, as measured using a typical circuit schematic with low-side local oscillator (LO), unless otherwise noted. Insertion loss of input and output baluns (TC1-1-13M+, TC4-1W+) is extracted from the gain measurement.

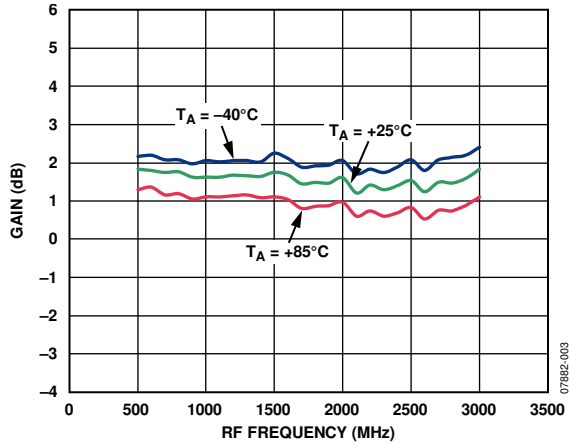


Figure 3. Power Conversion Gain vs. RF Frequency

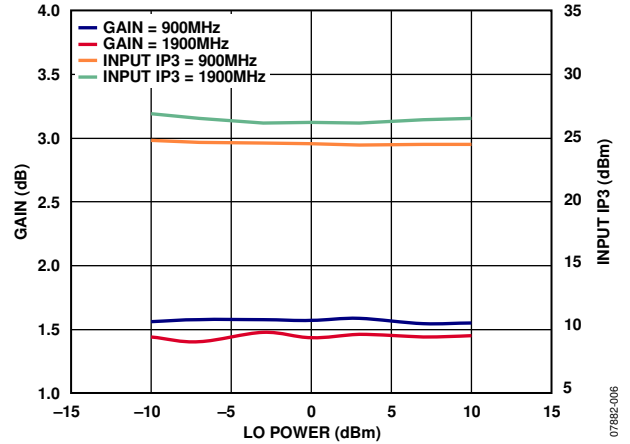


Figure 6. Power Conversion Gain and Input IP3 vs. LO Power

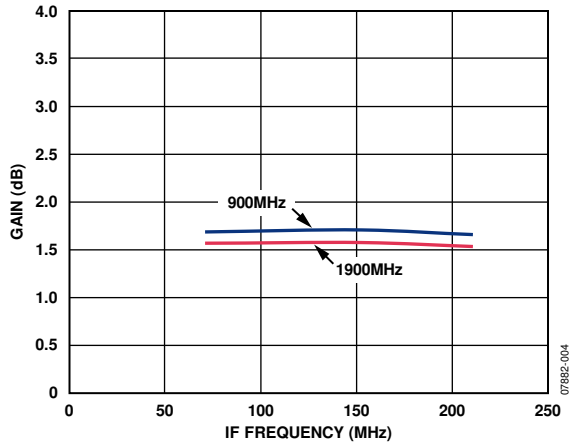


Figure 4. Power Conversion Gain vs. IF Frequency

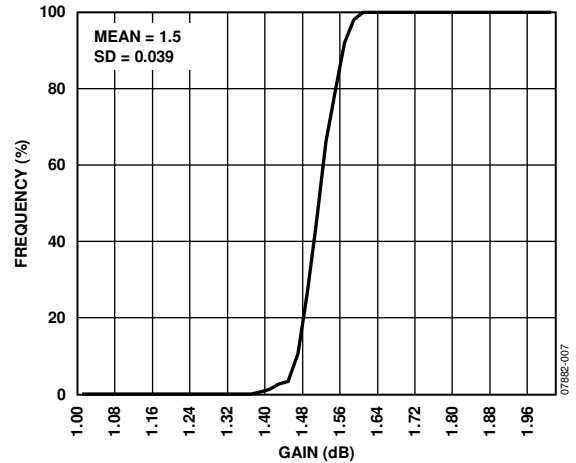


Figure 7. Power Conversion Gain Distribution

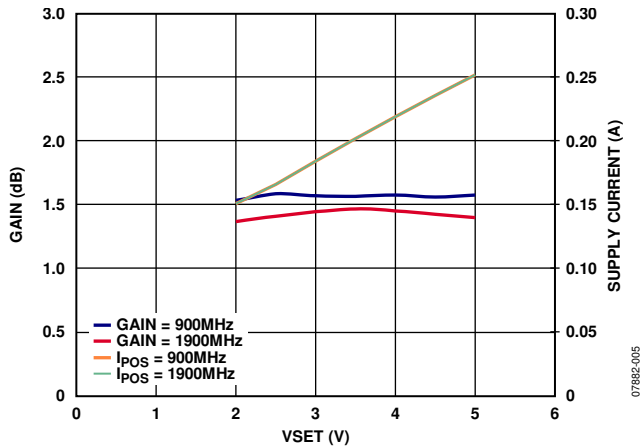


Figure 5. Power Conversion Gain and I_{POS} vs. V_{SET}

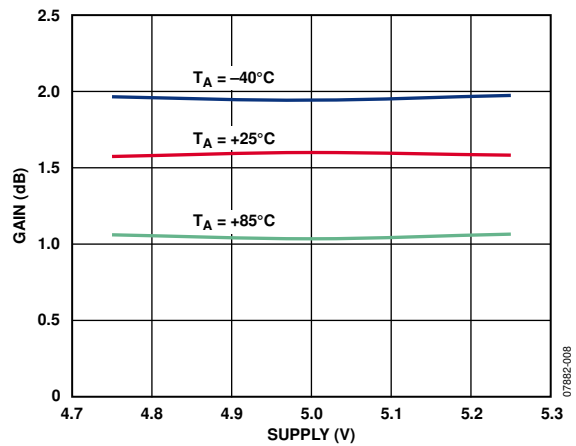


Figure 8. Power Conversion Gain vs. Supply Voltage

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 4\text{ V}$, $IF = 153\text{ MHz}$, as measured using a typical circuit schematic with low-side local oscillator (LO), unless otherwise noted. Insertion loss of input and output baluns (TC1-1-13M+, TC4-1W+) is extracted from the gain measurement.

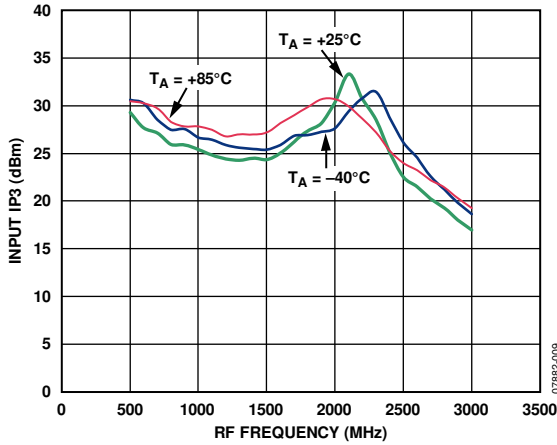


Figure 9. Input IP3 vs. RF Frequency

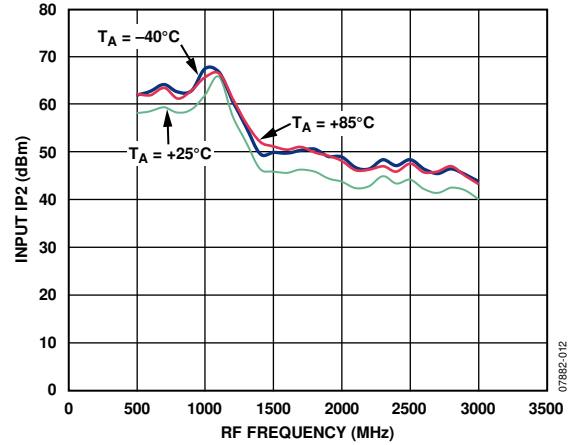


Figure 12. Input IP2 vs. RF Frequency

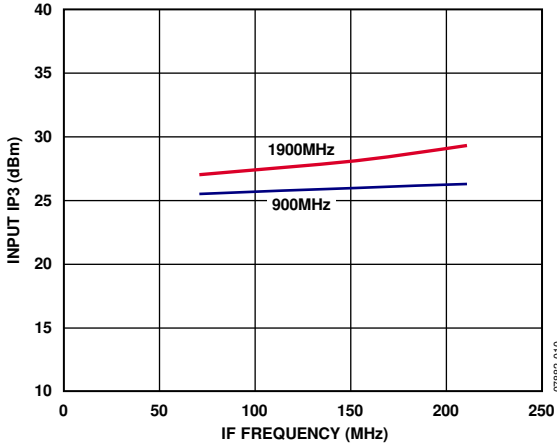


Figure 10. Input IP3 vs. IF Frequency

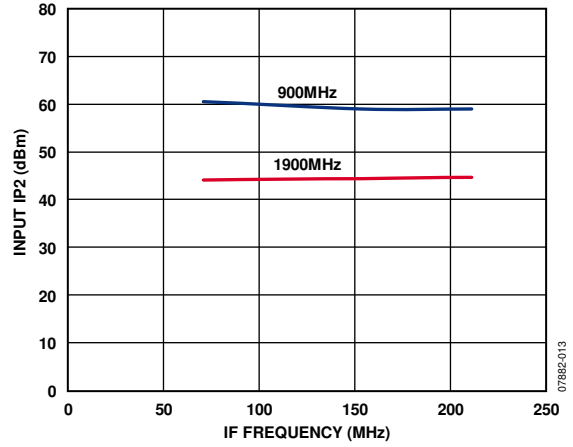


Figure 13. Input IP2 vs. IF Frequency

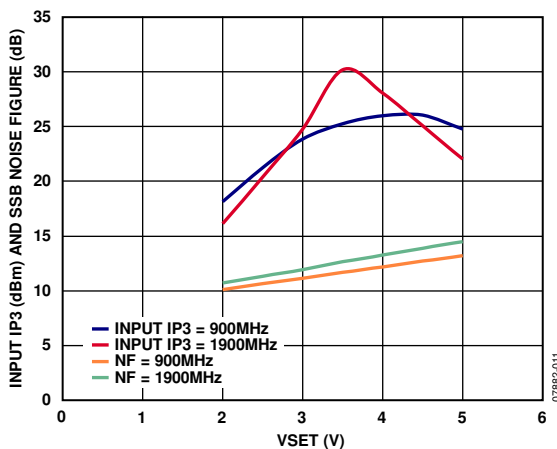


Figure 11. Input IP3, Noise Figure vs. VSET

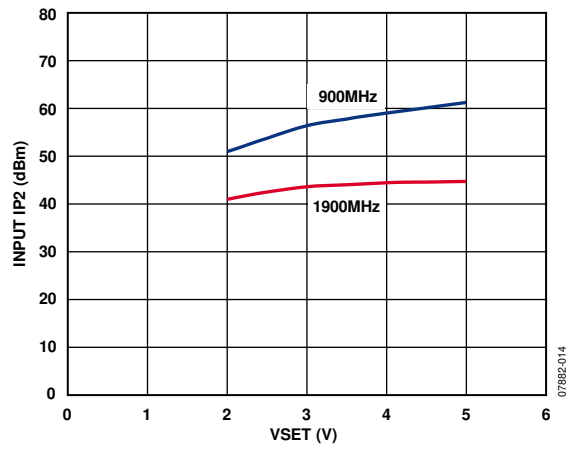


Figure 14. Input IP2 vs. VSET

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 4\text{ V}$, $IF = 153\text{ MHz}$, as measured using a typical circuit schematic with low-side local oscillator (LO), unless otherwise noted. Insertion loss of input and output baluns (TC1-1-13M+, TC4-1W+) is extracted from the gain measurement.

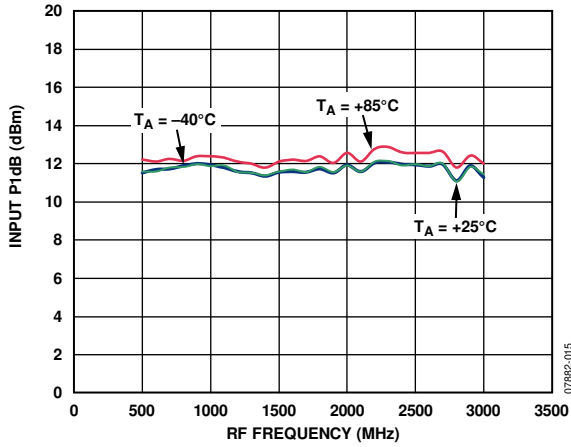


Figure 15. Input P1dB vs. RF Frequency

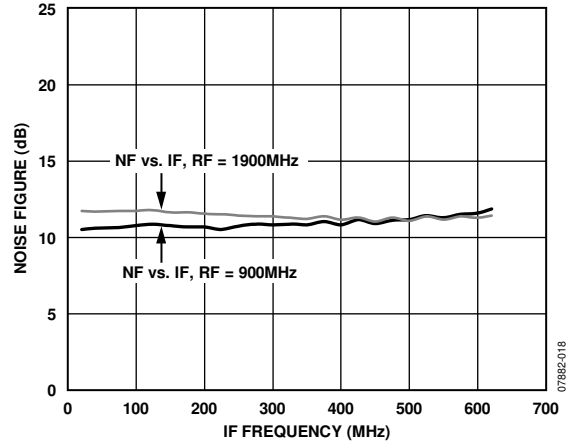


Figure 18. SSB Noise Figure vs. IF Frequency ($V_{SET} = 2.0\text{ V}$)

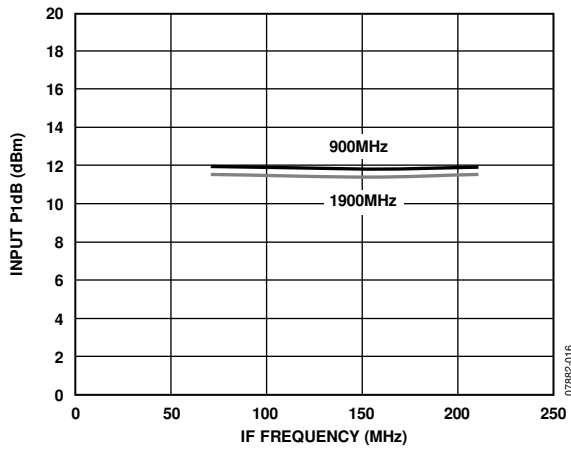


Figure 16. Input P1dB vs. IF Frequency

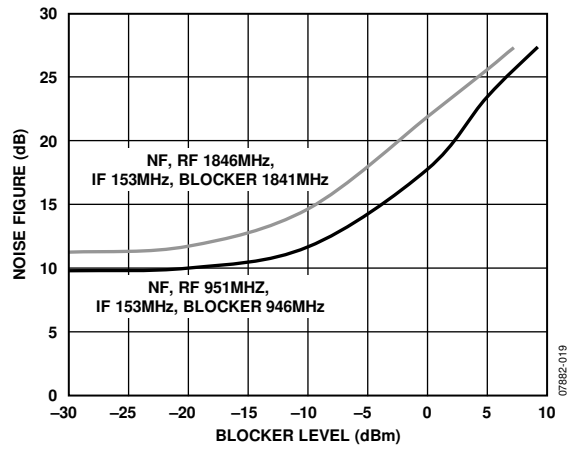


Figure 19. SSB Noise Figure vs. Blocker Level ($V_{SET} = 2.0\text{ V}$)

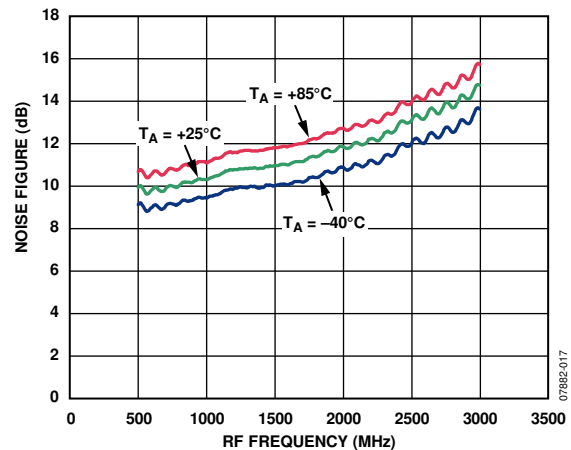


Figure 17. SSB Noise Figure vs. RF Frequency ($V_{SET} = 2.0\text{ V}$)

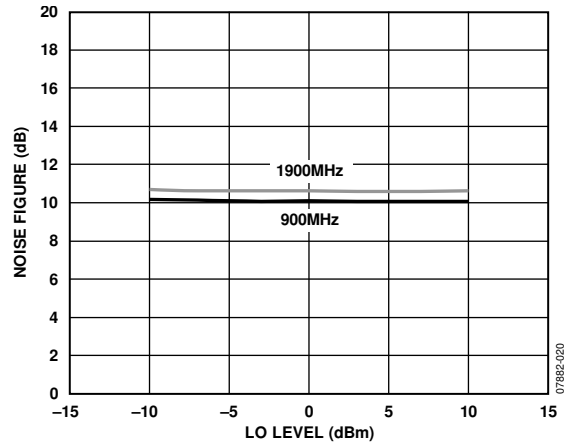


Figure 20. SSB Noise Figure vs. LO Drive ($V_{SET} = 2.0\text{ V}$)

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 4\text{ V}$, $IF = 153\text{ MHz}$, as measured using a typical circuit schematic with low-side local oscillator (LO), unless otherwise noted. Insertion loss of input and output baluns (TC1-1-13M+, TC4-1W+) is extracted from the gain measurement.

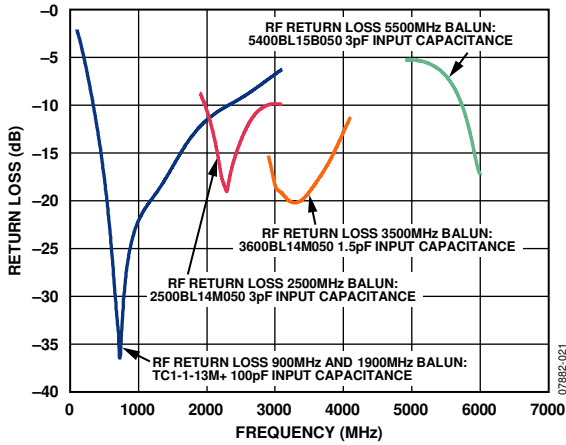


Figure 21. RF Return Loss Measured Differentially at the RF Port

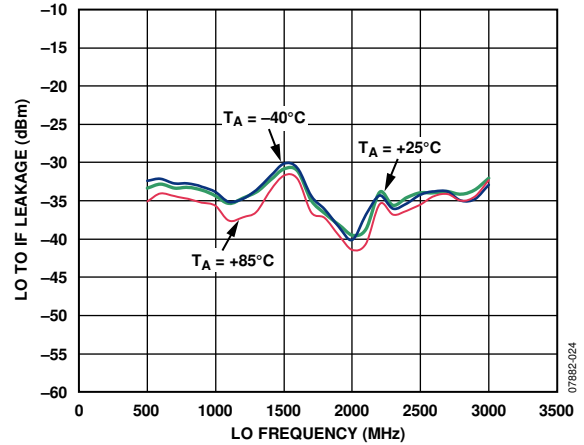


Figure 24. LO to IF Leakage vs. LO Frequency

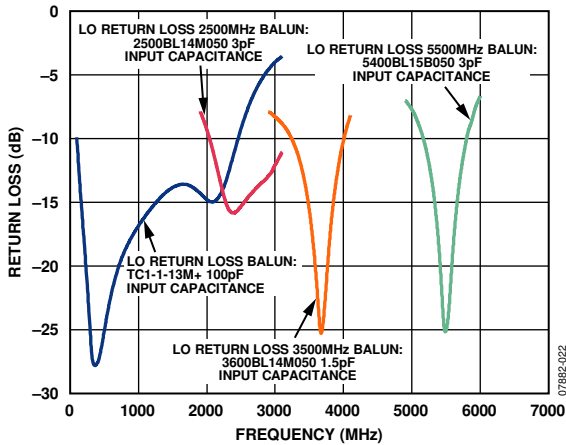


Figure 22. LO Return Loss Measured Differentially at the LO Port

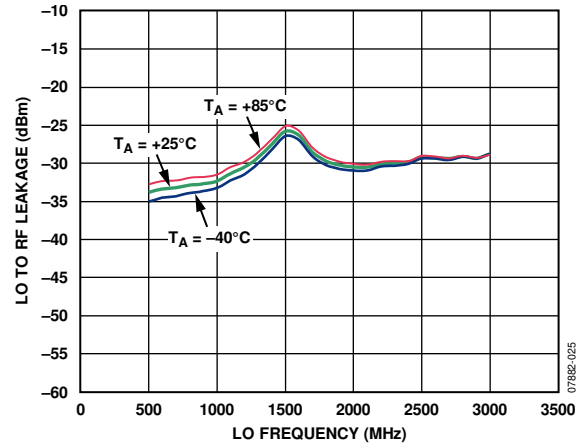


Figure 25. LO to RF Leakage vs. LO Frequency

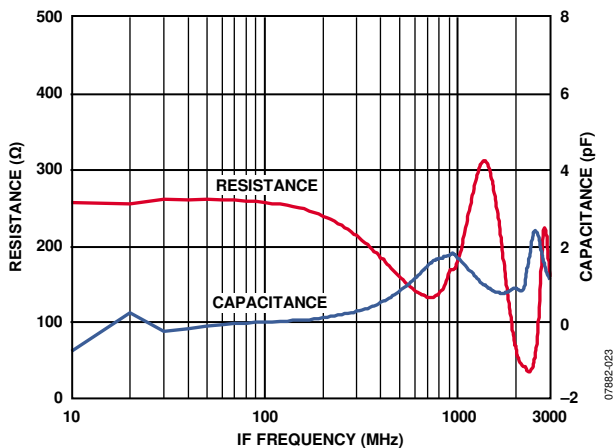


Figure 23. IF Differential Output Impedance (R Parallel C Equivalent)

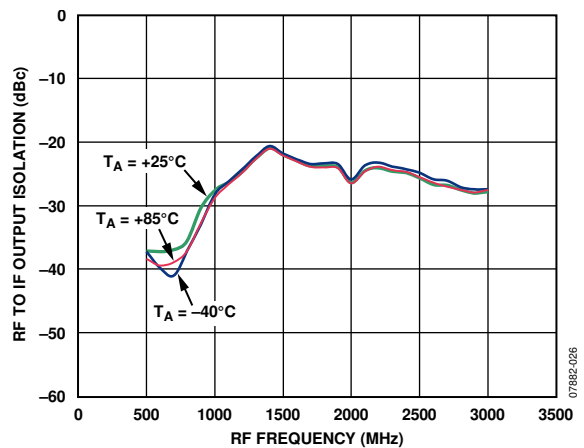


Figure 26. RF to IF Output Isolation vs. RF Frequency

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 4\text{ V}$, $IF = 153\text{ MHz}$, as measured using a typical circuit schematic with low-side local oscillator (LO), unless otherwise noted. Insertion loss of input and output baluns (TC1-1-13M+, TC4-1W+) is extracted from the gain measurement.

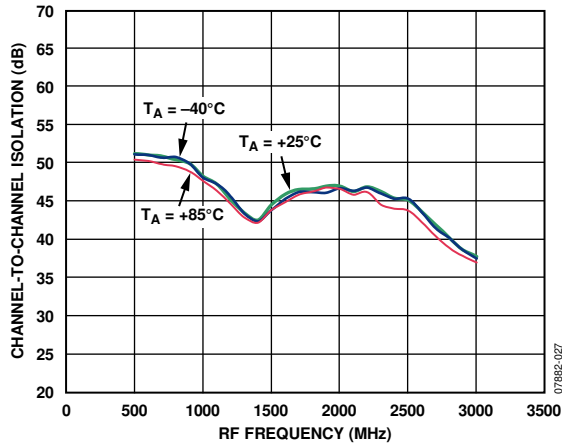


Figure 27. Channel-to-Channel Isolation

DOWNCONVERTER MODE USING A JOHANSON 2.5 GHZ BALUN

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 4.5\text{ V}$, $I_F = 211\text{ MHz}$, as measured using a typical circuit schematic with low-side LO, unless otherwise noted. Insertion loss of input and output baluns (2500BL14M050, TC4-1W+) is included in the gain measurement.

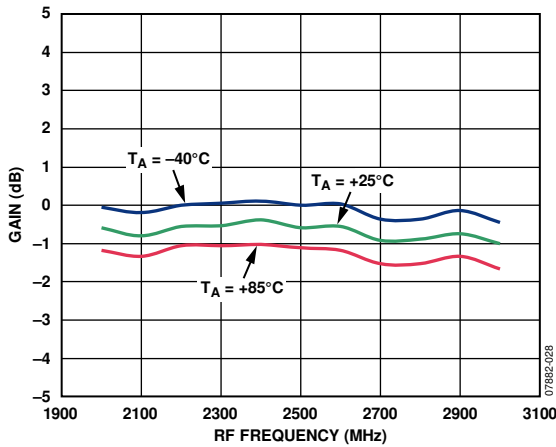


Figure 28. Power Conversion Gain vs. RF Frequency

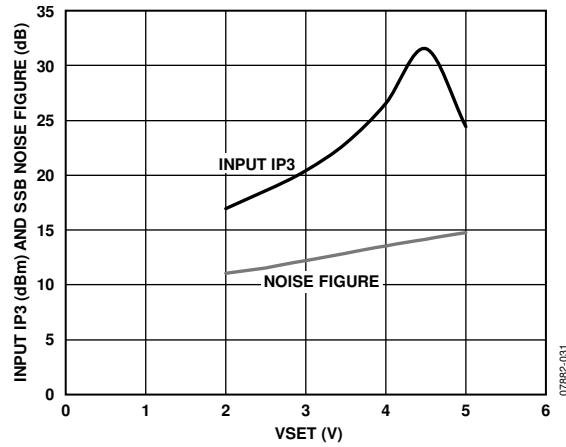


Figure 31. Input IP3, Noise Figure vs. VSET

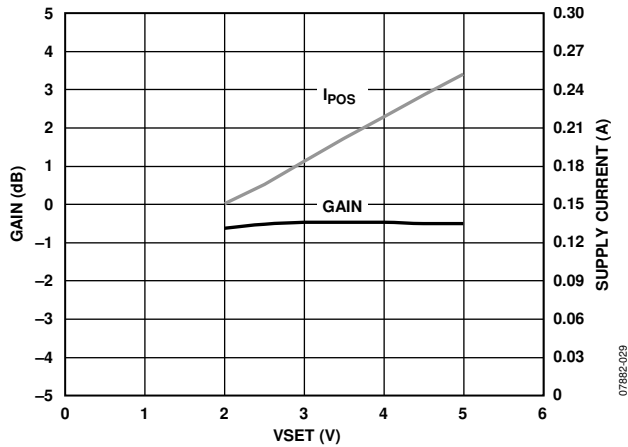


Figure 29. Power Conversion Gain and I_{POS} vs. VSET

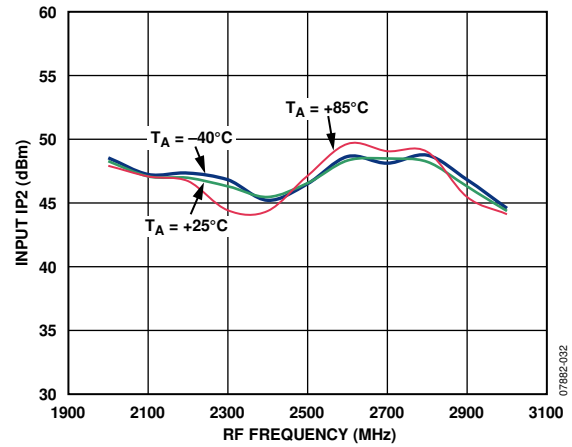


Figure 32. Input IP2 vs. RF Frequency

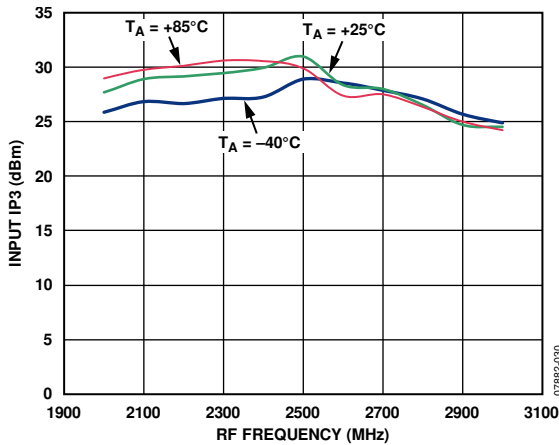


Figure 30. Input IP3 vs. RF Frequency

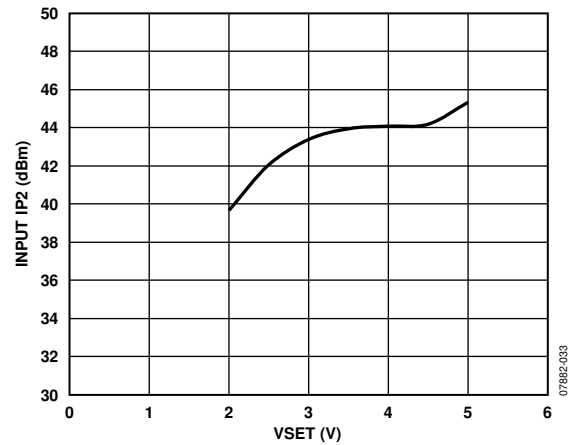


Figure 33. Input IP2 vs. VSET

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 4.5\text{ V}$, $IF = 211\text{ MHz}$, as measured using a typical circuit schematic with low-side LO, unless otherwise noted. Insertion loss of input and output baluns (2500BL14M050, TC4-1W+) is included in the gain measurement

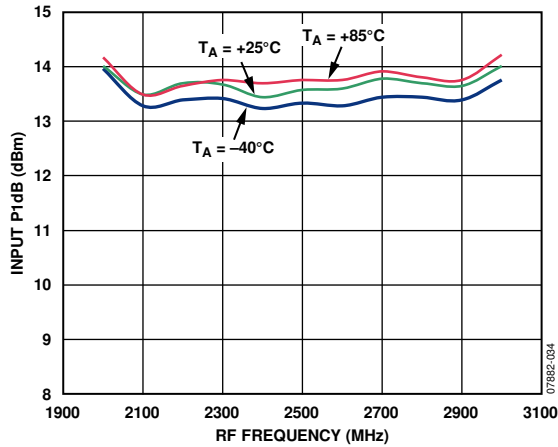


Figure 34. Input P1dB vs. RF Frequency

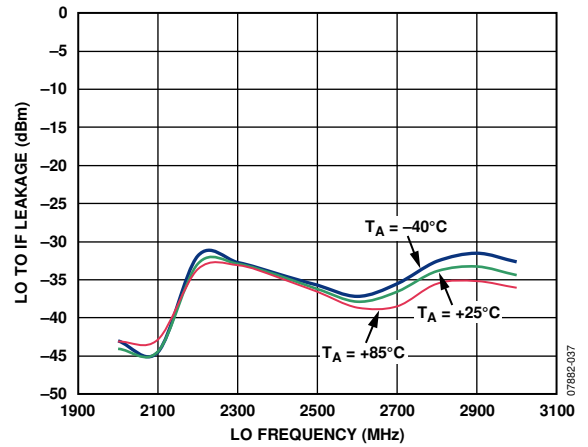


Figure 37. LO to IF Leakage vs. LO Frequency

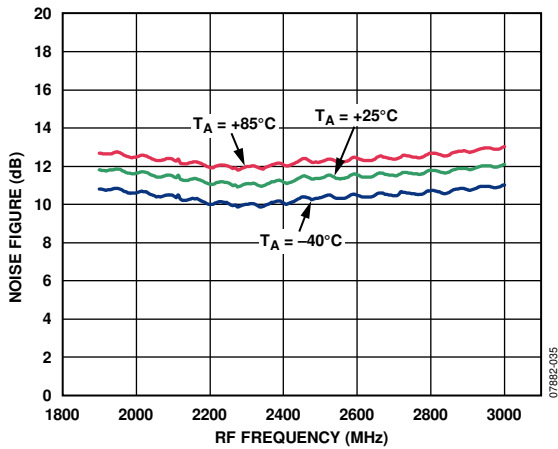


Figure 35. SSB Noise Figure vs. RF Frequency ($V_{SET} = 2.0\text{ V}$)

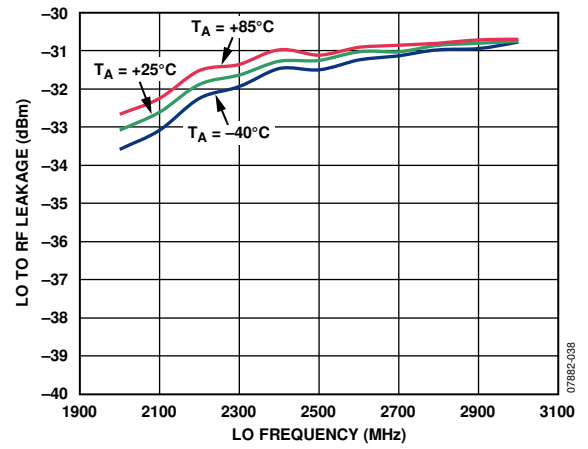


Figure 38. LO to RF Leakage vs. LO Frequency

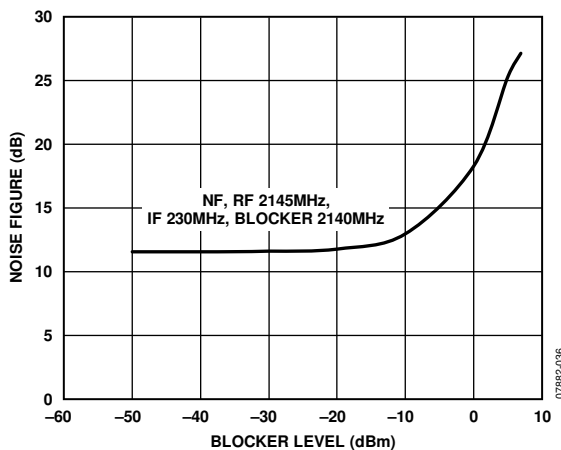


Figure 36. SSB Noise Figure vs. Blocker Level ($V_{SET} = 2.0\text{ V}$)

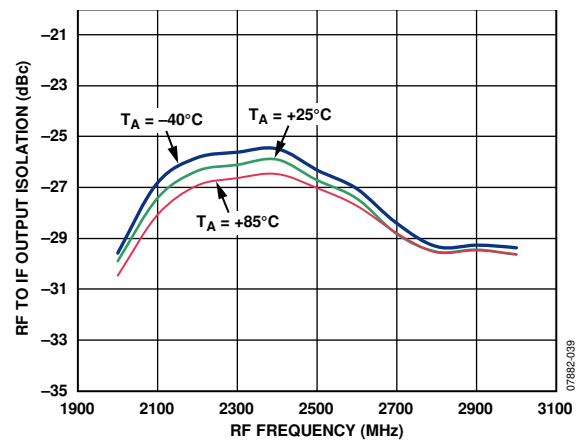


Figure 39. RF to IF Output Isolation vs. RF Frequency

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 4.5\text{ V}$, $IF = 211\text{ MHz}$, as measured using a typical circuit schematic with low-side LO, unless otherwise noted. Insertion loss of input and output baluns (2500BL14M050, TC4-1W+) is included in the gain measurement

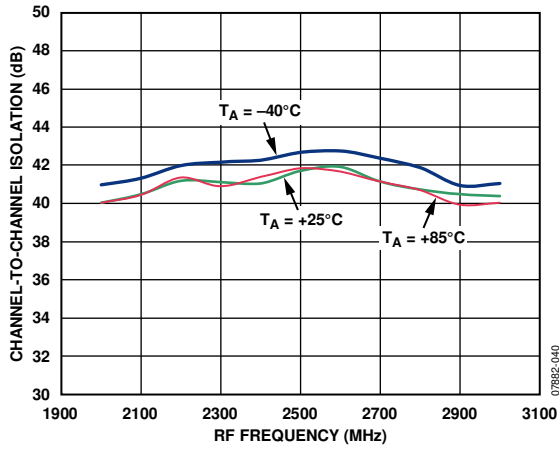


Figure 40. Channel-to-Channel Isolation

DOWNCONVERTER MODE USING A JOHANSON 3.5 GHZ BALUN

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 5\text{ V}$, $IF = 153\text{ MHz}$, as measured using a typical circuit schematic with low-side LO, unless otherwise noted. Insertion loss of input and output baluns (3600BL14M050, TC4-1W+) is included in the gain measurement.

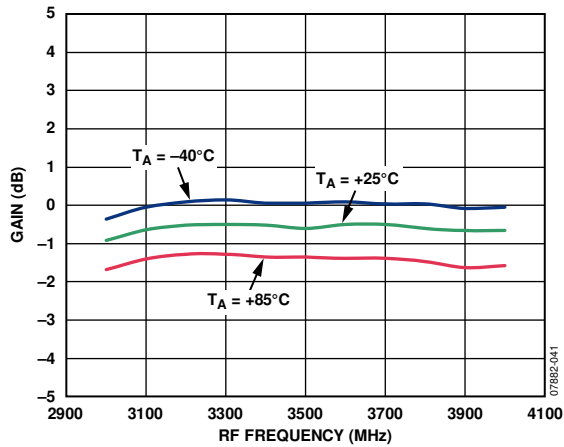


Figure 41. Power Conversion Gain vs. RF Frequency

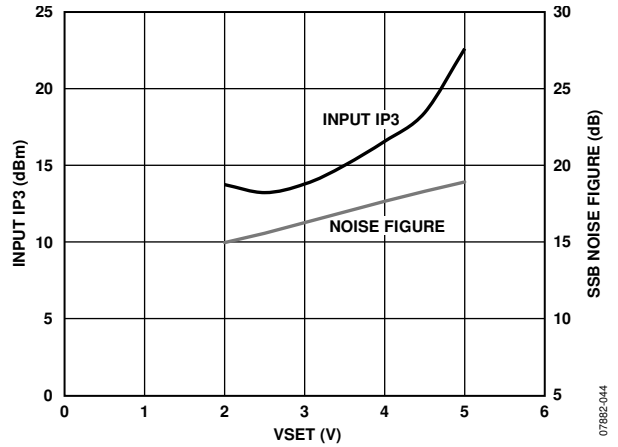


Figure 44. Input IP3, Noise Figure vs. VSET

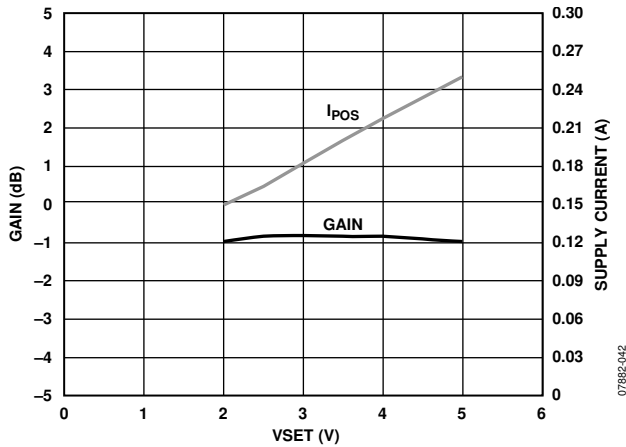


Figure 42. Power Conversion Gain and I_{POS} vs. VSET

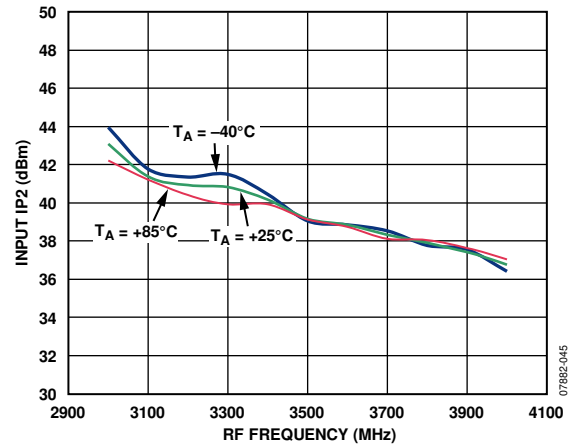


Figure 45. Input IP2 vs. RF Frequency

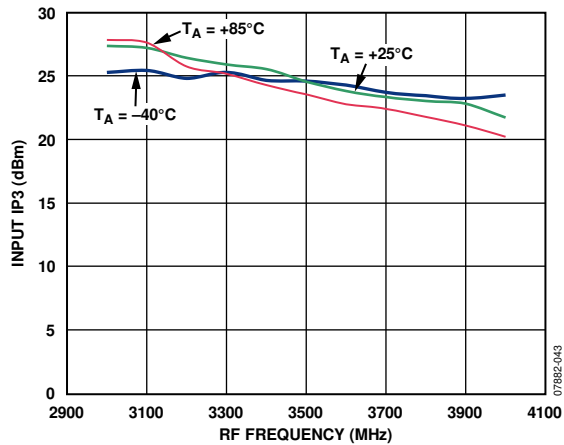


Figure 43. Input IP3 vs. RF Frequency

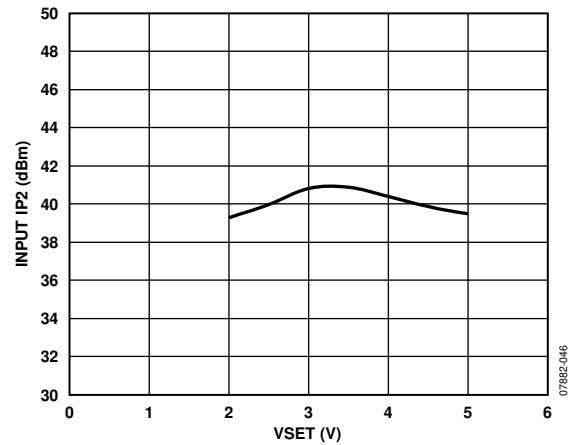


Figure 46. Input IP2 vs. VSET

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 5\text{ V}$, $IF = 153\text{ MHz}$, as measured using a typical circuit schematic with low-side LO, unless otherwise noted. Insertion loss of input and output baluns (3600BL14M050, TC4-1W+) is included in the gain measurement.

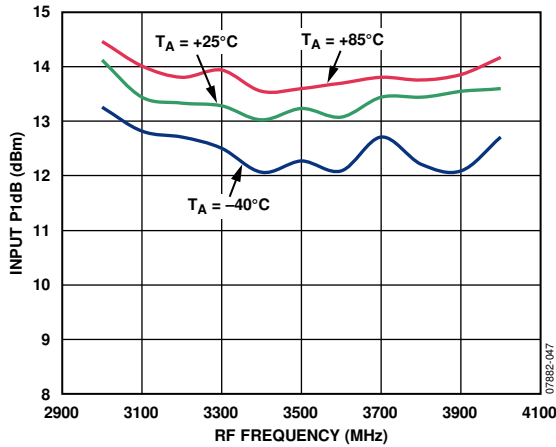


Figure 47. Input P1dB vs. RF Frequency

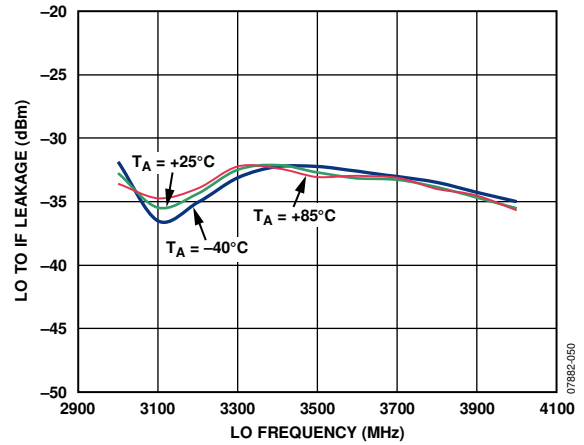


Figure 50. LO to IF Leakage vs. LO Frequency

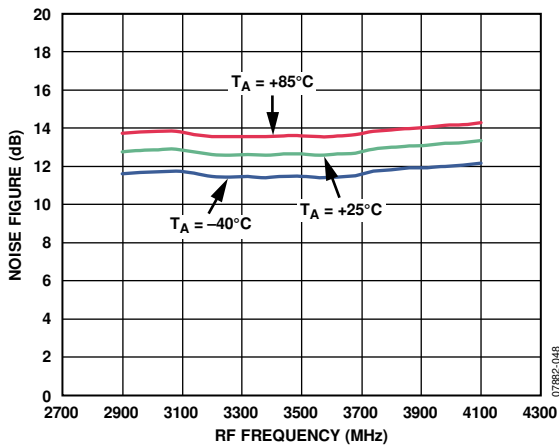


Figure 48. SSB Noise Figure vs. RF Frequency ($V_{SET} = 2.0\text{ V}$)

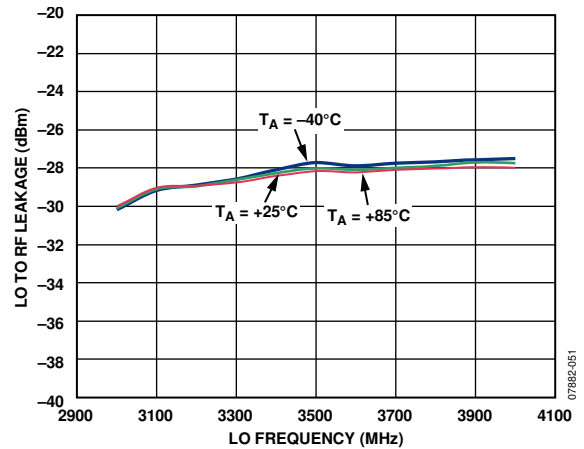


Figure 51. LO to RF Leakage vs. LO Frequency

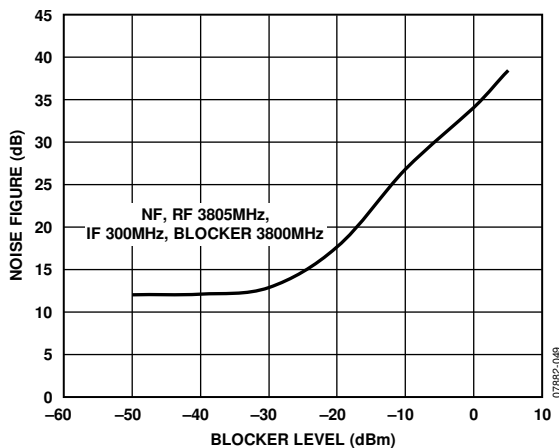


Figure 49. SSB Noise Figure vs. Blocker Level ($V_{SET} = 2.0\text{ V}$)

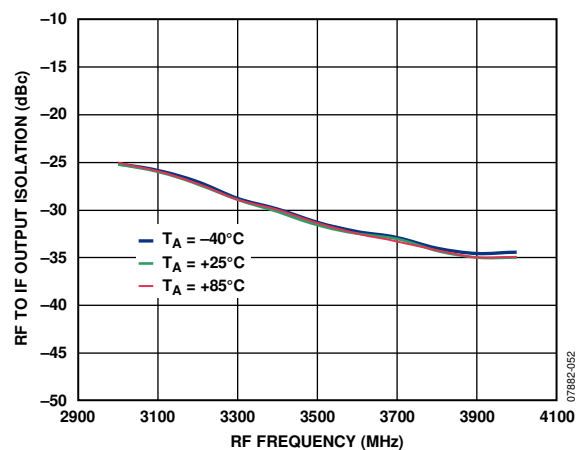


Figure 52. RF to IF Output Isolation vs. RF Frequency

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 5\text{ V}$, $IF = 153\text{ MHz}$, as measured using a typical circuit schematic with low-side LO, unless otherwise noted. Insertion loss of input and output baluns (3600BL14M050, TC4-1W+) is included in the gain measurement.

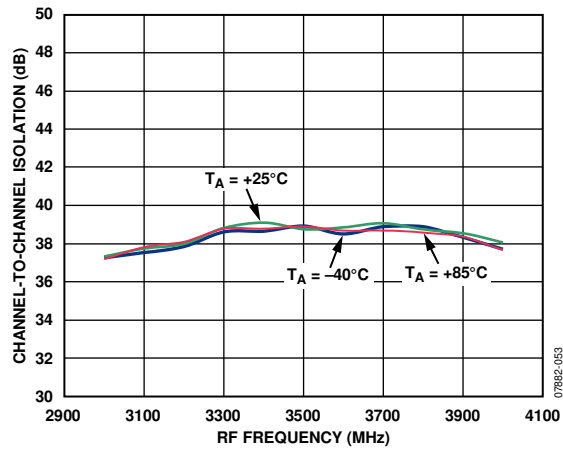


Figure 53. Channel-to-Channel Isolation

DOWNCONVERTER MODE USING A JOHANSON 5.5 GHZ BALUN

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 4.8\text{ V}$, $IF = 380\text{ MHz}$, as measured using a typical circuit schematic with low-side LO, unless otherwise noted. Insertion loss of input and output baluns (5400BL15B050, TC4-1W+) is included in the gain measurement.

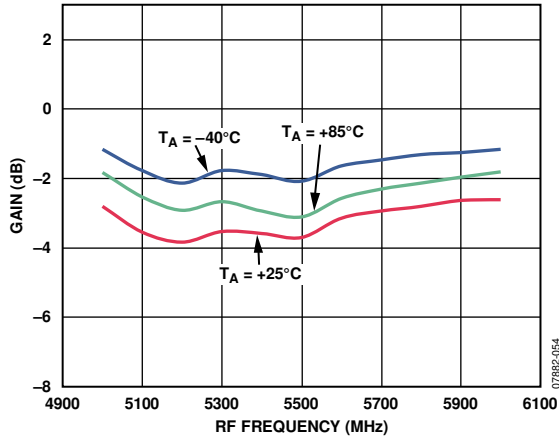


Figure 54. Power Conversion Gain vs. RF Frequency

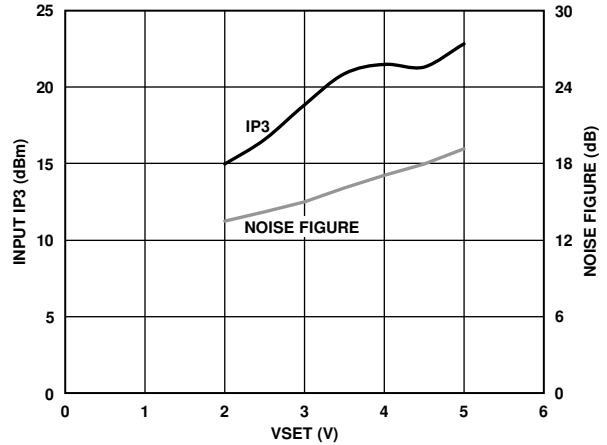


Figure 57. Input IP3, Noise Figure vs. VSET

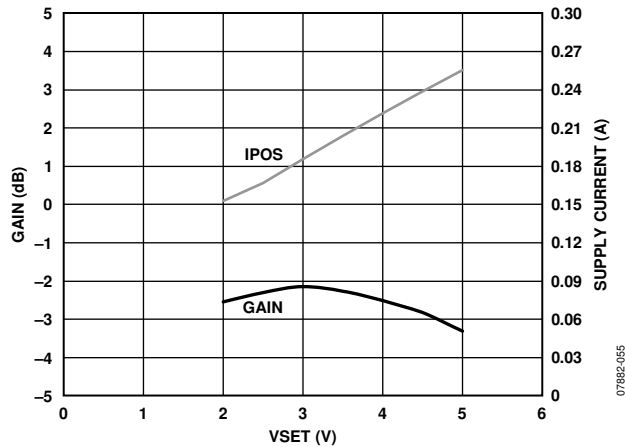


Figure 55. Power Conversion Gain and I_{POS} vs. VSET

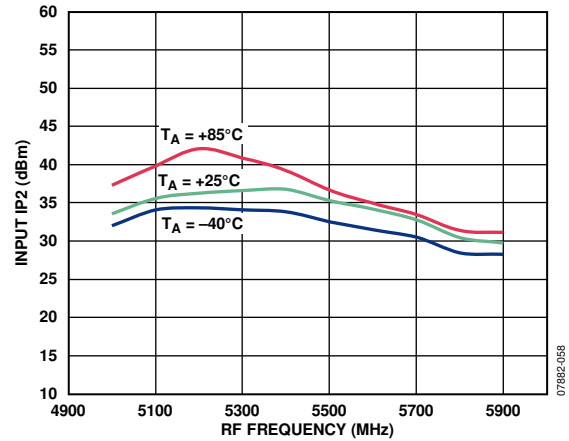


Figure 58. Input IP2 vs. RF Frequency

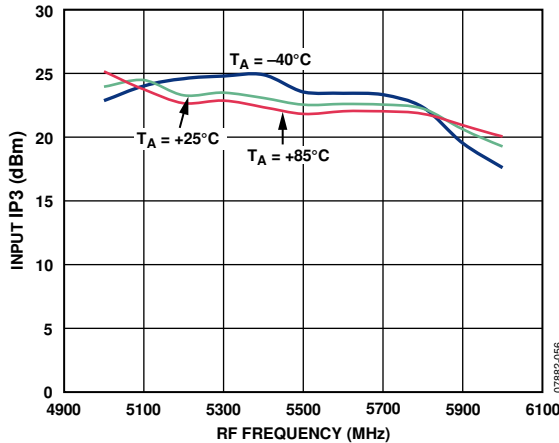


Figure 56. Input IP3 vs. RF Frequency

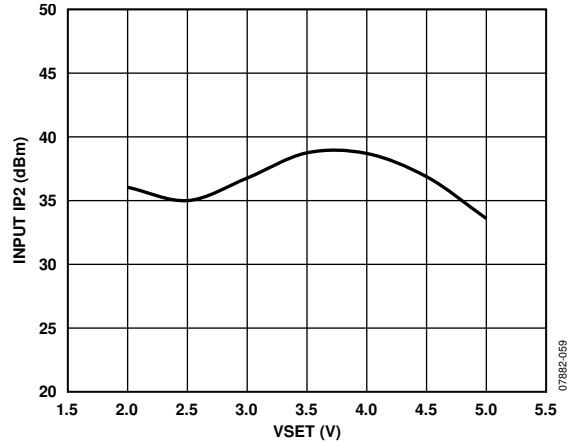


Figure 59. Input IP2 vs. VSET

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 5\text{ V}$, $IF = 153\text{ MHz}$, as measured using a typical circuit schematic with low-side LO, unless otherwise noted. Insertion loss of input and output baluns (3600BL14M050, TC4-1W+) is included in the gain measurement.

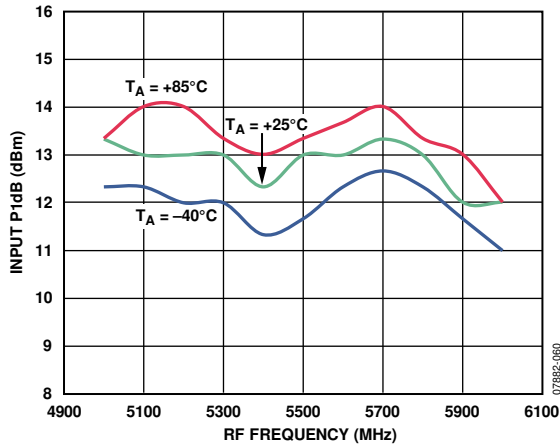


Figure 60. Input P1dB vs. RF Frequency

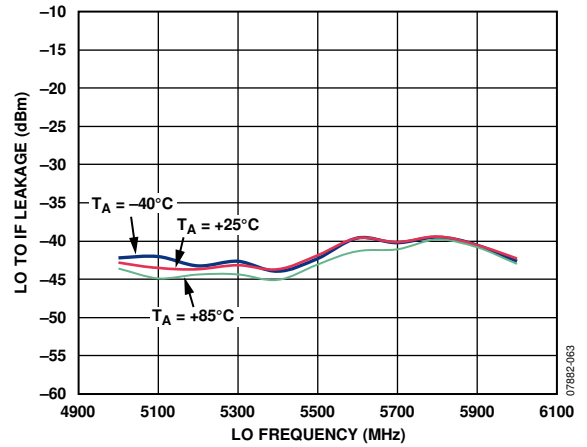


Figure 63. LO to IF Leakage vs. LO Frequency

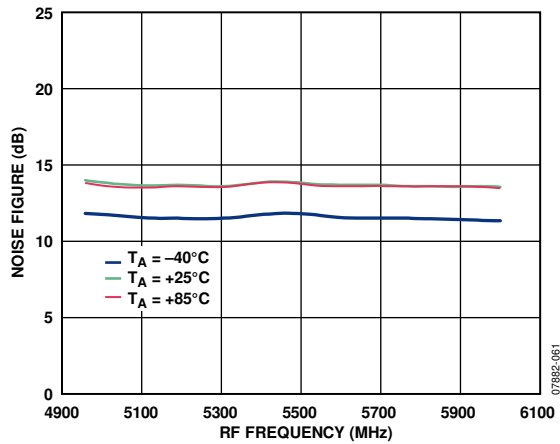


Figure 61. SSB Noise Figure vs. RF Frequency ($V_{SET} = 2.0\text{ V}$)

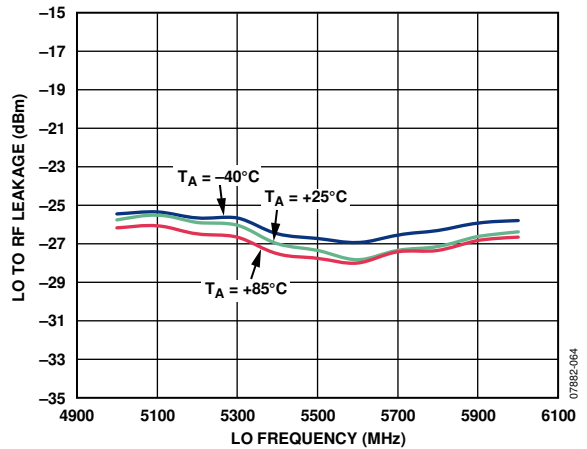


Figure 64. LO to RF Leakage vs. LO Frequency

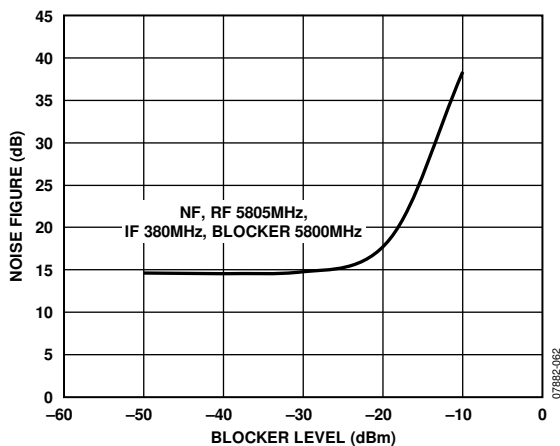


Figure 62. SSB Noise Figure vs. Blocker Level ($V_{SET} = 2.0\text{ V}$)

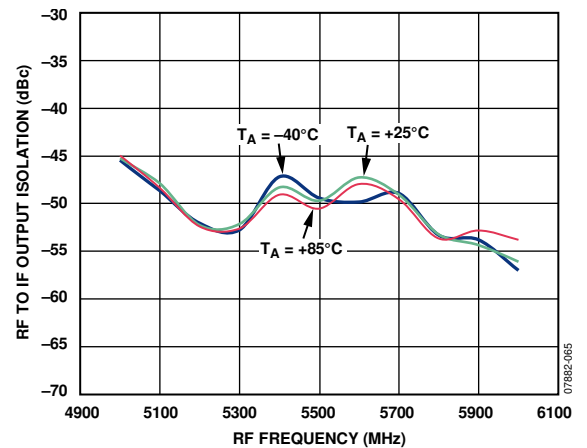


Figure 65. RF to IF Output Isolation vs. RF Frequency

$V_S = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{SET} = 5\text{ V}$, $IF = 153\text{ MHz}$, as measured using a typical circuit schematic with low-side LO, unless otherwise noted. Insertion loss of input and output baluns (3600BL14M050, TC4-1W+) is included in the gain measurement.

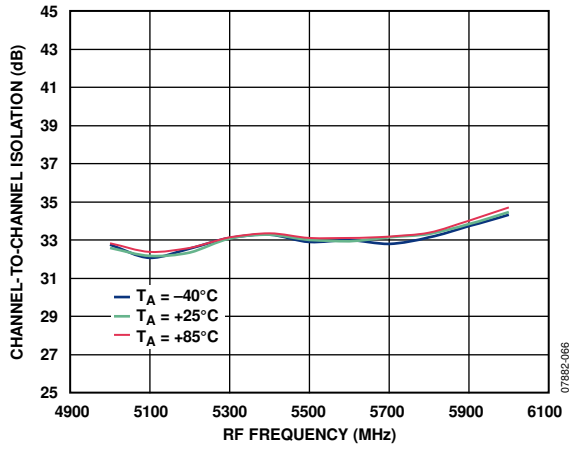


Figure 66. Channel-to-Channel Isolation

SPUR PERFORMANCE

All spur tables are $(N \times f_{RF}) - (M \times f_{LO})$ and were measured using the standard evaluation board (see the Evaluation Board section). Mixer spurious products are measured in decibels relative to the carrier (dBc) from the IF output power level. Data was measured for frequencies less than 6 GHz only. The typical noise floor of the measurement system is -100 dBm.

900 MHz Performance

$V_S = 5$ V, $V_{SET} = 4$ V, $T_A = 25^\circ\text{C}$, RF power = 0 dBm, LO power = 0 dBm, $f_{RF} = 900$ MHz, $f_{LO} = 703$ MHz, $Z_0 = 50 \Omega$.

		M														
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
N	0		-35.9	-25.5	-47.3	-27.4	-51.5	-37.5	-62.1	-47.5						
	1	-34.3	0.0	-46.3	-19.8	-64.3	-30.0	-75.6	-45.0	-67.8	-55.3					
	2	-49.1	-69.2	-68.2	-61.6	-68.7	-80.7	-67.5	-88.1	-79.1	-82.6	-91.5	≤ -100			
	3	-86.7	-79.6	≤ -100	-67.3	-98.0	-71.0	≤ -100	-86.3	≤ -100	≤ -100	≤ -100	≤ -100	-98.4	≤ -100	
	4	-91.8	≤ -100	-96.4	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	5	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	6	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	7		≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	8			≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	9				≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	10						≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	11							≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	12								≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	13										≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	14											≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
15												≤ -100	≤ -100	≤ -100	≤ -100	

2090 MHz Performance

$V_S = 5$ V, $V_{SET} = 4$ V, $T_A = 25^\circ\text{C}$, RF power = 0 dBm, LO power = 0 dBm, $f_{RF} = 2090$ MHz, $f_{LO} = 1842$ MHz, $Z_0 = 50 \Omega$.

		M														
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
N	0		-43.0	-23.7	-52.9											
	1	-26.8	0.0	-59.6	-42.2	-80.5										
	2	-59.8	-71.9	-53.8	-67.5	-68.2	-84.1									
	3		-67.6	-97.6	-59.3	-92.2	-79.3	≤ -100								
	4			≤ -100	≤ -100	-93.7	-97.8	≤ -100	≤ -100							
	5				≤ -100	≤ -100	-96.1	≤ -100	≤ -100	≤ -100						
	6					≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100				
	7						≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100			
	8							≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100		
	9								≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	
	10										≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	11											≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	12												≤ -100	≤ -100	≤ -100	≤ -100
	13													≤ -100	≤ -100	≤ -100
	14														≤ -100	≤ -100
15															≤ -100	

2600 MHz Performance

$V_S = 5\text{ V}$, $V_{SET} = 4.5\text{ V}$, $T_A = 25^\circ\text{C}$, RF power = 0 dBm, LO power = 0 dBm, $f_{RF} = 2600\text{ MHz}$, $f_{LO} = 2350\text{ MHz}$, $Z_0 = 50\ \Omega$.

		M														
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
N	0		-37.9	-31.5												
	1	-27.5	0.0	-62.6	-36.3											
	2	-75.5	-59.7	-52.2	-65.8	-68.8										
	3		-75.0	-88.7	-56.3	-86.8	-90.5									
	4			≤ -100	≤ -100	-82.5	-92.1	≤ -100								
	5				≤ -100	≤ -100	-94.4	≤ -100	≤ -100	≤ -100						
	6						≤ -100	≤ -100	≤ -100	≤ -100	≤ -100					
	7							≤ -100	≤ -100	≤ -100	≤ -100	≤ -100				
	8								≤ -100	≤ -100	≤ -100	≤ -100	≤ -100			
	9									≤ -100	≤ -100	≤ -100	≤ -100	≤ -100		
	10										≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	
	11											≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	12												≤ -100	≤ -100	≤ -100	≤ -100
	13													≤ -100	≤ -100	≤ -100
	14														≤ -100	≤ -100
	15															≤ -100

3500 MHz Performance

$V_S = 5\text{ V}$, $V_{SET} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, RF power = 0 dBm, LO power = 0 dBm, $f_{RF} = 3500\text{ MHz}$, $f_{LO} = 3800\text{ MHz}$, $Z_0 = 50\ \Omega$.

		M														
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
N	0		-43.0	-23.7	-52.9											
	1	-26.8	0.0	-59.6	-42.2	-80.5										
	2	-59.8	-71.9	-53.8	-67.5	-68.2	-84.1									
	3		-67.6	-97.6	-59.3	-92.2	-79.3	≤ -100								
	4			≤ -100	≤ -100	-93.7	-97.8	≤ -100	≤ -100							
	5				≤ -100	≤ -100	-96.1	≤ -100	≤ -100	≤ -100						
	6					≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100				
	7						≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100			
	8							≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100		
	9								≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	
	10										≤ -100	≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	11											≤ -100	≤ -100	≤ -100	≤ -100	≤ -100
	12												≤ -100	≤ -100	≤ -100	≤ -100
	13													≤ -100	≤ -100	≤ -100
	14														≤ -100	≤ -100
	15															≤ -100

5800 MHz Performance

$V_s = 5\text{ V}$, $V_{SET} = 4.8\text{ V}$, $T_A = 25^\circ\text{C}$, RF power = -10 dBm , LO power = 0 dBm , $f_{RF} = 5800\text{ MHz}$, $f_{LO} = 5600\text{ MHz}$, $Z_0 = 50\ \Omega$.

		M														
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
N	0		-28.3													
	1	-63.6	0.0	-80.5												
	2			-48.6	-92.6											
	3				-64.2	-98.7										
	4					-90.5	-98.3									
	5						≤ -100	-99.4								
	6							-81.6	-98.0							
	7								-87.2	-95.9						
	8									-84.0	-99.5					
	9										≤ -100	≤ -100				
	10											≤ -100	≤ -100			
	11												≤ -100	≤ -100		
	12													≤ -100	-99.6	
	13														≤ -100	-99.8
	14															≤ -100
15																

CIRCUIT DESCRIPTION

The [ADL5802](#) provides two double-balanced active mixers. These mixers are designed for a 50 Ω input impedance and a 200 Ω output impedance. Both are driven from a common local oscillator (LO) amplifier. The RF inputs and LO outputs are differential, providing maximum usable bandwidth at the input and output ports. The LO also operates with a 50 Ω input impedance and can, optionally, be operated differentially or single-ended. The input, output, and LO ports can be operated over an exceptionally wide frequency range. The [ADL5802](#) can be configured as a downconvert mixer or as an upconvert mixer.

The [ADL5802](#) can be divided into the following sections: the local oscillator (LO) amplifier and splitter, the RF voltage-to-current (V-to-I) converter, the mixer cores, the output loads, and the bias circuit. A simplified block diagram of the device is shown in Figure 67. The LO block generates a pair of differential LO signals to drive two mixer cores. The RF input is converted into current by the V-to-I converters that then feed into the two mixer cores. The internal differential load of the mixers is designed for a wideband 200 Ω output impedance from the mixer. Reference currents to each section are generated by the bias circuit, which can be enabled or disabled using the ENBL pin. A detailed description of each section of the [ADL5802](#) follows.

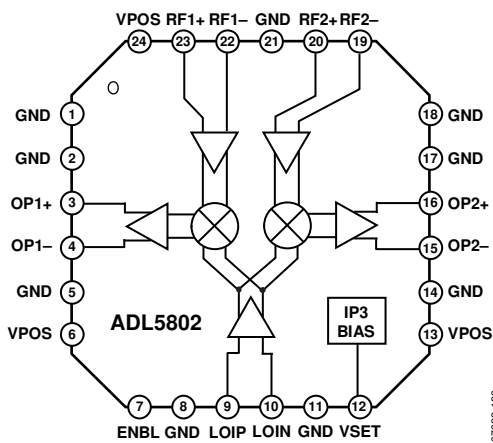


Figure 67. [ADL5802](#) Block Diagram

LO AMPLIFIER AND SPLITTER

The LO input is amplified using a broadband LNA and is then split and followed by separate LO limiting amplifiers. The LNA input impedance is nominally 50 Ω . The LO is designed to accommodate a wide range of LO input power levels. The LO input is conditioned by the series of amplifiers to provide a well controlled and limited LO swing to the mixer core, resulting in excellent IP3. The LO circuit exhibits low additive noise, resulting in an excellent mixer noise figure and output noise under RF blocking. For optimal performance, the LO inputs should be driven differentially but at lower frequencies; single-ended drive is acceptable.

RF VOLTAGE TO CURRENT (V-TO-I) CONVERTER

The differential RF input signal is applied to a voltage-to-current converter that converts the differential input voltage to output currents. The V-to-I converter provides a 50 Ω input impedance. The V-to-I section bias current can be adjusted up or down using the VSET pin. Adjusting the current up improves IP3 and P1dB input but degrades SSB NF. Adjusting the current down improves SSB NF but degrades IP3 and P1dB input. The conversion gain remains nearly constant over a wide range of VSET pin settings, allowing the part to be adjusted dynamically without affecting the conversion gain. The current adjustment can be made by connecting a resistor from the VSET pin to the positive supply to increase the bias current or from the VSET pin to ground to decrease the bias current. The VSET pin impedance is approximately 675 Ω in series with two diodes and an internal current source.

MIXER CORES

The [ADL5802](#) has two double-balanced mixers that use high performance SiGe NPN transistors. These mixers are based on the Gilbert cell design of four cross-connected transistors.

MIXER LOAD

Each mixer load is designed to use a pair of 100 Ω resistors connected to the positive supply. This provides a 200 Ω differential output resistance. The mixer output should be pulled to the positive supply externally using a pair of RF chokes or using an output transformer with the center tap connected to the positive supply. It is possible to exclude these components when the mixer core current is low, but both P1dB and IP3 are then reduced.

The mixer load output can operate from direct current (dc) up to approximately 500 MHz into a 200 Ω load. For upconversion applications, the mixer load can be matched using off-chip matching components. Transmit operation up to 2 GHz is possible. See the Applications Information section for matching circuit details.

BIAS CIRCUIT

A band gap reference circuit generates the reference currents used by the mixers. The bias circuit can be enabled and disabled using the ENBL pin. If the ENBL pin is grounded or left open, the part is enabled. Pulling the ENBL pin high shuts off the bias circuit and disables the part. However, the ENBL pin does not alter the current in the LO section and, therefore, does not provide a true power-down feature. Certain configurations may require the VSET pin to be connected to the positive supply through a resistor. This will result in an increased mixer core current. Unless this resistor to positive supply is removed, bias current will continue to be supplied to the mixer core.