Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MCP19110/11

Digitally-Enhanced Power Analog Controller with Integrated Synchronous Driver

Synchronous Buck Features

- Input Voltage: 4.5V to 32V
- Output Voltage: 0.5V to 3.6V
  - Greater than 3.6V requires external divider
- Switching Frequency: 100 kHz to 1.6 MHz
- Quiescent Current: 5 mA Typical
- High-Drive:
  - +5V Gate Drive
  - 1A/2A Source Current
  - 1A/2A Sink Current
- Low-Drive:
  - +5V Gate Drive
  - 2A Source Current
  - 4A Sink Current
- Peak Current Mode Control
- Differential Remote Output Sense
- Multi-Phase Systems:
  - Master or Slave
  - Frequency Synchronized
  - Common Error Signal
- Multiple Output Systems:
  - Master or Slave
  - Frequency Synchronized
  - AEC-Q100 Qualified
- Configurable Parameters:
  - Overcurrent Limit
  - Input Undervoltage Lockout
  - Output Overvoltage
  - Output Undervoltage
  - Internal Analog Compensation
  - Soft Start Profile
  - Synchronous Driver Dead Time
  - Switching Frequency
- Thermal Shutdown

Microcontroller Features

- Precision 8 MHz Internal Oscillator Block:
  - Factory Calibrated
- Interrupt Capable
  - Firmware
  - Interrupt-on-Change Pins
- Only 35 Instructions to Learn
- 4096 Words On-Chip Program Memory
- High Endurance Flash:
  - 100,000 write Flash Endurance
  - Flash Retention: >40 years
- Watchdog Timer (WDT) with Independent Oscillator for Reliable Operation
- Programmable Code Protection
- In-Circuit Debug (ICD) via Two Pins (**MCP19111**)
- In-Circuit Serial Programming™ (ICSP™) via Two Pins
- 11 I/O Pins and One Input-Only Pin (**MCP19110**)
  - Three Open-Drain Pins
- 14 I/O Pins and One Input-Only Pin (**MCP19111**)
  - Three Open-Drain Pins
- Analog-to-Digital Converter (ADC):
  - 10-bit Resolution
  - 12 Internal Channels
  - Eight External Channels
- Timer0: 8-bit Timer/Counter with 8-Bit Prescaler
- Enhanced Timer1:
  - 16-bit Timer/Counter with Prescaler
  - Two Selectable Clock Sources
- Timer2: 8-Bit Timer/Counter with Prescaler
  - 8-bit Period Register
- I^2C Communication:
  - 7-bit Address Masking
  - Two Dedicated Address Registers
  - SMBus/PMBus™ Compatibility

Pin Diagram – 24-Pin QFN (MCP19110)

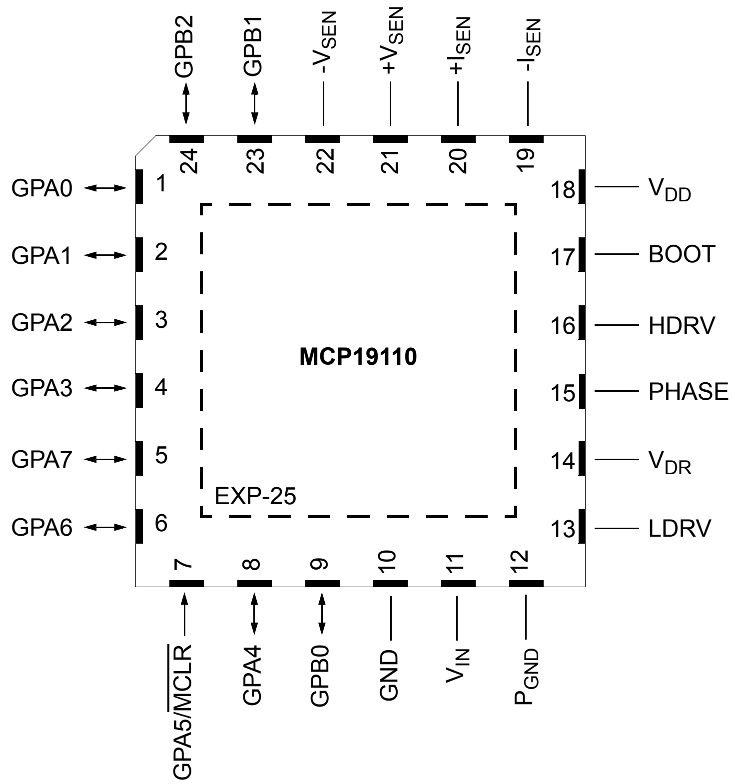


TABLE 1: 24-PIN SUMMARY

I/O	24-Pin QFN	ANSEL	A/D	Timers	MSSP	Interrupt	Pull-up	Basic	Additional
GPA0	1	Y	AN0	—	—	IOC	Y	—	Analog Debug Output [1]
GPA1	2	Y	AN1	—	—	IOC	Y	—	Sync. Signal In/Out [2, 3]
GPA2	3	Y	AN2	T0CKI	—	IOC INT	Y	—	—
GPA3	5	Y	AN3		—	IOC	Y	—	—
GPA4	8	N	—	—	—	IOC	N	—	—
GPA5	7	N	—	—	—	IOC[4]	Y[5]	$\overline{MCLR}$	—
GPA6	6	N	—	—	—	IOC	N	ICSPDAT	—
GPA7	5	N	—	—	SCL	IOC	N	ICSPCLK	—
GPB0	9	N	—	—	SDA	IOC	N	—	—
GPB1	23	Y	AN4	—	—	IOC	Y	—	Error Signal In/Out [3]
GPB2	24	Y	AN5	—	—	IOC	Y	—	—
V_{IN}	11	N	—	—	—	—	—	V_{IN}	Device Input Voltage
V_{DR}	14	N	—	—	—	—	—	V_{DR}	Gate Drive Supply Input Voltage
V_{DD}	18	N	—	—	—	—	—	V_{DD}	Internal Regulator Output
GND	10	N	—	—	—	—	—	GND	Small Signal Ground
P_{GND}	12	N	—	—	—	—	—	—	Large Signal Ground
LDRV	13	N	—	—	—	—	—	—	Low-Side MOSFET Connection
HDRV	16	N	—	—	—	—	—	—	High-Side MOSFET Connection
PHASE	15	N	—	—	—	—	—	—	Switch Node
BOOT	17	N	—	—	—	—	—	—	Floating Bootstrap Supply
$+V_{SEN}$	21	N	—	—	—	—	—	—	Output Voltage Differential Sense
$-V_{SEN}$	22	N	—	—	—	—	—	—	Output Voltage Differential Sense
$+I_{SEN}$	20	N	—	—	—	—	—	—	Current Sense Input
$-I_{SEN}$	19	N	—	—	—	—	—	—	Current Sense Input

Note 1: The Analog Debug Output is selected when the ATSTCON<BNCHEN> bit is set.
2: Selected when device is functioning as multiple output master or slave by proper configuration of the MLTPH<2:0> bits in the BUFFCON register.
3: Selected when device is functioning as multi-phase master or slave by proper configuration of the MLTPH<2:0> bits in the BUFFCON register.
4: The IOC is disabled when $\overline{MCLR}$ is enabled.
5: Weak pull-up always enabled when $\overline{MCLR}$ is enabled, otherwise the pull-up is under user control.

Pin Diagram – 28-Pin QFN (MCP19111)

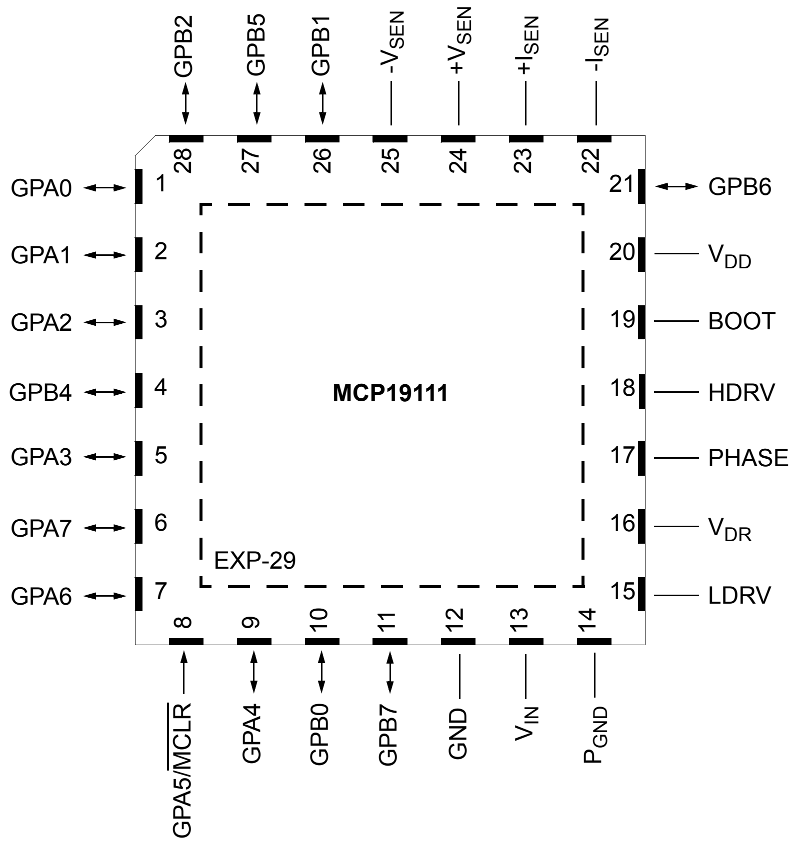


TABLE 2: 28-PIN SUMMARY

I/O	28-Pin QFN	ANSEL	A/D	Timers	MSSP	Interrupt	Pull-up	Basic	Additional
GPA0	1	Y	AN0	—	—	IOC	Y	—	Analog Debug Output (1)
GPA1	2	Y	AN1	—	—	IOC	Y	—	Sync. Signal In/Out (2, 3)
GPA2	3	Y	AN2	T0CKI	—	IOC INT	Y	—	—
GPA3	5	Y	AN3		—	IOC	Y	—	—
GPA4	9	N	—	—	—	IOC	N	—	—
GPA5	8	N	—	—	—	IOC(4)	Y(5)	$\overline{\text{MCLR}}$	—
GPA6	7	N	—	—	—	IOC	N	—	—
GPA7	6	N	—	—	SCL	IOC	N	—	—
GPB0	10	N	—	—	SDA	IOC	N	—	—
GPB1	26	Y	AN4	—	—	IOC	Y	—	Error Signal In/Out (3)
GPB2	28	Y	AN5	—	—	IOC	Y	—	—
GPB4	4	Y	AN6	—	—	IOC	Y	ICSPDAT ICDDAT	—
GPB5	27	Y	AN7	—	—	IOC	Y	ICSPCLK ICDCLK	Alternate Sync Signal In/Out (2, 3)
GPB6	21	N	—	—	—	IOC	Y	—	—
GPB7	11	N	—	—	—	IOC	Y	—	—
V_{IN}	13	N	—	—	—	—	—	V_{IN}	Device Input Voltage
V_{DR}	16	N	—	—	—	—	—	V_{DR}	Gate Drive Supply Input Voltage
V_{DD}	20	N	—	—	—	—	—	V_{DD}	Internal Regulator Output
GND	12	N	—	—	—	—	—	GND	Small Signal Ground
P_{GND}	14	N	—	—	—	—	—	—	Large Signal Ground
LDRV	15	N	—	—	—	—	—	—	Low-Side MOSFET Connection
HDRV	18	N	—	—	—	—	—	—	High-Side MOSFET Connection
PHASE	17	N	—	—	—	—	—	—	Switch Node
BOOT	19	N	—	—	—	—	—	—	Floating Bootstrap Supply
$+V_{SEN}$	24	N	—	—	—	—	—	—	Output Voltage Differential Sense
$-V_{SEN}$	25	N	—	—	—	—	—	—	Output Voltage Differential Sense
$+I_{SEN}$	23	N	—	—	—	—	—	—	Current Sense Input
$-I_{SEN}$	22	N	—	—	—	—	—	—	Current Sense Input

Note 1: The Analog Debug Output is selected when the ATSTCON<BNCHEN> bit is set.
2: Selected when device is functioning as multiple output master or slave by proper configuration of the MLTPH<2:0> bits in the BUFFCON register.
3: Selected when device is functioning as multi-phase master or slave by proper configuration of the MLTPH<2:0> bits in the BUFFCON register.
4: The IOC is disabled when $\overline{\text{MCLR}}$ is enabled.
5: Weak pull-up always enabled when $\overline{\text{MCLR}}$ is enabled, otherwise the pull-up is under user control.

Table of Contents

TO OUR VALUED CUSTOMERS

It is our intention to provide our valued customers with the best documentation possible to ensure successful use of your Microchip products. To this end, we will continue to improve our publications to better suit your needs. Our publications will be refined and enhanced as new volumes and updates are introduced.

If you have any questions or comments regarding this publication, please contact the Marketing Communications Department via E-mail at **docerrors@microchip.com**. We welcome your feedback.

Most Current Data Sheet

To obtain the most up-to-date version of this data sheet, please register at our Worldwide Web site at:

http://www.microchip.com

You can determine the version of a data sheet by examining its literature number found on the bottom outside corner of any page. The last character of the literature number is the version number, (e.g., DS30000000A is version A of document DS30000000).

Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

To determine if an errata sheet exists for a particular device, please check with one of the following:

- Microchip's Worldwide Web site; **http://www.microchip.com**
- Your local Microchip sales office (see last page)

When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

Customer Notification System

Register on our web site at **www.microchip.com** to receive the most current information on all of our products.

NOTES:

1.0 DEVICE OVERVIEW

The MCP19110/11 is a highly integrated, mixed signal, analog pulse-width modulation (PWM) current mode controller with an integrated microcontroller core for synchronous DC/DC step-down applications. Since the MCP19110/11 uses traditional analog control circuitry to regulate the output of the DC/DC converter, the integration of the PIC® microcontroller mid-range core is used to provide complete customization of device operating parameters, start-up and shut down profiles, protection levels and fault handling procedures.

The MCP19110/11 is designed to efficiently operate from a single 4.5V to 32V supply. It features integrated synchronous drivers, bootstrap device, internal linear regulator and 4 kW nonvolatile memory all in a space-saving 24-pin 4 mm x 4mm QFN package (MCP19110) or 28-pin 5 mm x 5 mm QFN package (MCP19111).

After initial device configuration using Microchip's MPLAB® X Integrated Development Environment (IDE) software, the PMBus or I^2C can be used by a host to communicate with, or modify, the operation of the MCP19110/11.

Two internal linear regulators generate two 5V rails. One 5V rail is used to provide power for the internal analog circuitry and is contained on-chip. The second 5V rail provides power to the PIC device and is present on the V_{DD} pin. It is recommended that a 1 µF capacitor be placed between V_{DD} and P_{GND}. The V_{DD} pin may also be directly connected to the V_{DR} pin, or connected through a low-pass RC filter. The V_{DR} pin provides power to the internal synchronous driver.

FIGURE 1-1: TYPICAL APPLICATION CIRCUIT

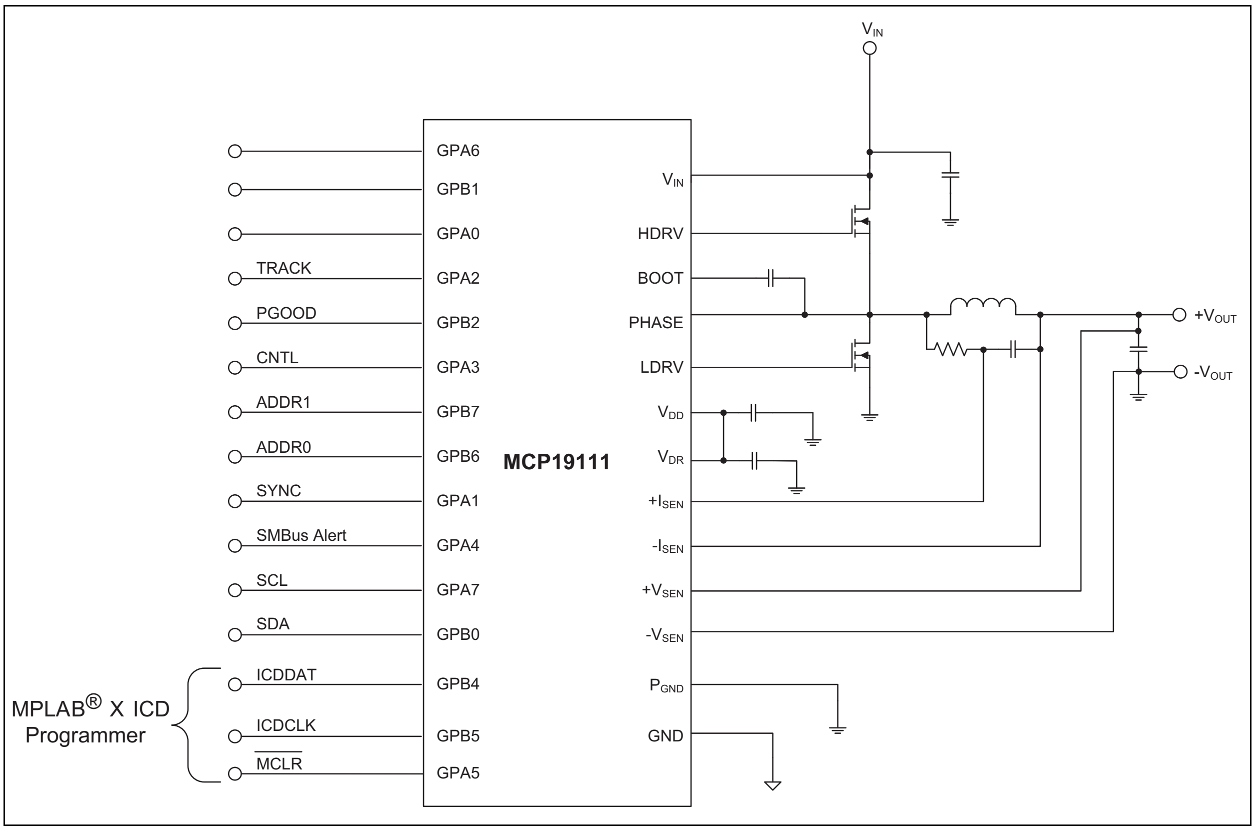


FIGURE 1-2: MCP19110/11 SYNCHRONOUS BUCK BLOCK DIAGRAM

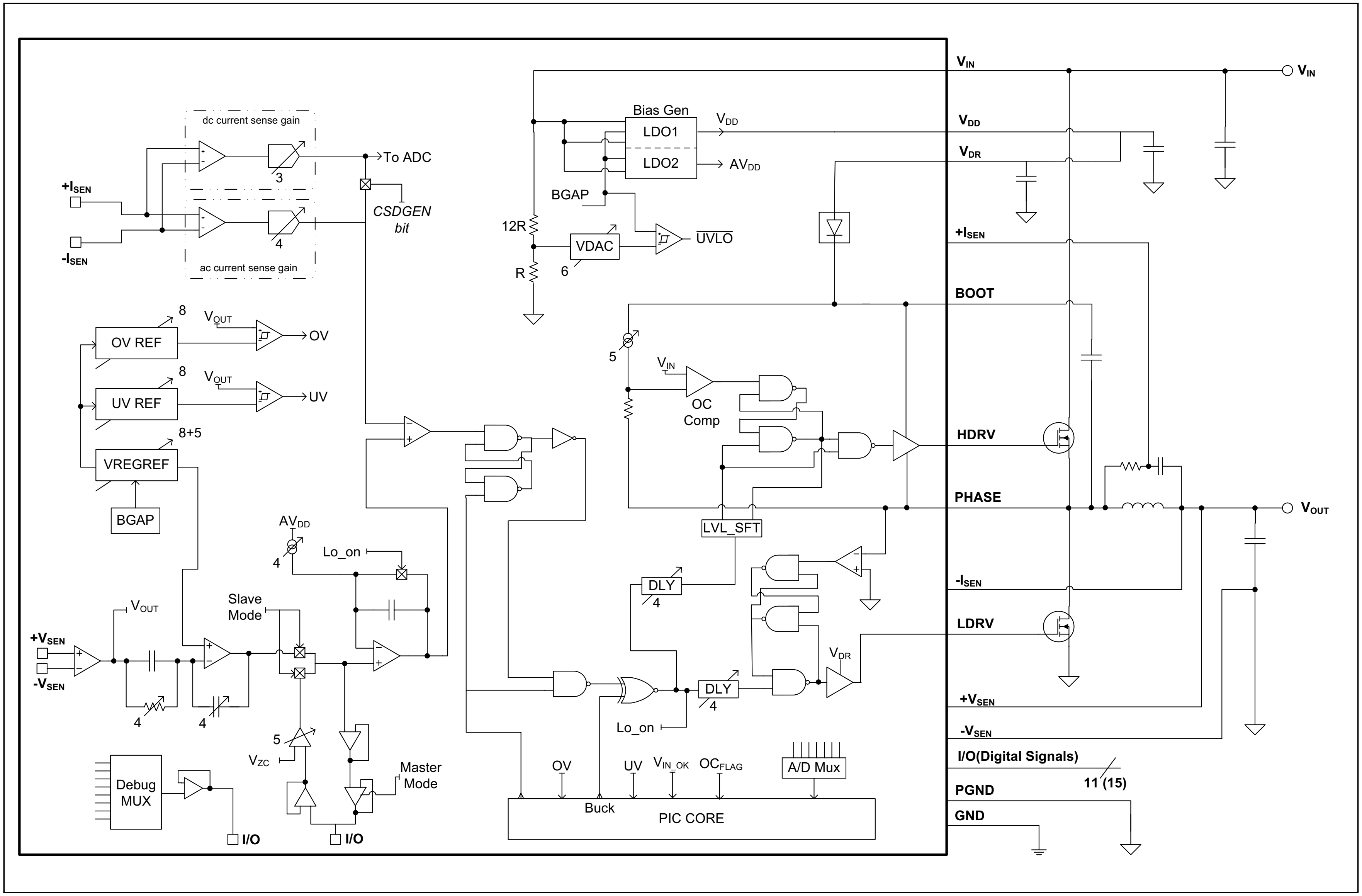
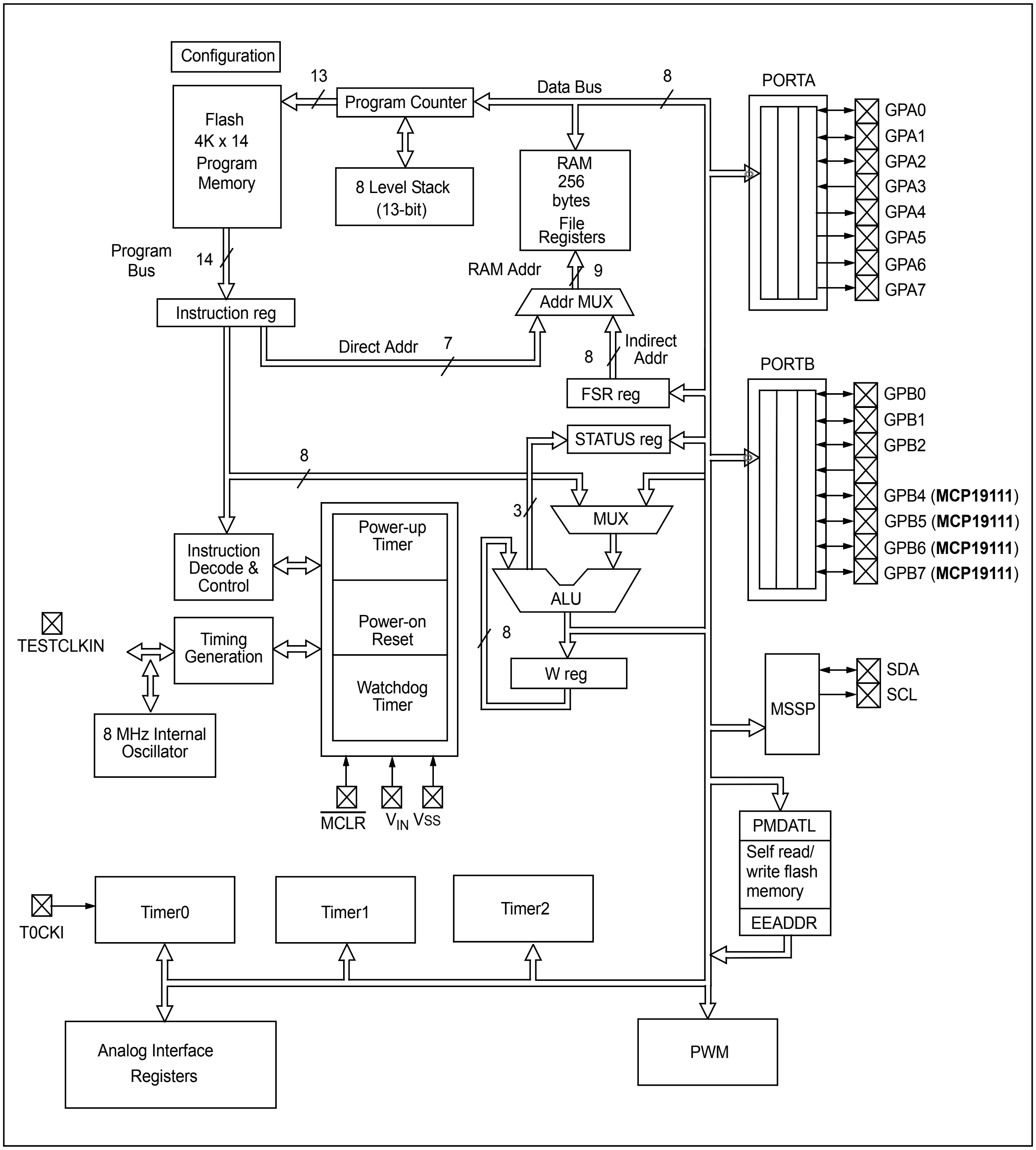


FIGURE 1-3: MICROCONTROLLER CORE BLOCK DIAGRAM



2.0 PIN DESCRIPTION

The MCP19110/11 family of devices feature pins that have multiple functions associated with each pin. Table 2-1 provides a description of the different functions. See **Section 2.1 "Detailed Pin Functional Description"** for more detailed information.

TABLE 2-1: MCP19110/11 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GPA0/AN0/ANALOG_TEST	GPA0	TTL	CMOS	General purpose I/O
	AN0	AN	—	A/D Channel 0 input.
	ANALOG_TEST	—	—	Internal analog signal multiplexer output (1)
GPA1/AN1/CLKPIN	GPA1	TTL	CMOS	General purpose I/O
	AN1	AN	—	A/D Channel 1 input.
	CLKPIN	—	—	Switching frequency clock input or output (2 ,3)
GPA2/AN2/T0CKI/INT	GPA2	TTL	CMOS	General purpose I/O
	AN2	AN	—	A/D Channel 2 input
	T0CKI	ST	—	Timer0 clock input
	INT	ST	—	External interrupt
GPA3/AN3	GPA3	TTL	CMOS	General purpose I/O
	AN3	AN	—	A/D Channel 3 input
GPA4	GPA4	TTL	OD	General purpose I/O
GPA5/$\overline{\text{MCLR}}$	GPA5	TTL	—	General purpose input only
	$\overline{\text{MCLR}}$	ST	—	Master Clear with internal pull-up
GPA6/ICSPDAT	GPA6	ST	CMOS	General purpose I/O
	ICSPDAT		CMOS	Serial Programming Data I/O (**MCP19110 Only**)
GPA7/SCL/ICSPCLK	GPA7	ST	OD	General purpose open-drain I/O
	SCL	I^2C	OD	I^2C clock
	ICSPCLK	ST	—	Serial Programming Clock (**MCP19110 Only**)
GPB0/SDA	GPB0	TTL	OD	General purpose I/O
	SDA	I^2C	OD	I^2C data input/output
GPB1/AN4/EAPIN	GPB1	TTL	CMOS	General purpose I/O
	AN4	AN	—	A/D Channel 4 input
	EAPIN	—	—	Error amplifier signal input/output (3)
GPB2/AN5	GPB2	TTL	CMOS	General purpose I/O
	AN5	AN	—	A/D Channel 5 input
GPB4/AN6/ICSPDAT (**MCP19111 Only**)	GPB4	TTL	CMOS	General purpose I/O
	AN6	AN	—	A/D Channel 6 input
	ICSPDAT	ST	CMOS	Serial Programming Data I/O

Legend: AN = Analog input or output CMOS =CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST =Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C

Note 1: Analog Test is selected when the ATSTCON<BNCHEN> bit is set.
2: Selected when device is functioning as multiple output master or slave by proper configuration of the MLTPH<2:0> bits in the BUFFCON register.
3: Selected when device is functioning as multi-phase master or slave by proper configuration of the MLTPH<2:0> bits in the BUFFCON register.

TABLE 2-1: MCP19110/11 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
GPB5/AN7/ICSPCLK/ ALT_CLKPIN (**MCP19111 Only**)	GPB5	TTL	CMOS	General purpose I/O
	AN7	AN	—	A/D Channel 7 input
	ISCPCLK	ST	—	Serial Programming Clock
	ALT_CLKPIN	—	—	Alternate switching frequency clock input or output (2,3)
GPB6 (**MCP19111 Only**)	GPB6	TTL	CMOS	General purpose I/O
GPB7 (**MCP19111 Only**)	GPB7	TTL	CMOS	General purpose I/O
V_{IN}	V_{IN}	—	—	Device input supply voltage
V_{DD}	V_{DD}	—	—	Internal +5V LDO output pin
V_{DR}	V_{DR}	—	—	Gate drive supply input voltage pin
GND	GND	—	—	Small signal quiet ground
P_{GND}	P_{GND}	—	—	Large signal power ground
LDRV	LDRV	—	—	High-current drive signal connected to the gate of the low-side MOSFET
HDRV	HDRV	—	—	Floating high-current drive signal connected to the gate of the high-side MOSFET
PHASE	PHASE	—	—	Synchronous buck switch node connection
BOOT	BOOT	—	—	Floating bootstrap supply
$+V_{SEN}$	$+V_{SEN}$	—	—	Positive input of the output voltage sense differential amplifier
$-V_{SEN}$	$-V_{SEN}$	—	—	Negative input of the output voltage sense differential amplifier
$+I_{SEN}$	$+I_{SEN}$	—	—	Current sense input
$-I_{SEN}$	$-I_{SEN}$	—	—	Current sense input
EP	—	—	—	Exposed Thermal Pad

Legend: AN = Analog input or output CMOS =CMOS compatible input or output OD = Open Drain
TTL = TTL compatible input ST =Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C

Note 1: Analog Test is selected when the ATSTCON<BNCHEN> bit is set.

2: Selected when device is functioning as multiple output master or slave by proper configuration of the MLTPH<2:0> bits in the BUFFCON register.

3: Selected when device is functioning as multi-phase master or slave by proper configuration of the MLTPH<2:0> bits in the BUFFCON register.

2.1 Detailed Pin Functional Description

2.1.1 GPA0 PIN

GPA0 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN0 is an input to the A/D. To configure this pin to be read by the A/D on channel 0, bits TRISA0 and ANSA0 must be set.

When the ATSTCON<BNCHEN> bit is set, this pin is configured as the ANALOG_TEST function. It is a buffered output of the internal analog signal multiplexer. Signals present on this pin are controlled by the BUFFCON register, see Register 8-2.

2.1.2 GPA1 PIN

GPA1 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN1 is an input to the A/D. To configure this pin to be read by the A/D on channel 1, bits TRISA1 and ANSA1 must be set.

When the MCP19110/11 is configured as a multiple output or multi-phase MASTER or SLAVE, this pin is configured to be the switching frequency synchronization input or output, CLKPIN. See **Section 3.10.6 “Multi-Phase System”** and **Section 3.10.7 “Multiple Output System”** for more information.

2.1.3 GPA2 PIN

GPA2 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN2 is an input to the A/D. To configure this pin to be read by the A/D on channel 2, bits TRISA2 and ANSA2 must be set.

When bit T0CS is set, the T0CKI function is enabled. See **Section 23.0 “Timer0 Module”** for more information.

GPA2 can also be configured as an external interrupt by setting of the INTE bit. See **Section 15.2 “GPA2/INT Interrupt”** for more information.

2.1.4 GPA3 PIN

GPA3 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPA. An internal weak pull-up and interrupt-on-change are also available.

AN3 is an input to the A/D. To configure this pin to be read by the A/D on channel 3, bits TRISA3 and ANSA3 must be set.

2.1.5 GPA4 PIN

GPA4 is a true open-drain general purpose pin whose data direction is controlled in TRISGPA. There is no internal connection between this pin and device V_{DD}, making this pin ideal to be used as an SMBus Alert pin. This pin does not have a weak pull-up, but interrupt-on-change is available.

2.1.6 GPA5 PIN

GPA5 is a general purpose TTL input-only pin. An internal weak pull-up and interrupt-on-change are also available.

For programming purposes, this pin is to be connected to the $\overline{\text{MCLR}}$ pin of the serial programmer. See **Section 28.0 “In-Circuit Serial Programming™ (ICSP™)”** for more information.

2.1.7 GPA6 PIN

GPA6 is a general purpose CMOS input/output pin whose data direction is controlled in TRISGPA. An interrupt-on-change is also available.

On the MCP19110, the ISCPDAT is the serial programming data input function. This is used in conjunction with ICSPCLK to serial program the device. This pin function is only implemented on the MCP19110.

2.1.8 GPA7 PIN

GPA7 is a true open-drain general purpose pin whose data direction is controlled in TRISGPA. There is no internal connection between this pin and device V_{DD}. This pin does not have a weak pull-up, but interrupt-on-change is available.

When the MCP19110/11 is configured for I^2C communication (see **Section 27.2 “I^2C Mode Overview”**), GPA7 functions as the I^2C clock, SCL.

On the MCP19110, the ISCPCLK is the serial programming clock function. This is used in conjunction with ICSPDAT to serial program the device. This pin function is only implemented on the MCP19110.

2.1.9 GPB0 PIN

GPB0 is a true open-drain general purpose pin whose data direction is controlled in TRISGPB. There is no internal connection between this pin and device V_{DD}. This pin does not have a weak pull-up, but interrupt-on-change is available.

When the MCP19110/11 is configured for I^2C communication (see **Section 27.2 “I^2C Mode Overview”**), GPB0 functions as the I^2C clock, SDA.

2.1.10 GPB1 PIN

GPB1 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN4 is an input to the A/D. To configure this pin to be read by the A/D on channel 4, bits TRISB1 and ANSB1 must be set.

When the MCP19110/11 is configured as a multiple output or multi-phase MASTER or SLAVE, this pin is configured to be the error amplifier signal input or output. See **Section 3.10.6 "Multi-Phase System"** and **Section 3.10.7 "Multiple Output System"**, for more information.

2.1.11 GPB2 PIN

GPB2 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN5 is an input to the A/D. To configure this pin to be read by the A/D on channel 5, bits TRISB2 and ANSB2 must be set.

2.1.12 GPB4 PIN

This pin and its associated functions are only available on the MCP19111 device.

GPB4 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN6 is an input to the A/D. To configure this pin to be read by the A/D on channel 6, bits TRISB4 and ANSB4 must be set.

On the MCP19111, the ISCPDAT is the serial programming data input function. This is used in conjunction with ICSPCLK to serial program the device. This pin function is only implemented on the MCP19111.

2.1.13 GBP5 PIN

This pin and its associated functions are only available on the MCP19111 device.

GPB5 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

AN7 is an input to the A/D. To configure this pin to be read by the A/D on channel 7, bits TRISB5 and ANSB5 must be set.

On the MCP19111, the ISCPCLK is the serial programming clock function. This is used in conjunction with ICSPDAT to serial program the device. This pin function is only implemented on the MCP19111.

This pin can also be configured as an alternate switching frequency synchronization input or output, ALT_CLKPIN, for use in multiple output or multi-phase systems. See **Section 19.1 "Alternate Pin Function"** for more information.

2.1.14 GPB6 PIN

This pin and associated functions is only available on the MCP19111 device.

GPB6 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

2.1.15 GPB7 PIN

This pin and associated functions is only available on the MCP19111 device.

GPB7 is a general purpose TTL input or CMOS output pin whose data direction is controlled in TRISGPB. An internal weak pull-up and interrupt-on-change are also available.

2.1.16 V_{IN} PIN

Device input power connection pin. It is recommended that capacitance be placed between this pin and the GND pin of the device.

2.1.17 V_{DD} PIN

The output of the internal +5.0V regulator is connected to this pin. It is recommended that a 1.0 µF bypass capacitor be connected between this pin and the GND pin of the device. The bypass capacitor should be placed physically close to the device.

2.1.18 V_{DR} PIN

The 5V supply for the low-side driver is connected to this pin. The pin can be connected by an RC filter to the V_{DD} pin.

2.1.19 GND PIN

GND is the small signal ground connection pin. This pin should be connected to the exposed pad, on the bottom of the package.

2.1.20 P_{GND} PIN

Connect all large signal level ground returns to P_{GND}. These large-signal level ground traces should have a small loop area and minimal length to prevent coupling of switching noise to sensitive traces.

2.1.21 LDRV PIN

The gate of the low-side or rectifying MOSFET is connected to LDRV. The PCB tracing connecting LDRV to the gate must be of minimal length and appropriate width to handle the high peak drive currents and fast voltage transitions.

2.1.22 HDRV PIN

The gate of the high-side MOSFET is connected to HDRV. This is a floating driver referenced to PHASE. The PCB trace connecting HDRV to the gate must be of minimal length and appropriate width to handle the high-peak drive current and fast voltage transitions.

2.1.23 PHASE PIN

The PHASE pin provides the return path for the high-side gate driver. The source of the high-side MOSFET, drain of the low-side MOSFET and the inductor are connected to this pin.

2.1.24 BOOT PIN

The BOOT pin is the floating bootstrap supply pin for the high-side gate driver. A capacitor is connected between this pin and the PHASE pin to provide the necessary charge to turn on the high-side MOSFET.

2.1.25 $+V_{SEN}$ PIN

The non-inverting input of the unity gain amplifier used for output voltage remote sensing is connected to the $+V_{SEN}$ pin. This pin can be internally pulled-up to V_{DD} by setting PE1<PUEN> bit.

2.1.26 $-V_{SEN}$ PIN

The inverting input of the unity gain amplifier used for output voltage remote sensing is connected to the $-V_{SEN}$ pin. This pin can be internally pull-down to GND by setting PE1<PDEN> bit.

2.1.27 $+I_{SEN}$ PIN

The non-inverting input of the current sense amplifier is connected to the $+I_{SEN}$ pin.

2.1.28 $-I_{SEN}$ PIN

The inverting input of the current sense amplifier is connected to the $-I_{SEN}$ pin.

2.1.29 EXPOSED PAD (EP)

There is no internal connection to the Exposed Thermal Pad. The EP should be connected to the GND pin and to the GND PCB plane to aid in the removal of the heat.

3.0 FUNCTIONAL DESCRIPTION

3.1 Linear Regulators

Two internal linear regulators generate two 5V rails. One 5V rail is used to provide power for the internal analog circuitry and is contained on-chip. The second 5V rail provides power to the internal PIC core and it is present on the V_{DD} pin. It is recommended that a 1 µF capacitor be placed between V_{DD} and P_{GND}.

The V_{DR} pin provides power to the internal synchronous MOSFET driver. V_{DD} can be directly connected to V_{DR} or connected through a low-pass RC filter to provide noise filtering. A 1 µF ceramic bypass capacitor should be placed between V_{DR} and P_{GND}. When connecting V_{DD} to V_{DR}, the gate drive current required to drive the external MOSFETs must be added to the MCP19110/11 quiescent current, $I_{Q(max)}$. This total current must be less than the maximum current, $I_{DD\text{-}OUT}$, available from V_{DD} that is specified in **Section 4.2 "Electrical Characteristics"**.

EQUATION 3-1: TOTAL REGULATOR CURRENT

$$I_{DD-OUT} > (I_Q + I_{DRIVE} + I_{EXT})$$

Where:

- $I_{DD\text{-}OUT}$ is the total current available from V_{DD}
- I_Q is the device quiescent current
- I_{DRIVE} is the current required to drive the external MOSFETs
- I_{EXT} is the amount of current used to power additional external circuitry.

EQUATION 3-2: GATE DRIVE CURRENT

$$I_{DRIVE} = (Q_{gHIGH} + Q_{gLOW}) \times F_{SW}$$

Where:

- I_{DRIVE} is the current required to drive the external MOSFETs
- Q_{gHIGH} is the total gate charge of the high-side MOSFET
- Q_{gLOW} is the total gate charge of the low-side MOSFET
- F_{SW} is the switching frequency

Alternatively, an external regulator can be used to power the synchronous driver. An external 5V source can be connected to V_{DR}. The amount of current required from this external source can be found in Equation 3-2. Care must be taken that the voltage applied to V_{DR} does not exceed the maximum ratings found in **Section 4.1 "Absolute Maximum Ratings (†)"**.

3.2 Internal Synchronous Driver

The internal synchronous driver is capable of driving two N-Channel MOSFETs in a synchronous rectified buck converter topology. The gate of the floating MOSFET is connected to the HDRV pin. The source of this MOSFET is connected to the PHASE pin. The HDRV pin source and sink current is configurable. By setting the DRVSTR bit in the PE1 register, the high-side is capable of sourcing and sinking a peak current of 1A. By clearing this bit, the source and sink peak current is 2A.

> **Note 1:** The PE1<DRVSTR> bit configures the peak source/sink current of the HDRV pin.

The MOSFET connected to the LDRV pin is not floating. The low-side MOSFET gate is connected to the LDRV pin and the source of this MOSFET is connected to P_{GND}. The drive strength of the LDRV pin is not configurable. This pin is capable of sourcing a peak current of 2A. The peak sink current is 4A. This helps keep the low-side MOSFET off when the high-side MOSFET is turning on.

> **Note 1:** Refer to Figure 1-1 for a graphical representation of the MOSFET connections.

3.2.1 MOSFET DRIVER DEAD TIME

The MOSFET driver dead time is defined as the time between one drive signal going low and the complimentary drive signal going high. Refer to Figure 6-2. The MCP19110/11 has the capability to adjust both the high-side and low-side driver dead time independently. The adjustment of the driver dead time is controlled by the DEADCON register and is adjustable in 4 ns increments.

> **Note 1:** The DEADCON register controls the amount of dead time added to the HDRV or LDRV signal. The dead time circuitry is enabled by the LDLYBY and HDLYBY bits in the PE1 register.

3.2.2 MOSFET DRIVER CONTROL

The MCP19110/11 has the ability to disable the entire synchronous driver or just one side of the synchronous drive signal. The bits that control the MOSFET driver can be found in the Register 8-1.

By setting ATSTCON<DRVDIS>, the entire synchronous driver is disabled. The HDRV and LDRV signals are set low and the PHASE pin is floating. Clearing this bit allows normal operation.

Individual control of the HDRV or LDRV signal is accomplished by setting or clearing the HIDIS or LODIS bits in the ATSTCON register. When either driver is disabled, the output signal is set low.

3.3 Output Voltage

The output voltage is configured by the settings contained in the OVCCON and OVFCON registers. No external resistor divider is needed to set the output voltage. Refer to **Section 6.10 "Output Voltage Configuration"**.

The MCP19110/11 contains a unity gain differential amplifier used for remote sensing of the output voltage. Connect the $+V_{SEN}$ and $-V_{SEN}$ pins directly at the load for better load regulation. The $+V_{SEN}$ and $-V_{SEN}$ are the positive and negative inputs, respectively, of the differential amplifier.

3.4 Switching Frequency

The switching frequency is configurable over the range of 100 kHz to 1.6 MHz. The Timer2 module is used to generate the HDRV/LDRV switching frequency. Refer to **Section 26.0 "PWM Module"** for more information. Example 3-1 shows how to configure the MCP19110/11 for a switching frequency of 300 kHz.

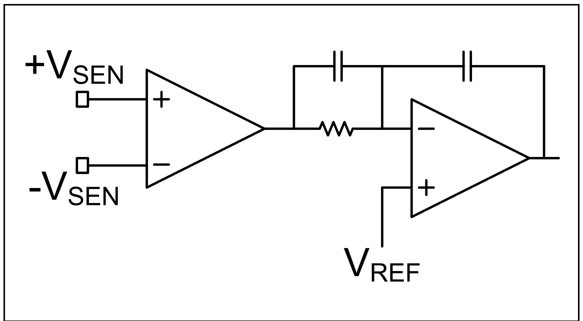
EXAMPLE 3-1: CONFIGURING F_{SW}

```
BANKSEL    T2CON
CLRF       T2CON   ;Turn off Timer2
CLRF       TMR2    ;Initialize module
MOVLW      0x19    ;Fsw=300 kHz
MOVWF      PR2
MOVLW      0x0A    ;Max duty cycle=40%
MOVWF      PWMRL
MOVLW      0x00    ;No phase shift
MOVWF      PWMPHL
MOVLW      0x04    ;Turn on Timer2
MOVWF      T2CON
```

3.5 Compensation

The MCP19110/11 is an analog peak current mode controller with integrated adjustable compensation. The CMPZCON register is used to adjust the compensation zero frequency and gain. Figure 3-1 shows the internal compensation network with the output differential amplifier.

FIGURE 3-1: SIMPLIFIED INTERNAL COMPENSATION



3.6 Slope Compensation

In current mode control systems, slope compensation needs to be added to the control path to help prevent subharmonic oscillation when operating with greater than 50% duty cycle. In the MCP19110/11, a negative slope is added to the error amplifier output signal before it is compared to the current sense signal. The amount of slope added is controlled by the SLPCRCON register, Register 6-7.

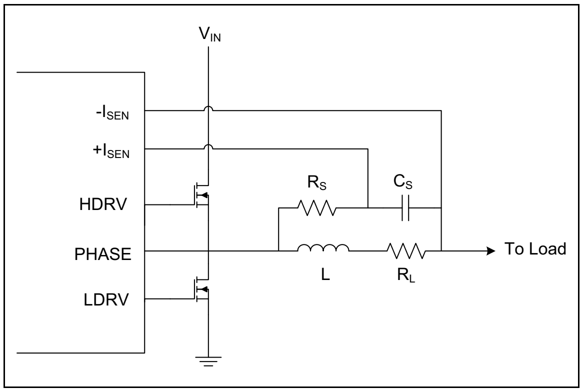
> **Note 1:** To enable the slope compensation circuitry, the ABECON<SLCPBY> bit must be cleared.

The amount of slope compensation added should be equal to the inductor current down slope during the high-side off time.

3.7 Current Sense

The output current is differentially sensed by the MCP19110/11. The sense element can be either a resistor placed in series with the output, or the series resistance of the inductor. If the inductor series resistance is used, a filter is needed to remove the large AC component of the voltage that appears across the inductor and leave only the small AC voltage that appears across the inductor resistance, as shown in Figure 3-2. This small AC voltage is representative of the output current.

FIGURE 3-2: INDUCTOR CURRENT SENSE FILTER



The value of R_S and C_S can be found by using Equation 3-3. When the current sense filter time constant is set equal to the inductor time constant, the voltage appearing across C_S approximates the current flowing in the inductor, multiplied by the inductor resistance.

EQUATION 3-3: CALCULATING FILTER VALUES

$$\frac{L}{R_L} = (R_S \times C_S)$$

Where:

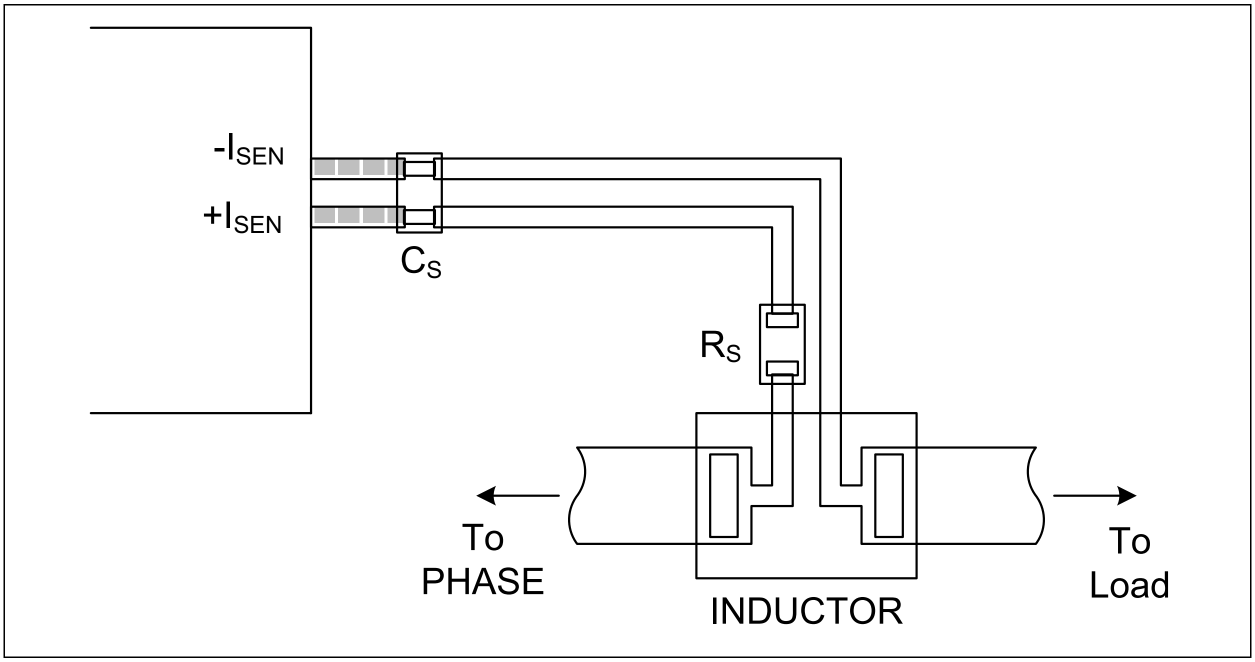
- L is the inductance value of the output inductor
- R_L is the series resistance of the output inductor
- R_S is the current sense filter resistor
- C_S is the current sense filter capacitor

Both AC gain and DC gain can be added to the current sense signal. Refer to **Section 6.3 "Current Sense AC Gain"** and **Section 6.4 "Current Sense DC Gain"** for more information.

3.7.1 PLACEMENT OF THE CURRENT SENSE FILTER COMPONENTS

The amplitude of the current sense signal is typically less than 100 mV peak-to-peak. Therefore, the small signal current sense traces are very susceptible to circuit noise. When designing the printed circuit board, placement of R_S and C_S is very important. The $+I_{SEN}$ and $-I_{SEN}$ traces should be routed parallel to each other with minimum spacing. This Kelvin sense routing technique helps minimize noise sensitivity. The filter capacitor (C_S), should be placed as close to the MCP19110/11 as possible. This will help filter any noise that is injected onto the current sense lines. The trace connecting C_S to the inductor should occur directly at the inductor and not at any other $+V_{SEN}$ trace. The filter resistor (R_S), should be placed close to the inductor. See Figure 3-3 for component placement. Care should also be taken to avoid routing the $+I_{SEN}$ and $-I_{SEN}$ traces near the high current switching nodes of the HDRV, LDRV, PHASE, or BOOST traces. It is recommended that a ground layer be placed between these high current traces and the small signal current sense traces.

FIGURE 3-3: CURRENT SENSE FILTER COMPONENT PLACEMENT



3.8 Protection Features

3.8.1 INPUT UNDERVOLTAGE LOCKOUT

The input Undervoltage Lockout (UVLO) threshold is configurable by the VINLVL register, Register 6-1. When the voltage at the V_{IN} pin of the MCP19110/11 is below the configurable threshold, the PIR2<VINIF> flag will be set. This flag is cleared by hardware once the V_{IN} voltage is greater than the configurable threshold. By enabling the global interrupts or polling the VINIF bit, the MCP19110/11 can be disabled when the V_{IN} voltage is below the threshold.

> **Note 1:** The UVLO DAC must be enabled by setting the VINLVL<UVLOEN> bit.
>
> **2:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit (GIE) of the INTCON register.

Some techniques that can be used to disable the switching of the MCP19110/11 while the VINIF flag is set include setting the ATSTCON<DVRDIS> bit, setting the reference voltage to 0V, setting the PE1<PUEN> bit, or setting the ATSTCON<HIDIS> and ATSTCON<LODIS> bits.

3.8.2 OUTPUT OVERCURRENT

The MCP19110/11 senses the voltage drop across the high-side MOSFET to determine when an output overcurrent (OC) exists. This voltage drop is configurable by the OCCON register (Register 6-2), and is measured when the high-side MOSFET is conducting. To avoid false OC events, leading edge blanking is applied to the measurements. The amount of blanking is controlled by the OCLEB<1:0> bits in the OCCON register. See **Section 6.2 "Output Overcurrent"** for more information.

When the input voltage is greater than 20V, or if the R_{DSON} of the high-side MOSFET is such that the programmed overcurrent threshold does not produce acceptable peak overcurrent protection, an alternative method must be used to determine an overcurrent situation. An alternative technique can use the configurable output undervoltage protection, and the PE1<UVTEE> bit, to quickly terminate switching when the output voltage drops because of an overcurrent event.

> **Note 1:** The OC DAC must be enabled by setting the OCCON<OCEN> bit.

3.8.3 OUTPUT UNDERVOLTAGE

When the output undervoltage DAC is enabled by setting the ABECON<UVDCEN> bit, the voltage measured between the $+V_{SEN}$ and $-V_{SEN}$ pins is monitored and compared to the UV threshold controlled by the OUVCON register (Register 6-12). When the output voltage is below the threshold, the PIR2<UVIF> flag will be set. Once set, firmware can determine how the MCP19110/11 responds to the fault condition and it must clear the UVIF flag.

By setting the PE1<UVTEE> bit, the HDRV and LDRV signals will be asserted low when the UVIF flag is set. The signals will remain low until the flag is cleared.

> **Note 1:** The UV DAC must be enabled by setting the ABECON<UVDCEN> bit.
>
> **2:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit (GIE) of the INTCON register.
>
> **3:** The output of the remote sense comparator is compared to the UV threshold. Therefore, the offset in this comparator should be considered when calculating the UV threshold.

3.8.4 OUTPUT OVERVOLTAGE

When the output overvoltage DAC is enabled by setting the ABECON<OVDCEN> bit, the voltage measured between the $+V_{SEN}$ and $-V_{SEN}$ pins is monitored and compared to the OV threshold controlled by the OOVCON register (Register 6-13). When the output voltage is above the threshold, the PIR2<OVIF> flag will be set. Once set, firmware can determine how the MCP19110/11 responds to the fault condition and it must clear the OVIF flag.

By setting the PE1<OVTEE> bit, the HDRV and LDRV signals will be asserted low when the OVIF flag is set. The signals will remain low until the flag is cleared.

> **Note 1:** The OV DAC must be enabled by setting the ABECON<UVDCEN> bit.
>
> **2:** Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit (GIE) of the INTCON register.
>
> **3:** The output of the remote sense comparator is compared to the OV threshold. Therefore, the offset in this comparator should be considered when calculating the OV threshold.

3.8.5 OVERTEMPERATURE

The MCP19110/11 features a hardware overtemperature shutdown protection typically set at +160°C. No firmware fault-handling procedure is required to shutdown the MCP19110/11 for an overtemperature condition. The ABECON<TMPSEN> bit must be set to enable the over temperature circuitry.

3.9 PIC Microcontroller Core

Integrated into the MCP19110/11 is the PIC microcontroller mid-range core. This is a fully functional microcontroller, allowing proprietary features to be implemented. Setting the CONFIG<CP> bit enables the code protection. The firmware is then protected from external reads or writes. Various status and fault bits are available to customize the fault handling response.

A minimal amount of firmware is required to properly configure the MCP19110/11. **Section 6.0 “Configuring the MCP19110/11”** contains detailed information about each register that needs to be set for the MCP19110/11 device to operate. To aid in the development of the required firmware, a Graphical User Interface (GUI) has been developed. This GUI can be used to quickly configure the MCP19110/11 for basic operation. Customized or proprietary features can then be added to the GUI generated firmware.

> **Note 1:** The GUI can be found on the MCP19110/11 product page on www.microchip.com.
>
> **2:** Microchip's MPLAB X Integrated Development Environment Software is required to use the GUI.

The MCP19110/11 device features firmware debug support. See **Section 30.0 “Development Support”** for more information.

3.10 Miscellaneous Features

3.10.1 DEVICE ADDRESSING

The communication address of the MCP19110/11 is stored in the SSPADD register. This value can be loaded when the device firmware is programmed or configured by external components. By reading a voltage on a GPIO with the ADC, a device specific address can be stored into the SSPADD register.

The MCP19110/11 contains a second address register, SSPADD2. This is a 7-bit address that can be used as the SMBus alert address when PMBus communication is used. See **Section 27.0 “Master Synchronous Serial Port (MSSP) Module”** for more information.

3.10.2 DEVICE ENABLE

A GPIO pin can be configured to be a device enable pin. By configuring the pin as an input, the PORT register or the interrupt on change (IOC) can be used to enable the device. Example 3-2 shows how to configure a GPIO as an enable pin by testing the PORT register.

EXAMPLE 3-2: CONFIGURING GPA3 AS DEVICE ENABLE

```
    BANKSEL     TRISGPA
    BSF         TRISGPA, 3      ;Set GPA3 as input
    BANKSEL     ANSELA
    BCF         ANSELA, 3       ;Set GPA3 as digital input
    :
    :                           ;Insert additional user code here
    :
WAIT_ENABLE:
    BANKSEL     PORTGPA
    BTFSS       PORTGPA, 3      ;Test GPA3 to see if pulled high
                                ;A high on GPA3 indicated device to be enabled
    GOTO        WAIT_ENABLE     ;Stay in loop waiting for device enable
    BANKSEL     ATSTCON
    BSF         ATSTCON, 0      ;Enable the device by enabling drivers
    :
    :                           ;Insert additional code here
    :
```

3.10.3 OUTPUT POWER GOOD

The output voltage measured between the +V_{SEN} and -V_{SEN} pins can be monitored by the internal ADC. In firmware, when this ADC reading matches a user-defined power good value, a GPIO can be toggled to indicate the system output voltage is within a specified range. Delays, hysteresis and time-out values can all be configured in firmware.

3.10.4 OUTPUT VOLTAGE SOFT-START

During start-up, soft start of the output voltage is accomplished in firmware. By using one of the internal timers and incrementing the OVCCON or OVFCON register on a timer overflow, very long soft start times can be achieved.

3.10.5 OUTPUT VOLTAGE TRACKING

The MCP19110/11 can be configured to track another voltage signal at start-up or shutdown. The ADC is configured to read a GPIO that has the desired tracking voltage applied to it. The firmware then handles the tracking of the internal output voltage reference to this ADC reading.

3.10.6 MULTI-PHASE SYSTEM

In a multi-phase system, the output of each converter is connected together. There is one master device that sets the system switching frequency and provides each slave device with an error signal, in order to regulate the output to the same value.

The MCP19110/11 can be configured as a multi-phase master or slave by the setting of the MLTPH<2:0> bits in the BUFFCON register (Register 8-2). When set as a multi-phase master device, the internal switching frequency clock is connected to GPA1 and the output of the error amplifier is connected to GPB1. The GPIOs need to be configured as outputs.

When set as a multi-phase slave device, the GPA1 pin is configured as the CLKPIN function. The switching frequency clock from the master device must be connected to GPA1. The slave device will synchronize its internal switching frequency clock to the master clock. Phase shift can be applied by setting the PWMPHL register of the slave device. The slave GPB1 pin is configured as the error signal input pin (EAPIN). The master error amplifier output must be connected to GPB1. Gain can be added to the master error amplifier output signal by the SLVGNCON register setting (Register 6-8). The slave device will use this master error signal to regulate the output voltage. When set as a slave device, GPA1 and GPB1 need to be configured as inputs. Refer to **Section 26.1 “Standard Pulse-Width Modulation (PWM) Mode”** for additional information.

Note 1:	The ALT_CLKPIN can also be used by setting the APFCON<CLKSEL> bit. This function is only available in the MCP19111.

3.10.7 MULTIPLE OUTPUT SYSTEM

In a multiple output system, the switching frequency of each converter should be synchronized to a master clock to prevent beat frequencies from developing. Phase shift is often added to the master clock to help smooth the system input current. The MCP19110/11 has the ability to function as a multiple output master or slave by setting the appropriate MLTPH<2:0> bits in the BUFFCON register (Register 8-2).

When configured as a multiple output master, the GPA1 pin is set as the CLKPIN output function. The internal switching frequency clock is applied to this pin and is to be connected to the GPA1 pin of the slave units.

When configured as a multiple output slave, the GPA1 pin is set as the CLKPIN input function. The switching frequency clock of the master device is connected to this pin. Phase shift can be applied by appropriately setting the PWMPHL register of the slave device. Refer to **Section 26.1 “Standard Pulse-Width Modulation (PWM) Mode”**.

Note 1:	The ALT_CLKPIN can also be used by setting the APFCON<CLKSEL> bit. This function is only available in the MCP19111.

3.10.8 SYSTEM BENCH TESTING

The MCP19110/11 is a highly integrated controller. To facilitate system prototyping, various internal signals can be measured by configuring the MCP19110/11 in bench test mode. To accomplish this, the ATSTCON<BNCHEN> bit is set. This configures GPA0 as the ANALOG_TEST feature. The signals measured on GPA0 are controlled by the ASEL<4:0> bits of the BUFFCON register. See **Section 8.0 “System Bench Testing”** for more information.

Note 1:	The factory-set calibration words are write-protected even when the MCP19110/11 is placed in a Bench Test mode.

4.0 ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS (†)

$V_{IN} – V_{GND}$	-0.3V to +32V
$V_{BOOT} - V_{PHASE}$	-0.3V to +6.5V
V_{PHASE} (continuous)	GND – 0.3V to +38V
V_{PHASE} (transient < 100 ns)	GND – 5.0V to +38V
V_{DD} internally generated	+5V ±20%
V_{HDRV}, HDRV Pin	$+V_{PHASE}$ – 0.3V to V_{BOOT} + 0.3V
V_{LDRV}, LDRV Pin	$+(V_{GND}$ – 0.3V) to (V_{DD} + 0.3V)
Voltage on $\overline{\text{MCLR}}$ with respect to GND	-0.3V to +13.5V
Maximum Voltage: any other pin	$+(V_{GND}$ – 0.3V) to (V_{DD} + 0.3V)
Maximum output current sunk by any single I/O pin	25 mA
Maximum output current sourced by any single I/O pin	25 mA
Maximum current sunk by all GPIO	65 mA
Maximum current sourced by all GPIO	65 mA
ESD protection on all pins (HBM)	1.0 kV
ESD protection on all pins (MM)	100V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

4.2 Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, V_{REF} = 1.2V, F_{SW} = 300 kHz, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +125°C.						
Input						
Input Voltage	V_{IN}	**4.5**	—	**32**	V	
Input Quiescent Current	I_Q	—	5	**10**	mA	Not switching
Shutdown Current	I_{SHDN}	—	1.8	**2.2**	mA	Note 4
Adjustable Input Under-voltage Lockout Range	UVLO	**3**	—	**32**	V	VINLVL is a LOG DAC
Input Undervoltage Lock-out Hysteresis	$UVLO_{HYS}$	**—**	13	**—**	%	Hysteresis applied to adjustable UVLO setpoint
Overcurrent						
Overcurrent Minimum Threshold	OC_{MIN}	—	160	—	mV	
Overcurrent Maximum Threshold	OC_{MAX}	—	620	—	mV	
Overcurrent Mid-Scale Threshold	OC_{MID}	**240**	400	**550**	mV	
Overcurrent Step Size	OC_{STEP_SIZE}	**10**	15	**20**	mV	
Adjustable OC Leading Edge Blanking Minimum Set Point	LEB_{min}	—	114	—	ns	
Adjustable OC Leading Edge Blanking Maximum Set Point	LEB_{max}	—	780	—	ns	
Current Sense						
Current Sense Minimum AC Gain	I_{AC_GAIN}	—	0	—	dB	
Current Sense Maximum AC Gain	I_{AC_GAIN}	—	22.8	—	dB	
Current Sense AC Gain Mid-Set Point	I_{AC_GAIN}	8.5	11.5	14	dB	
Current Sense AC Gain Step Size	$I_{AC\_GAIN\_STEP}$	—	1.5	—	dB	
Current Sense AC Gain Offset Voltage	I_{AC_OFFSET}	-175	9	135	mV	
Current Sense Minimum DC Gain	I_{DC_GAIN}	—	19.5	—	dB	
Current Sense Maximum DC Gain	I_{DC_GAIN}	—	35.7	—	dB	
Current Sense DC Gain Mid-Set Point	I_{DC_GAIN}	27	28.6	30.3	dB	
Current Sense DC Gain Step Size	$I_{DC\_GAIN\_STEP}$	—	2.3	—	dB	

Note 1: Ensured by design. Not production tested.

2: $V_{DD\text{-}OUT}$ is the voltage present at the V_{DD} pin. V_{DD} is the internally generated bias voltage.

3: This is the total source current for all GPIO pins combined. Individually, each pin can source a maximum of 25 mA.

4: PE1 = 0x00h, ABECON = 0x00h, ATSTCON = 0x80h, WPUGPA = 0x00h, WPUGPB = 0x00h, and SLEEP command issued to PIC core, see SECTION 16.0.

4.2 Electrical Characteristics (Continued)

Electrical Specifications: Unless otherwise noted, V_{IN} = 12V, V_{REF} = 1.2V, F_{SW} = 300 kHz, T_A = +25°C. **Boldface** specifications apply over the T_A range of -40°C to +125°C.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Current Sense DC Gain Offset Voltage	I_{DC_OFFSET}	1.4	1.56	1.7	V	
Voltage for Zero Current	VZC	—	1.45	—	V	VZCCON = 0x80h
Voltage Reference						
Adjustable V_{OUT} Range	V_{OUT_RANGE}	**0.5**	—	**3.6**	V	V_{OUT} range with no external voltage divider
V_{OUT} Coarse Resolution	V_{OUT_COARSE}	**10.8**	15.8	**25.8**	mV	
V_{OUT} Coarse Mid Set Point	$V_{OUT\_COARSE\_MID}$	**1.85**	2.04	**2.25**	V	
V_{OUT} Fine Resolution	V_{OUT_FINE}	—	0.8	**1**	mV	
Output Overvoltage						
Adjustable Overvoltage Range	OV_{RANGE}	**0**	—	**4.5**	V	
Adjustable Overvoltage Mid-Set Point	OV_{MID}	**1.8**	2	**2.3**	V	
Adjustable Overvoltage Resolution	OV_R	**—**	15	**—**	mV	
Output Undervoltage						
Adjustable Undervoltage Range	UV_{RANGE}	**0**	—	**4.5**		
Adjustable Undervoltage Mid-Set Point	UV_{MID}	**1.8**	2	**2.3**	V	
Adjustable Undervoltage Resolution	UV_R	**—**	15	**—**	mV	
Remote Sense Differential Amplifier						
Closed Loop Voltage Gain	A_{VOL}	**0.95**	1	**1.05**	V/V	
Common Mode Range	V_{CMR}	**GND – 0.3**	—	**V_{DD} + 1.0**	V	Note 1
Common Mode Reject Ratio	CMRR	**—**	57	—	dB	
Differential Amplifier Offset	V_{OS}	—	40	—	mV	See **Section 9.5 "Calibration Word 5"** and **Section 9.6 "Calibration Word 6"**
Compensation						
Minimum Zero Frequency	F_{ZERO_MIN}	—	350	—	Hz	
Maximum Zero Frequency	F_{ZERO_MAX}	—	35000	—	Hz	
Minimum Error Amplifier Gain	G_{EA_MIN}	—	0	—	dB	
Maximum Error Amplifier Gain	G_{EA_MAX}	—	36.15	—	dB	

Note 1: Ensured by design. Not production tested.

2: $V_{DD\text{-}OUT}$ is the voltage present at the V_{DD} pin. V_{DD} is the internally generated bias voltage.

3: This is the total source current for all GPIO pins combined. Individually, each pin can source a maximum of 25 mA.

4: PE1 = 0x00h, ABECON = 0x00h, ATSTCON = 0x80h, WPUGPA = 0x00h, WPUGPB = 0x00h, and SLEEP command issued to PIC core, see SECTION 16.0.