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ADM1026

Complete Thermal System Management Controller

The ADM1026 is a complete system hardware monitor for microprocessor-based systems, providing measurement and limit comparison of various system parameters. The ADM1026 has up to 19 analog measurement channels. Fifteen analog voltage inputs are provided, five of which are dedicated to monitoring +3.3 V, +5.0 V, and ±12 V power supplies, and the processor core voltage. The ADM1026 can monitor two other power supply voltages by measuring its own V_{CC} and the main system supply. One input (two pins) is dedicated to a remote temperature-sensing diode. Two additional pins can be configured as general-purpose analog inputs to measure 0 V to 2.5 V, or as a second temperature sensing input. The eight remaining inputs are general-purpose analog inputs with a range of 0 V to 2.5 V or 0 V to 3.0 V. The ADM1026 also has an on-chip temperature sensor.

The ADM1026 has eight pins that can be configured for fan speed measurement or as general-purpose logic I/O pins. Another eight pins are dedicated to general-purpose logic I/O. An additional pin can be configured as a general-purpose I/O or as the bidirectional $\overline{\text{THERM}}$ pin.

Measured values can be read out via a 2-wire serial system management bus, and values for limit comparisons can be programmed over the same serial bus. The high speed, successive approximation ADC allows frequent sampling of all analog channels to ensure a fast interrupt response to any out-of-limit measurement.

Features

- Up to 19 Analog Measurement Channels (Including Internal Measurements)
- Up to 8 Fan Speed Measurement Channels
- Up to 17 General-Purpose Logic I/O Pins
- Remote Temperature Measurement with Remote Diode (Two Channels)
- On-Chip Temperature Sensor
- Analog and PWM Fan Speed Control Outputs
- 2-Wire Serial System Management Bus (SMBus)
- 8 kB On-Chip EEPROM
- Full SMBus 1.1 Support Includes Packet Error Checking (PEC)
- Chassis Intrusion Detection
- Interrupt Output (SMBAlert)
- Reset Input, Reset Outputs
- Thermal Interrupt ($\overline{\text{THERM}}$) Output
- Limit Comparison of All Monitored Values
- This is a Pb-Free Device*

Applications

- Network Servers and Personal Computers
- Telecommunications Equipment
- Test Equipment and Measuring Instruments

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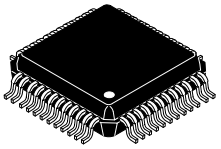
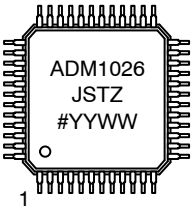


LQFP−48
CASE 932

MARKING DIAGRAM



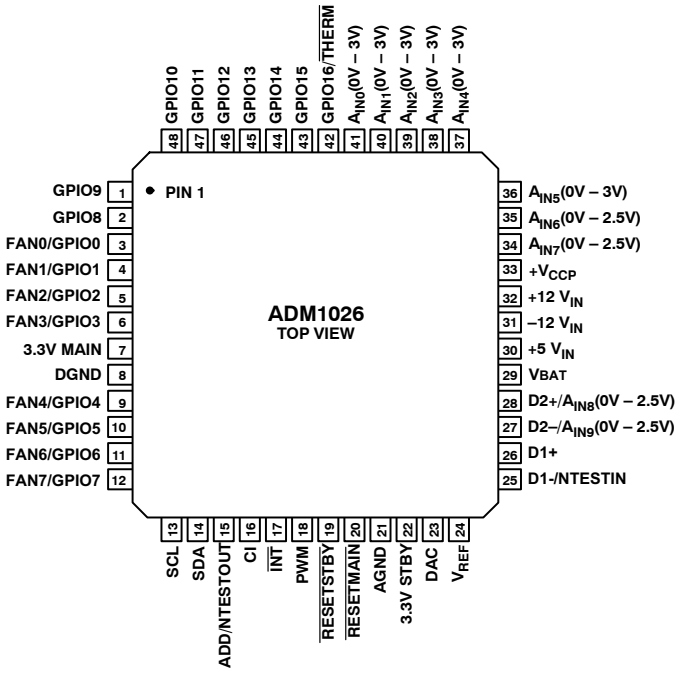
ADM1026JSTZ = Special Device Code
# = Pb-Free Package
YYWW = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 54 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PIN ASSIGNMENT



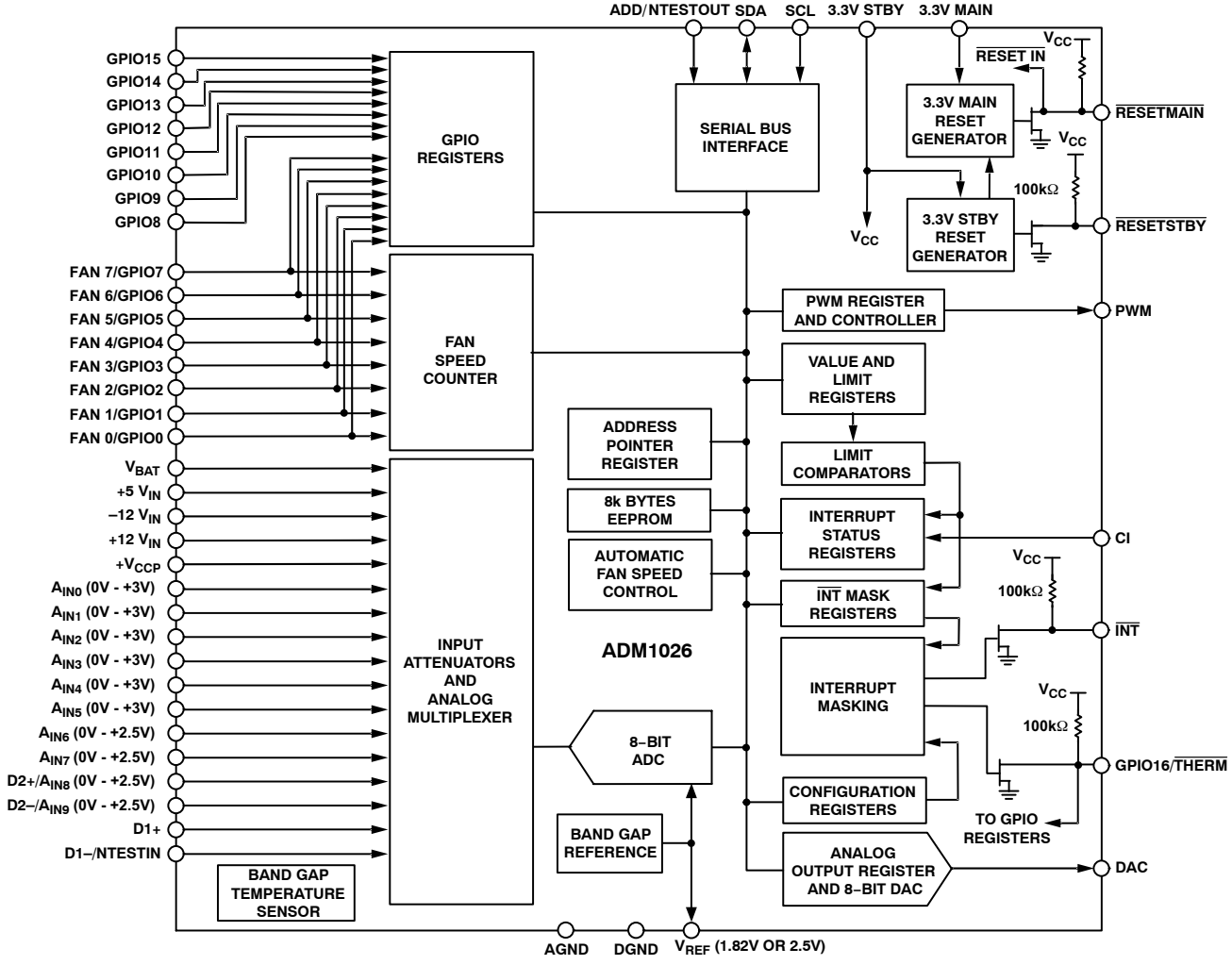


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{CC})	6.5	V
Voltage on +12 V_{IN} Pin	+20	V
Voltage on −12 V_{IN} Pin	−20	V
Voltage on Analog Pins	−0.3 to (V_{CC} + 0.3)	V
Voltage on Open-drain Digital Pins	−0.3 to +6.5	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature (T_{JMAX})	150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature, Soldering Vapor Phase (60 sec) Infrared (15 sec)	 215 200	°C
ESD Rating −12 V_{IN} Pin All Other Pins	 1000 2000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

Table 2. THERMAL CHARACTERISTICS

Package Type	θ_{JA}	θ_{JC}	Unit
48-lead LQFP	50	10	°C/W

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Type	Description
1	GPIO9	Digital I/O†	General-purpose I/O pin that can be configured as digital inputs or outputs.
2	GPIO8	Digital I/O†	General-purpose I/O pin that can be configured as digital inputs or outputs.
3	FAN0/GPIO0	Digital I/O	Fan tachometer input with internal 10 kΩ pullup resistor to 3.3 V STBY. Can be reconfigured as a general-purpose, open drain, digital I/O pin.
4	FAN1/GPIO1	Digital I/O	Fan tachometer input with internal 10 kΩ pullup resistor to 3.3 V STBY. Can be reconfigured as a general-purpose, open drain, digital I/O pin.
5	FAN2/GPIO2	Digital I/O	Fan tachometer input with internal 10 kΩ pullup resistor to 3.3 V STBY. Can be reconfigured as a general-purpose, open drain, digital I/O pin.
6	FAN3/GPIO3	Digital I/O	Fan tachometer input with internal 10 kΩ pullup resistor to 3.3 V STBY. Can be reconfigured as a general-purpose, open drain, digital I/O pin.
7	3.3 V MAIN	Analog Input	Monitors the main 3.3 V system supply. Does not power the device.
8	DGND	Ground	Ground pin for digital circuits.
9	FAN4/GPIO4	Digital I/O	Fan tachometer input with internal 10 kΩ pullup resistor to 3.3 V STBY. Can be reconfigured as a general-purpose, open drain, digital I/O pin.
10	FAN5/GPIO5	Digital I/O	Fan tachometer input with internal 10 kΩ pullup resistor to 3.3 V STBY. Can be reconfigured as a general-purpose, open drain, digital I/O pin.
11	FAN6/GPIO6	Digital I/O	Fan tachometer input with internal 10 kΩ pullup resistor to 3.3 V STBY. Can be reconfigured as a general-purpose, open drain, digital I/O pin.
12	FAN7/GPIO7	Digital I/O	Fan tachometer input with internal 10 kΩ pullup resistor to 3.3 V STBY. Can be reconfigured as a general-purpose, open drain, digital I/O pin.
13	SCL	Digital Input	Open Drain Serial Bus Clock. Requires a 2.2 kΩ pullup resistor.
14	SDA	Digital I/O	Serial Bus Data. Open drain I/O. Requires a 2.2 kΩ pullup resistor.
15	ADD/NTESTOUT	Digital Input	This is a three-state input that controls the two LSBs of the serial bus address. It also functions as the output for NAND tree testing.
16	CI	Digital Input	An active high input that captures a chassis intrusion event in Bit 6 of Status Register 4. This bit remains set until cleared, as long as battery voltage is applied to the V_{BAT} input, even when the ADM1026 is powered off.

Table 3. PIN ASSIGNMENT

Pin No.	Mnemonic	Type	Description
17	$\overline{\text{INT}}$	Digital Output	Interrupt Request (Open Drain). The output is enabled when Bit 1 of the configuration register is set to 1. The default state is disabled. It has an on-chip 100 kΩ pullup resistor.
18	PWM	Digital Output	Open drain pulse width modulated output for control of the fan speed. This pin defaults to high for the 100% duty cycle for use with NMOS drive circuitry. If a PMOS device is used to drive the fan, the PWM output may be inverted by setting Bit 1 of Test Register 1 = 1.
19	$\overline{\text{RESETSTBY}}$	Digital Output	Power-on Reset. 5 mA driver (weak 100 kΩ pullup), active low output (100 kΩ pullup) with a 180 ms typical pulse width. $\overline{\text{RESETSTBY}}$ is asserted whenever 3.3 V STBY is below the reset threshold. It remains asserted for approximately 180 ms after 3.3 V STBY rises above the reset threshold.
20	$\overline{\text{RESETMAIN}}$	Digital I/O	Power-on Reset. 5 mA driver (weak 100 kΩ pullup), active low output (100 kΩ pullup) with a 180 ms typical pulse width. $\overline{\text{RESETMAIN}}$ is asserted whenever 3.3 V MAIN is below the reset threshold. It remains asserted for approximately 180 ms after 3.3 V MAIN rises above the reset threshold. If, however, 3.3 V STBY rises with or before 3.3 V MAIN, then $\overline{\text{RESETMAIN}}$ remains asserted for 180 ms after $\overline{\text{RESETSTBY}}$ is deasserted. Pin 20 also functions as an active low RESET input.
21	AGND	Ground	Ground pin for analog circuits.
22	3.3 V STBY	Power Supply	Supplies 3.3 V power. Also monitors the 3.3 V standby power rail.
23	DAC	Analog Output	0 V to 2.5 V output for analog control of the fan speed.
24	V_{REF}	Analog Output	Reference Voltage Output. Can be selected as 1.8 V (default) or 2.5 V.
25	D1−/NTESTIN	Analog Input	Connected to a cathode of the first remote temperature sensing diode. If it is held high at power-on, it activates the NAND tree test mode.
26	D1+	Analog Input	Connected to the anode of the first remote temperature sensing diode.
27	D2−/A_{IN9}	Programmable	Connected to the cathode of the second remote temperature sensing diode or the analog input may be reconfigured as a 0 V − 2.5 V analog input.
28	D2+/A_{IN8}	Programmable	Connected to the anode of the second remote temperature sensing diode, or the analog input may be reconfigured as a 0 V − 2.5 V analog input.
29	V_{BAT}	Analog Input	Monitors battery voltage, nominally +3.0 V.
30	+5.0 V_{IN}	Analog Input	Monitors the +5.0 V supply.
31	−12 V_{IN}	Analog Input	Monitors the −12 V supply.
32	+12 V_{IN}	Analog Input	Monitors the +12 V supply.
33	$+V_{CCP}$	Analog Input	Monitors the processor core voltage (0 V to 3.0 V).
34	A_{IN7}	Analog Input	General-purpose 0 V to 2.5 V analog inputs.
35	A_{IN6}	Analog Input	General-purpose 0 V to 2.5 V analog inputs.
36	A_{IN5}	Analog Input	General-purpose 0 V to 3.0 V analog inputs.
37	A_{IN4}	Analog Input	General-purpose 0 V to 3.0 V analog inputs.
38	A_{IN3}	Analog Input	General-purpose 0 V to 3.0 V analog inputs.
39	A_{IN2}	Analog Input	General-purpose 0 V to 3.0 V analog inputs.
40	A_{IN1}	Analog Input	General-purpose 0 V to 3.0 V analog inputs.
41	A_{IN0}	Analog Input	General-purpose 0 V to 3.0 V analog inputs.
42	GPIO16/$\overline{\text{THERM}}$	Digital I/O†	General-purpose I/O pin that can be configured as a digital input or output. Can also be configured as a bidirectional $\overline{\text{THERM}}$ pin (100 kΩ pullup).
43	GPIO15	Digital I/O†	General-purpose I/O pin that can be configured as a digital input or output.
44	GPIO14	Digital I/O†	General-purpose I/O pin that can be configured as a digital input or output.
45	GPIO13	Digital I/O†	General-purpose I/O pin that can be configured as a digital input or output.
46	GPIO12	Digital I/O†	General-purpose I/O pin that can be configured as a digital input or output.
47	GPIO11	Digital I/O†	General-purpose I/O pin that can be configured as a digital input or output.
48	GPIO10	Digital I/O†	General-purpose I/O pin that can be configured as a digital input or output.

†GPIO pins are open drain and require external pullup resistors. Fan inputs have integrated 10 kΩ pullups, but these pins become open drain when reconfigured as GPIOs.

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted. (Note 1, 2, and 3))

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Voltage, 3.3 V STBY		3.0	3.3	5.5	V
Supply Current, I_{CC}	Interface Inactive, ADC Active	–	2.5	4.0	mA
TEMPERATURE-TO-DIGITAL CONVERTER					
Internal Sensor Accuracy		–	–	±3.0	°C
Resolution		–	±1.0	–	°C
External Diode Sensor Accuracy	0°C < T_D < 100°C	–	–	±3.0	°C
Resolution		–	±1.0	–	°C
Remote Sensor Source Current	High Level Low Level	– –	90 5.5	– –	μA
ANALOG-TO-DIGITAL CONVERTER (Including MUX and ATTENUATORS)					
Total Unadjusted Error (TUE) (Note 4)		–	–	±2.0	%
Differential Non-linearity (DNL)		–	–	±1.0	LSB
Power Supply Sensitivity		–	±0.1		%/V
Conversion Time (Analog Input or Internal Temperature) (Note 5)		–	11.38	12.06	ms
Conversion Time (External Temperature) (Note 5)		–	34.13	36.18	ms
Input Resistance (+5.0 V_{IN}, V_{CCP}, $A_{IN0} – A_{IN5}$)		80	100	120	kΩ
Input Resistance of +12 V_{IN} pin		70	100	115	kΩ
Input Resistance of –12 V_{IN} pin		8.0	10	12	kΩ
Input Resistance ($A_{IN6} – A_{IN9}$)		5.0	–	–	MΩ
Input Resistance of V_{BAT} pin (Note 4)		80	100	120	kΩ
V_{BAT} Current Drain (when measured)	CR2032 Battery Life >10 Years	–	80	100	nA
V_{BAT} Current Drain (when not measured)		–	6.0	–	nA
ANALOG OUTPUT (DAC)					
Output Voltage Range		0	–2.5	–	V
Total Unadjusted Error (TUE)	I_L = 2 mA	–	–	±5.0	%
Zero Error	No Load	–	1.0	–	LSB
Differential Non-linearity (DNL)	Monotonic by Design	–	–	±1.0	LSB
Integral Non-linearity		–	±0.5	–	LSB
Output Source Current		–	2.0	–	mA
Output Sink Current		–	1.0	–	mA
REFERENCE OUTPUT					
Output Voltage	Bit 2 of Register 07h = 0 Bit 2 of Register 07h = 1	1.8 2.47	1.82 2.50	1.84 2.53	V
Load Regulation (I_{SINK} = 2 mA)		–	0.15	–	%
Load Regulation (I_{SOURCE} = 2 mA)		–	0.15	–	%
Short Circuit Current	V_{CC} = 3.3 V	–	25	–	mA
Output Current Source		–	2.0	–	mA
Output Current Sink		–	2.0	–	mA

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted. (Note 1, 2, and 3))

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
FAN RPM-TO-DIGITAL CONVERTER (Note 6)					
Accuracy		–	–	±12	%
Full-scale Count		–	–	255	
FAN0 to FAN7 Nominal Input RPM (Note 5)	Divisor = 1, fan count = 153 Divisor = 2, fan count = 153 Divisor = 4, fan count = 153 Divisor = 8, fan count = 153	– – – –	8800 4400 2200 1100	– – – –	RPM
Internal Clock Frequency		20	22.5	25	kHz
OPEN DRAIN O/Ps, PWM, GPIO0 to 16					
Output High Voltage, V_{OH}	I_{OUT} = 3.0 mA, V_{CC} = 3.3 V	2.4	–	–	V
High Level Output Leakage Current, I_{OH}	$V_{OUT} = V_{CC}$	–	0.1	1.0	μA
Output Low Voltage, V_{OL}	I_{OUT} = –3.0 mA, V_{CC} = 3.3 V	–	–	0.4	V
PWM Output Frequency		–	75	–	Hz
DIGITAL OUTPUTS ($\overline{\text{INT}}$, $\overline{\text{RESETMAIN}}$, $\overline{\text{RESETSTBY}}$)					
Output Low Voltage, V_{OL}	I_{OUT} = –3.0 mA, V_{CC} = 3.3 V	–	–	0.4	V
$\overline{\text{RESET}}$ Pulse Width		140	180	240	ms
OPEN DRAIN SERIAL DATABUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = –3.0 mA, V_{CC} = 3.3 V	–	–	0.4	V
High Level Output Leakage Current, I_{OH}	$V_{OUT} = V_{CC}$	–	0.1	1.0	μA
SERIAL BUS DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}		2.2	–	–	V
Input Low Voltage, V_{IL}		–	–	0.8	V
Hysteresis		–	500	–	mV
DIGITAL INPUT LOGIC LEVELS (ADD, CI, FAN 0 to 7, GPIO 0 to 16) (Note 7 and 8)					
Input High Voltage, V_{IH}	V_{CC} = 3.3 V	2.4	–	–	V
Input Low Voltage, V_{IL}	V_{CC} = 3.3 V	0.8	–	–	V
Hysteresis (Fan 0 to 7)	V_{CC} = 3.3 V	–	250	–	mV
$\overline{\text{RESETMAIN}}$, $\overline{\text{RESETSTBY}}$					
$\overline{\text{RESETMAIN}}$ Threshold	Falling Voltage	2.89	2.94	2.97	V
$\overline{\text{RESETSTBY}}$ Threshold	Falling Voltage	3.01	3.05	3.10	V
$\overline{\text{RESETMAIN}}$ Hysteresis		–	60	–	mV
$\overline{\text{RESETSTBY}}$ Hysteresis		–	70	–	mV
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	$V_{IN} = V_{CC}$	–1.0	–	–	μA
Input Low Current, I_{IL}	V_{IN} = 0	–	–	1.0	μA
Input Capacitance, C_{IN}		–	20	–	pF
EEPROM RELIABILITY					
Endurance (Note 9)		100	700	–	kcycles
Data Retention (Note 10)		10	–	–	Years
SERIAL BUS TIMING					
Clock Frequency, f_{SCLK}	See Figure 2 for All Parameters.	–	–	400	kHz
Glitch Immunity, t_{SW}		–	–	50	ns
Bus Free Time, t_{BUF}		4.7	–	–	μs
Start Setup Time, $t_{SU;\,STA}$		4.7	–	–	μs

Table 4. ELECTRICAL CHARACTERISTICS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted. (Note 1, 2, and 3))

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL BUS TIMING					
Start Hold Time, $t_{HD; STA}$		4.0	–	–	μs
SCL Low Time, t_{LOW}		4.7	–	–	μs
SCL High Time, t_{HIGH}		4.0	–	–	μs
SCL, SDA Rise Time, t_r		–	–	1000	ns
SCL, SDA Fall Time, t_f		–	–	300	ns
Data Setup Time, $t_{SU; DAT}$		250	–	–	ns
Data Hold Time, $t_{HD; DAT}$		300	–	–	ns

1. All voltages are measured with respect to GND, unless otherwise specified.
2. Typicals are at T_A = 25°C and represent the most likely parametric norm. Shutdown current typ is measured with V_{CC} = 3.3 V.
3. Timing specifications are tested at logic levels of V_{IL} = 0.8 V for a falling edge and V_{IH} = 2.1 V for a rising edge.
4. Total unadjusted error (TUE) includes offset, gain, and linearity errors of the ADC, multiplexer, and on-chip input attenuators. V_{BAT} is accurate only for V_{BAT} voltages greater than 1.5 V (see Figure 14).
5. Total analog monitoring cycle time is nominally 273 ms, made up of 18 ms × 11.38 ms measurements on analog input and internal temperature channels, and 2 ms × 34.13 ms measurements on external temperature channels.
6. The total fan count is based on two pulses per revolution of the fan tachometer output. The total fan monitoring time depends on the number of fans connected and the fan speed. See the Fan Speed Measurement section for more details.
7. ADD is a three-state input that may be pulled high, low, or left open circuit.
8. Logic inputs accept input high voltages up to 5.0 V even when device is operating at supply voltages below 5.0 V.
9. Endurance is qualified to 100,000 cycles as per JEDEC Std. 22 method A117, and measured at −40°C, +25°C, and +85°C. Typical endurance at +25°C is 700,000 cycles.
10. Retention lifetime equivalent at junction temperature (T_J) = 55°C as per JEDEC Std. 22 method A117. Retention lifetime based on activation energy of 0.6 V derates with junction temperature as shown in Figure 15.

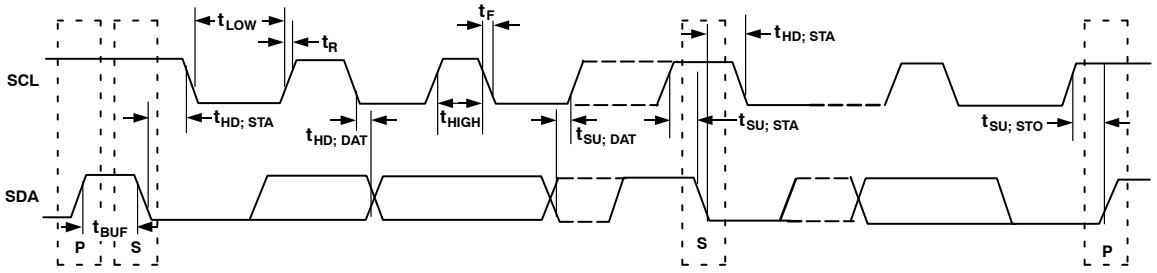


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

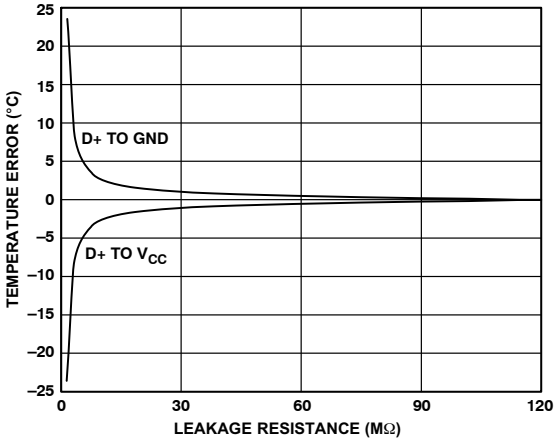


Figure 3. Temperature Error vs. PCB Track Resistance

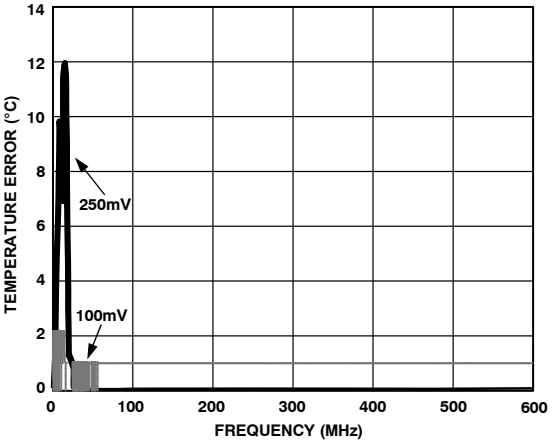


Figure 4. Temperature Error vs. Power Supply Noise Frequency

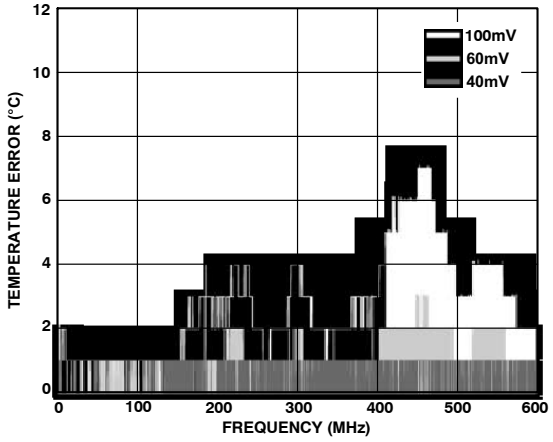


Figure 5. Temperature Error vs. Common-mode Noise Frequency

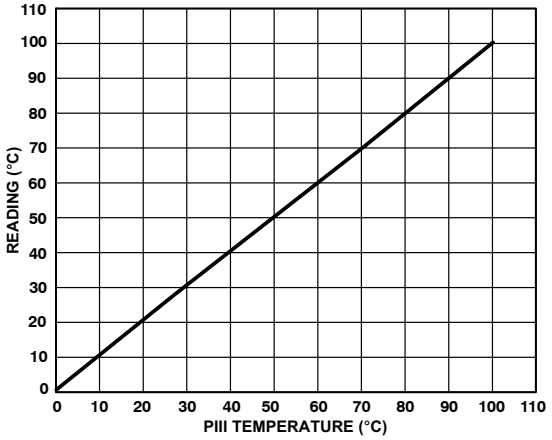


Figure 6. Pentium® III Temperature vs. ADM1026 Reading

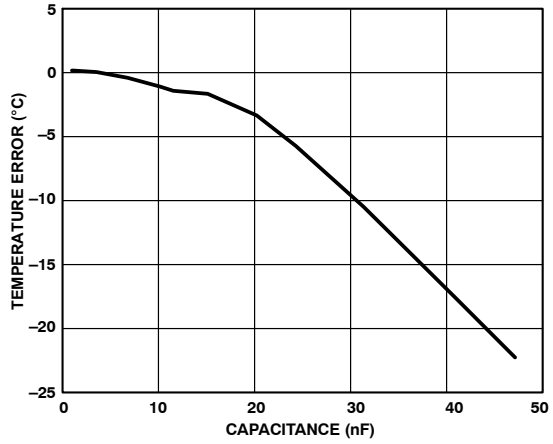


Figure 7. Temperature Error vs. Capacitance Between D+ and D–

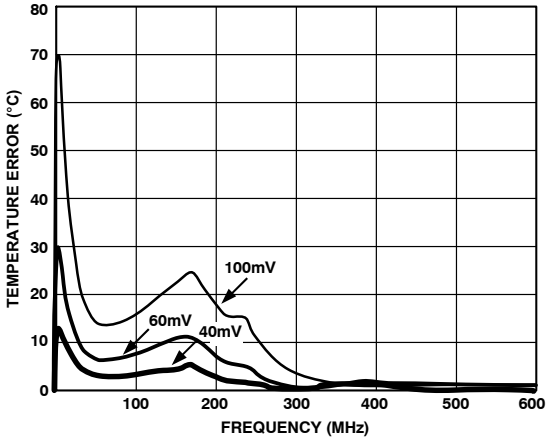


Figure 8. Temperature Error vs. Differential-mode Noise Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

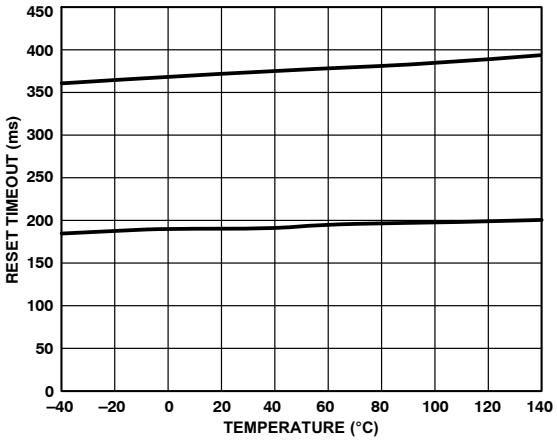


Figure 9. Powerup Reset Timeout vs. Temperature

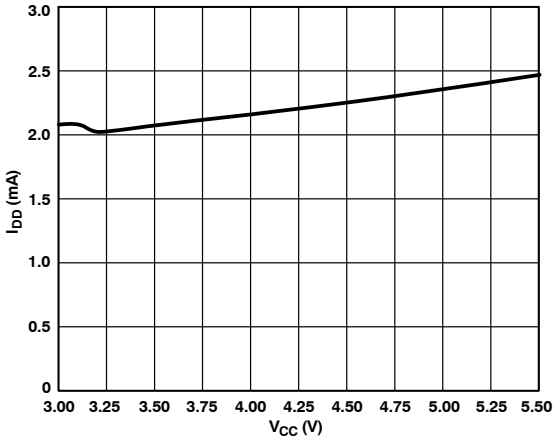


Figure 10. Supply Current vs. Supply Voltage

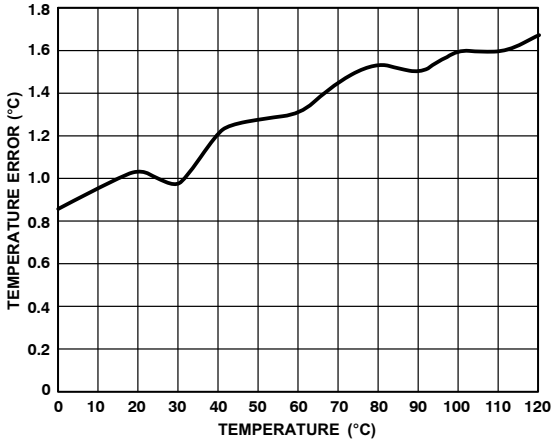


Figure 11. Local Sensor Temperature Error

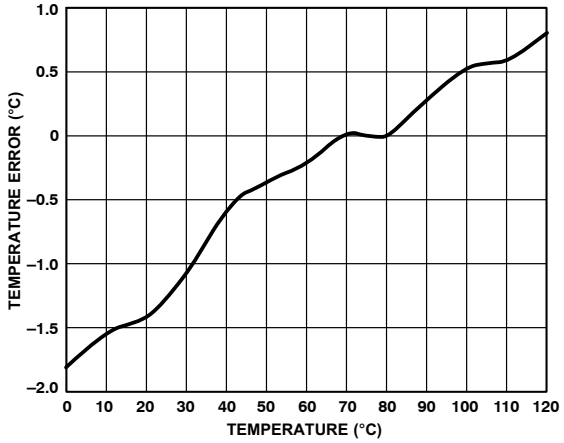


Figure 12. Remote Sensor Temperature Error

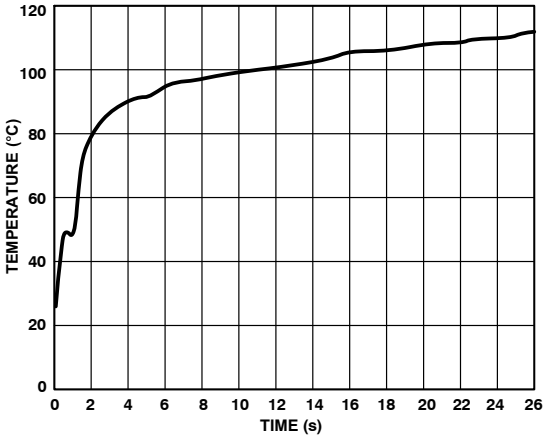


Figure 13. Response to Thermal Shock

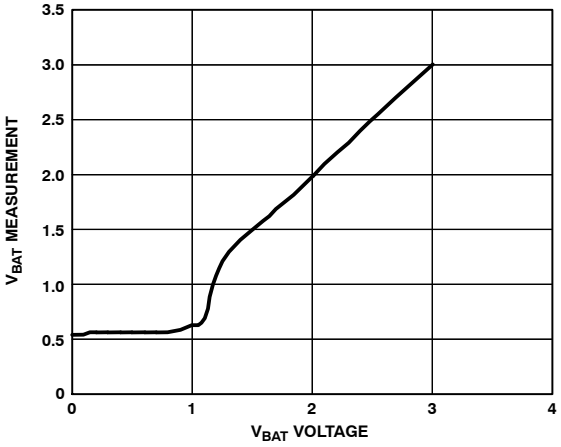


Figure 14. V_{BAT} Measurement vs. Voltage

Functional Description

The ADM1026 is a complete system hardware monitor for microprocessor-based systems. The device communicates with the system via a serial system management bus. The serial bus controller has a hardwired address line for device selection (ADD, Pin 15), a serial data line for reading and writing addresses and data (SDA, Pin 14), and an input line for the serial clock (SCL, Pin 13). All control and programming functions of the ADM1026 are performed over the serial bus.

Measurement Inputs

Programmability of the analog and digital measurement inputs makes the ADM1026 extremely flexible and versatile. The device has an 8-bit A/D converter, and 17 analog measurement input pins that can be configured in different ways.

Pins 25 and 26 are dedicated temperature inputs and may be connected to the cathode and anode of a remote temperature sensing diode.

Pins 27 and 28 may be configured as temperature inputs and connected to a second temperature-sensing diode, or may be reconfigured as analog inputs with a range of 0 V to 2.5 V.

Pins 29 to 33 are dedicated analog inputs with on-chip attenuators configured to monitor V_{BAT}, +5.0 V, −12 V, +12 V, and the processor core voltage V_{CCP}, respectively.

Pins 34 to 41 are general-purpose analog inputs with a range of 0 V to 2.5 V or 0 V to 3.0 V. These are mainly intended for monitoring SCSI termination voltages, but may be used for other purposes.

The ADC also accepts input from an on-chip band gap temperature sensor that monitors system ambient temperature.

In addition, the ADM1026 monitors the supply from which it is powered, 3.3 V STBY, so there is no need for a separate pin to monitor the power supply voltage.

The ADM1026 has eight pins that are general-purpose logic I/O pins (Pins 1, 2, and 43 to 48), a pin that can be configured as GPIO or as a bidirectional thermal interrupt ($\overline{\text{THERM}}$) pin (Pin 42), and eight pins that can be configured for fan speed measurement or as general-purpose logic pins (Pins 3 to 6 and Pins 9 to 12).

Sequential Measurement

When the ADM1026 monitoring sequence is started, it cycles sequentially through the measurement of analog inputs and the temperature sensor, while at the same time the fan speed inputs are independently monitored. Measured values from these inputs are stored in value registers. These can be read over the serial bus, or can be compared with programmed limits stored in the limit registers. The results of out-of-limit comparisons are stored in the interrupt status registers. An out-of-limit event generates an interrupt on the $\overline{\text{INT}}$ line (Pin 17).

Any or all of the interrupt status bits can be masked by appropriate programming of the interrupt mask registers.

Chassis Intrusion

A chassis intrusion input (Pin 16) is provided to detect unauthorized tampering with the equipment. This event is latched in a battery-backed register bit.

Resets

The ADM1026 has two power-on reset outputs, $\overline{\text{RESETMAIN}}$ and $\overline{\text{RESETSTBY}}$, that are asserted when 3.3 V MAIN or 3.3 V STBY fall below the reset threshold. These give a 180 ms reset pulse at powerup. $\overline{\text{RESETMAIN}}$ also functions as an active-low $\overline{\text{RESET}}$ input.

Fan Speed Control Outputs

The ADM1026 has two outputs intended to control fan speed, though they can also be used for other purposes. Pin 18 is an open drain, Pulse Width Modulated (PWM) output with a programmable duty cycle and an output frequency of 75 Hz. Pin 23 is connected to the output of an on-chip, 8-bit, digital-to-analog converter with an output range of 0 V to 2.5 V.

Either or both of these outputs may be used to implement a temperature-controlled fan by controlling the speed of a fan using the temperature measured by the on-chip temperature sensor or remote temperature sensors.

Internal Registers

Table 5 describes the principal registers of the ADM1026. For more detailed information, see Table 12 to Table 125.

Table 5. PRINCIPLE REGISTERS

Type	Description
Address Pointer	Contains the address that selects one of the other internal registers. When writing to the ADM1026, the first byte of data is always a register address, and is written to the address pointer register.
Configuration Registers	Provide control and configuration for various operating parameters.
Fan Divisor Registers	Contain counter prescaler values for fan speed measurement.
DAC/PWM Control Registers	Contain speed values for PWM and DAC fan drive outputs.
GPIO Configuration Registers	Configure the GPIO pins as input or output and for signal polarity.
Value and Limit Registers	Store the results of analog voltage inputs, temperature, and fan speed measurements, along with their limit values.
Status Registers	Store events from the various interrupt sources.
Mask Registers	Allow masking of individual interrupt sources.

EEPROM

The ADM1026 has 8 kB of non-volatile, electrically erasable, programmable read-only memory (EEPROM) from register Addresses 8000h to 9FFFh. This may be used for permanent storage of data that is not lost when the

ADM1026 is powered down, unlike the data in the volatile registers. Although referred to as read-only memory, the EEPROM can be written to (as well as read from) via the serial bus in exactly the same way as the other registers. The main differences between the EEPROM and other registers are:

- An EEPROM location must be blank before it can be written to. If it contains data, it must first be erased.
- Writing to EEPROM is slower than writing to RAM.
- Writing to the EEPROM should be restricted because its typical cycle life is 100,000 write operations, due to the usual EEPROM wear-out mechanisms.

The EEPROM in the ADM1026 has been qualified for two key EEPROM memory characteristics: memory cycling endurance and memory data retention.

Endurance qualifies the ability of the EEPROM to be cycled through many program, read, and erase cycles. In real terms, a single endurance cycle is composed of four independent, sequential events, as follows:

1. Initial page erase sequence
2. Read/verify sequence
3. Program sequence
4. Second read/verify sequence

In reliability qualification, every byte is cycled from 00h to FFh until a first fail is recorded, signifying the endurance limit of the EEPROM memory.

Retention quantifies the ability of the memory to retain its programmed data over time. The EEPROM in the ADM1026 has been qualified in accordance with the formal JEDEC Retention Lifetime Specification (A117) at a specific junction temperature (T_J = 55°C) to guarantee a minimum of 10 years retention time. As part of this qualification procedure, the EEPROM memory is cycled to its specified endurance limit described above before data retention is characterized. This means that the EEPROM memory is guaranteed to retain its data for its full specified retention lifetime every time the EEPROM is reprogrammed. Note that retention lifetime based on an activation energy of 0.6 V derates with T_J, as shown in Figure 15.

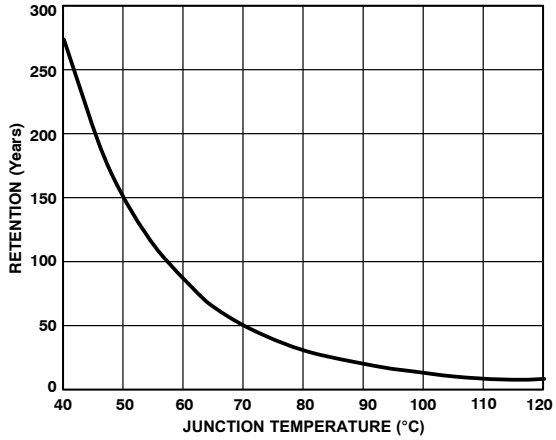


Figure 15. Typical EEPROM Memory Retention

Serial Bus Interface

Control of the ADM1026 is carried out via the serial system management bus (SMBus). The ADM1026 is connected to this bus as a slave device, under the control of a master device.

The ADM1026 has a 7-bit serial bus slave address. When the device is powered on, it does so with a default serial bus address. The 5 MSBs of the address are set to 01011, and the 2 LSBs are determined by the logical states of Pin 15 ADD/NTESTOUT. This pin is a three-state input that can be grounded, connected to V_{CC}, or left open-circuit to give three different addresses.

Table 6. ADDRESS PIN TRUTH TABLE

ADD Pin	A1	A0
GND	0	0
No Connect	1	0
V_{CC}	0	1

If ADD is left open-circuit, the default address is 0101110 (5Ch). ADD is sampled only at powerup on the first valid SMBus transaction, so any changes made while the power is on (and the address is locked) have no effect.

The facility to make hardwired changes to device addresses allows the user to avoid conflicts with other devices sharing the same serial bus, for example if more than one ADM1026 is used in a system.

General SMBus Timing

Figure 16 and Figure 17 show timing diagrams for general read and write operations using the SMBus. The SMBus specification defines specific conditions for different types of read and write operations, which are discussed later in this section. The general SMBus protocol* operates as follows:

1. The master initiates data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line (SDA) while the serial clock line SCL remains high. This indicates that a data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next 8 bits, consisting of a 7-bit slave address (MSB first) and an R/$\overline{W}$ bit, which determine the direction of the data transfer, that is, whether data is written to or read from the slave device (0 = write, 1 = read).
   The peripheral whose address corresponds to the trans-mitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is 0, the master writes to the slave device. If the R/$\overline{W}$ bit is 1, the master reads from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses, 8 bits of data followed by an acknowledge bit from the slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high may be interpreted as a stop signal.
   If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It may be an instruction telling the slave device to expect a block write, or it may simply be a register address that tells the slave where subsequent data is to be written.
   Because data can flow in only one direction as defined by the R/$\overline{W}$ bit, it is not possible to send a command to a slave device during a read operation. Before doing a read operation, it may first be necessary to do a write operation to tell the slave what type of read operation to expect and/or the address from which data is to be read.
3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device releases the SDA line during the low period before the ninth clock pulse, but the slave device does not pull it low (called No Acknowledge). The master takes the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a stop condition.

*If it is required to perform several read or write operations in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

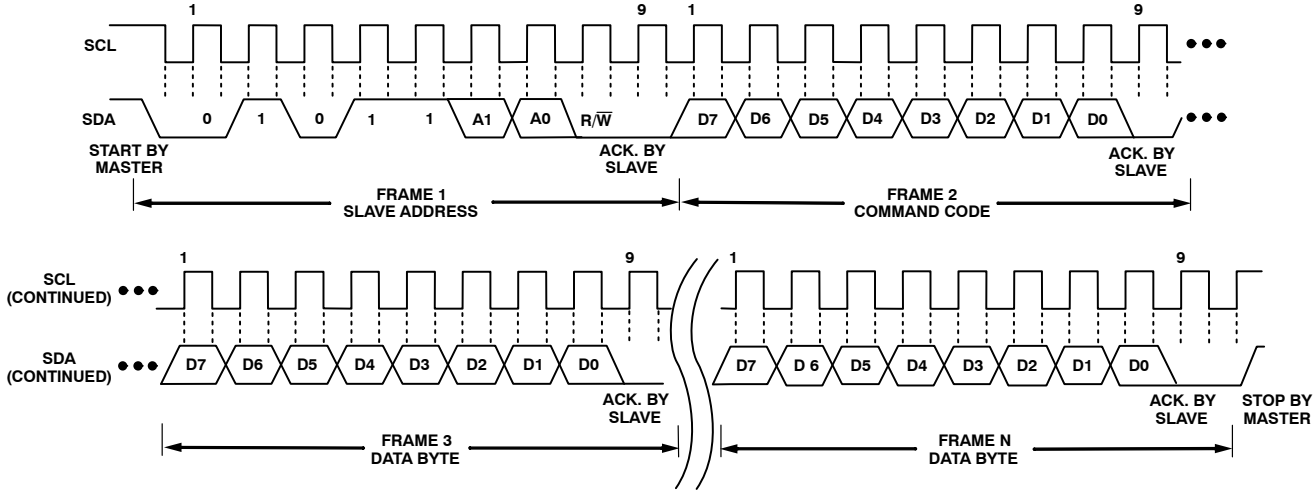


Figure 16. General SMBus Write Timing Diagram

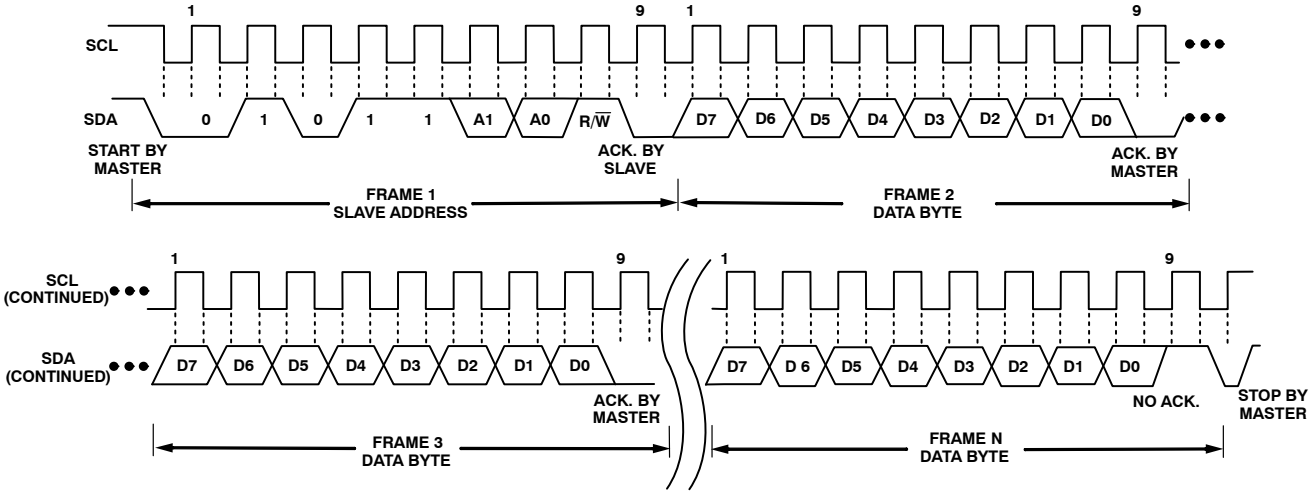


Figure 17. General SMBus Read Timing Diagram

SMBus Protocols for RAM and EEPROM

The ADM1026 contains volatile registers (RAM) and non-volatile EEPROM. RAM occupies Addresses 00h to 6Fh, while EEPROM occupies Addresses 8000h to 9FFFh.

Data can be written to and read from both RAM and EEPROM as single data bytes and as block (sequential) read or write operations of 32 data bytes, the maximum block size allowed by the SMBus specification.

Data can only be written to unprogrammed EEPROM locations. To write new data to a programmed location, it is first necessary to erase it. EEPROM erasure cannot be done at the byte level; the EEPROM is arranged as 128 pages of 64 bytes, and an entire page must be erased. Note that of these 128 pages, only 124 pages are available to the user. The last four pages are reserved for manufacturing purposes and cannot be erased/rewritten.

The EEPROM has three RAM registers associated with it, EEPROM Registers 1, 2, and 3 at Addresses 06h, 0Ch, and 13h. EEPROM Registers 1 and 2 are for factory use only. EEPROM Register 3 sets up the EEPROM operating mode. Setting Bit 0 of EEPROM Register 3 puts the EEPROM into read mode. Setting Bit 1 puts it into programming mode. Setting Bit 2 puts it into erase mode.

Only one of these bits must be set before the EEPROM may be accessed. Setting no bits or more than one of them causes the device to respond with No Acknowledge if an EEPROM read, program, or erase operation is attempted.

It is important to distinguish between SMBus write operations, such as sending an address or command, and EEPROM programming operations. It is possible to write an EEPROM address over the SMBus, whatever the state of EEPROM Register 3. However, EEPROM Register 3 must be correctly set before a subsequent EEPROM operation can be performed. For example, when reading from the EEPROM, Bit 0 of EEPROM Register 3 can be set, even though SMBus write operations are required to set up the EEPROM address for reading. Bit 3 of EEPROM Register 3 is used for EEPROM write protection. Setting this bit prevents accidental programming or erasure of the EEPROM. If an EEPROM write or erase operation is attempted when this bit is set, the ADM1026 responds with No Acknowledge. This bit is write-once and can only be cleared by a power-on reset.

EEPROM Register 3 Bit 7 is used for clock extend. Programming an EEPROM byte takes approximately 250 μs, which would limit the SMBus clock for repeated or block write operations. Because EEPROM block read/write access is slow, it is recommended that this clock extend bit typically be set to 1. This allows the ADM1026 to pull SCL low and extend the clock pulse when it cannot accept any more data.

ADM1026 SMBus Operations

The SMBus specifications define several protocols for different types of read and write operations. The ones used in the ADM1026 are discussed below. The following abbreviations are used in the diagrams:

S – START
W – WRITE
P – STOP
A – ACKNOWLEDGE
R –READ
$\overline{A}$ – NO ACKNOWLEDGE

ADM1026 Write Operations

Send Byte

In this operation, the master device sends a single command byte to a slave device, as follows:

1. The master device asserts a start condition on the SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an ACK on the SDA.
4. The master sends a command code.
5. The slave asserts ACK on the SDA.
6. The master asserts a stop condition on the SDA and the transaction ends.

In the ADM1026, the send byte protocol is used to write a register address to RAM for a subsequent single−byte read from the same address or block read or write starting at that address. This is illustrated in Figure 18.

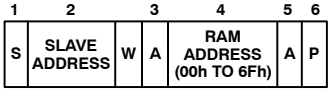


Figure 18. Setting a RAM Address for Subsequent Read

If it is required to read data from the RAM immediately after setting up the address, the master can assert a repeat start condition immediately after the final ACK and carry out a single byte read, block read, or block write operation without asserting an intermediate stop condition.

Write Byte/Word

In this operation, the master device sends a command byte and one or two data bytes to the slave device as follows:

1. The master device asserts a start condition on the SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an ACK on the SDA.
4. The master sends a command code.
5. The slave asserts an ACK on the SDA.
6. The master sends a data byte.
7. The slave asserts an ACK on the SDA.
8. The master sends a data byte (or may assert stop here.)
9. The slave asserts an ACK on the SDA.
10. The master asserts a stop condition on the SDA to end the transaction.

In the ADM1026, the write byte/word protocol is used for four purposes. The ADM1026 knows how to respond by the value of the command byte and EEPROM Register 3.

The first purpose is to write a single byte of data to RAM. In this case, the command byte is the RAM address from 00h to 6Fh and the (only) data byte is the actual data. This is illustrated in Figure 19.

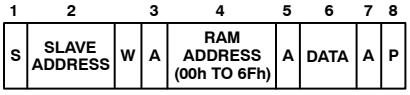


Figure 19. Single Byte Write to RAM

The protocol is also used to set up a 2-byte EEPROM address for a subsequent read or block read. In this case, the command byte is the high byte of the EEPROM address from 80h to 9Fh. The (only) data byte is the low byte of the EEPROM address. This is illustrated in Figure 20.

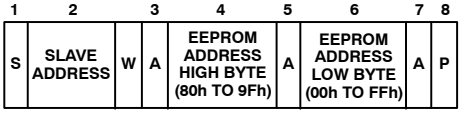


Figure 20. Setting an EEPROM Address

If it is required to read data from the EEPROM immediately after setting up the address, the master can assert a repeat start condition immediately after the final ACK and carry out a single-byte read or block read operation without asserting an intermediate stop condition. In this case, Bit 0 of EEPROM Register 3 should be set.

The third use is to erase a page of EEPROM memory. EEPROM memory can be written to only if it is previously erased. Before writing to one or more EEPROM memory locations that are already programmed, the page or pages containing those locations must first be erased. EEPROM memory is erased by writing an EEPROM page address plus an arbitrary byte of data with Bit 2 of EEPROM Register 3 set to 1.

Because the EEPROM consists of 128 pages of 64 bytes, the EEPROM page address consists of the EEPROM address high byte (from 80h to 9Fh) and the two MSBs of the low byte. The lower six bits of the EEPROM address (low byte only) specify addresses within a page and are ignored during an erase operation.

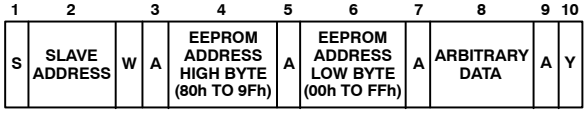


Figure 21. EEPROM Page Erasure

Page erasure takes approximately 20 ms. If the EEPROM is accessed before erasure is complete, the ADM1026 responds with No Acknowledge.

Last, this protocol is used to write a single byte of data to EEPROM. In this case, the command byte is the high byte of the EEPROM address from 80h to 9Fh. The first data byte is the low byte of the EEPROM address, and the second data byte is the actual data. Bit 1 of EEPROM Register 3 must be set. This is illustrated in Figure 22.

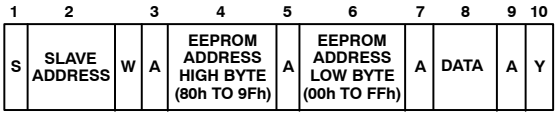


Figure 22. Single-Byte Write to EEPROM

Block Write

In this operation, the master device writes a block of data to a slave device. The start address for a block write must have been set previously. In the case of the ADM1026, this is done by a Send Byte operation to set a RAM address or by a write byte/word operation to set an EEPROM address.

1. The master device asserts a start condition on the SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an ACK on the SDA.
4. The master sends a command code that tells the slave device to expect a block write. The ADM1026 command code for a block write is A0h (10100000).
5. The slave asserts an ACK on the SDA.
6. The master sends a data byte (20h) that tells the slave device that 32 data bytes are being sent to it. The master should always send 32 data bytes to the ADM1026.
7. The slave asserts an ACK on the SDA.
8. The master sends 32 data bytes.
9. The slave asserts an ACK on the SDA after each data byte.
10. The master sends a packet error checking (PEC) byte.
11. The ADM1026 checks the PEC byte and issues an ACK if correct. If incorrect (NACK), the master resends the data bytes.
12. The master asserts a stop condition on the SDA to end the transaction.

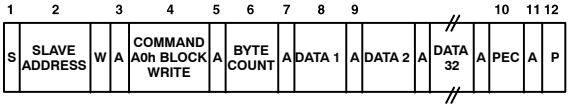


Figure 23. Block Write to EEPROM or RAM

When performing a block write to EEPROM, Bit 1 of EEPROM Register 3 must be set. Unlike some EEPROM devices that limit block writes to within a page boundary, there is no limitation on the start address when performing a block write to EEPROM, except:

- There must be at least 32 locations from the start address to the highest EEPROM address (9FF) to avoid writing to invalid addresses.
- If the addresses cross a page boundary, both pages must be erased before programming.

ADM1026 Read Operations

The ADM1026 uses the SMBus read protocols described here.

Receive Byte

In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on the SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an ACK on the SDA.
4. The master receives a data byte.
5. The master asserts a NO ACK on the SDA.
6. The master asserts a stop condition on the SDA to end the transaction.

In the ADM1026, the receive byte protocol is used to read a single byte of data from a RAM or EEPROM location whose address has previously been set by a send byte or write byte/word operation. Figure 24 shows this. When reading from EEPROM, Bit 0 of EEPROM Register 3 must be set.

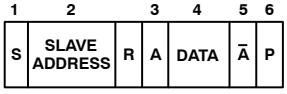


Figure 24. Single-Byte Read from EEPROM or RAM

Block Read

In this operation, the master device reads a block of data from a slave device. The start address for a block read must have been set previously. In the case of the ADM1026 this is done by a send byte operation to set a RAM address, or by a write byte/word operation to set an EEPROM address. The block read operation consists of a send byte operation that sends a block read command to the slave, immediately followed by a repeated start and a read operation that reads out multiple data bytes as follows:

1. The master device asserts a start condition on the SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an ACK on the SDA.
4. The master sends a command code that tells the slave device to expect a block read. The ADM1026 command code for a block read is A 1h (10100001).
5. The slave asserts an ACK on the SDA.
6. The master asserts a repeat start condition on the SDA.
7. The master sends the 7-bit slave address followed by the read bit (high).
8. The slave asserts an ACK on the SDA.
9. The ADM1026 sends a byte count data byte that tells the master how many data bytes to expect. The ADM1026 always returns 32 data bytes (20h), the maximum allowed by the SMBus 1.1 specification.
10. The master asserts an ACK on the SDA.
11. The master receives 32 data bytes.
12. The master asserts an ACK on the SDA after each data byte.
13. The ADM1026 issues a PEC byte to the master. The master should check the PEC byte and issue another block read if the PEC byte is incorrect.
14. A NACK is generated after the PEC byte to signal the end of the read.
15. The master asserts a stop condition on the SDA to end the transaction.

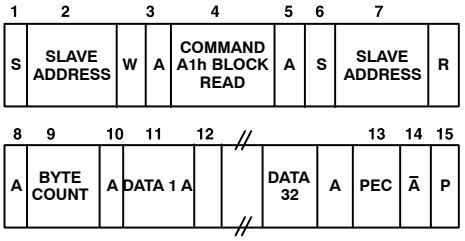


Figure 25. Block Read from EEPROM or RAM

When block reading from EEPROM, Bit 0 of EEPROM Register 3 must be set.

Note that although the ADM1026 supports Packet Error Checking (PEC), its use is optional. The PEC byte is calculated using CRC-8. The Frame Check Sequence (FCS) conforms to CRC-8 by the polynomial:

$$C(x) = x^8 + x^2 + x + 1 \qquad \text{(eq. 1)}$$

Consult the SMBus 1.1 Specification for more information.

Measurement Inputs

The ADM1026 has 17 external analog measurement pins that can be configured to perform various functions. It also measures two supply voltages, 3.3 V MAIN and 3.3 V STBY, and the internal chip temperature.

Pins 25 and 26 are dedicated to remote temperature measurement, while Pins 27 and 28 can be configured as analog inputs with a range of 0 V to 2.5 V, or as inputs for a second remote temperature sensor.

Pins 29 to 33 are dedicated to measuring V_{BAT}, +5.0 V, −12 V, +12 V supplies, and the processor core voltage V_{CCP}. The remaining analog inputs, Pins 34 to 41, are general-purpose analog inputs with a range of 0 V to 2.5 V (Pins 34 and 35) or 0 V to 3.0 V (Pins 36 to 41).

A-to-D Converter (ADC)

These inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter. The ADC has a resolution of 8 bits. The basic input range is 0 V to 2.5 V, which is the input range of A_{IN6} to A_{IN9}, but five of the inputs have built-in attenuators to allow measurement of V_{BAT}, +5.0 V, -12 V, +12 V, and the processor core voltage V_{CCP}, without any external components. To allow the tolerance of these supply voltages, the ADC produces an

output of 3/4 full scale (decimal 192) for the nominal input voltage, and so has adequate headroom to cope with over voltages. Table 7 shows the input ranges of the analog inputs and output codes of the ADC.

When the ADC is running, it samples and converts an analog or local temperature input every 711 μs (typical value). Each input is measured 16 times and the measurements are averaged to reduce noise, so the total conversion time for each input is 11.38 ms.

Measurements on the remote temperature (D1 and D2) inputs take 2.13 ms. These are also measured 16 times and are averaged, so the total conversion time for a remote temperature input is 34.13 ms.

Table 7. A-TO-D OUTPUT CODES VS. V_{IN}

Input Voltage								A-to-D Output	
+12 V_{IN}	–12 V_{IN}	+5.0 V_{IN}	3.3 V MAIN	V_{BAT}	V_{CCP}	$A_{IN\ (0–5)}$	$A_{IN\ (6–9)}$	Decimal	Binary
< 0.0625	< –15.928	< 0.026	< 0.0172	NA	< 0.012	< 0.012	< 0.010	0	00000000
0.062–0.125	–15.928–15.855	0.026–0.052	0.017–0.034	NA	0.012–0.023	0.012–0.023	0.010–0.019	1	00000001
0.125–0.187	–15.855–15.783	0.052–0.078	0.034–0.052	NA	0.023–0.035	0.023–0.035	0.019–0.029	2	00000010
0.188–0.250	–15.783–15.711	0.078–0.104	0.052–0.069	NA	0.035–0.047	0.035–0.047	0.029–0.039	3	00000011
0.250–0.313	–15.711–15.639	0.104–0.130	0.069–0.086	NA	0.047–0.058	0.047–0.058	0.039–0.049	4	00000100
0.313–0.375	–15.639–15.566	0.130–0.156	0.086–0.103	NA	0.058–0.070	0.058–0.070	0.049–0.058	5	00000101
0.375–0.438	–15.566–15.494	0.156–0.182	0.103–0.120	NA	0.070–0.082	0.070–0.082	0.058–0.068	6	00000110
0.438–0.500	–15.494–15.422	0.182–0.208	0.120–0.138	NA	0.082–0.094	0.082–0.094	0.068–0.078	7	00000111
0.500–0.563	–15.422–15.349	0.208–0.234	0.138–0.155	NA	0.094–0.105	0.094–0.105	0.078–0.087	8	00001000
	–								
	–								
	–								
4.000–4.063	–11.375–11.303	1.667–1.693	1.110–1.127	NA	0.750–0.780	0.750–0.780	0.625–0.635	64 (1/4 scale)	01000000
	–								
	–								
	–								
8.000–8.063	–6.750–6.678	3.333–3.359	2.000–2.016	2.000–2.016	1.500–1.512	1.500–1.512	1.250–1.260	128 (1/2 scale)	10000000
	–								
	–								
	–								
12.000–12.063	–2.125–2.053	5–5.026	3.330–3.347	3.000–3.016	2.250–2.262	2.250–2.262	1.875–1.885	192 (3/4 scale)	11000000
	–								
	–								
	–								
15.313–15.375	1.705–1.777	6.38–6.406	4.249–4.267	3.828–3.844	2.871–2.883	2.871–2.883	2.392–2.402	245	11110101
15.375–15.437	1.777–1.850	6.406–6.432	4.267–4.284	3.844–3.860	2.883–2.895	2.883–2.895	2.402–2.412	246	11110110
15.437–15.500	1.850–1.922	6.432–6.458	4.284–4.301	3.860–3.875	2.895–2.906	2.895–2.906	2.412–2.422	247	11110111
15.500–15.563	1.922–1.994	6.458–6.484	4.301–4.319	3.875–3.890	2.906–2.918	2.906–2.918	2.422–2.431	248	11111000
15.562–15.625	1.994–2.066	6.484–6.51	4.319–4.336	3.890–3.906	2.918–2.930	2.918–2.930	2.431–2.441	249	11111001
15.625–15.688	2.066–2.139	6.51–6.536	4.336–4.353	3.906–3.921	2.930–2.941	2.930–2.941	2.441–2.451	250	11111010
15.688–15.750	2.139–2.211	6.536–6.563	4.353–4.371	3.921–3.937	2.941–2.953	2.941–2.953	2.451–2.460	251	11111011
15.750–15.812	2.211–2.283	6.563–6.589	4.371–4.388	3.937–3.953	2.953–2.965	2.953–2.965	2.460–2.470	252	11111100
15.812–15.875	2.283–2.355	6.589–6.615	4.388–4.405	3.953–3.969	2.965–2.977	2.965–2.977	2.470–2.480	253	11111101
15.875–15.938	2.355–2.428	6.615–6.641	4.405–4.423	3.969–3.984	2.977–2.988	2.977–2.988	2.480–2.490	254	11111110
>15.938	>2.428	>6.634	>4.423	>3.984	>2.988	>2.988	>2.490	255	11111111

1. * V_{BAT} is not accurate for voltages under 1.5 V (see Figure 14).

Voltage Measurement Inputs

The internal structure for all the analog inputs is shown in Figure 26. Each input circuit consists of an input protection diode, an attenuator, plus a capacitor to form a first-order low-pass filter that gives each voltage measurement input immunity to high frequency noise. The −12 V input also has a resistor connected to the on-chip reference to offset the negative voltage range so that it is always positive and can be handled by the ADC. This allows most popular power supply voltages to be monitored directly by the ADM1026 without requiring any additional resistor scaling.

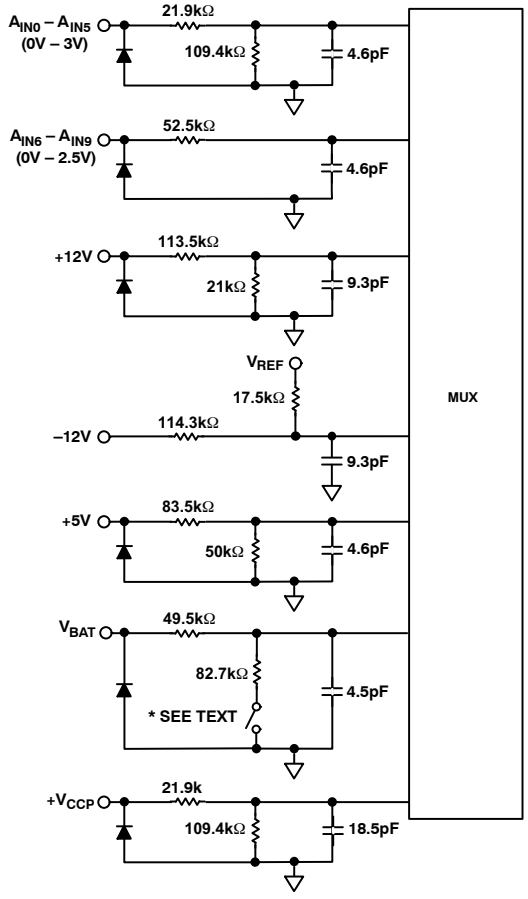


Figure 26. Voltage Measurement Inputs

Setting Other Input Ranges

A_{IN0} to A_{IN9} can easily be scaled to voltages other than 2.5 V or 3.0 V. If the input voltage range is zero to some positive voltage, all that is required is an input attenuator, as shown in Figure 27.

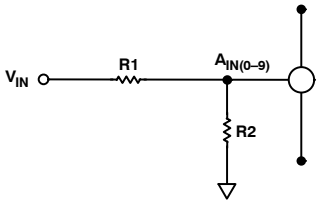


Figure 27. Scaling A_{IN0} – A_{IN9}

However, when scaling A_{IN0} to A_{IN5}, it should be noted that these inputs already have an on-chip attenuator, because their primary function is to monitor SCSI termination voltages. This attenuator loads any external attenuator. The input resistance of the on-chip attenuator can be between 100 kΩ and 200 kΩ. For this tolerance not to affect the accuracy, the output resistance of the external attenuator should be very much lower than this, that is, 1 kΩ in order to add not more than 1% to the total unadjusted error (TUE). Alternatively, the input can be buffered using an op amp.

$$\frac{R1}{R2} = \frac{\left(V_{f_s} - 3.0\right)}{3.0}\left(\text{for } A_{IN0} \text{ through } A_{IN5}\right) \quad \text{(eq. 2)}$$

$$\frac{R1}{R2} = \frac{\left(V_{f_s} - 2.5\right)}{2.5}\left(\text{for } A_{IN6} \text{ through } A_{IN9}\right) \quad \text{(eq. 3)}$$

Negative and bipolar input ranges can be accommodated by using a positive reference voltage to offset the input voltage range so that it is always positive. To monitor a negative input voltage, an attenuator can be used as shown in Figure 28.

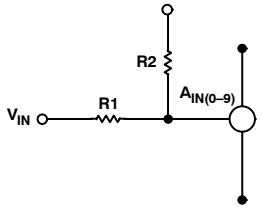


Figure 28. Scaling and Offsetting A_{IN0} – A_{IN9} for Negative Inputs

This offsets the negative voltage so that the ADC always sees a positive voltage. R1 and R2 are chosen so that the ADC input voltage is zero when the negative input voltage is at its maximum (most negative) value, that is:

$$\frac{R1}{R2} = \left|\frac{V_{f_s} -}{V_{OS}}\right| \quad \text{(eq. 4)}$$

This is a simple and low cost solution, but note the following:

- Because the input signal is offset but not inverted, the input range is transposed. An increase in the magnitude of the negative voltage (going more negative) causes the input voltage to fall and give a lower output code from the ADC. Conversely, a decrease in the magnitude of the negative voltage causes the ADC code to increase. The maximum negative voltage corresponds to zero output from the ADC. This means that the upper and lower limits are transposed.
- For the ADC output to be full scale when the negative voltage is zero, V_{OS} must be greater than the full–scale voltage of the ADC, because V_{OS} is attenuated by R1 and R2. If V_{OS} is equal to or less than the full–scale voltage of the ADC, the input range is bipolar but not necessarily symmetrical.

This is a problem only if the ADC output must be full scale when the negative voltage is zero.

Symmetrical bipolar input ranges can be accommodated easily by making V_{OS} equal to the full-scale voltage of the analog input, and by adding a third resistor to set the positive full scale.

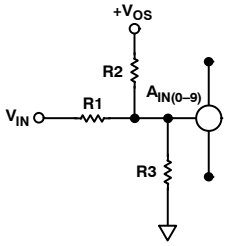


Figure 29. Scaling and Offsetting A_{IN0} − A_{IN9} for Bipolar Inputs

$$\frac{R1}{R2} = \frac{\left|V_{f_s} - \right|}{V_{OS}} \quad \text{(eq. 5)}$$

Note that R3 has no effect as the input voltage at the device pin is zero when V_{IN} = negative full scale.

$$\frac{R1}{R3} = \frac{\left(V_{f_s} - 3.0\right)}{3.0}\left(\text{for } A_{IN0} \text{ through } A_{IN5}\right) \quad \text{(eq. 6)}$$

$$\frac{R1}{R3} = \frac{\left(V_{f_s} - 2.5\right)}{2.5}\left(\text{for } A_{IN6} \text{ through } A_{IN9}\right) \quad \text{(eq. 7)}$$

Also, note that R2 has no effect as the input voltage at the device pin is equal to V_{OS} when V_{IN} = positive full scale.

Battery Measurement Input (V_{BAT})

The V_{BAT} input allows the condition of a CMOS backup battery to be monitored. This is typically a lithium coin cell such as a CR2032. The V_{BAT} input is accurate only for voltages greater than 1.5 V (see Figure 14). Typically, the battery in a system is required to keep some device powered on when the system is in a powered-off state. The V_{BAT} measurement input is specially designed to minimize battery drain. To reduce current drain from the battery, the lower resistor of the V_{BAT} attenuator is not connected, except whenever a V_{BAT} measurement is being made. The total current drain on the V_{BAT} pin is 80 nA typical (for a maximum V_{BAT} voltage = 4.0 V), so a CR2032 CMOS battery functions in a system in excess of the expected 10 years. Note that when a V_{BAT} measurement is not being made, the current drain is reduced to 6 nA typical. Under normal voltage measurement operating conditions, all measurements are made in a round-robin format, and each reading is actually the result of 16 digitally averaged measurements. However, averaging is not carried out on the V_{BAT} measurement to reduce measurement time and therefore reduce the current drain from the battery.

The V_{BAT} current drain when a measurement is being made is calculated by:

$$I = \frac{V_{BAT}}{100\ k\Omega} \times \frac{T_{PULSE}}{T_{PERIOD}} \quad \text{(eq. 8)}$$

For example, when V_{BAT} = 3.0 V,

$$I = \frac{3.0\ V}{100\ k\Omega} \times \frac{711\ \mu s}{273\ ms} = 78\ nA \quad \text{(eq. 9)}$$

where T_{PULSE} = V_{BAT} measurement time (711 μs typical), T_{PERIOD} = time to measure all analog inputs (273 ms typical), and V_{BAT} input battery protection.

V_{BAT} Input Battery Protection

In addition to minimizing battery current drain, the V_{BAT} measurement circuitry was specifically designed with battery protection in mind. Internal circuitry prevents the battery from being back-biased by the ADM1026 supply or through any other path under normal operating conditions. In the unlikely event of a catastrophic ADM1026 failure, the ADM1026 includes a second level of battery protection including a series 3 kΩ resistor to limit current to the battery, as recommended by UL. Thus, it is not necessary to add a series resistor between the battery and the V_{BAT} input; the battery can be connected directly to the V_{BAT} input to improve voltage measurement accuracy.

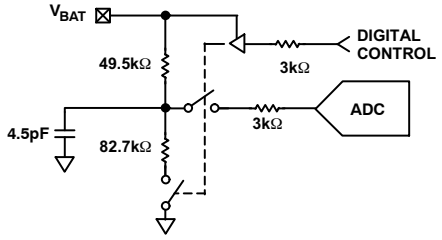


Figure 30. Equivalent V_{BAT} Input Protection Circuit

Reference Output (V_{REF})

The ADM1026 offers an on-chip reference voltage (Pin 24) that can be used to provide a 1.82 V or 2.5 V reference voltage output. This output is buffered and specified to sink or source a load current of 2 mA. The reference voltage outputs 1.82 V if Bit 2 of Configuration Register 3 (Address 07h) is 0; it outputs 2.5 V when this bit is set to 1. This voltage reference output can be used to provide a stable reference voltage to external circuitry such as LDOs. The load regulation of the V_{REF} output is typically 0.15% for a sink current of 2 mA and 0.15% for 2 mA source current. There may be some ripple present on the V_{REF} output that requires filtering (±4 m V_{MAX}). Figure 31 shows the recommended circuitry for the V_{REF} output for loads less than 2 mA. For loads in excess of 2 mA, external circuitry, such as that shown in Figure 32, can be used to buffer the V_{REF} output.

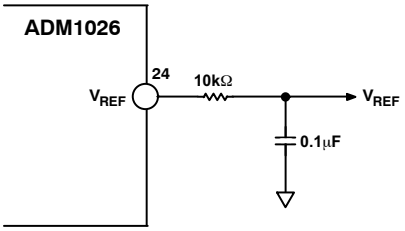


Figure 31. V_{REF} Interface Circuit for V_{REF} Loads < 2 mA

If the V_{REF} output is not being used, it should be left unconnected. Do not connect V_{REF} to GND using a capacitor. The internal output buffer on the voltage reference is capacitively loaded, which can cause the voltage reference to oscillate. This affects temperature readings reported back by the ADM1026. The recommended interface circuit for the V_{REF} output is shown in Figure 32.

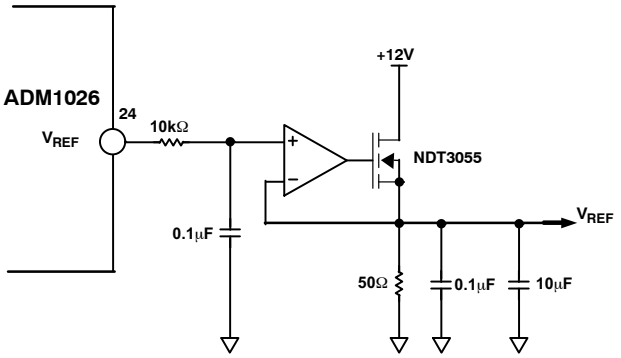


Figure 32. V_{REF} Interface Circuit for V_{REF} Loads > 2 mA

Temperature Measurement System

Local Temperature Measurement

The ADM1026 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip ADC. The temperature data is stored in the local temperature value register (Address 1Fh). As both positive and negative temperatures can be measured, the temperature data is stored in twos complement format, as shown in Table 8. Theoretically, the temperature sensor and ADC can measure temperatures from −128°C to +127°C with a resolution of 1°C. Temperatures below T_{MIN} and above T_{MAX} are outside the operating temperature range of the device; however, so local temperature measurements outside this range are not possible. Temperature measurement from −128°C to +127°C is possible using a remote sensor.

Remote Temperature Measurement

The ADM1026 can measure the temperature of two remote diode sensors, or diode-connected transistors, connected to Pins 25 and 26, or 27 and 28.

Pins 25 and 26 are a dedicated temperature input channel. Pins 27 and 28 can be configured to measure a diode sensor by clearing Bit 3 of Configuration Register 1 (Address 00h) to 0. If this bit is 1, then Pins 27 and 28 are A_{IN8} and A_{IN9}.

The forward voltage of a diode or diode-connected transistor, operated at a constant current, exhibits a negative temperature coefficient of about −2 mV/°C. Unfortunately, the absolute value of V_{be} varies from device to device, and individual calibration is required to null this out, so the technique is unsuitable for mass production.

The technique used in the ADM1026 is to measure the change in V_{be} when the device is operated at two different currents, given by:

$$\Delta V_{be} = \frac{K \times T}{q} \times \log n\ (N) \qquad \text{(eq. 10)}$$

where K is Boltzmann's constant, q is the charge on the carrier, T is the absolute temperature in Kelvins, and N is the ratio of the two currents.

Figure 33 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor provided for temperature monitoring on some microprocessors, but it could equally well be a discrete transistor such as a 2N3904.

If a discrete transistor is used, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D− input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D− input and the base to the D+ input.

To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D− input.

To measure ΔV_{be}, the sensor is switched between operating currents of I and N × I. The resulting waveform is passed through a 65 kHz low−pass filter to remove noise, and to a chopper-stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a DC voltage proportional to ΔV_{be}. This voltage is measured by the ADC to give a temperature output in 8-bit, twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles. A remote temperature measurement takes nominally 2.14 ms.

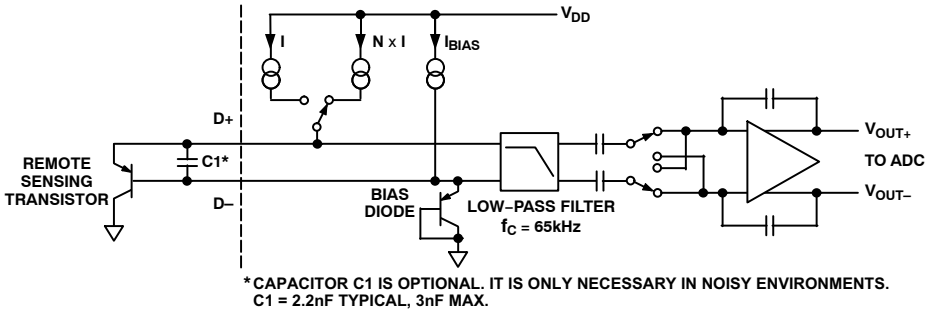


Figure 33. Signal Conditioning for Remote Diode Temperature Sensors

The results of external temperature measurements are stored in 8-bit, twos complement format, as illustrated in Table 8.

Table 8. TEMPERATURE DATA FORMAT

Temperature	Digital Output	Hex
−128°C	1000 0000	80
−125°C	1000 0011	83
−100°C	1001 1100	9C
−75°C	1011 0101	B5
−50°C	1100 1110	CE
−25°C	1110 0111	E7
−10°C	1111 0110	F6
0°C	0000 0000	00
10°C	0000 1010	0A
25°C	0001 1001	19
50°C	0011 0010	32
75°C	0100 1011	4B
100°C	0110 0100	64
125°C	0111 1101	7D
127°C	0111 1111	7F

Layout Considerations

Digital boards can be electrically noisy environments. Take these precautions to protect the analog inputs from noise, particularly when measuring the very small voltages from a remote diode sensor.

- Place the ADM1026 as close as possible to the remote sensing diode. Provided that the worst noise sources such as clock generators, data/address buses, and CRTs are avoided, this distance can be 4 to 8 inches.
- Route the D+ and D− tracks close together, in parallel, with grounded guard tracks on each side. Provide a ground plane under the tracks if possible.
- Use wide tracks to minimize inductance and reduce noise pickup. A 10 mil track minimum width and spacing is recommended.

Figure 34. Arrangement of Signal Tracks

- Try to minimize the number of copper/solder joints, which can cause thermocouple effects. Where copper/solder joints are used, make sure that they are in both the D+ and D− paths and are at the same temperature.
- Thermocouple effects should not be a major problem because 1°C corresponds to about 240 μV, and thermocouple voltages are about 3 μV/°C of temperature difference. Unless there are two thermocouples with a big temperature differential between them, thermocouple voltages should be much less than 200 mV.
- Place a 0.1 μF bypass capacitor close to the ADM1026.
- If the distance to the remote sensor is more than eight inches, the use of twisted-pair cable is recommended. This works from about 6 to 12 feet.
- For very long distances (up to 100 feet), use shielded twisted pair such as Belden #8451 microphone cable. Connect the twisted pair to D+ and D− and the shield to GND close to the ADM1026. Leave the remote end of the shield unconnected to avoid ground loops.

Because the measurement technique uses switched current sources, excessive cable and/or filter capacitance can affect the measurement. When using long cables, the filter capacitor may be reduced or removed. Cable resistance can also introduce errors. A 1 Ω series resistance introduces about 0.5°C error.

Limit Values

Limit values for analog measurements are stored in the appropriate limit registers. In the case of voltage measurements, high and low limits can be stored so that an interrupt request is generated if the measured value goes above or below acceptable values. In the case of temperature, a hot temperature or high limit can be programmed, and a hot temperature hysteresis or low limit can be programmed, which is usually some degrees lower. This can be useful because it allows the system to be shut down when the hot limit is exceeded, and restarted automatically when it has cooled down to a safe temperature.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0), and a 0 to the INT_Clear bit (Bit 2) of the configuration register. INT_Enable (Bit 1) should be set to 1 to enable the $\overline{\text{INT}}$ output. The ADC measures each analog input in turn, starting with Remote Temperature Channel 1 and ending with local temperature. As each measurement is completed, the result is automatically stored in the appropriate value register. This round-robin monitoring cycle continues until it is disabled by writing a 0 to Bit 0 of the configuration register. Because the ADC is typically left to free-run in this way, the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can easily be calculated.

The total number of channels measured is:

- Five Dedicated Supply Voltage Inputs
- Ten General-purpose Analog Inputs
- 3.3 V MAIN
- 3.3 V STBY
- Local Temperature
- Two Remote Temperature

Pins 28 and 27 are measured both as analog inputs A_{IN8}/A_{IN9} and as remote temperature input D2+/D2−, irrespective of which configuration is selected for these pins.

If Pins 28 and 27 are configured as A_{IN8}/A_{IN9}, the measurements for these channels are stored in Registers 27h and 29h, and the invalid temperature measurement is discarded. On the other hand, if Pins 28 and 27 are configured as D2+/D2−, the temperature measurement is stored in Register 29h, and there is no valid result in Register 27h.

As mentioned previously, the ADC performs a conversion every 711 μs on the analog and local temperature inputs and every 2.13 ms on the remote temperature inputs. Each input is measured 16 times and averaged to reduce noise.

The total monitoring cycle time for voltage and temperature inputs is therefore nominally:

$$(18 \times 16 \times 0.711) + (2 \times 16 \times 2.13) = 273 \text{ ms} \quad \text{(eq. 11)}$$

The ADC uses the internal 22.5 kHz clock, which has a tolerance of ±6%, so the worst-case monitoring cycle time is 290 ms. The fan speed measurement uses a completely separate monitoring loop, as described later.

Input Safety

Scaling of the analog inputs is performed on-chip, so external attenuators are typically not required. However, because the power supply voltages appear directly at the pins, it is advisable to add small external resistors (that is, 500 Ω) in series with the supply traces to the chip to prevent damaging the traces or power supplies should an accidental short such as a probe connect two power supplies together.

Because the resistors form part of the input attenuators, they affect the accuracy of the analog measurement if their value is too high. The worst such accident would be connecting −12 V to +12 V where there is a total of 24 V difference. With the series resistors, this would draw a maximum current of approximately 24 mA.

Analog Output

The ADM1026 has a single analog output from an unsigned 8-bit DAC that produces 0 V to 2.5 V (independent of the reference voltage setting). The input data for this DAC is contained in the DAC control register (Address 04h). The DAC control register defaults to FFh during a power-on reset, which produces maximum fan speed. The analog output may be amplified and buffered with external circuitry such as an op amp and a transistor to provide fan speed control. During automatic fan speed control, described later, the four MSBs of this register set the minimum fan speed.

Suitable fan drive circuits are shown in Figure 35 through Figure 39. When using any of these circuits, note the following:

- All of these circuits provide an output range from 0 V to almost +12 V, apart from Figure 35, which loses the base-emitter voltage drop of Q1 due to the emitter-follower configuration.
- To amplify the 2.5 V range of the analog output up to 12 V, the gain of these circuits needs to be about 4.8.
- Take care when choosing the op amp to ensure that its input common-mode range and output voltage swing are suitable.
- The op amp may be powered from the +12 V rail alone or from ±12 V. If it is powered from +12 V, the input common-mode range should include ground to accommodate the minimum output voltage of the DAC, and the output voltage should swing below 0.6 V to ensure that the transistor can be turned fully off.
- If the op amp is powered from −12 V, precautions such as a clamp diode to ground may be needed to prevent the base-emitter junction of the output transistor being reverse-biased in the unlikely event that the output of the op amp should swing negative for any reason.
- In all these circuits, the output transistor must have an I_{CMAX} greater than the maximum fan current, and be capable of dissipating power due to the voltage dropped across it when the fan is not operating at full speed.
- If the fan motor produces a large back EMF when switched off, it may be necessary to add clamp diodes to protect the output transistors in the event that the output goes from full scale to zero very quickly.

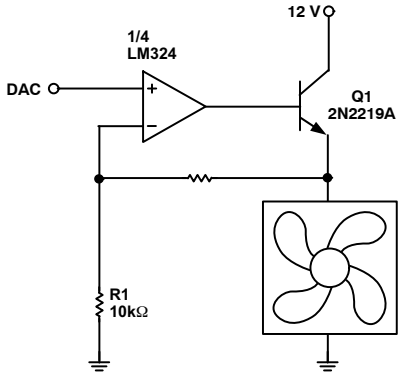


Figure 35. Fan Drive Circuit with Op Amp and Emitter-follower

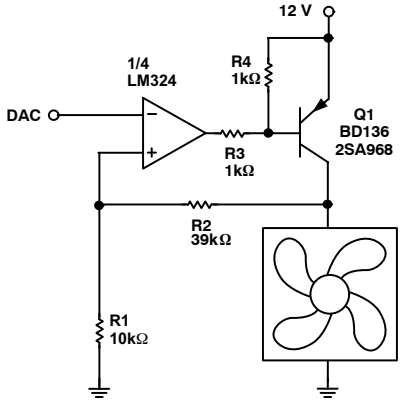


Figure 36. Fan Drive Circuit with Op Amp and PNP Transistor

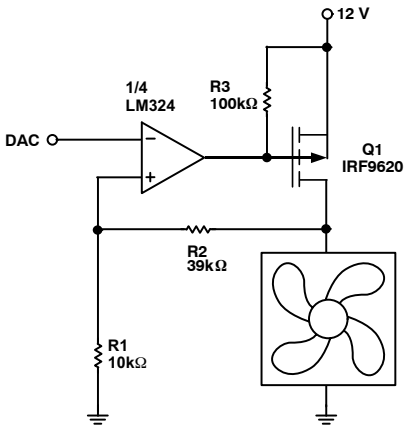


Figure 37. Fan Drive Circuit with Op Amp and P-channel MOSFET

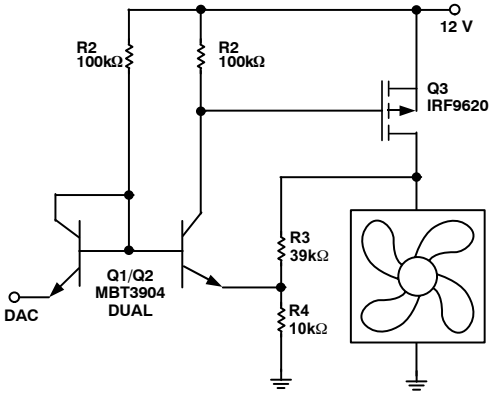


Figure 38. Discrete Fan Drive Circuit with P-channel MOSFET, Single Supply

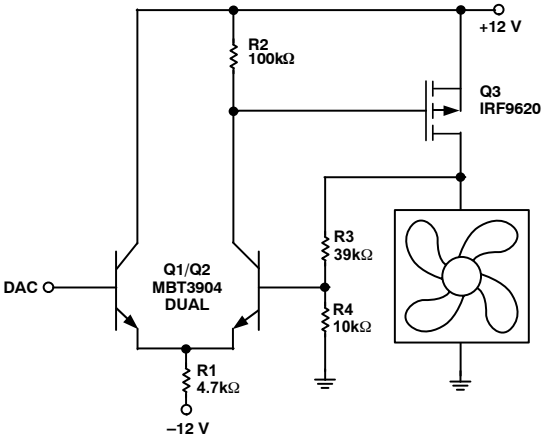


Figure 39. Discrete Fan Drive Circuit with P-channel MOSFET, Dual Supply

PWM Output

Fan speed may also be controlled using pulse width modulation (PWM). The PWM output (Pin 18) produces a pulsed output with a frequency of approximately 75 Hz and a duty cycle defined by the contents of the PWM control register (Address 05h). During automatic fan speed control, described below, the four MSBs of this register set the minimum fan speed.

The open drain PWM output must be amplified and buffered to drive the fans. The PWM output is intended to be used with an NMOS driver, but may be inverted by setting Bit 1 of Test Register 1 (Address 14h) if using PMOS drivers. Figure 40 shows how a fan may be driven under PWM control using an N-channel MOSFET.

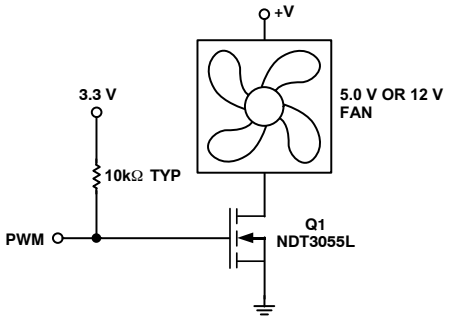


Figure 40. PWM Fan Drive Circuit Using an N-channel MOSFET

Automatic Fan Speed Control

The ADM1026 offers a simple method of controlling fan speed according to temperature without intervention from the host processor. Monitoring must be enabled by setting Bit 0 of Configuration Register 1 (Address 00h), to enable automatic fan speed control. Automatic fan speed control can be applied to the DAC output, the PWM output, or both, by setting Bit 5 and/or Bit 6 of Configuration Register 1.

The T_{MIN} registers (Addresses 10h to 12h) contain minimum temperature values for the three temperature channels (on-chip sensor and two remote diodes). This is the temperature at which a fan starts to operate when the temperature sensed by the controlling sensor exceeds T_{MIN}. T_{MIN} can be the same or different for all three channels. T_{MIN} is set by writing a twos complement temperature value to the T_{MIN} registers. If any sensor channel is not required for automatic fan speed control, T_{MIN} for that channel should be set to 127°C (01111111).

In automatic fan speed control mode, (as shown Figure 41 and Figure 42) the four MSBs of the DAC control register (Address 04h) and PWM control register (Address 05h) set the minimum values for the DAC and PWM outputs. Note that, if both DAC control and PWM control are enabled (Bits 5 and 6 of Configuration Register 1 = 1), the four MSBs of the DAC control register (Address 04h) define the minimum fan speed values for both the DAC and PWM outputs. The value in the PWM control register (Address 05h) has no effect.

Minimum DAC Code $DAC_{MIN} = 16 \times D$

$$\text{DAC Output Voltage} = 2.5 \times \frac{\text{Code}}{256} \qquad \text{(eq. 12)}$$

Minimum PWM Duty Cycle $PWM_{MIN} = 6.67 \times D$

where D is the decimal equivalent of Bits 7 to 4 of the register.

When the temperature measured by any of the sensors exceeds the corresponding T_{MIN}, the fan is spun up for 2 seconds with the fan drive set to maximum (full scale from the DAC or 100% PWM duty cycle). The fan speed is then set to the minimum as previously defined. As the temperature increases, the fan drive increases until the temperature reaches T_{MIN} + 20°C.

The fan drive at any temperature up to 20°C above T_{MIN} is given by:

$$PWM = PWM_{MIN} + (100 - PWM_{MIN}) \times \frac{T_{ACTUAL} - T_{MIN}}{20} \quad \text{(eq. 13)}$$

or

$$DAC = DAC_{MIN} + (240 - DAC_{MIN}) \times \frac{T_{ACTUAL} - T_{MIN}}{20} \quad \text{(eq. 14)}$$

For simplicity of the automatic fan speed algorithm, the DAC code increases linearly up to 240, not its full scale of 255. However, when the temperature exceeds T_{MIN} +20°C, the DAC output jumps to full scale. To ensure that the maximum cooling capacity is always available, the fan drive is always set by the sensor channel demanding the highest fan speed.

If the temperature falls, the fan does not turn off until the temperature measured by all three temperature sensors has fallen to their corresponding T_{MIN} − 4°C. This prevents the fan from cycling on and off continuously when the temperature is close to T_{MIN}.

Whenever a fan starts or stops during automatic fan speed control, a one-off interrupt is generated at the $\overline{INT}$ output. This is described in more detail in the section on the ADM1026 Interrupt Structure.

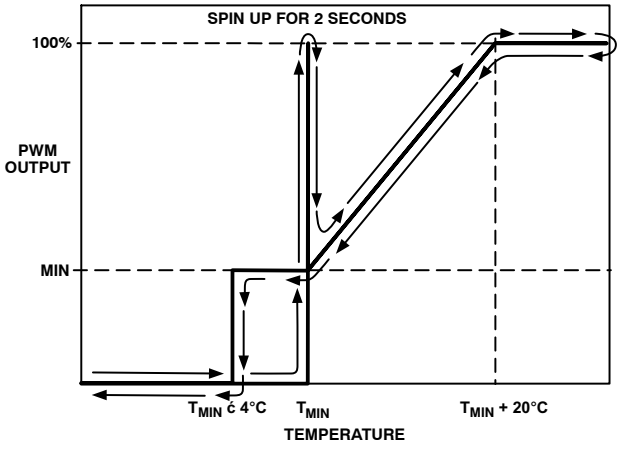


Figure 41. Automatic PWM Fan Control Transfer Function

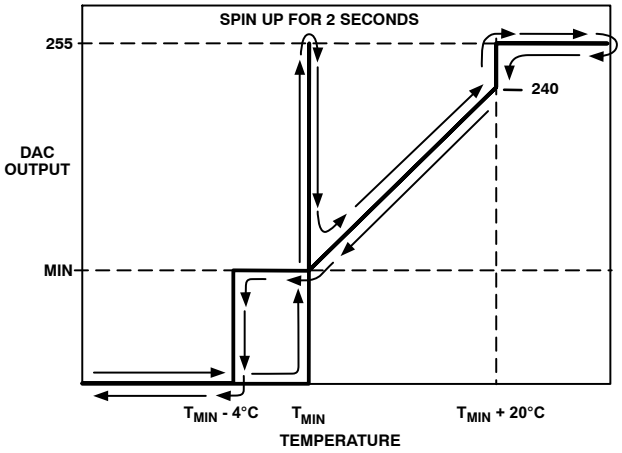


Figure 42. Automatic DAC Fan Control Transfer Function

Fan Inputs

Pins 3 to 6 and 9 to 12 may be configured as fan speed measuring inputs by clearing the corresponding bit(s) of Configuration Register 2 (Address 01h), or as general-purpose logic inputs/outputs by setting bits in this register. The power-on default value for this register is 00h, which means all the inputs are set for fan speed measurement.

Signal conditioning in the ADM1026 accommodates the slow rise and fall times typical of fan tachometer outputs. The fan tach inputs have internal 10 kΩ pullup resistors to 3.3 V STBY. In the event that these inputs are supplied from fan outputs that exceed the supply, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range. Figure 43 through Figure 47 show circuits for common fan tach outputs.

If the fan tach output is open-drain or has a resistive pullup to V_{CC}, then it can be connected directly to the fan input, as shown in Figure 44.

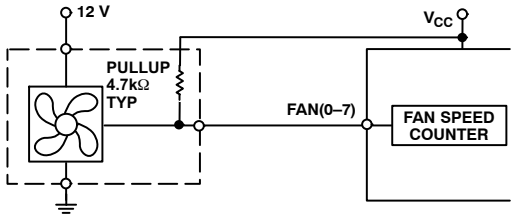


Figure 43. Fan with Tach Pullup to +V_{CC}

If the fan output has a resistive pullup to +12 V (or other voltage greater than 3.3 V STBY), the fan output can be clamped with a Zener diode, as shown in Figure 46. The Zener voltage should be chosen so that it is greater than V_{IH} but less than 3.3 V STBY, allowing for the voltage tolerance of the Zener.

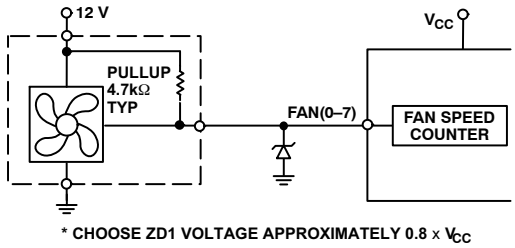


Figure 44. Fan with Tach Pullup to Voltage > V_{CC} (e.g. 12 V), Clamped with Zener Diode

If the fan has a strong pullup (less than 1 kΩ) to +12 V, or a totem pole output, a series resistor can be added to limit the Zener current, as shown in Figure 45. Alternatively, a resistive attenuator may be used, as shown in Figure 47.

R1 and R2 should be chosen such that:

$$2.0\ V < V_{PULLUP} \times \frac{R2}{(R_{PULLUP} + R1 + R2)} < 3.3\ V\ STBY \quad \text{(eq. 15)}$$

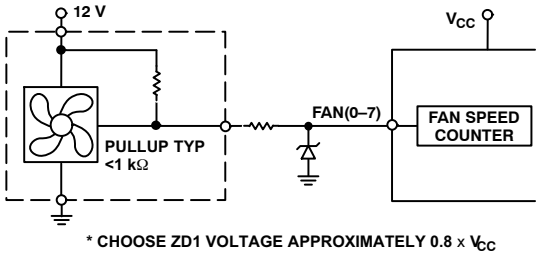


Figure 45. Fan with Strong Tach Pullup to >V_{CC} or Totem Pole Output, Attenuated with R1/R2

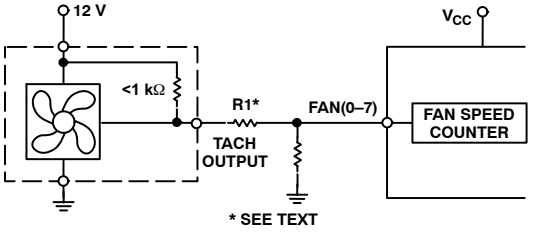


Figure 46. Fan with Strong Tach Pullup to > V_{CC} or Totem Pole Output, Clamped with Zener and Resistor

Fan Speed Measurement

The fan counter does not count the fan tach output pulses directly because the fan speed may be less than 1000 RPM and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 22.5 kHz oscillator into the input of an 8-bit counter for two periods of the fan tach output, as shown in Figure 47, so the accumulated count is actually proportional to the fan tach period and inversely proportional to the fan speed.

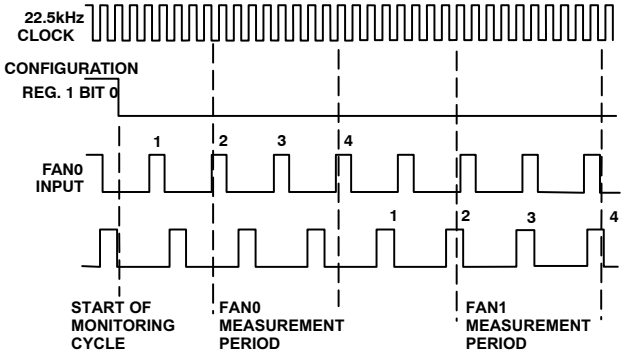


Figure 47. Fan Speed Measurement

The monitoring cycle begins when a 1 is written to the monitor bit (Bit 0 of Configuration Register 1). The INT_Enable (Bit 1) should be set to 1 to enable the $\overline{INT}$ output.

The fan speed counter starts counting as soon as the fan channel has been switched to. If the fan tach count reaches 0xFF, the fan has failed or is not connected. If a fan is connected and running, the counter is reset on the second tach rising edge, and oscillator pulses are actually counted from the second rising tach edge to the fourth rising edge. The measurement then switches to the next fan channel. Here again, the counter begins counting and is reset on the second tach rising edge, and oscillator pulses are counted from the second rising edge to the fourth rising edge. This is repeated for the other six fan channels.

Note that fan speed measurement does not occur until 1.8 seconds after the monitor bit has been set. This is to allow the fans adequate time to spin up. Otherwise, the ADM1026 could generate false fan failure interrupts. During the 1.8 second fan spin-up time, all fan tach registers read 0x00.

To accommodate fans of different speed and/or different numbers of output pulses per revolution, a prescaler (divisor) of 1, 2, 4, or 8 may be added before the counter. Divisor values for Fans 0 to 3 are contained in the Fan 0–3 divisor register (Address 02h) and those for Fans 4 to 7 in the Fan 4–7 divisor register (Address 03h). The default value is 2, which gives a count of 153 for a fan running at 4400 RPM producing two output pulses per revolution. The count is calculated by the equation:

$$Count = \frac{22.5 \times 10^3 \times 60}{RPM \times Divisor} \quad \text{(eq. 16)}$$

For constant-speed fans, fan failure is typically considered to have occurred when the speed drops below 70% of nominal, corresponding to a count of 219. Full scale (255) is reached if the fan speed fell to 60% of its nominal value. For temperature-controlled, variable-speed fans, the situation is different.

Table 9 shows the relationship between fan speed and time per revolution at 60%, 70%, and 100% of nominal RPM for fan speeds of 1100, 2200, 4400, and 8800 RPM, and the divisor that would be used for each of these fans, based on two tach pulses per revolution.

Limit Values

Fans generally do not over-speed if run from the correct voltage, so the failure condition of interest is under speed due to electrical or mechanical failure. For this reason, only low speed limits are programmed into the limit registers for the fans. It should be noted that because fan period rather than speed is being measured, a fan failure interrupt occurs when the measurement exceeds the limit value.

Fan Monitoring Cycle Time

The fan speeds are measured in sequence from 0 to 7. The monitoring cycle time depends on the fan speed, the number of tach output pulses per revolution, and the number of fans being monitored.

If a fan is stopped or running so slowly that the fan speed counter reaches 255 before the second tach pulse after initialization or before the fourth tach pulse during measurement, the measurement is terminated. This also occurs if an input is configured as GPIO instead of fan. Any channels connected in this manner time out after 255 clock pulses.

The worst-case measurement time for a fan−configured channel occurs when the counter reaches 254 from start to the second tach pulse and reaches 255 after the second tach pulse. Taking into account the tolerance of the oscillator frequency, the worst-case measurement time is:

$$509 \times D \times 0.05\ \text{ms} \qquad \text{(eq. 17)}$$

where:

509 is the total number of clock pulses.

D is the divisor: 1, 2, 4, or 8.

0.05 ms is the worst-case oscillator period in ms.

The worst-case fan monitoring cycle time is the sum of the worst-case measurement time for each fan.

Although the fan monitoring cycle and the analog input monitoring cycle are started together, they are not synchronized in any other way.

Table 9. FAN SPEEDS AND DIVISORS

		Time Per				
Divisor RPM	Nominal Rev	RPM (ms)	70% RPM	Rev 70% (ms)	60% RPM	Rev 60% (ms)
÷ 1	8800	6.82	6160	9.74	5280	11.36
÷ 2	4400	13.64	3080	19.48	2640	22.73
÷ 4	2200	27.27	1540	38.96	1320	45.45
÷ 8	1100	54.54	770	77.92	660	90.9

Chassis Intrusion Input

The chassis intrusion input is an active high input intended for detection and signaling of unauthorized tampering with the system. When this input goes high, the event is latched in Bit 6 of Status Register 4, and an interrupt is generated. The bit remains set until cleared by writing a 1 to CI clear, Bit 1 of Configuration Register 3 (05h), as long as battery voltage is connected to the V_{BAT} input. The CI clear bit itself is cleared by writing a 0 to it.

The CI input detects chassis intrusion events even when the ADM1026 is powered off (provided battery voltage is applied to V_{BAT}) but does not immediately generate an interrupt. Once a chassis intrusion event is detected and latched, an interrupt is generated when the system is powered on.

The actual detection of chassis intrusion is performed by an external circuit that detects, for example, when the cover has been removed. A wide variety of techniques may be used for the detection, for example:

- A Microswitch that Opens or Closes when the Cover is Removed
- A Reed Switch Operated by Magnet Fixed to the Cover
- A Hall-effect Switch Operated by Magnet Fixed to the Cover
- A Phototransistor that Detects Light when the Cover is Removed

The chassis intrusion input can also be used for other types of alarm input. Figure 48 shows a temperature alarm circuit using an AD22105 temperature switch sensor. This produces a low-going output when the preset temperature is exceeded, so the output is inverted by Q1 to make it compatible with the CI input. Q1 can be almost any small-signal NPN transistor, or a TTL or CMOS inverter gate may be used if one is available.

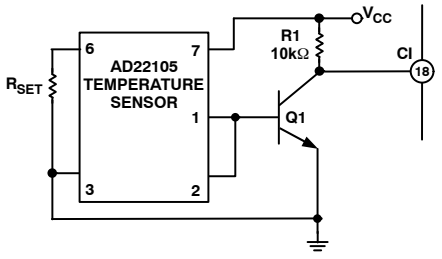


Figure 48. Using the CI Input with a Temperature Sensor

General-Purpose I/O Pins (Open Drain)

The ADM1026 has eight pins that are dedicated to general-purpose logic input/output (Pins 1, 2, and 43 to 48), eight pins that can be configured as general-purpose logic pins or fan speed inputs (Pins 3 to 6, and 9 to 12), and one pin that can be configured as GPIO16 or the bidirectional $\overline{\text{THERM}}$ pin (Pin 42). The GPIO/FAN pins are configured as general-purpose logic pins by setting Bits 0 to 7 of